

UCCx808A Low-Power Current-Mode Push-Pull PWM

1 Features

- Dual-Output Drive Stages in Push-Pull Configuration
- Current-Sense Discharge Transistor to Improve Dynamic Response
- 130- μ A Typical Starting Current
- 1-mA Typical Run Current
- Operation to 1 MHz
- Internal Soft Start
- On-Chip Error Amplifier With 2-MHz Gain Bandwidth Product
- On-Chip VDD Clamping
- Output Drive Stages Capable of 500-mA Peak-Source Current, 1-A Peak-Sink Current

2 Applications

- High-Efficiency Switch-Mode Power Supplies
- Telecom DC-to-DC Converters
- Point-of-Load Power Modules
- Low-Cost Push-Pull and Half-Bridge Applications

3 Description

The UCCx808A devices are a family of BiCMOS push-pull, high-speed, low-power, pulse-width modulators. The UCCx808A contains all of the control and drive circuitry required for off-line or DC-to-DC fixed frequency current-mode switching power supplies with minimal external parts count.

The UCCx808A dual-output drive stages are arranged in a push-pull configuration. Both outputs switch at half the oscillator frequency using a toggle flip-flop. The dead time between the two outputs is typically 60 ns to 200 ns depending on the values of the timing capacitor and resistors, thus limiting each output stage duty cycle to less than 50%.

The UCCx808A family offers a variety of package options, temperature range options, and choice of undervoltage lockout levels. The family has UVLO thresholds and hysteresis options for off-line and battery-powered systems.

The UCCx808A is an enhanced version of the UCC3808 family. The significant difference is that the A versions feature an internal discharge transistor from the CS pin to ground, which is activated each clock cycle during the oscillator dead time. The feature discharges any filter capacitance on the CS pin during each cycle and helps minimize filter capacitor values and current sense delay.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC2808A-1, UCC2808A-2, UCC3808A-2	SOIC (8)	4.90 mm x 3.91 mm
	PDIP (8)	9.81 mm x 6.35 mm
	TSSOP (8)	3.00 mm x 4.40 mm
UCC3808A-1	SOIC (8)	4.90 mm x 3.91 mm
	PDIP (8)	9.81 mm x 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application

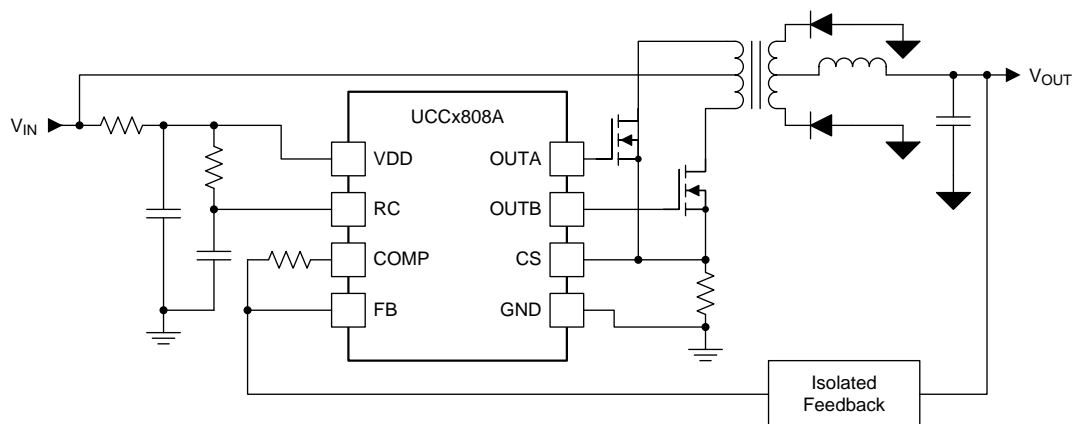


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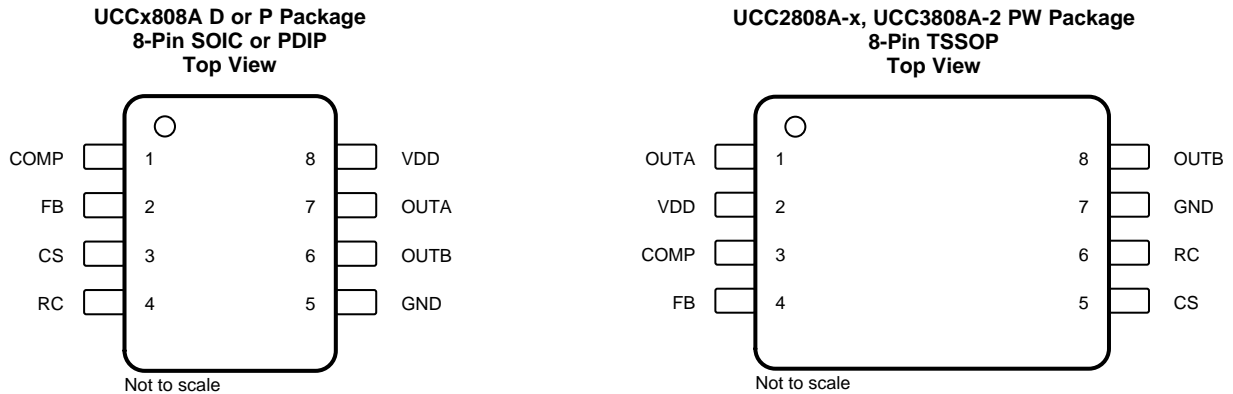
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2016) to Revision F	Page
• Changed the <i>Simplified Application</i>	1
• Changed references of N package to P package (PDIP)	5
• Changed the <i>Electrostatic Discharge Caution</i> statement	15

Changes from Revision D (August 2002) to Revision E	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Deleted Lead temperature, soldering (10 s): 300°C maximum	5

5 Pin Configuration and Functions



Pin Functions

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	SOIC, PDIP	TSSOP		
COMP	1	3	O	COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCCx808A is a true low-output impedance, 2-MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND. The UCCx808A family features built-in full-cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.
CS	3	5	I	The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft-start cycle. An internal MOSFET discharges the current sense filter capacitor to improve dynamic performance of the power converter.
FB	2	4	I	The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.
GND	5	7	G	Reference ground and power ground for all functions. Because of high currents, and high-frequency operation of the UCC3808A, a low impedance circuit board ground plane is highly recommended.
OUTA	7	1	O	Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak-source current, and 1-A peak-sink current. The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This <i>dead time</i> between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60 ns to 200 ns and depends upon the values of the timing capacitor and resistor. The high-current-output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external-schottky-clamp diodes are not required.
OUTB	6	8	O	Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak-source current, and 1-A peak-sink current. The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This <i>dead time</i> between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60 ns to 200 ns and depends upon the values of the timing capacitor and resistor. The high-current-output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external-schottky-clamp diodes are not required.

(1) P = Power, G = Ground, I = Input, O = Output

Pin Functions (continued)

PIN			TYPE ⁽¹⁾	DESCRIPTION
NAME	SOIC, PDIP	TSSOP		
RC	4	6	O	<p>The oscillator programming pin. The UCC3808A's oscillator tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. Functional Block Diagrams shows the oscillator block diagram. Only two components are required to program the oscillator: a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by the simple formula in Equation 1.</p> <p>The recommended range of timing resistors is between 10 kΩ and 200 kΩ and range of timing capacitors is between 100 pF and 1000 pF. Timing resistors less than 10 kΩ must be avoided. For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.</p>
VDD	8	2	P	<p>The power input connection for this device. Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from Equation 2.</p> <p>To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. A 1-μF decoupling capacitor is recommended.</p>

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
Supply voltage (IDD ≤ 10 mA)			15	V
Supply current			20	mA
OUTA/OUTB source current (peak)			−0.5	A
OUTA/OUTB sink current (peak)			1	A
Analog inputs (FB, CS)		−0.3	VDD + 0.3 (not to exceed 6)	V
Power dissipation at TA = 25°C	P package		1	W
	D package		650	mW
	PW package		400	
Junction temperature, TJ		−55	150	°C
Storage temperature, Tstg		−65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Currents are positive into, negative out of the specified terminal. Consult the packaging section of the [Power Supply Control Products Data Book](#) for thermal limitations and considerations of packages.

6.2 ESD Ratings

		VALUE	UNIT
V(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VDD Supply voltage	UCCx808-1	13	14	V
	UCCx808-2	5	14	
TJ Junction temperature	UCC2808-x	−40	85	°C
	UCC3808-x	0	70	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		UCCx808A		UCC2808A-x UCC3808A-2	UNIT
		D (SOIC)	P (PDIP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
RθJA	Junction-to-ambient thermal resistance	105.4	57	151.9	°C/W
RθJC(top)	Junction-to-case (top) thermal resistance	47.9	49.6	36.5	°C/W
RθJB	Junction-to-board thermal resistance	46.5	34.3	81.5	°C/W
ψJT	Junction-to-top characterization parameter	8.7	19.5	1.7	°C/W
ψJB	Junction-to-board characterization parameter	45.9	34.2	79.6	°C/W
RθJC(bot)	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

- For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

$T_A = 0^\circ\text{C}$ to 70°C for the UCC3808A-x and -40°C to $+85^\circ\text{C}$ for the UCC2808A-x, $V_{DD} = 10\text{ V}^{(1)}$, 1- μF capacitor from VDD to GND, $R = 22\text{ k}\Omega$, $C = 330\text{ pF}$, and $T_A = T_J$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR					
Oscillator frequency		175	194	213	kHz
Oscillator amplitude/VDD ⁽²⁾		0.44	0.5	0.56	V/V
ERROR AMPLIFIER					
Input voltage	COMP = 2 V	1.95	2	2.05	V
Input bias current		-1		1	μA
Open loop voltage gain		60	80		dB
COMP sink current	FB = 2.2 V, COMP = 1 V	0.3	2.5		mA
COMP source current	FB = 1.3 V, COMP = 3.5 V	-0.2	-0.5		mA
PWM					
Maximum duty cycle	Measured at OUTA or OUTB	48%	49%	50%	
Minimum duty cycle	COMP = 0 V			0%	
CURRENT SENSE					
Gain ⁽³⁾		1.9	2.2	2.5	V/V
Maximum input signal	COMP = 5 V ⁽⁴⁾	0.45	0.5	0.55	V
CS to output delay	COMP = 3.5 V, CS from 0 mV to 600 mV		100	200	ns
CS source current		-200			nA
CS sink current	CS = 0.5 V, RC = 5.5 V ⁽⁵⁾	5	10		mA
Over current threshold		0.7	0.75	0.8	V
COMP to CS offset	CS = 0 V	0.35	0.8	1.2	V
OUTPUT					
OUT low level	I = 100 mA		0.5	1	V
OUT high level	I = -50 mA, VDD – OUT		0.5	1	V
Rise time	$C_L = 1\text{ nF}$		25	60	ns
Fall time	$C_L = 1\text{ nF}$		25	60	ns
UNDERVOLTAGE LOCKOUT					
Start threshold	UCCx808A-1 ⁽¹⁾	11.5	12.5	13.5	V
	UCCx808A-2	4.1	4.3	4.5	
Minimum operating voltage after start	UCCx808A-1	7.6	8.3	9	V
	UCCx808A-2	3.9	4.1	4.3	
Hysteresis	UCCx808A-1	3.5	4.2	5.1	V
	UCCx808A-2	0.1	0.2	0.3	
SOFT START					
COMP rise time	FB = 1.8 V, rise from 0.5 V to 4 V		3.5	20	ms
OVERALL					
Start-up current	VDD < start threshold		130	260	μA
Operating supply current	FB = 0 V, CS = 0 V ⁽¹⁾⁽⁶⁾		1	2	mA
VDD zener shunt voltage	IDD = 10 mA ⁽⁷⁾	13	14	15	V

(1) For UCCx808A-1, set VDD above the start threshold before setting at 10 V.

(2) Measured at RC. Signal amplitude tracks VDD.

(3) Gain is defined by: $A = \Delta V_{\text{COMP}} / \Delta V_{\text{CS}}$, $0\text{ V} \leq V_{\text{CS}} \leq 0.4\text{ V}$.

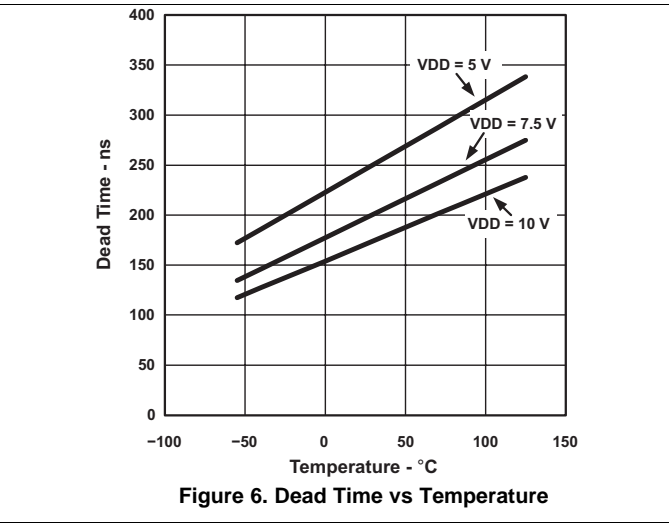
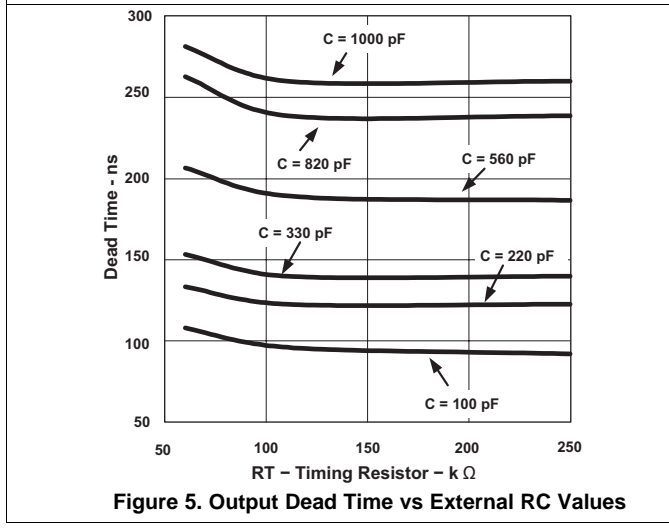
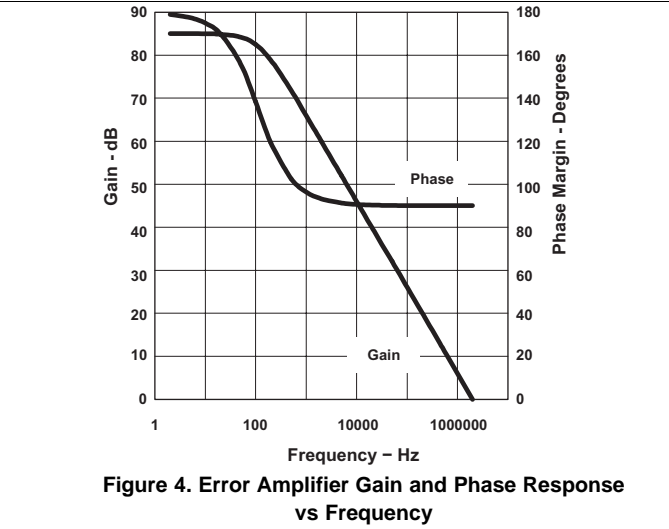
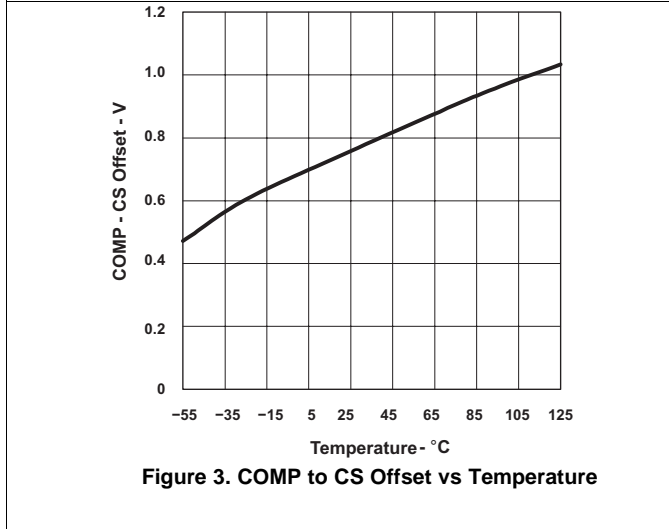
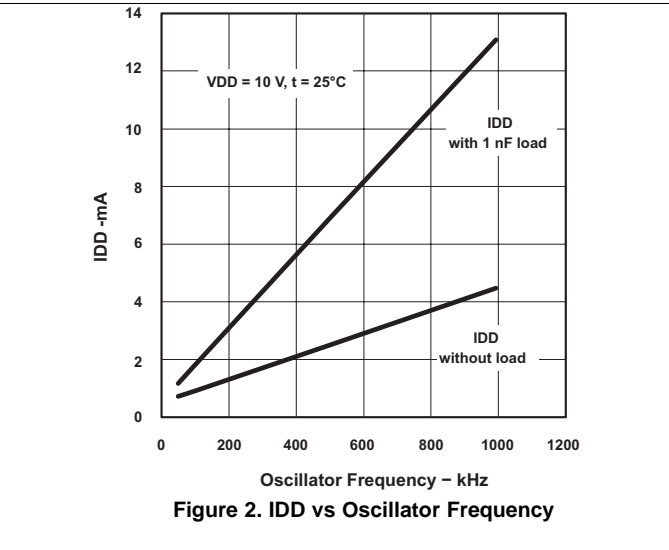
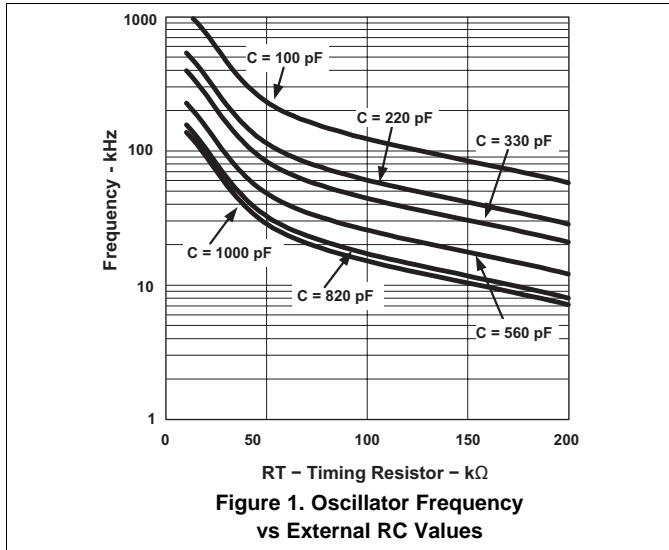
(4) Parameter measured at trip point of latch with FB at 0 V.

(5) The internal current sink on the CS pin is designed to discharge an external filter capacitor. It is not intended to be a DC sink path.

(6) Does not include current in the external oscillator network.

(7) Start threshold and Zener shunt threshold track one another.

6.6 Typical Characteristics



Typical Characteristics (continued)

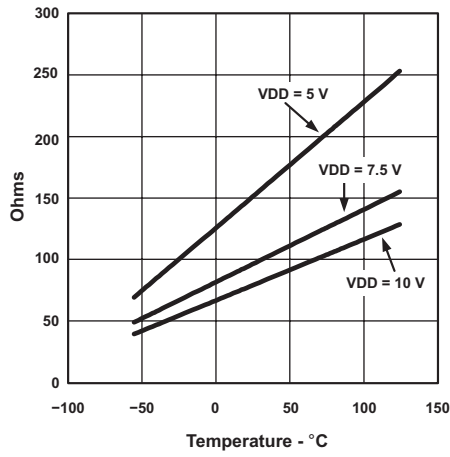


Figure 7. RC $R_{DS(on)}$ vs Temperature

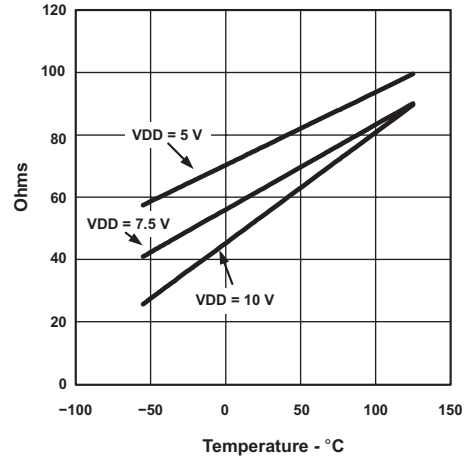


Figure 8. CS $R_{DS(on)}$ vs Temperature

7 Detailed Description

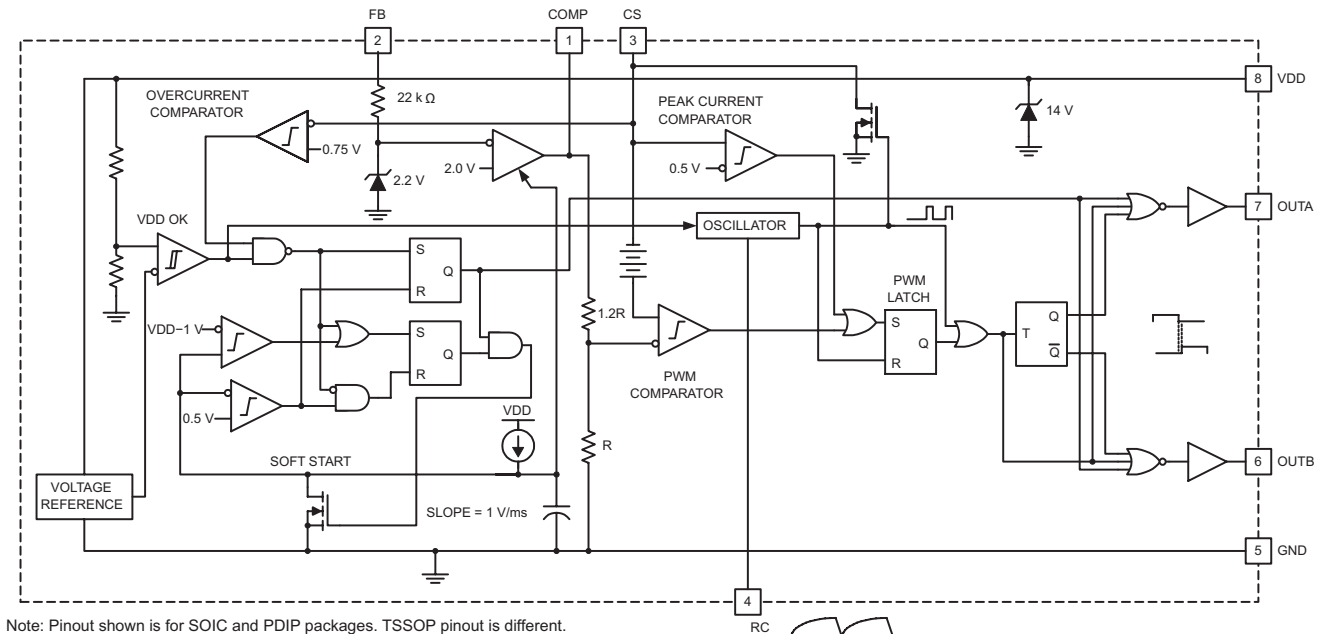
7.1 Overview

The UCCx808A-x device is a highly integrated, low-power current mode push-pull PWM controller. The controller employs low starting current and an internal control algorithm that offers accurate output voltage regulation in the presence of line and load variations. The UCCx808A-x family of parts has UVLO thresholds and hysteresis options for off-line and battery-powered systems.

Table 1. Undervoltage Lockout Levels

PART NUMBER	TURNON THRESHOLD	TURNOFF THRESHOLD
UCCx808A-1	12.5	8.3
UCCx808A-1	4.3	4.1

7.2 Functional Block Diagrams



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The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time. The output stages switch a 1/2 the oscillator frequency, with ensured duty cycle of < 50% for both outputs.

Figure 9. Block Diagram

Functional Block Diagrams (continued)

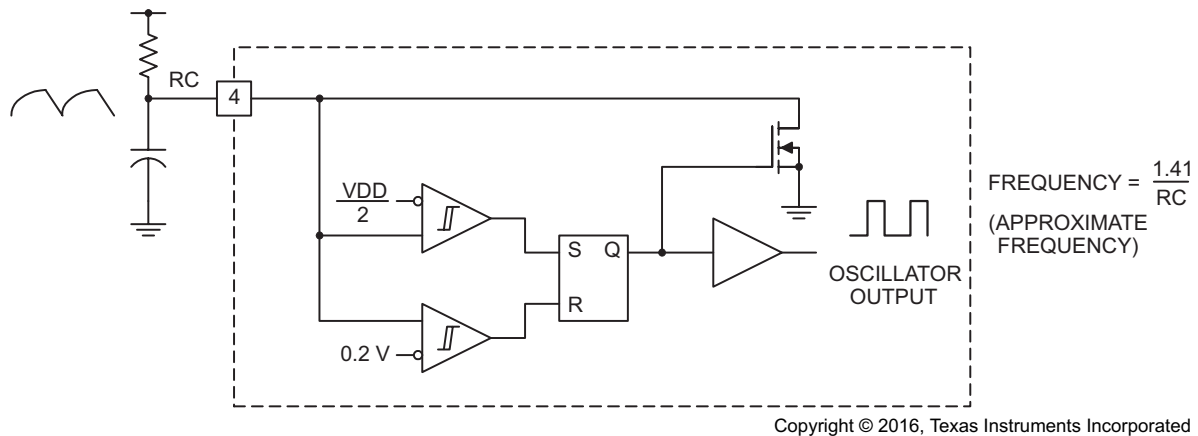


Figure 10. Block Diagram of Oscillator

7.3 Feature Description

7.3.1 Pin Descriptions

7.3.1.1 COMP

The COMP pin is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC3808 is a true low-output impedance, 2-MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND.

The UCC3808 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

7.3.1.2 CS

The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft-start cycle.

7.3.1.3 FB

The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

7.3.1.4 GND

Reference ground and power ground for all functions. Because of high currents, and high-frequency operation of the UCC3808, a low-impedance printed-circuit board ground plane is highly recommended.

7.3.1.5 OUTA and OUTB

Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak source current, and 1-A peak sink current.

The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This dead time between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60 ns to 200 ns and depends upon the values of the timing capacitor and resistor.

The high-current output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external Schottky clamp diodes are not required.

Feature Description (continued)

7.3.1.6 RC

The oscillator programming pin. The oscillator of the UCC3808-x tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. [Figure 10](#) shows the oscillator block diagram.

Only two components are required to program the oscillator: a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by [Equation 1](#).

$$f_{\text{OSCILLATOR}} = \frac{1.41}{RC}$$

where

- frequency is in Hz
 - resistance in Ω
 - capacitance in Farads
- (1)

The recommended range of timing resistors is between 10 k Ω and 200 k Ω and range of timing capacitors is between 100 pF and 1000 pF. Timing resistors less than 10 k Ω must be avoided.

For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.

7.3.1.7 VDD

The power input connection for this device. Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated with [Equation 2](#).

$$I_{\text{OUT}} = Q_g \times F$$

where

- F is frequency
- (2)

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. TI recommends a 1- μ F decoupling capacitor.

7.4 Device Functional Modes

7.4.1 VCC

When VCC rises above 12.5 V (for the UCCx808A-1) or above 4.3 V (for the UCCx808-2) the device is enabled. When any fault conditions are cleared, a soft-start condition is initiated and the gate driver outputs begin switching.

When VCC drops below 8.3 V (for the UCCx808-1) or 4.1 V (for the UCCx808-2) the device enters the UVLO protection mode and both gate drivers are actively pulled low.

7.4.2 Push-Pull or Half-Bridge Function

Because the device provides alternate 180° out-of-phase gate drive signals (OUTA and OUTB), it may be used as a controller for the push-pull or half-bridge topologies. For the half-bridge topology the UCCx808A-x requires an external high side gate driver or pulse transformer on one or both of the OUTA and OUTB signals.

8 Application and Implementation

NOTE

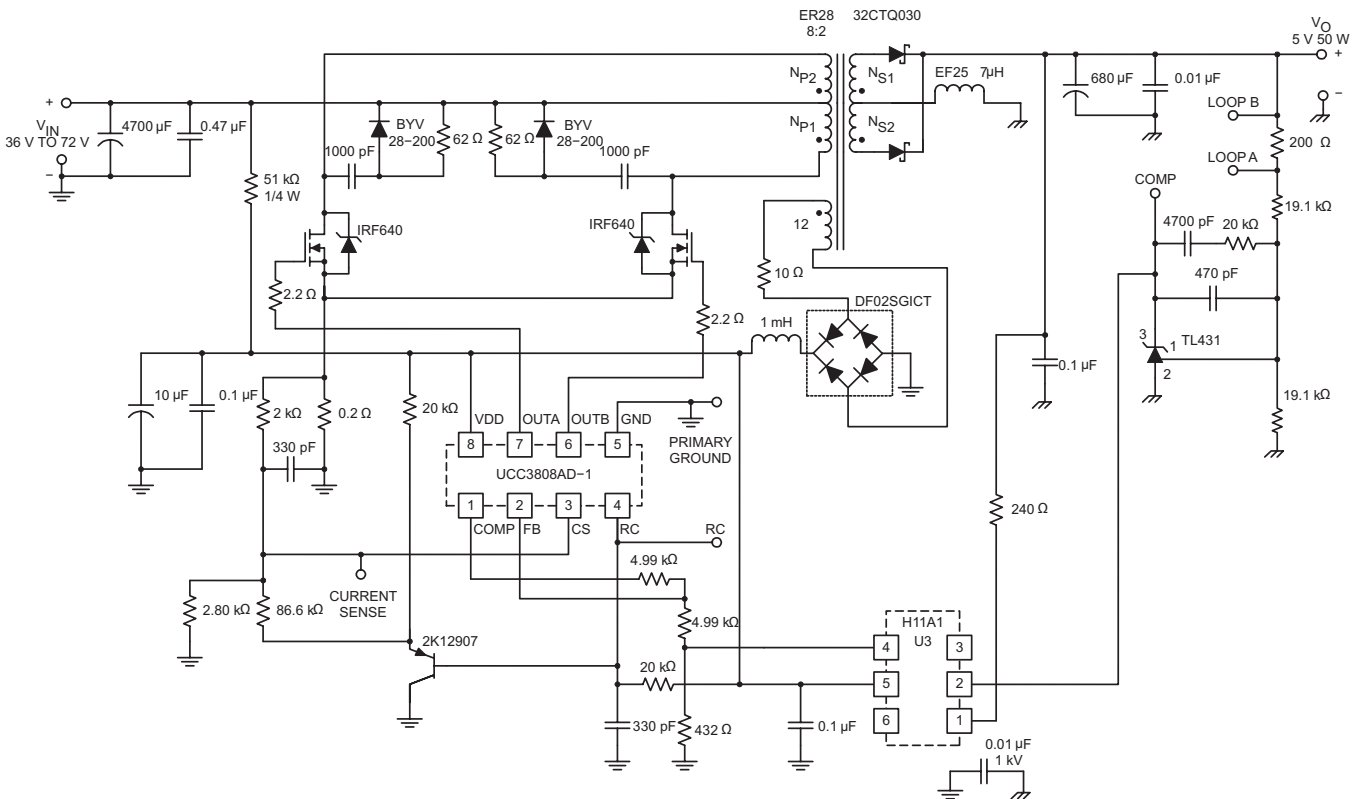
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A 200-kHz push-pull application circuit with a full-wave rectifier is shown in Figure 11. The output, V_O , provides 5 V at 50 W maximum and is electrically isolated from the input. Because the UCC3808A is a peak-current-mode controller the 2N2907 emitter following amplifier (buffers the CT waveform) provides slope compensation which is necessary for duty ratios greater than 50%. Capacitor decoupling is very important with a single ground IC controller, and a 1 μ F is suggested as close to the IC as possible. The controller supply is a series RC for start-up, paralleled with a bias winding on the output inductor used in steady-state operation.

Isolation is provided by an optocoupler with regulation done on the secondary side using the TL431 adjustable precision shunt regulator. Small signal compensation with tight voltage regulation is achieved using this part on the secondary side. Many choices exist for the output inductor depending on cost, volume, and mechanical strength. Several design options are iron powder, molypermalloy (MPP), or a ferrite core with an air gap as shown here. The main power transformer has a Magnetics Inc. ER28 size core made of P material for efficient operation at this frequency and temperature. The input voltage may range from 36 Vdc to 72 Vdc.

8.2 Typical Application



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Figure 11. Typical Application Diagram: 48-Vin, 5-V, 50-W Output

Typical Application (continued)

8.2.1 Design Requirements

Table 2 lists the design parameters for the UCC3808A-x.

Table 2. Design Parameters

PARAMETER	VALUE
Output voltage	5 V
Rated output power	50 W
Input DC voltage range	36 V to 72 V
Switching frequency	210 kHz

8.2.2 Detailed Design Procedure

The output, VO, provides 5 V at 50 W maximum and is electrically isolated from the input. Because the UCC3808A is a peak current mode controller, the 2N2907 emitter follower amplifier buffers the oscillator waveform (RC pin) and provides slope compensation to the current sense (CS) input. This is necessary for duty cycle ratios of greater than 50%.

Capacitor decoupling is provided on the VDD pin. TI recommends using a minimum decoupling capacitance of 10- μ F electrolytic and 0.1- μ F ceramic. The ceramic capacitor must be as close to the VDD pin as possible. The UCC3808A is initially powered up from the 36-V to 72-V input supply. Once the power supply has started, the bias supply is provided by an auxiliary winding on the main power transformer.

Isolation is provided by an optocoupler with regulation done on the secondary side using the TL431 precision programmable reference. The internal error amplifier of the UCC3808A is set up as a unity gain amplifier and the compensation network is provided on the secondary side.

Many choices exist for the output inductor depending on cost and size constraints. Design options are powdered iron, molypermalloy or the ferrite core option used in this design. The power transformer is a low profile design, EFD25 size, using the Magnetics Inc. P material. This material is a good choice for low power loss at high switching frequency.

The switching frequency is set at 210 kHz with the RC network on the RC pin.

8.2.3 Application Curves

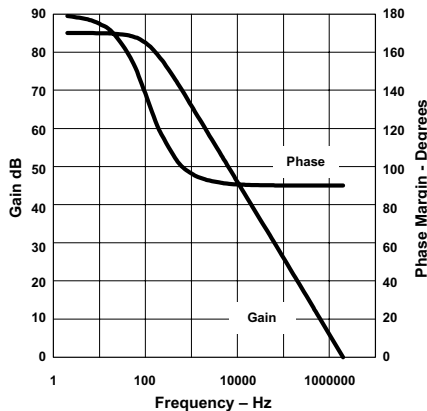


Figure 12. Error Amplifier Gain and Phase Response vs Frequency

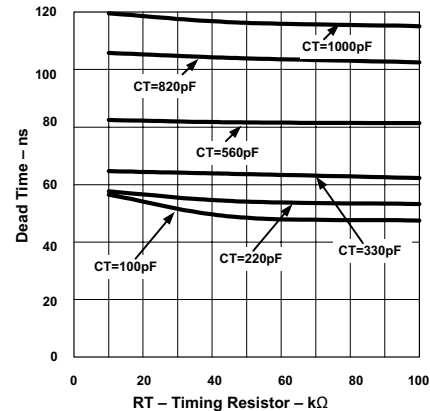


Figure 13. Dead Time vs Timing Resistor

9 Power Supply Recommendations

The VDD power terminal for the device requires the placement of electrolytic capacitor as energy storage capacitor because of the 1-A drive capability of the UCCx808A-x controller. Also a low-ESR noise decoupling capacitor is required and it must be placed as close as possible to the VDD and GND pins. Ceramic capacitors with stable dielectric characteristics over temperature are recommended. X7R is a suitable dielectric material for use here.

TI recommends a 10- μ F, 25-V electrolytic capacitor part.

10 Layout

10.1 Layout Guidelines

1. Place the VDD capacitor as close as possible between the VDD pin and GND of the UCCx808A-x, tracked directly to both pins.
2. A small, external filter capacitor is recommended on the CS pin. Track the filter capacitor as directly as possible from the CS to GND pins.
3. The tracking and layout of the FB pin and connecting components is critical to minimizing noise pickup and interference. Reduce the total surface area of traces on the FB net to a minimum.
4. The OUTA and OUTB pins have a high-current source and sink capability. An external gate resistor is recommended to damp oscillations. A value of around a few Ohms is recommended. A pull-down resistor on the gate to source is recommended to prevent the MOSFET gate from floating on if there is an open-circuit fault in the gate drive path.

10.2 Layout Example

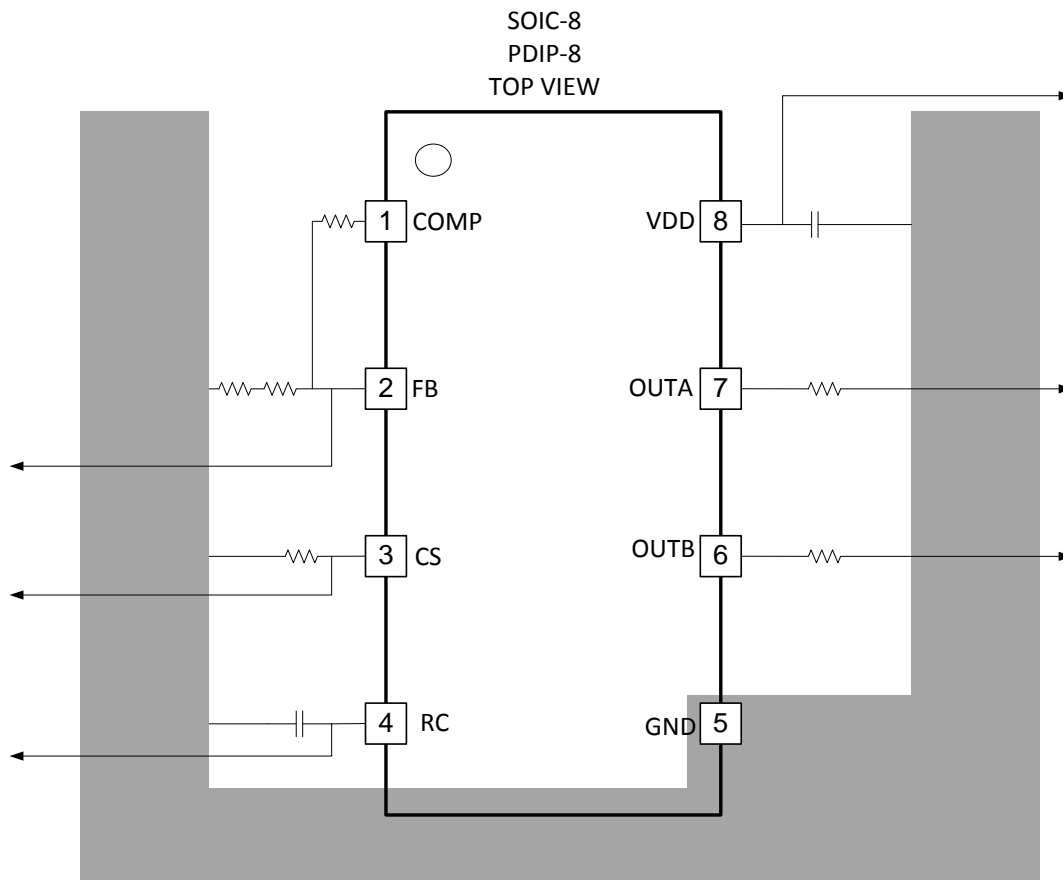


Figure 14. Recommended Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

[Power Supply Control Products Data Book](#)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC2808A-1	Click here	Click here	Click here	Click here	Click here
UCC2808A-2	Click here	Click here	Click here	Click here	Click here
UCC3808A-1	Click here	Click here	Click here	Click here	Click here
UCC3808A-2	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2808AD-1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-1	Samples
UCC2808AD-1G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-1	Samples
UCC2808AD-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-2	Samples
UCC2808AD-2G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-2	Samples
UCC2808ADTR-1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-1	Samples
UCC2808ADTR-1G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-1	Samples
UCC2808ADTR-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-2	Samples
UCC2808ADTR-2G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-2	Samples
UCC2808AN-1	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2808A N-1	Samples
UCC2808AN-2	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2808A N-2	Samples
UCC2808AN-2G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2808A N-2	Samples
UCC2808APW-1	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2808A1	Samples
UCC2808APW-1G4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2808A1	Samples
UCC2808APW-2	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2808A2	Samples
UCC2808APW-2G4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2808A2	Samples
UCC2808APWTR-2	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2808A2	Samples
UCC3808AD-1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-1	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC3808AD-1G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-1	Samples
UCC3808AD-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-2	Samples
UCC3808AD-2G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-2	Samples
UCC3808ADTR-1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-1	Samples
UCC3808ADTR-1G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-1	Samples
UCC3808ADTR-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-2	Samples
UCC3808ADTR-2G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-2	Samples
UCC3808AN-1	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3808A N-1	Samples
UCC3808AN-1G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3808A N-1	Samples
UCC3808AN-2	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3808A N-2	Samples
UCC3808APW-2	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3808A2	Samples
UCC3808APWTR-2	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3808A2	Samples
UCC3808APWTR-2G4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3808A2	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2808ADTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2808ADTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2808APWTR-2	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3808ADTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3808ADTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3808APWTR-2	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2808ADTR-1	SOIC	D	8	2500	340.5	338.1	20.6
UCC2808ADTR-2	SOIC	D	8	2500	340.5	338.1	20.6
UCC2808APWTR-2	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC3808ADTR-1	SOIC	D	8	2500	340.5	338.1	20.6
UCC3808ADTR-2	SOIC	D	8	2500	340.5	338.1	20.6
UCC3808APWTR-2	TSSOP	PW	8	2000	367.0	367.0	35.0

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