

200V N-Channel Enhancement Mode MOSFET

Description

The IRFB260N is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

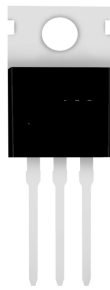
Product Summary

VDS =200V, ID =60A
RDS(ON) <50mΩ@ VGS=10V

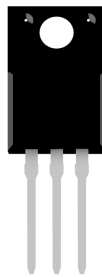
Application

Power amplifier

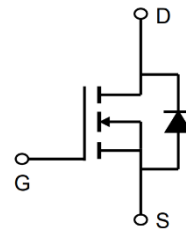
Pin Configuration



TO-220-3L



TO-220F



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
IRFB260N	TO-220-3L	60N20G	1000
IRFB260NF	TO-220F	60N20GF	1000

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage	200	V
ID	Drain Current -continuous	60	A
IDM	Drain Current -pulse	120	A
VGSS	Gate-Source Voltage	±30	V
EAS	Single Pulsed Avalanche Energy	588	mJ
IAR	Avalanche Current	40	A
EAR	Repetitive Avalanche Current	15.8	mJ
dv/dt	Peak Diode Recovery dv/dt	5.5	V/ns
PD TC=25°C	Power Dissipation	158	W
TJ, TSTG	Operating and Storage Temperature Range	-55~+150	°C
TL	Maximum Lead Temperature for Soldering Purposes	300	°C
Rth(j-c)	Thermal Resistance, Junction to Case	0.79	°C/W
Rth(j-A)	Thermal Resistance, Junction to Ambient	62.5	°C/W

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Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Tests conditions	Min	Typ	Max	Units
BV _{DSS}	Drain-Source Voltage	I _D =250μA, V _{GS} =0V	200	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D =250μA, referenced to 25°C	-	0.19	-	V/°C
IDSS	Zero Gate Voltage Drain Current	V _{DS} =200V, V _{GS} =0V, T _C =25°C	-	-	1	μA
IGSSF	Gate-body leakage current, forward	V _{DS} =0V, V _{GS} =30V	-	-	100	nA
IGSSR	Gate-body leakage current, reverse	V _{DS} =0V, V _{GS} =-30V	-	-	-100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250μA	2.0	-	4.0	V
RDS(ON)	Static Drain-Source On-Resistance	V _{GS} =10V , I _D =14.0A	-	38	50	mΩ
g _{fs}	Forward Transconductance	V _{DS} = 40V , I _D =14.0A	-	24	-	S
C _{iss}	Input capacitance	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	-	2879	3742	pF
C _{oss}	Output capacitance		-	362	470	pF
C _{rss}	Reverse transfer capacitance		-	81	105	pF
t _{d(on)}	Turn-On delay time	V _{DD} =100V, I _D =28A, R _G =25Ω, V _{GS} =10V (note 4, 5)	-	28	69	ns
t _r	Turn-On rise time		-	251	494	ns
t _{d(off)}	Turn-Off delay time		-	309	617	ns
t _f	Turn-Off Fall time		-	220	412	ns
Q _g	Total Gate Charge	V _{DS} =160V , I _D =28A, V _{GS} =10V (note 4, 5)	-	103	136	nC
Q _{gs}	Gate-Source charge		-	16	-	nC
Q _{gd}	Gate-Drain charge		-	53	-	nC
I _S	Maximum Continuous Drain-Source Diode Forward Current		-	-	28	A
ISM	Maximum Pulsed Drain-Source Diode Forward Current		-	-	112	A
VSD	Maximum Continuous Drain-Source Diode Forward Current	V _{GS} =0V, I _S =28A	-		1.4	V
t _{rr}	Reverse recovery time	V _{GS} =0V, I _S =28A di/dt=100A/μs (note 4)		218		ns
Q _{rr}	Reverse recovery charge			1.91		μC

Notes:

- 1: Pulse width limited by maximum junction temperature
- 2: L=1.5mH, I_{AS}=28A, V_{DD}=50V, R_G=25 Ω, Starting T_J=25°C
- 3: I_{SD} ≤28A, di/dt ≤200A/μs, V_{DD}≤BV_{DSS}, Starting T_J=25°C
- 4: Pulse Test: Pulse Width ≤300μs, Duty Cycle≤2%
- 5: Essentially independent of operating temperature

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Electrical Characteristics Diagrams

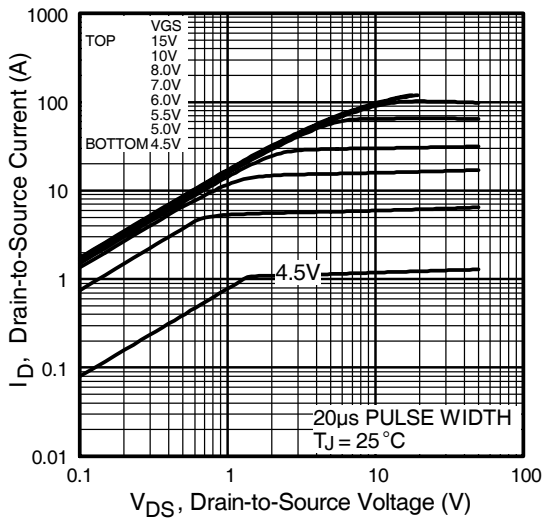


Fig 1. Typical Output Characteristics

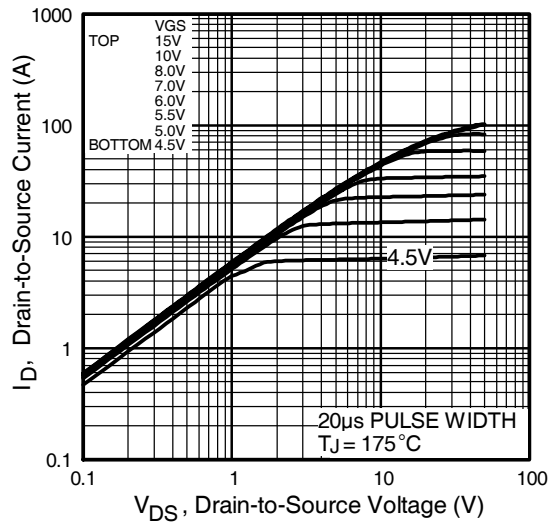


Fig 2. Typical Output Characteristics

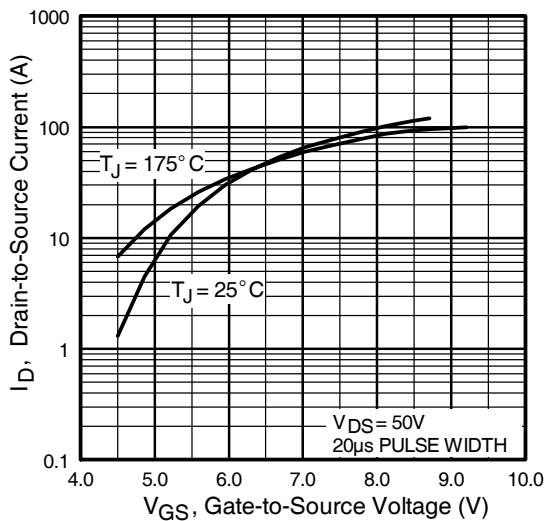


Fig 3. Typical Transfer Characteristics

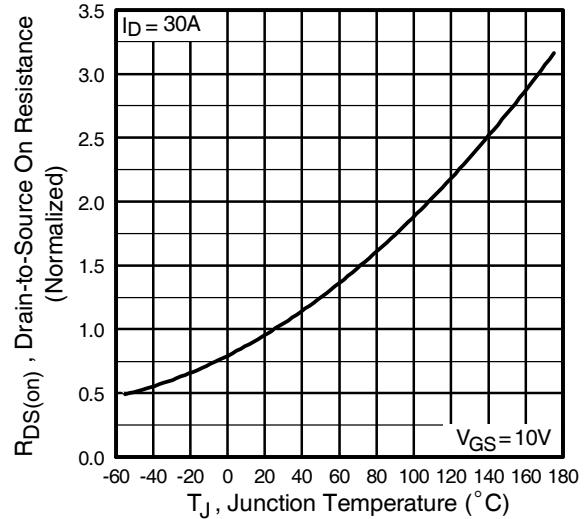


Fig 4. Normalized On-Resistance Vs. Temperature

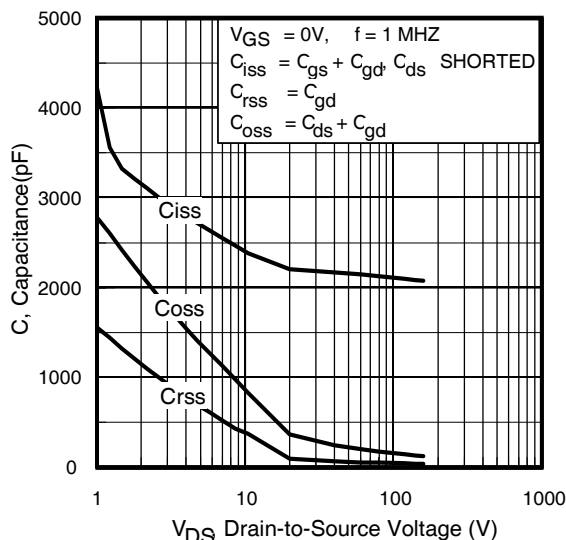


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

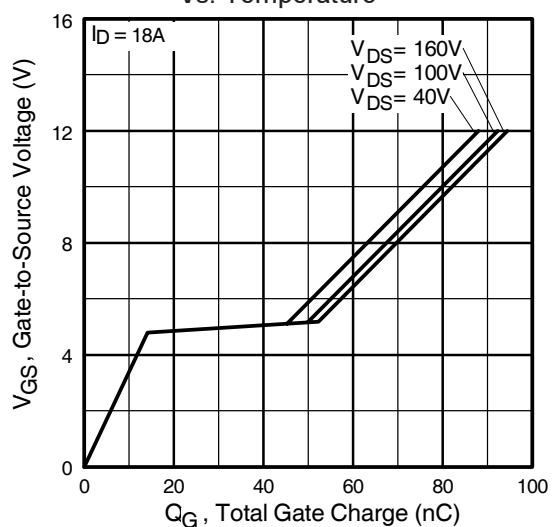


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

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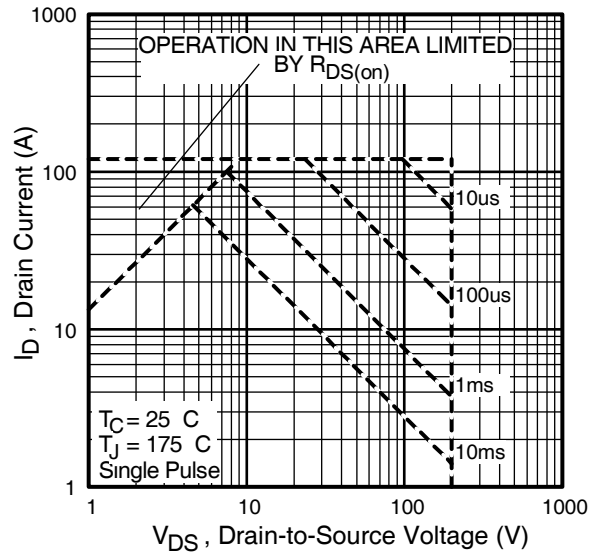
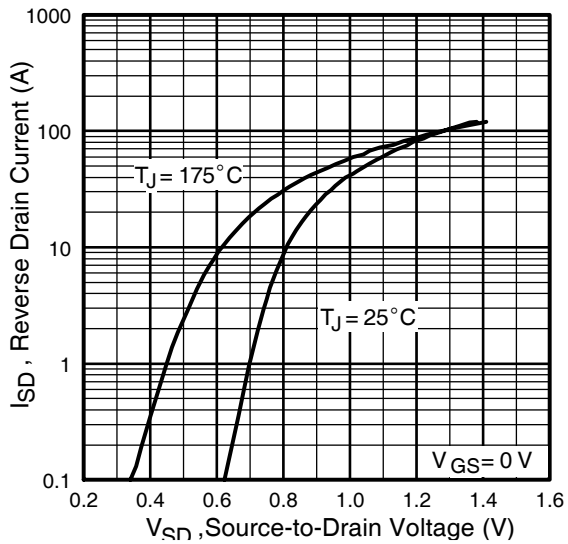


Fig 8. Maximum Safe Operating Area

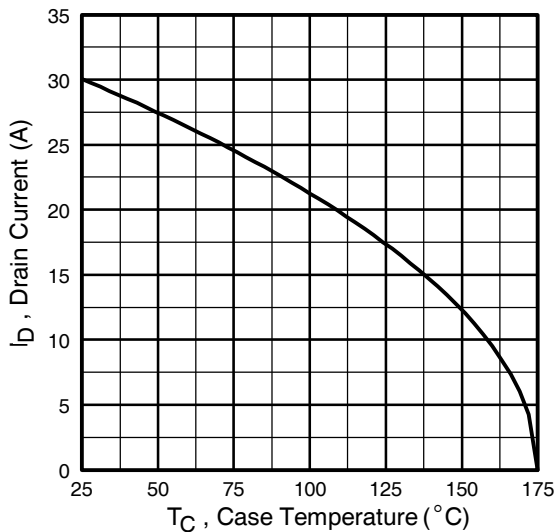


Fig 9. Maximum Drain Current Vs. Case Temperature

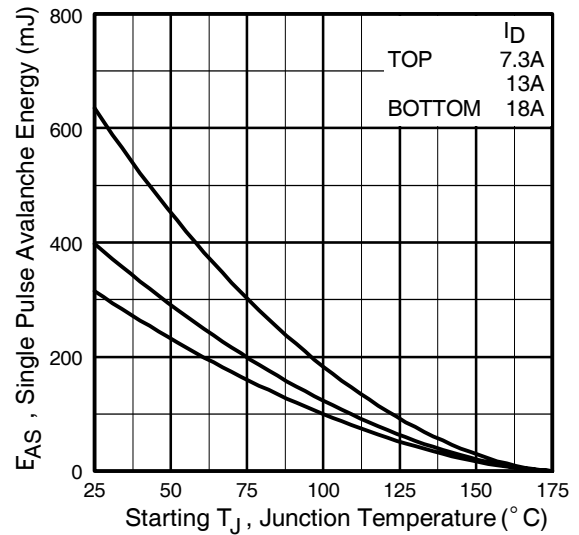


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

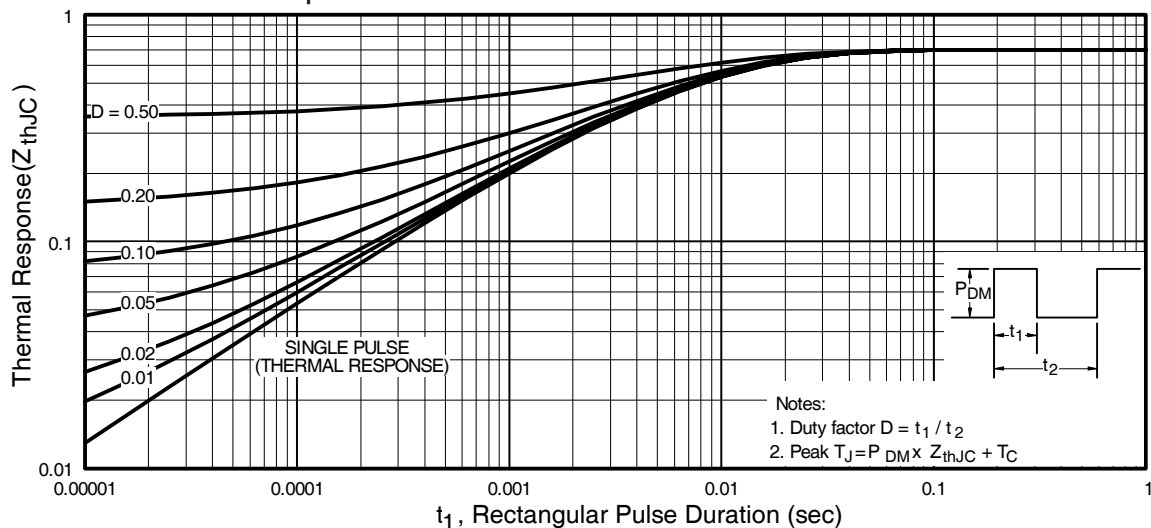


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

TO-220-3L

