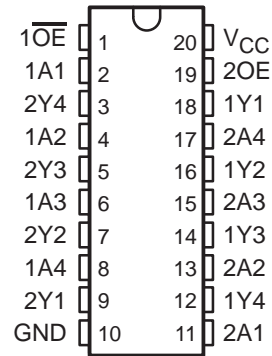


SN64BCT757 OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS

SCBS479 – MARCH 1993 – REVISED MAY 1994

- BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- High-Impedance State During Power Up and Power Down
- Open-Collector Outputs Drive Bus Lines or Buffer-Memory Address Registers
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic and Ceramic 300-mil DIPs (N)

DW OR N PACKAGE
(TOP VIEW)



description

This octal buffer and line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device provides complementary output-enable (OE and \overline{OE}) inputs and noninverting outputs.

The SN64BCT757 is characterized for operation from -40°C to 85°C and 0°C to 70°C .

FUNCTION TABLES

INPUTS		OUTPUT
$\overline{1OE}$	1A	1Y
H	X	H
L	L	L
L	H	H

INPUTS		OUTPUT
2OE	2A	2Y
L	X	H
H	L	L
H	H	H

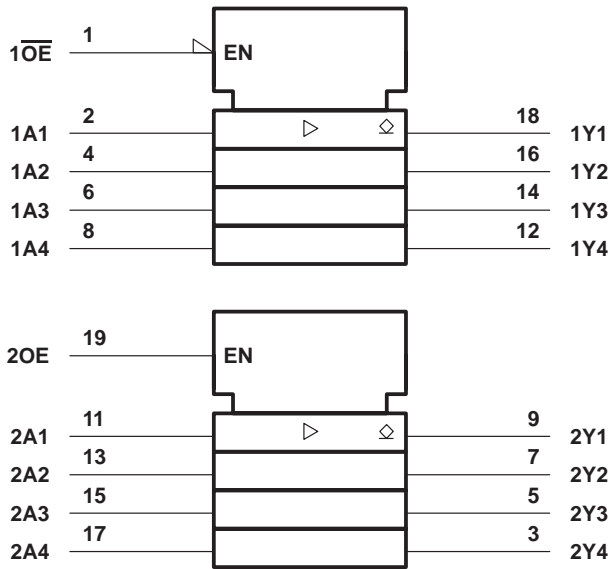
SN64BCT757

OCTAL BUFFER/DRIVER

WITH OPEN-COLLECTOR OUTPUTS

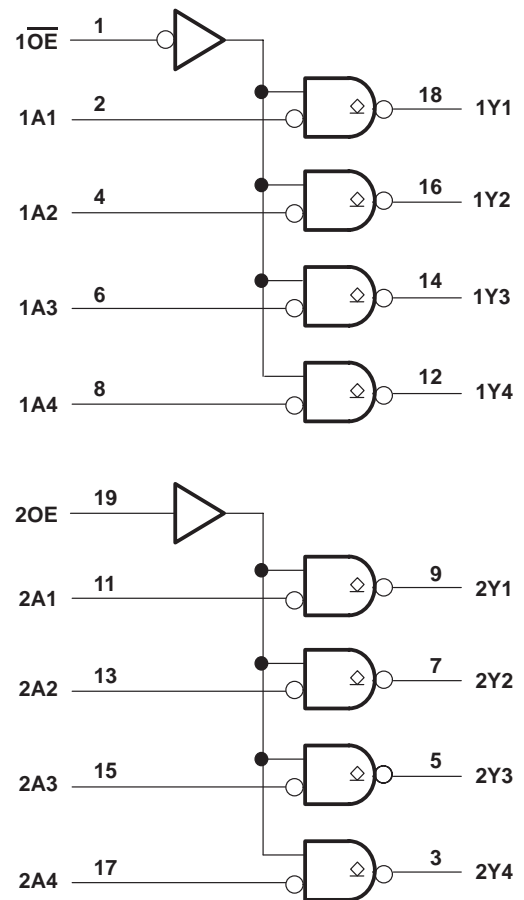
SCBS479 – MARCH 1993 – REVISED MAY 1994

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	-0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	-0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$)	-30 mA
Current into any output in the low state, I_O	128 mA
Operating free-air temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage ratings may be exceeded if the input clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
V _{OH}	High-level output voltage			5.5	V
I _{IK}	Input clamp current			-18	mA
I _{OL}	Low-level output current			64	mA
Δt/ΔV _{CC}	Power-up ramp rate	2			μs/V
T _A	Operating free-air temperature	-40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2	V
I _{OH}	V _{CC} = 4.5 V,	V _{OH} = 5.5 V			0.1	mA
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 64 mA	0.42	0.55		V
I _{OZ}	V _{CC} = 0 to 2.3 V (power up),	V _O = 2.7 V, \overline{OE} = 0.8 V or OE = 2 V			50	μA
I _{OZ}	V _{CC} = 1.8 V to 0 (power down),	V _O = 2.7 V, \overline{OE} = 0.8 V or OE = 2 V			50	μA
I _I	V _{CC} = 5.5 V,	V _I = 7 V			0.1	mA
I _{IH}	V _{CC} = 5.5 V,	V _I = 2.7 V			20	μA
I _{IL}	V _{CC} = 5.5 V,	V _I = 0.5 V			-1	mA
I _{CC}	V _{CC} = 5.5 V,	Outputs open	Outputs high		34	mA
			Outputs low		77	
			OE and \overline{OE} inactive		10	
C _i	V _{CC} = 5 V,	V _I = 2.5 V or 0.5 V		6		pF
C _o	V _{CC} = 5 V,	V _O = 2.5 V or 0.5 V		4		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended range of supply voltage, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			T _A = -40°C to 85°C		T _A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	6.9	8.3	9.6	6.5	11.2	6.6	10.1	ns
t _{PHL}			2.4	4.2	6	1.9	7	2	6.6	
t _{PLH}	2OE	Y	11	14.8	17.9	10.4	21.3	10.8	19.7	ns
t _{PHL}			2.9	4.6	6.2	2.6	7.5	2.6	6.9	
t _{PLH}	$\overline{1OE}$	Y	11.4	13.9	16.1	8.9	19.9	10	18	ns
t _{PHL}			4.4	6.1	7.8	4	9.2	4	8.5	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN64BCT757DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6BCT757	Samples
SN64BCT757DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6BCT757	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

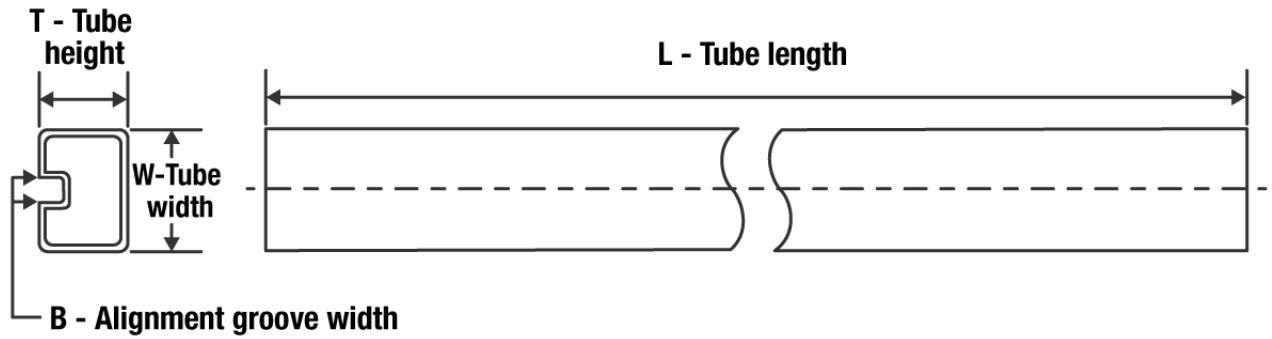

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN64BCT757DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN64BCT757DWR	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN64BCT757DW	DW	SOIC	20	25	507	12.83	5080	6.6

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated