LP2980-ADJ Micropower 50 mA Ultra Low-Dropout Adjustable Voltage Regulator in SOT-23

Check for Samples: LP2980-ADJ

FEATURES

- **Ultra Low Dropout Voltage**
- **Output Adjusts from 1.23V to 15V**
- **Specified 50 mA Output Current**
- **Uses Tiny SOT-23 Package**
- **Requires Few External Components**
- **<1 µA Quiescent Current when Shutdown**
- **Low Ground Pin Current at All Loads**
- **High Peak Current Capability (150 mA Typical)**
- **Wide Supply Voltage Range (2.5V–16V)**
- **Overtemperature/overcurrent Protection**
- **−40°C to +125°C Junction Temperature Range**

APPLICATIONS

- **Cellular Phone**
- **Palmtop/Laptop Computer**
- **Camcorder, Personal Stereo, Camera**

DESCRIPTION

The LP2980-ADJ is a 50 mA adjustable voltage regulator designed to provide ultra low dropout in battery powered applications.

Using an optimized VIP (vertically Integrated PNP) process, the LP2980-ADJ delivers unequaled performance in all specifications critical to battery-powered designs:

Adjustable Output: output voltage can be set from 1.23V to 15V.

Precision Reference: 1.0% tolerance.

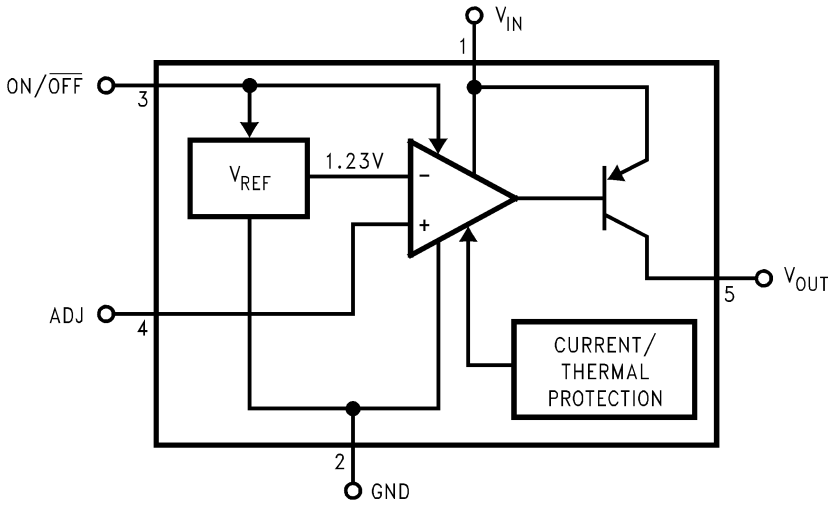
Dropout Voltage: typically 120 mV @ 50 mA load, and 7 mV @ 1 mA load.

Ground Pin Current: typically 320 µA @ 50 mA load, and 80 µA @ 1 mA load.

Sleep Mode: less than 1 µA quiescent current when on/off pin is pulled low.

Smallest Possible Size: Package uses minimum board space.

Block Diagram



Connection Diagram

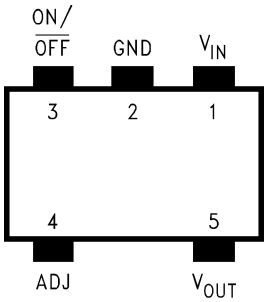


Figure 1. 5-Lead Small Outline Package
Top View
See Package Number DBV0005A

PIN DESCRIPTIONS

Name	Pin Number	Function
V_{IN}	1	Input Voltage
GND	2	Common Ground (device substrate)
ON/OFF	3	Logic high enable pin
ADJ	4	Output voltage feedback pin
V_{OUT}	5	Regulated output voltage

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Storage Temperature Range	−65 to +150°C
Operating Junction Temperature Range	−40 to +125°C
Lead Temp. (Soldering, 5 seconds)	260°C
ESD Rating (3)	2 kV
Power Dissipation (4)	Internally Limited
Input Supply Voltage (Survival)	−0.3V to +16V
Input Supply Voltage (Operating)	2.5V to +16V
Shutdown Input Voltage (Survival)	−0.3V to +16V
Output Voltage (Survival) (5)	−0.3V to 16V
I_{OUT} (Survival)	Short Circuit Protected
Input-Output Voltage (Survival) (6)	−0.3V to 16V

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The ESD rating of pins 3 and 4 is 1 kV.
(4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$. The value of θ_{J-A} for the SOT-23 package is 300°C/W. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(5) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2980-ADJ output must be diode-clamped to ground.
(6) The output PNP structure contains a diode between the V_{IN} and V_{OUT} terminals that is normally reverse-biased. Reversing the polarity from V_{IN} to V_{OUT} will turn on this diode (see APPLICATION HINTS).

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 4.3V, V_{OUT} = 3.3V, I_L = 1 mA, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, $V_{ON/OFF}$ = 2V.

Symbol	Parameter	Conditions	Typ	LP2980I-ADJ (1)		Units
				Min	Max	
V_{REF}	Reference Voltage		1.225	1.213	1.237	V
		1 mA < I_L < 50 mA V_{OUT} + 1 ≤ V_{IN} ≤ 16V	1.225	1.206 **1.182**	1.243 **1.268**	
$\Delta V_{REF}/\Delta V_{IN}$	Reference Voltage Line Regulation	2.5V ≤ V_{IN} ≤ 16V	3		6.0 **15.0**	mV
$V_{IN}–V_O$	Dropout Voltage (2)	I_L = 0	1		3 **5**	mV
		I_L = 1 mA	7		10 **15**	
		I_L = 10 mA	40		60 **90**	
		I_L = 50 mA	120		150 **225**	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1V differential.

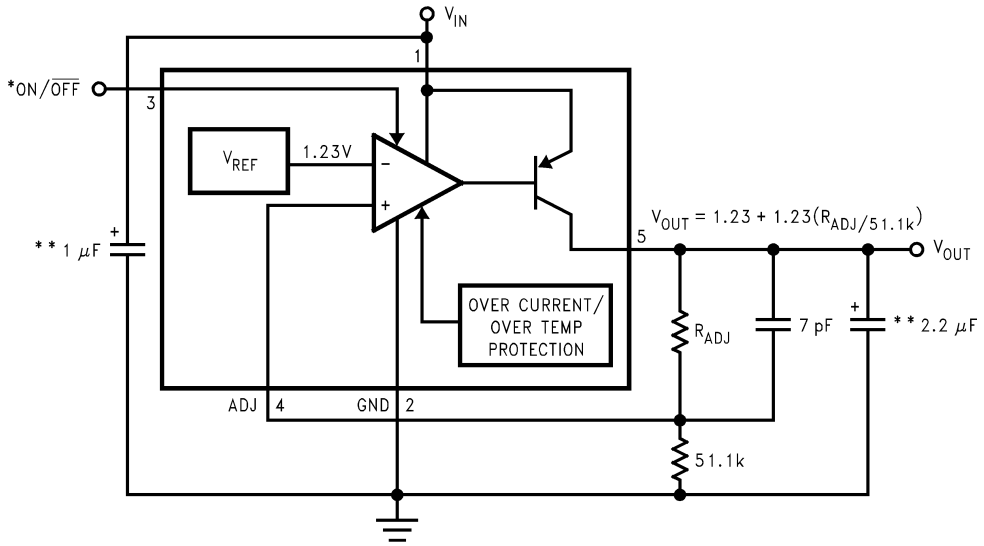
ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 4.3V, V_{OUT} = 3.3V, I_L = 1 mA, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, $V_{ON/OFF}$ = 2V.

Symbol	Parameter	Conditions	Typ	LP2980I-ADJ (1)		Units
				Min	Max	
I_{GND}	Ground Pin Current	I_L = 0	60		95 **125**	µA
		I_L = 1 mA	80		110 **170**	
		I_L = 10 mA	120		220 **460**	
		I_L = 50 mA	320		600 **1200**	
		$V_{ON/OFF}$ < 0.18V	0.01		**1**	
I_{ADJ}	ADJ Pin Bias Current	1 mA ≤ I_L ≤ 50 mA	150		350	nA
$V_{ON/OFF}$	ON/OFF Input Voltage (3)	High = O/P ON	1.4	**1.6**		V
		Low = O/P OFF	0.55		**0.18**	
$I_{ON/OFF}$	ON/OFF Input Current	$V_{ON/OFF}$ = 0	0.01		**−1**	µA
		$V_{ON/OFF}$ = 5V	5		**15**	
I_O(PK)	Peak Output Current	V_{OUT} ≥ V_O(NOM) − 5%	150	100		mA
e_n	Output Noise Voltage (RMS)	BW = 300 Hz to 50 kHz, C_{OUT} = 10 µF	160			µV
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple Rejection	f = 1 kHz C_{OUT} = 10 µF	68			dB
I_O(MAX)	Short Circuit Current	R_L = 0 (Steady State) (4)	150			mA

(3) The ON/OFF input must be properly driven to prevent possible misoperation. For details, refer to APPLICATION HINTS.
(4) See TYPICAL PERFORMANCE CHARACTERISTICS curves.

TYPICAL APPLICATION CIRCUIT



*ON/$\overline{OFF}$ INPUT MUST BE ACTIVELY TERMINATED. TIE TO V_{IN} IF THIS FUNCTION IS NOT TO BE USED.
**MINIMUM CAPACITANCE IS SHOWN TO ENSURE STABILITY OVER FULL LOAD CURRENT RANGE (SEE APPLICATION HINTS).

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: T_A = 25°C, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA, ON/OFF pin tied to V_{IN}, R_{ADJ} = 86.6k, and test circuit is as shown in Basic Application Circuit.

Output Voltage vs. Temperature

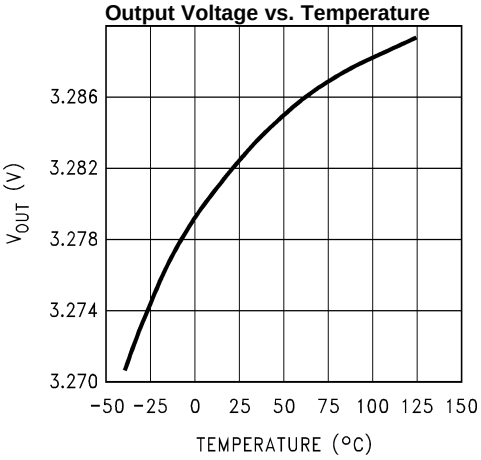


Figure 2.

Dropout Characteristics

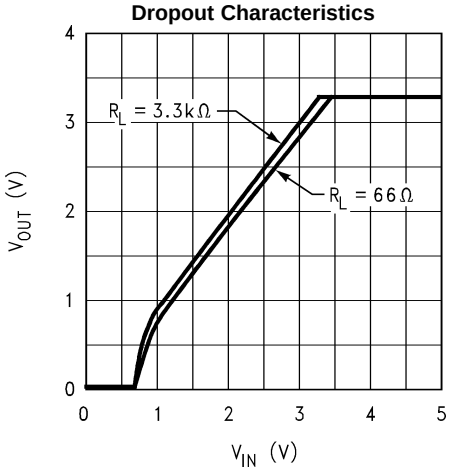


Figure 3.

Dropout Voltage vs. Temperature

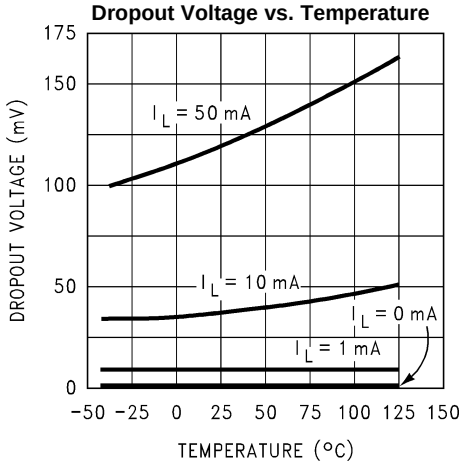


Figure 4.

Dropout Voltage vs. Load Current

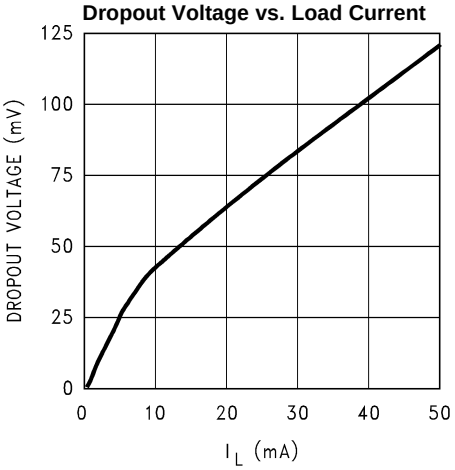


Figure 5.

Ground Pin Current vs. Temperature

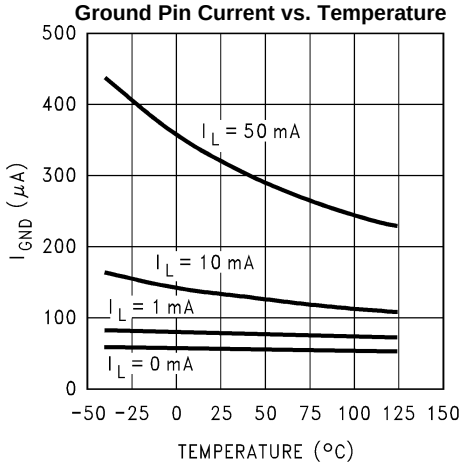


Figure 6.

Ground Pin Current vs. Load Current

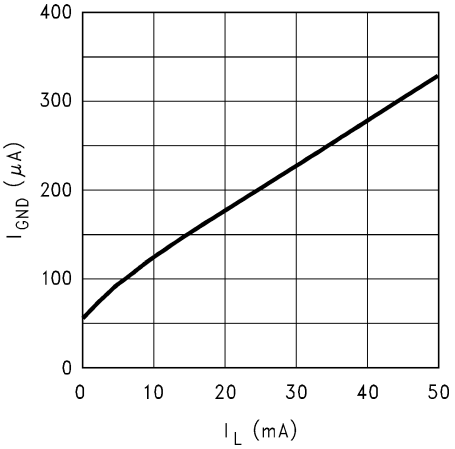


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA, ON/OFF pin tied to V_{IN}, R_{ADJ} = 86.6k, and test circuit is as shown in Basic Application Circuit.

Input Current vs. V_{IN}

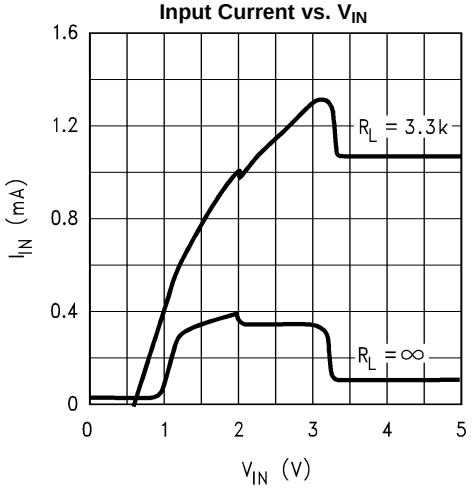


Figure 8.

Load Transient Response

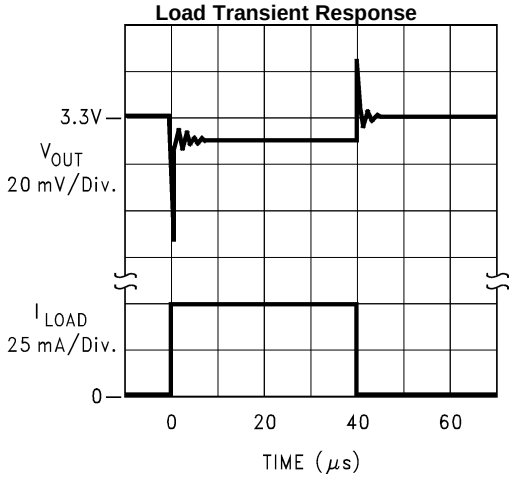


Figure 9.

Line Transient Response

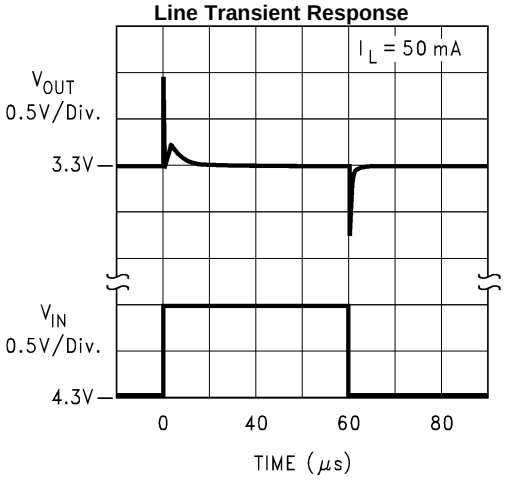


Figure 10.

Short Circuit Current

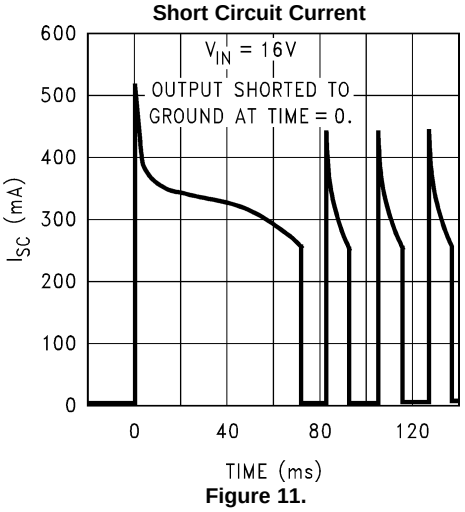


Figure 11.

Short Circuit Current

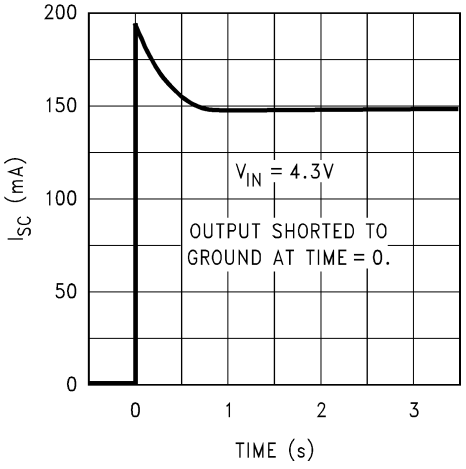


Figure 12.

Load Regulation

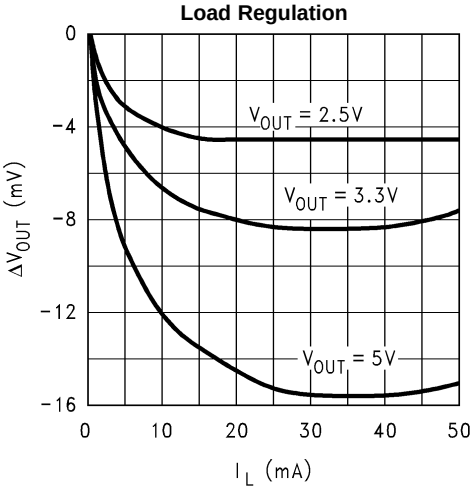


Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA, ON/OFF pin tied to V_{IN}, R_{ADJ} = 86.6k, and test circuit is as shown in Basic Application Circuit.

ADJ Pin Bias Current vs. Load Current

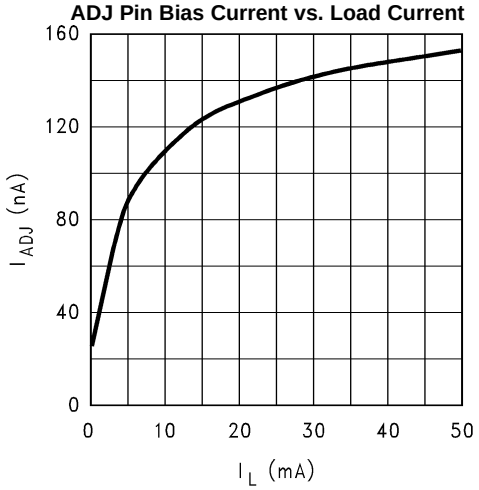


Figure 14.

ADJ Pin Bias Current vs. Temperature

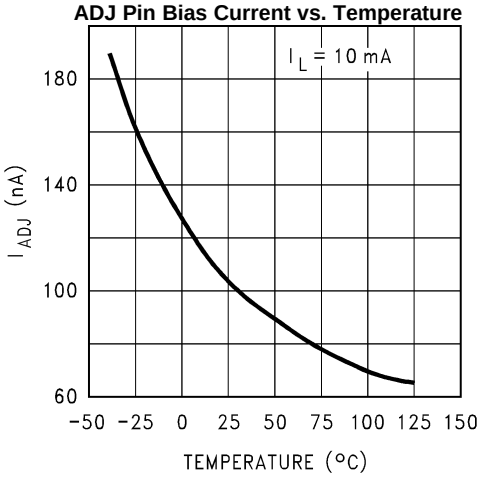


Figure 15.

ON/OFF Threshold vs.Temperature

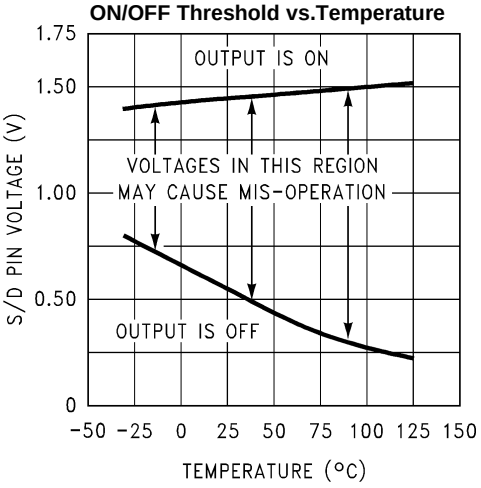


Figure 16.

Output Noise Density

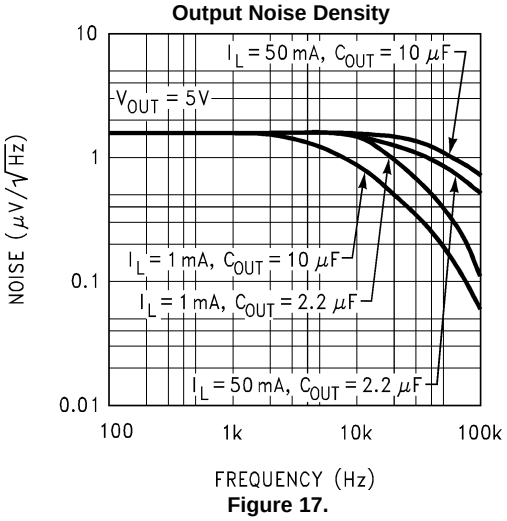


Figure 17.

Ripple Rejection

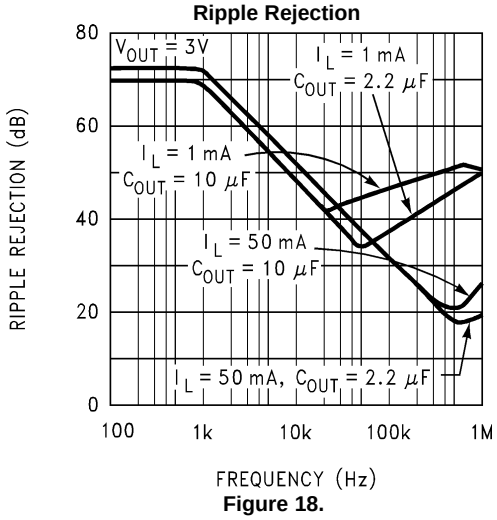


Figure 18.

APPLICATION HINTS

EXTERNAL CAPACITORS

Like any low-dropout regulator, the external capacitors must be selected carefully to assure regulator loop stability.

INPUT CAPACITOR: An input capacitor whose value is ≥1 µF is *required* (the amount of capacitance may be increased without limit).

Any good quality Tantalum or Ceramic capacitor may be used here. The capacitor must be located not more than 0.5″ from the input pin and returned to a clean analog ground.

OUTPUT CAPACITOR: The output capacitor must meet both the requirement for minimum amount of capacitance and E.S.R. (Equivalent Series Resistance) for stable operation.

Curves are provided below which show the allowable ESR of the output capacitor as a function of load current for both 2.2 µF and 4.7 µF. A solid Tantalum capacitor is the best choice for the output.

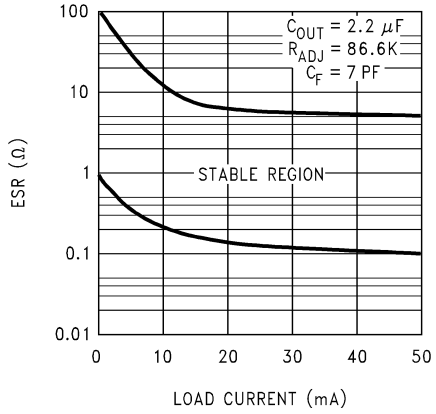


Figure 19. 2.2 µF ESR Curves

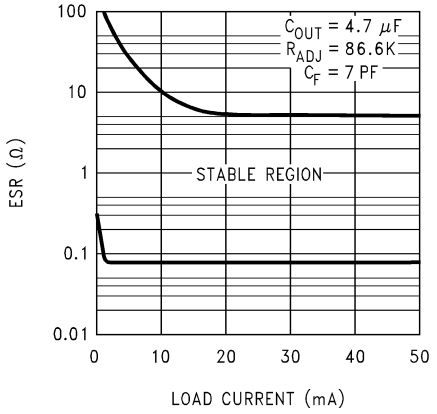


Figure 20. 4.7 µF ESR Curves

IMPORTANT: The output capacitor must maintain its ESR in the stable region *over the full operating temperature range* to assure stability. Also, capacitor tolerance and variation with temperature must be considered to assure the minimum amount of capacitance is provided at all times.

Note that this capacitor must be located not more than 0.5” from the output pin and returned to a clean analog ground.

FEED-FORWARD CAPACITOR: A 7 pF feed-forward capacitor is required (see Basic Application Circuit). The function of this capacitor is to provide the lead compensation necessary for loop stability.

A temperature-stable ceramic capacitor (type NPO or COG) should be used here.

CAPACITOR CHARACTERISTICS

TANTALUM: The best capacitor choice for the LP2980-ADJ output is solid Tantalum. The ESR of a good quality Tantalum is almost perfectly centered in the middle of the “stable” range of the ESR curve (about 0.5Ω–1Ω).

The temperature stability of Tantalums is typically very good, with a total variation of only about 2:1 over the temperature range of −40°C to +125°C (ESR increases at colder temperatures).

Off-brand capacitors should be avoided, as some poor quality Tantalums are seen with ESR's > 10Ω, and this usually causes oscillation problems.

One caution about Tantalums if they are used on the input: the ESR of a Tantalum is low enough that it can be destroyed by surge current if powered up from a low impedance source (like a battery) that has no limit on inrush current. In these cases, use a ceramic input capacitor which does not have this problem.

CERAMIC: Ceramics are generally larger and more costly than Tantalums for a given amount of capacitance. Also, they have a very low ESR which is quite stable with temperature.

Be warned that the ESR of a ceramic capacitor is typically low enough to make an LDO oscillate: a 2.2 µF ceramic demonstrated an ESR of about 15 mΩ when tested. If used as an output capacitor, this will cause instability (see ESR Curves).

If a ceramic is used on the output of an LDO, a small resistance (about 1Ω) should be placed in series with the capacitor. If it is used as an input capacitor, no resistor is needed as there is no requirement for ESR on capacitors used on the input.

EXTERNAL RESISTORS

The output voltage is set using two external resistors (see Basic Application Circuit). It is recommended that the resistor from the ADJ pin to ground be 51.1 kΩ.

The other resistor (R_{ADJ}) which connects between V_{OUT} and the ADJ pin is selected to set V_{OUT} as given by the formula:

$$V_{OUT} = V_{REF} + (V_{REF} \times (R_{ADJ} / 51.1\ k\Omega))$$

REVERSE CURRENT PATH

The PNP power transistor used as the pass element in the LP2980-ADJ has an inherent diode connected between the regulator output and input. During normal operation (where the input voltage is higher than the output) this diode is reverse biased (See Figure 21).

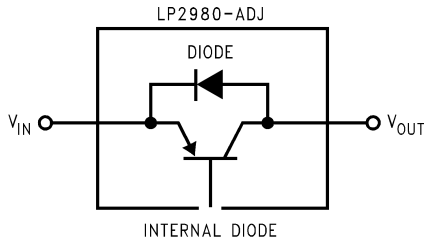


Figure 21. LP2980–ADJ Reverse Current Path

However, if the input voltage is more than a V_{BE} below the output voltage, this diode will turn ON and current will flow into the regulator output. In such cases, a parasitic SCR can latch which will allow a high current to flow into the V_{IN} pin and out the ground pin, which can damage the part.

The internal diode can also be turned on if the input voltage is abruptly stepped down to a voltage which is a V_{BE} below the output voltage.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT}. See Figure 22), to limit the reverse voltage across the LP2980-ADJ to 0.3V (see Absolute Maximum Ratings).

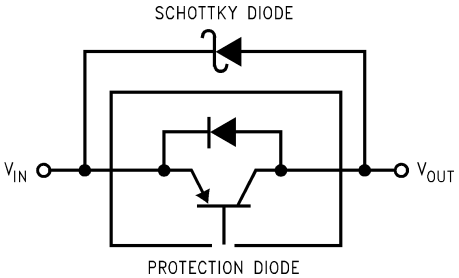


Figure 22. Adding External Schottky Diode Protection

ON/OFF INPUT OPERATION

The LP2980-ADJ is shut off by driving the ON/OFF input low, and turned on by pulling the ON/OFF input high. If this feature is not to be used, the ON/OFF input must be tied to V_{IN} to keep the regulator output on at all times (the ON/OFF input must not be left floating).

To ensure proper operation, the signal source used to drive the ON/OFF input must be able to swing above and below the specified turn-on/turn-off voltage thresholds which specify an ON or OFF state (see Electrical Characteristics).

It is also important that the turn-on (and turn-off) voltage signals applied to the ON/OFF input have a slew rate which is greater than 40 mV/µs.

IMPORTANT: The ON/OFF function will not operate correctly if a slow-moving signal is used to drive the ON/OFF input.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2980IM5-ADJ	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L06B	
LP2980IM5-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L06B	Samples
LP2980IM5X-ADJ	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	L06B	
LP2980IM5X-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L06B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

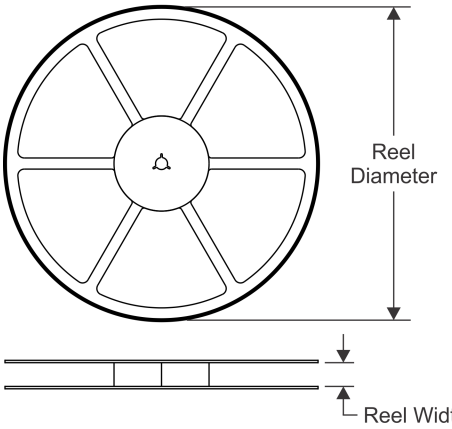
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

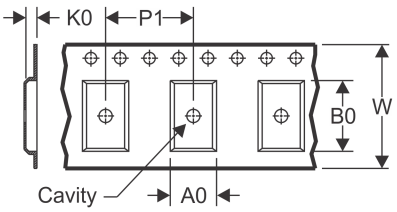
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

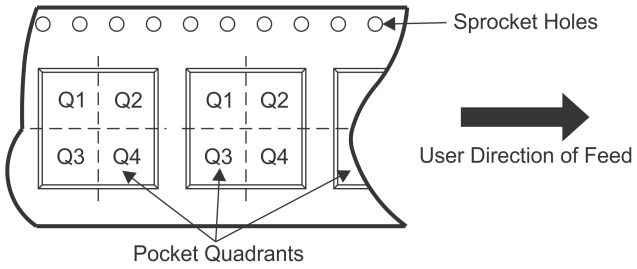


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

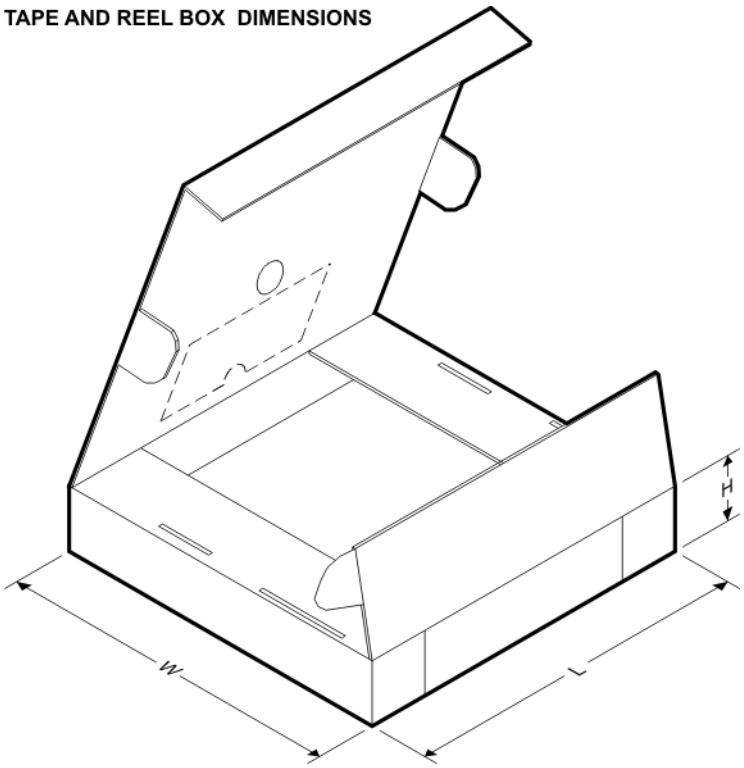
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2980IM5-ADJ	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5-ADJ/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5X-ADJ	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5X-ADJ/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

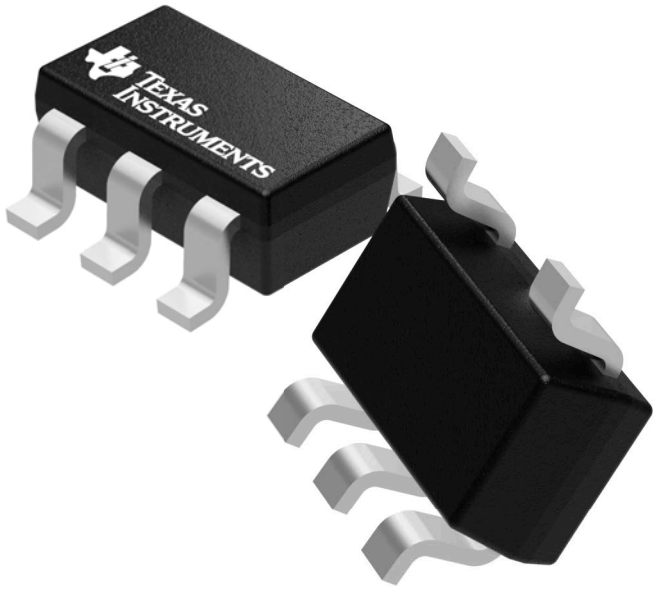


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2980IM5-ADJ	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980IM5-ADJ/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980IM5X-ADJ	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980IM5X-ADJ/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



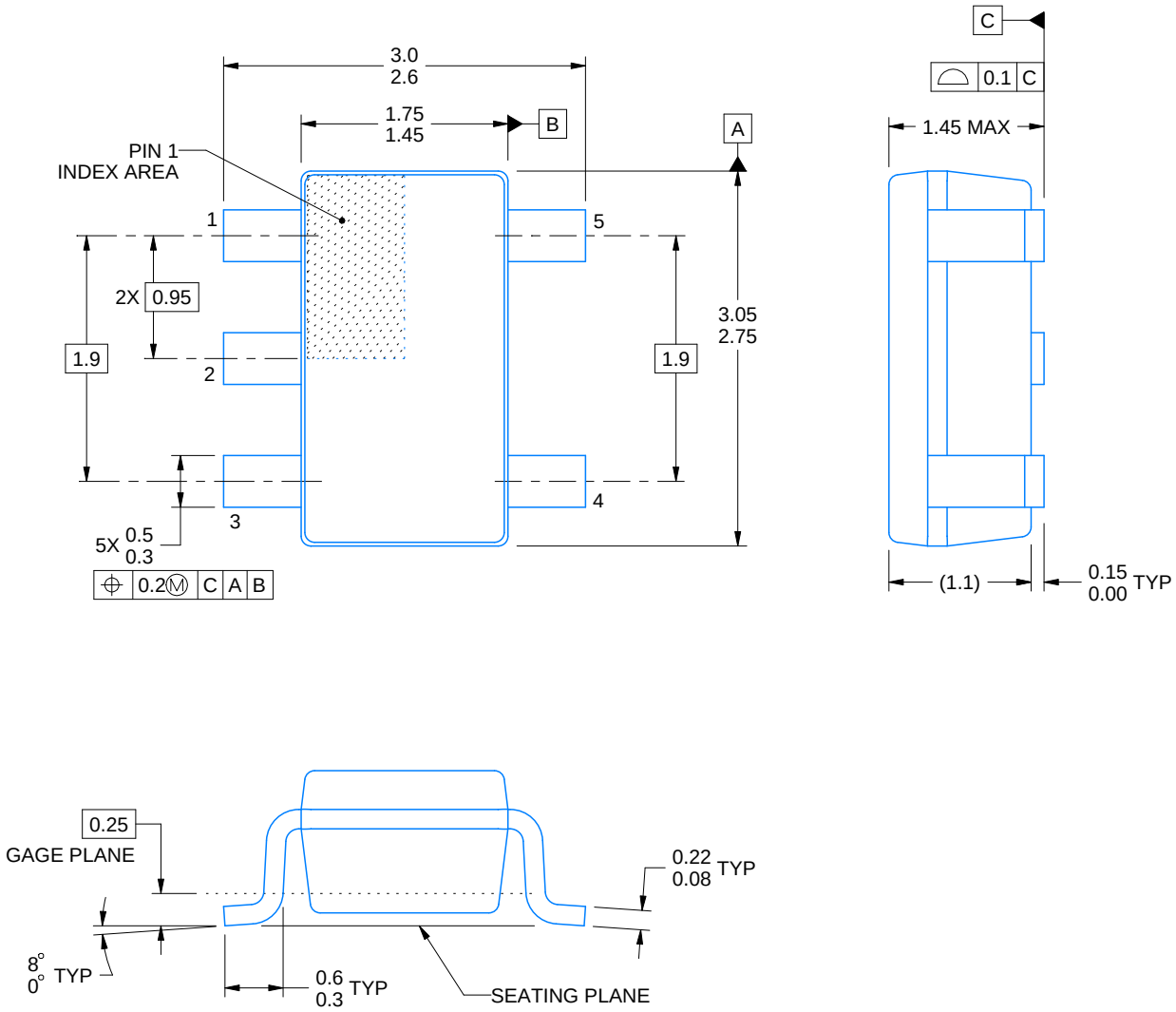
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

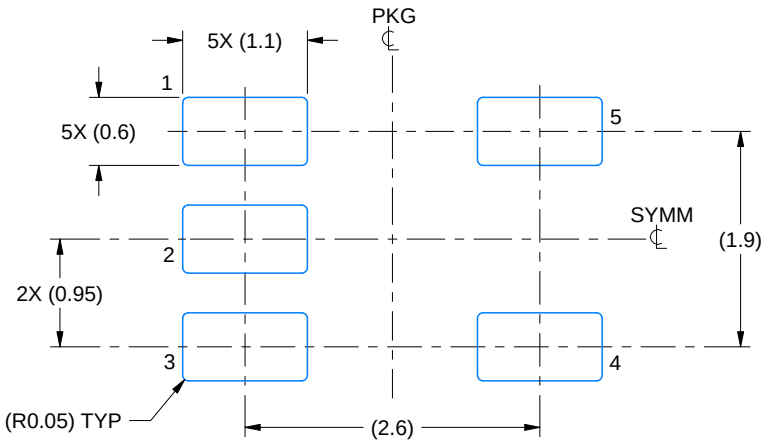
SMALL OUTLINE TRANSISTOR



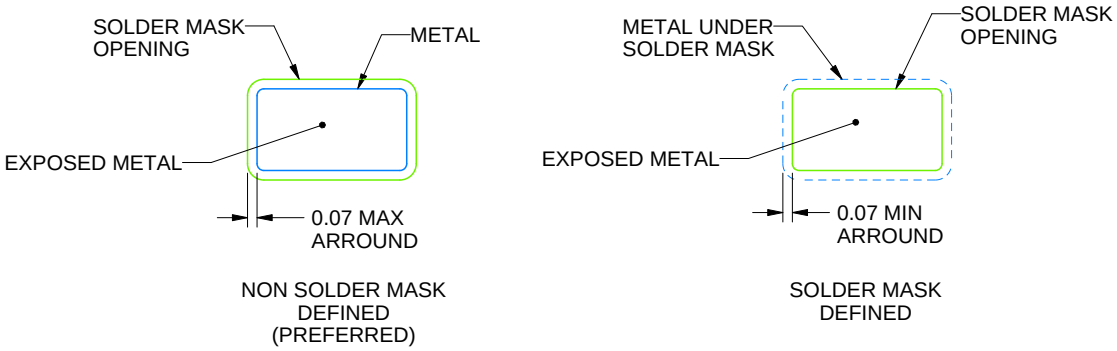
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

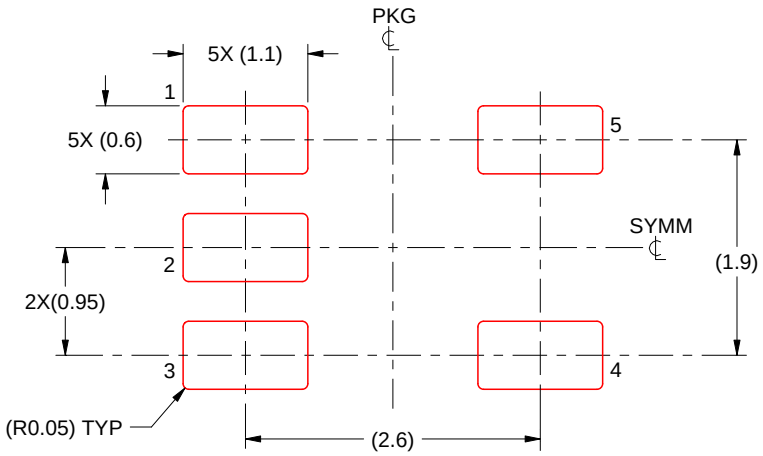


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

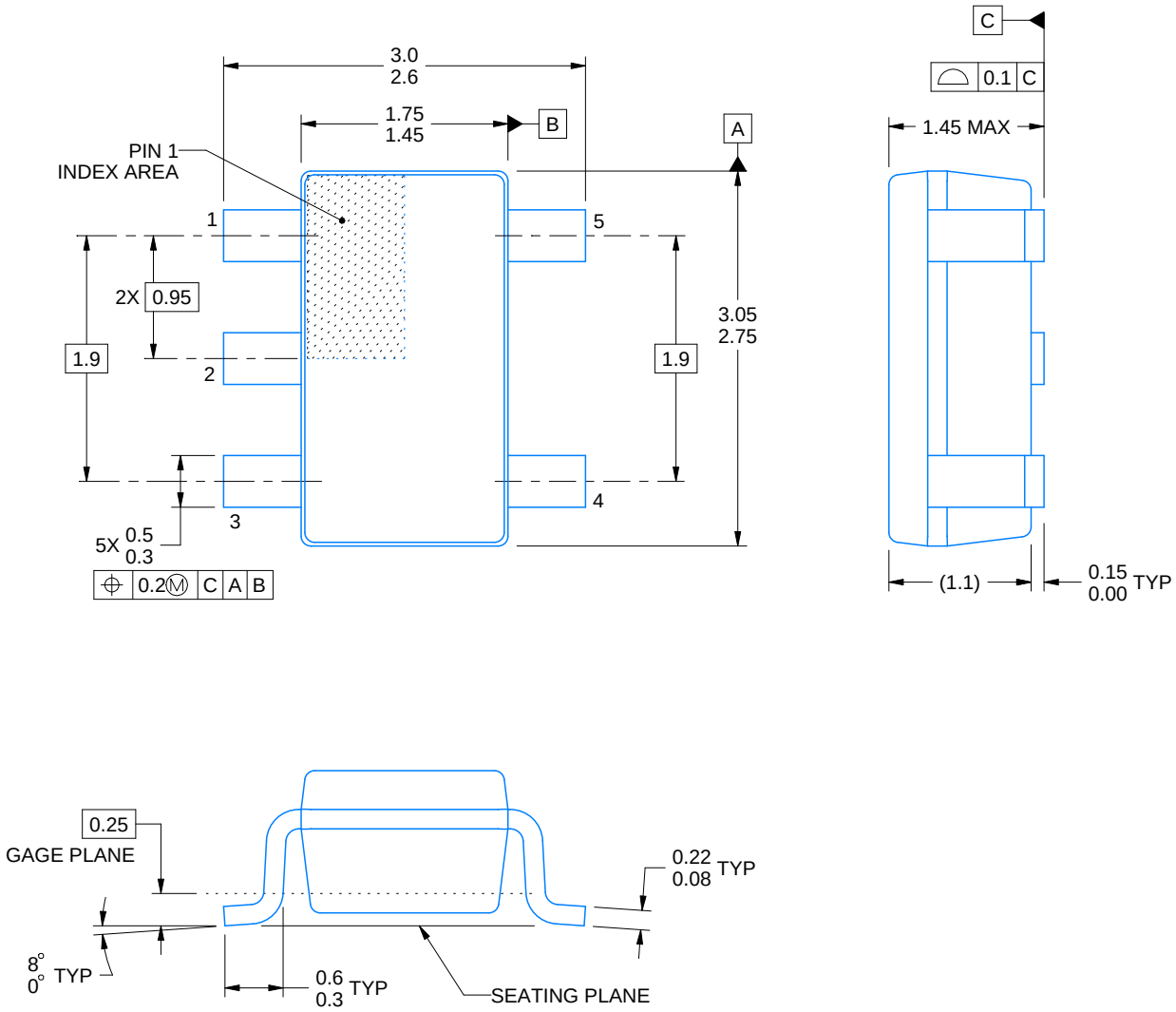
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

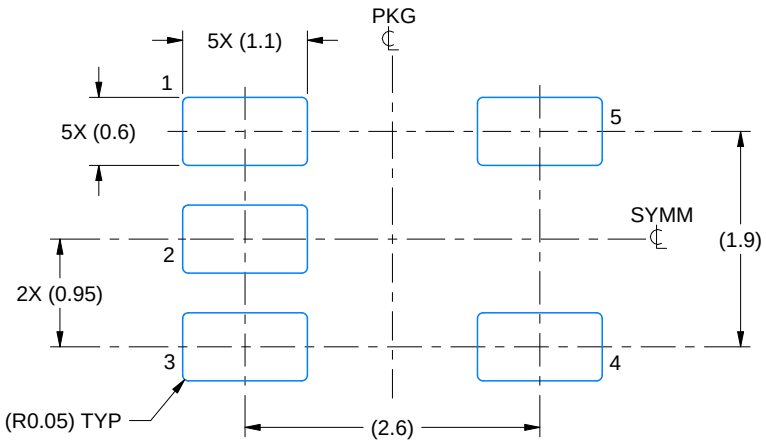
SMALL OUTLINE TRANSISTOR



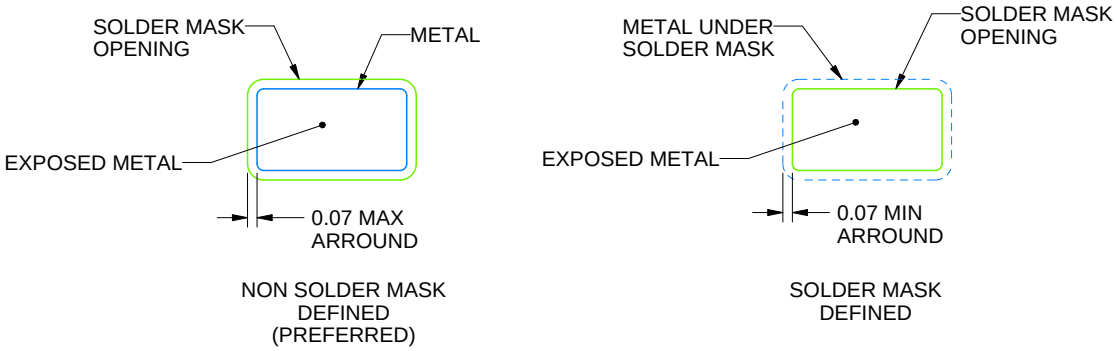
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

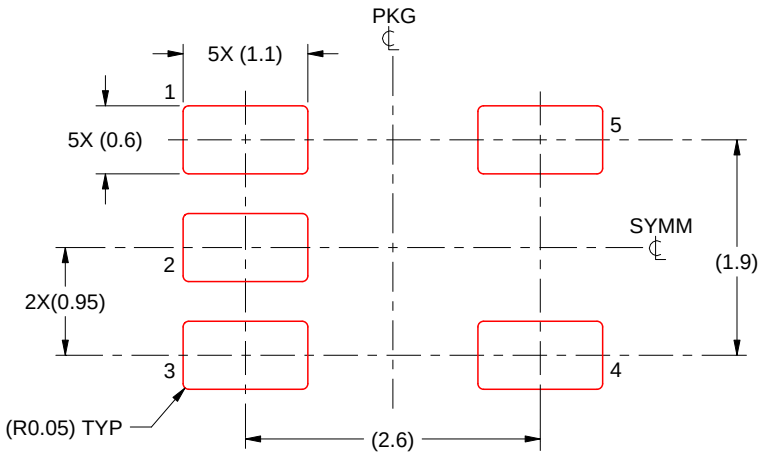


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265