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PRODUCT SPECIFICATIONS

For Customer: _____

: APPROVAL FOR SPECIFICATION

Customer Model No. _____

: APPROVAL FOR SAMPLE

Module No.: ZW-T035BQSA-01

Date : 2023-03-29

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For Customer's Acceptance:

Approved By	Comment

PREPARED	CHECKED	APPROVER
ZKJ		

2. Revision Record

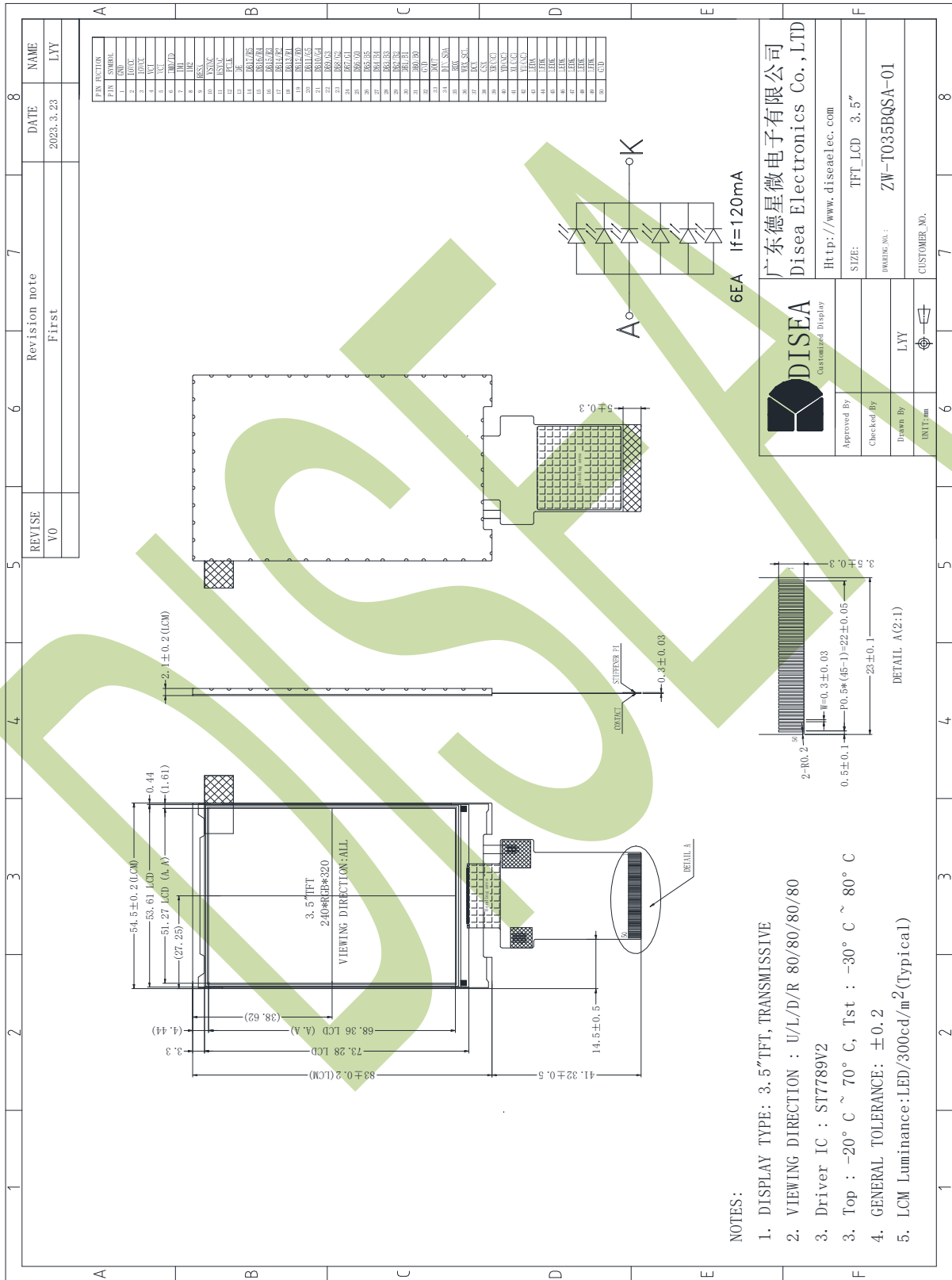
Date	Rev.No.	Page	Revision Items	Prepared
2023-03-29	V0		The first release	ZKJ

3. General Specifications

ZW-T035BQSA-01 is a TFT-LCD module. It is composed of a TFT-LCD panel, driver IC, FPC, a back light unit. The 3.5" display area contains 240X320 pixels and can display up to 16.7M colors. This product accords with RoHS environmental criterion.

Item	Contents	Unit	Note
LCD Type	TFT	-	
Display color	16.7M		
Viewing Direction	ALL	O'Clock	
Operating temperature	-20~+70	°C	
Storage temperature	-30~+80	°C	
Module size	Refer to outline drawing	mm	
Active Area(W×H)	51.27X68.36	mm	
Number of Dots	240X320	dots	
Driver IC	ST7789V2	-	
Power Supply Voltage	3.3	V	
Outline Dimensions	Refer to outline drawing	-	
Backlight	1X6-LEDs	pcs	
Interface	RGB&SPI&MCU	-	

4.Outline.Drawing



5. Absolute Maximum Ratings($T_a=25^\circ\text{C}$)

5.1 Electrical Absolute Maximum Ratings.($V_{ss}=0\text{V}$, $T_a=25^\circ\text{C}$)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VCI	-0.3	4.6	V	1, 2
Power Supply Voltage	IOVCC	-0.3	4.6	V	

Notes:

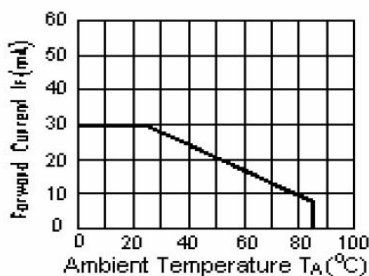
1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
2. $V_{DD} > V_{SS}$ must be maintained.
3. Please be sure users are grounded when handing LCD Module.

5.2 Environmental Absolute Maximum Ratings.

Item	Storage		Operating		Note
	MIN.	MAX.	MIN.	MAX.	
Ambient Temperature	-30°C	80°C	-20°C	70°C	
Humidity	-	-	-	-	

1. The response time will become lower when operated at low temperature.
2. Background color changes slightly depending on ambient temperature.
The phenomenon is reversible.
3. $T_a \leq 40^\circ\text{C}$: 85%RH MAX.

$T_a \geq 40^\circ\text{C}$: Absolute humidity must be lower than the humidity of 85%RH at 40°C .



ILED VS TEMP

6. Electrical Specifications and Instruction Code

6.1 Electrical characteristics($V_{SS}=0V, T_a=25^\circ C$)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Power Supply Voltage	V _{CI}	T _a =25°C	2.4	2.75	3.3	V	
	IOVCC	IOVCC	1.65	1.8	3.3	V	
Input voltage	'H'	V _{IH}	V _{CI} =3.3V	0.7V _{CI}	-	V _{CI}	V
	'L'	V _{IL}	V _{CI} =3.3V	0	-	0.3V _{CI}	V

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

6.2 LED backlight specification($V_{SS}=0V, T_a=25^\circ C$)

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply voltage VLED	V _f	I _f =120mA	-	3.0	-	V	
Uniformity	Δ Bp	I _f =120mA	80	-	-	%	
LED Life Time	Time	I _f =120mA	20K	-	-	hr	1

Note 1: Brightness to be decreased to 50% of the initial value at ambient temperature T_A=25 °C

6.3 Interface signals

6.3.1 LCM PIN

Pin No.	Symbol	I/O	Function																																			
1	GND	P	Ground.																																			
2-3	IOVCC	P	Power Supply for IO.																																			
4-5	VCI	P	Power supply.																																			
6	IM0	I	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>MPU Interface Mode</th> <th>Data pin</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>80-8bit parallel I/F</td> <td>DB[7:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>80-16bit parallel I/F</td> <td>DB[15:0]</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>80-9bit parallel I/F</td> <td>DB[8:0]</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>80-18bit parallel I/F</td> <td>DB[17:0].</td> </tr> </tbody> </table>	IM2	IM1	IM0	MPU Interface Mode	Data pin	0	0	0	80-8bit parallel I/F	DB[7:0]	0	0	1	80-16bit parallel I/F	DB[15:0]	0	1	0	80-9bit parallel I/F	DB[8:0]	0	1	1	80-18bit parallel I/F	DB[17:0].										
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8	IM2	I	<table border="1" style="width: 100%; border-collapse: collapse;"> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>3-line 9bit serial I/F II</td> <td>SDA: in/ SDO: out</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>4-line 8bit serial I/F II</td> <td>SDA:in/ SDO: out</td> </tr> </tbody> </table>	1	0	1	3-line 9bit serial I/F II	SDA: in/ SDO: out	1	1	0	4-line 8bit serial I/F II	SDA:in/ SDO: out																									
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1	1	0	4-line 8bit serial I/F II	SDA:in/ SDO: out																																		
9	RESX	I	Global reset signal input pin.																																			
10	VSYNC	I	Vertical svnc signal.																																			
11	HSYNC	I	Horizontal svnc signal.																																			
12	PCLK	I	Dot clock signal for RGB interface operation.																																			
13	DE	I	Data enable signal for RGB interface operation.																																			
14-31	DB17-DB0	I	Data input.																																			
32	GND	P	Ground.																																			
33	DOUT	O	SPI interface output pin.																																			
34	DIN-SDA	I	serial Input/output data bus.																																			
35	RD	I	Read enable in 8080 MCU parallel interface.																																			
36	WR/SCL	I	Write enable in MCU parallel interface.																																			
37	DCX	I	Display data/command selection (RS) pin in MCU interface.																																			
38	CS	I	Chip select input pin.																																			
39	XR(NC)	O	RTP pin ,not use please NC.																																			
40	YD(NC)	O																																				
41	XL(NC)	O																																				
42	YU(NC)	O																																				
43	LEDA	P		LED anode.																																		
44-49	LEDK	P	LED cathode.																																			
50	GND	P	Ground.																																			

6.4 AC Characteristics

8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

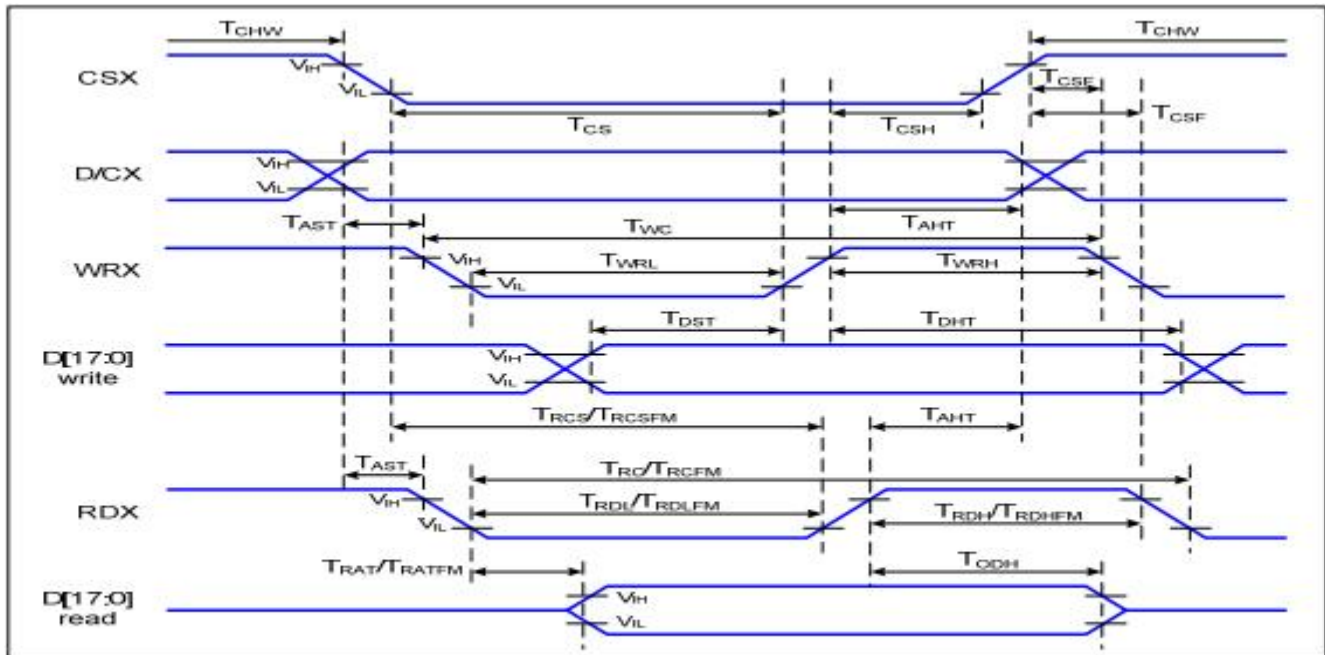


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T _{AST}	Address setup time	0		ns	
	T _{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T _{CHW}	Chip select "H" pulse width	0		ns	
	T _{CS}	Chip select setup time (Write)	15		ns	
	T _{RCs}	Chip select setup time (Read ID)	45		ns	
	T _{RCsFM}	Chip select setup time (Read FM)	355		ns	
	T _{CsF}	Chip select wait time (Write/Read)	10		ns	
	T _{CsH}	Chip select hold time	10		ns	
WRX	T _{WC}	Write cycle	66		ns	
	T _{WRH}	Control pulse "H" duration	15		ns	
	T _{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T _{RC}	Read cycle (ID)	160		ns	When read ID data
	T _{RDH}	Control pulse "H" duration (ID)	90		ns	
	T _{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T _{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T _{RDHF}	Control pulse "H" duration (FM)	90		ns	
	T _{RDLF}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T _{DST}	Data setup time	10		ns	For CL=30pF

T_{DHT}	Data hold time	10		ns
T_{RAT}	Read access time (ID)		40	ns
T_{RATFM}	Read access time (FM)		340	ns
T_{ODH}	Output disable time	20	80	ns

Table 4 8080 Parallel Interface Characteristics

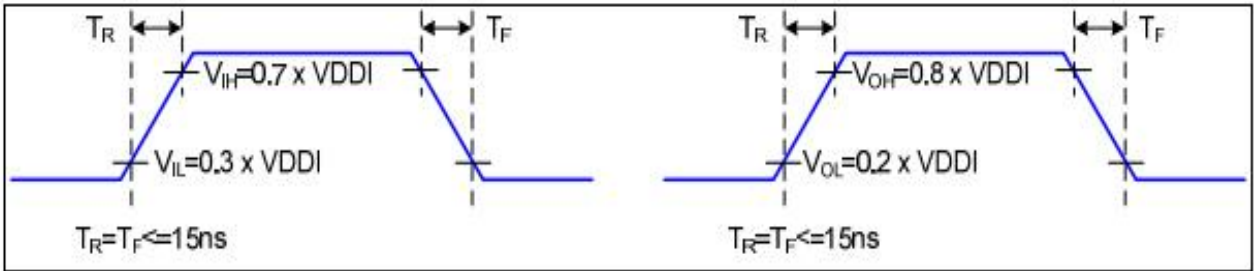


Figure 2 Rising and Falling Timing for I/O Signal

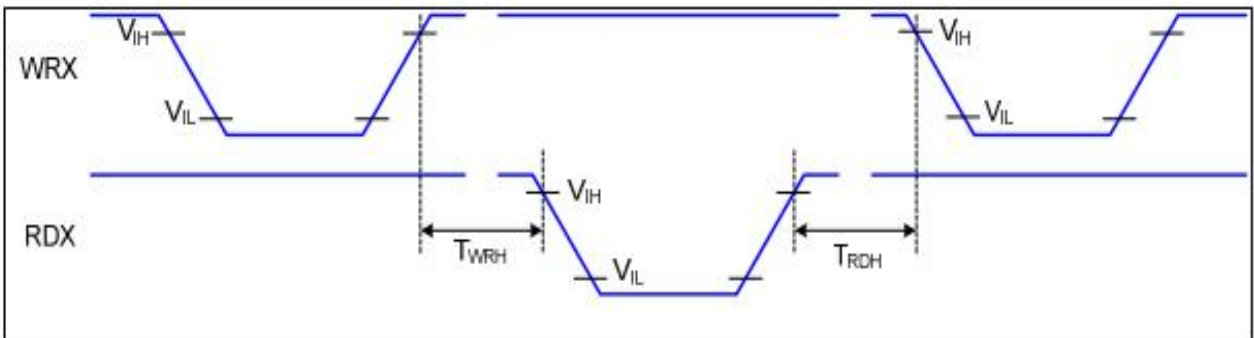


Figure 3 Write-to-Read and Read-to-Write Timing

Serial Interface Characteristics (3-line serial)

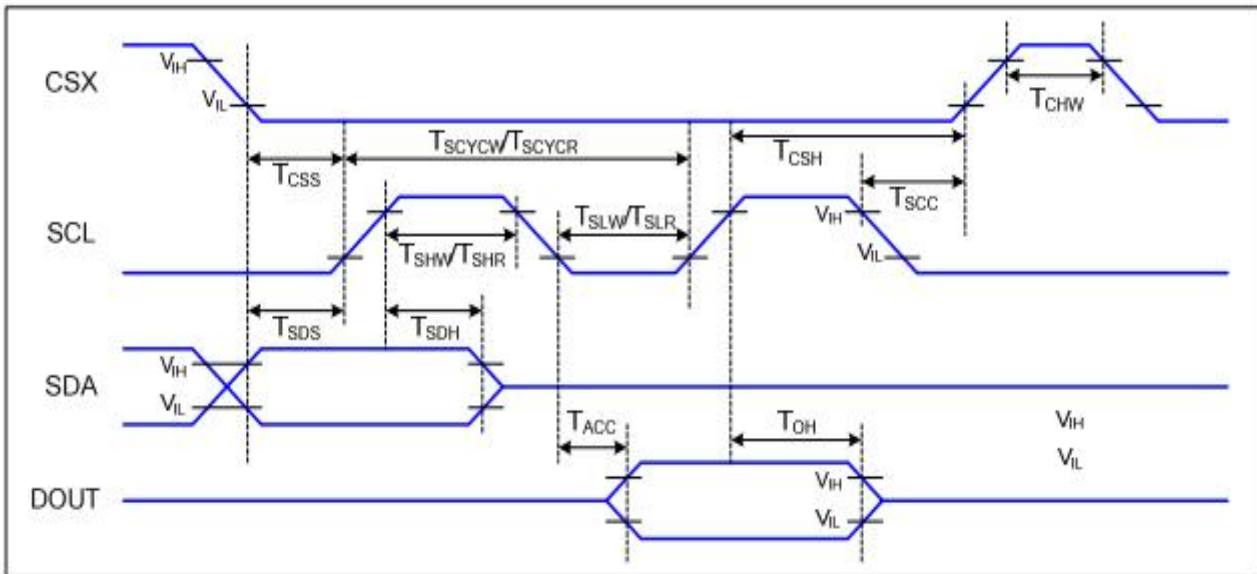


Figure 4 3-line serial Interface Timing Characteristics

$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=25^\circ C$

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum $CL=30pF$
	T_{OH}	Output disable time	15	50	ns	For minimum $CL=8pF$

Table 5 3-line serial Interface Characteristics

Serial Interface Characteristics (4-line serial):

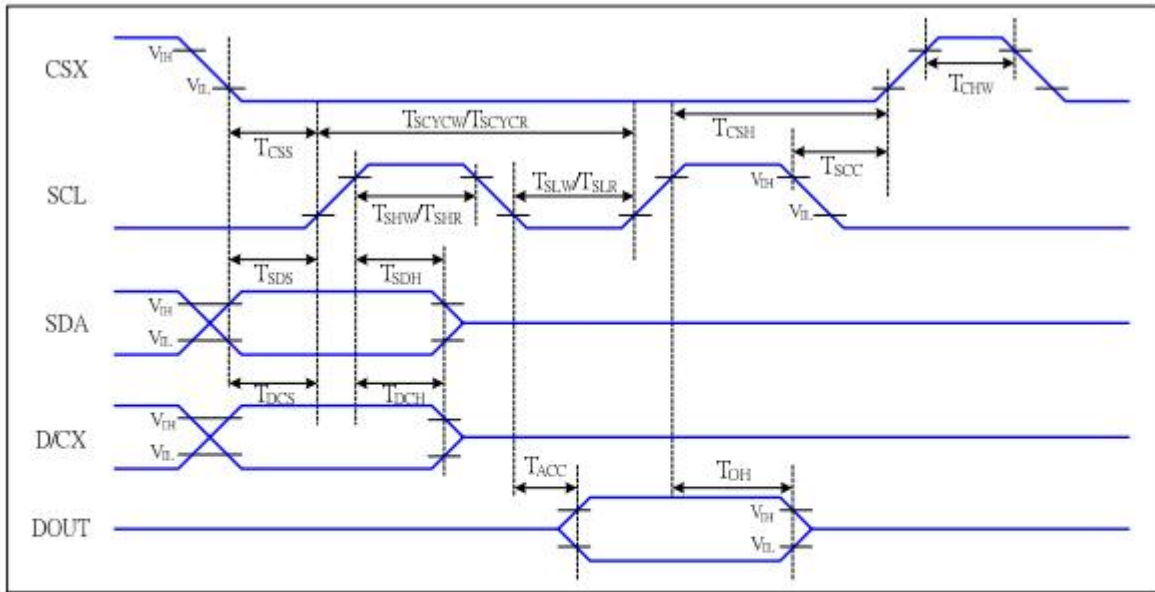


Figure 5 4-line serial Interface Timing Characteristics

$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=25^{\circ}C$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum $CL=30pF$
	T_{OH}	Output disable time	15	50	ns	For minimum $CL=8pF$

Table 6 4-line serial Interface Characteristics

RGB Interface Characteristics

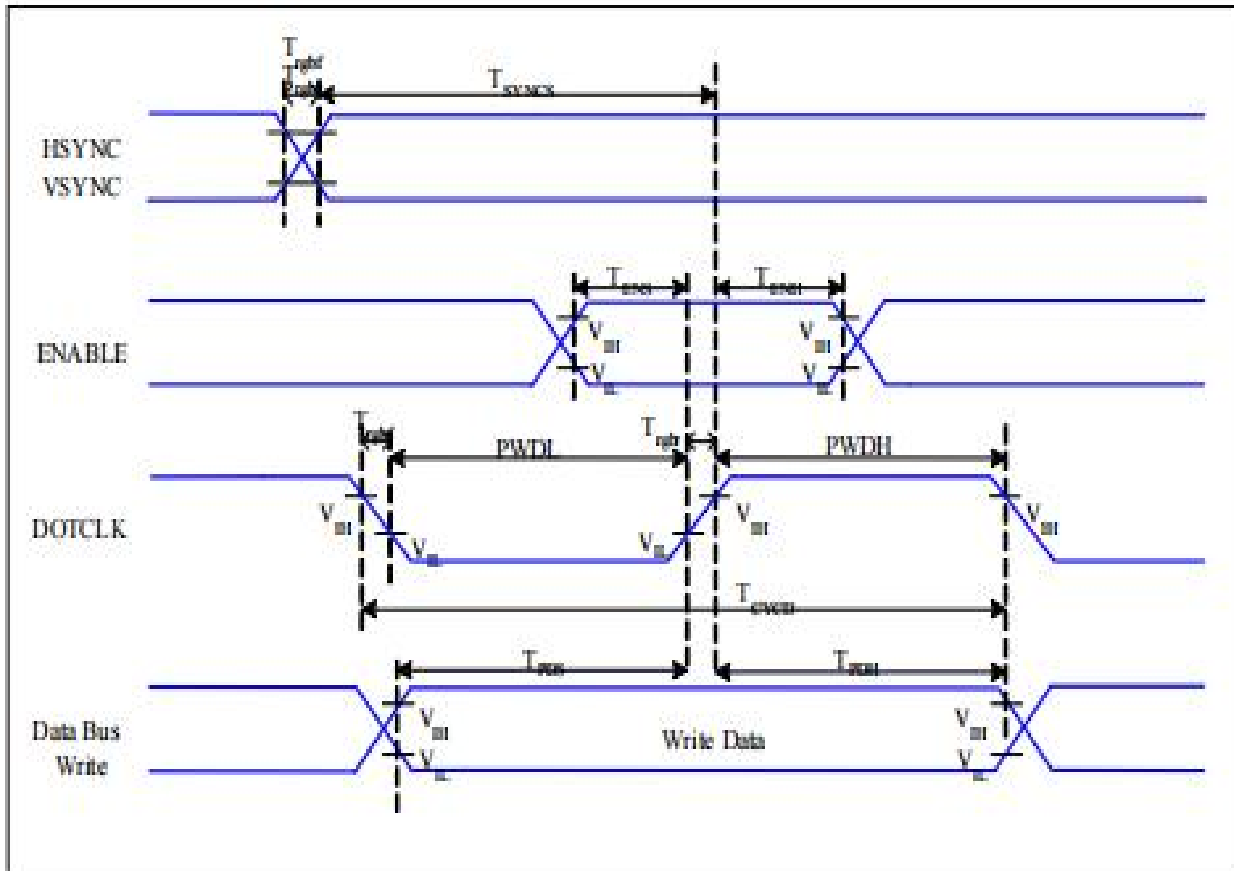


Figure 6 RGB Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25°C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{syncs}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ens}	Enable Setup Time	25	-	ns	
	T_{enh}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{cyc}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{fos}	PD Data Setup Time	50	-	ns	
	T_{foh}	PD Data Hold Time	50	-	ns	

Table 7 18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	35	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	35	-	ns	

	T_{ENH}	Enable Hold Time	35	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	35	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	35	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	80	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	35	-	ns	
	T_{PDH}	PD Data Hold Time	35	-	ns	

Table 8 6 Bits RGB Interface Timing Characteristics

Reset Timing

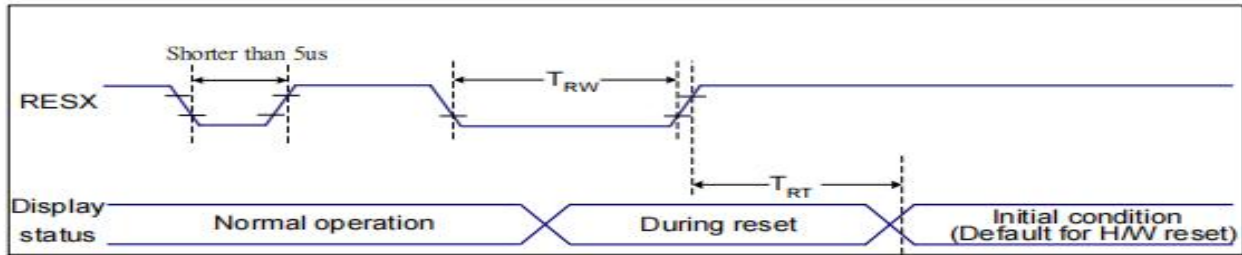


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25°C

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5) 120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

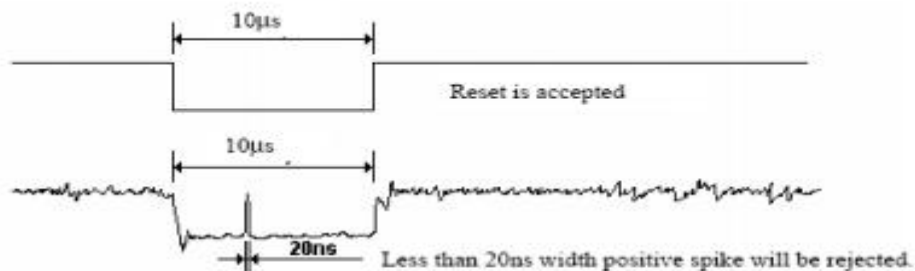
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp	$\theta=0^\circ$ $\Phi=0^\circ$	-	300	-	Cd/m ²	1
Uniformity	Δ Bp		80	-	-	%	1,2
Viewing Angle	3:00	Cr \geq 10	-	80	-	Deg	3
	6:00		-	80	-		
	9:00		-	80	-		
	12:00		-	80	-		
Contrast Ratio	Cr	$\theta=0^\circ$ $\Phi=0^\circ$	900	1100	-	-	4
Response Time	T _r +T _f	$\theta=0^\circ$ $\Phi=0^\circ$	-	35	53	ms	5
Color of CIE Coordinate	W	x	Typ. -0.05	0.29	Typ. +0.05	-	1,6
		y		0.32		-	
	R	x		0.65		-	
		y		0.32		-	
	G	x		0.26		-	
		y		0.57		-	
	B	x		0.14		-	
		y		0.08		-	

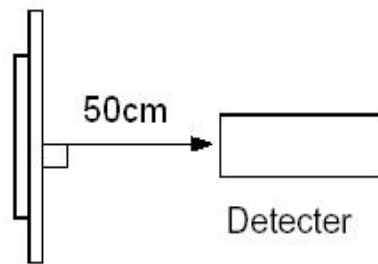
Note: The parameter is slightly changed by temperature, driving voltage and materiel

Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment BM-7 (Φ 5mm)

Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: $T_a=25\text{ }^\circ\text{C}$.
- Adjust operating voltage to get optimum contrast at the center of the display.

Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.

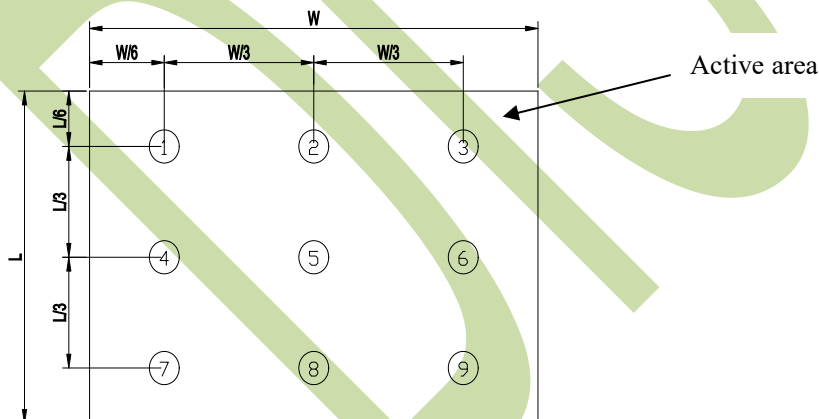


Note 2: The luminance uniformity is calculated by using following formula.

$$\Delta Bp = Bp (\text{Min.}) / Bp (\text{Max.}) \times 100 (\%)$$

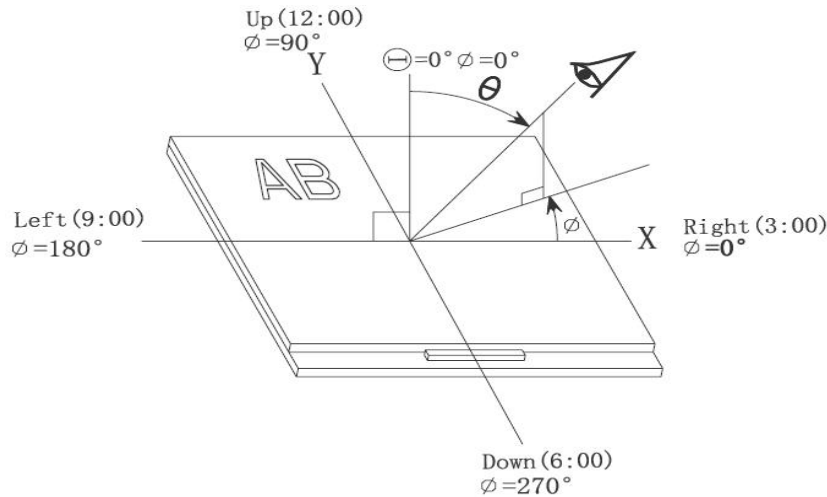
$Bp (\text{Max.})$ = Maximum brightness in 9 measured spots

$Bp (\text{Min.})$ = Minimum brightness in 9 measured spots.

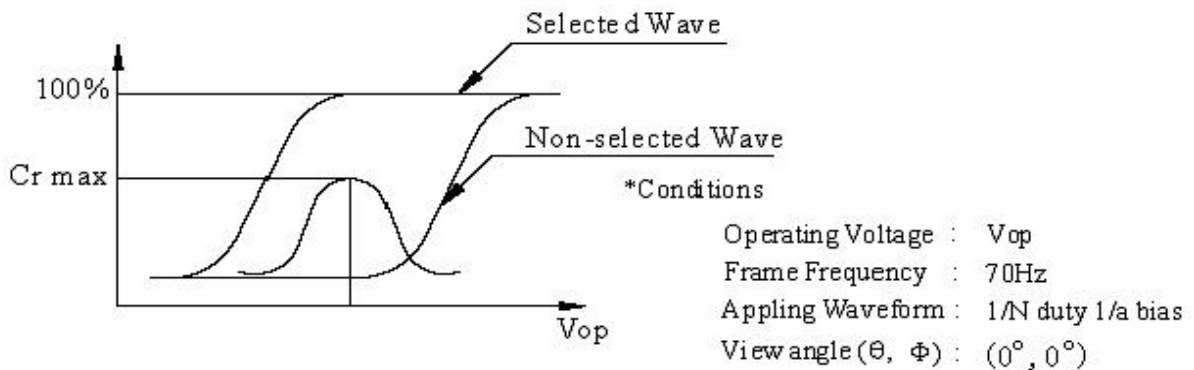


Note 3: The definition of viewing angle:

Refer to the graph below marked by ϑ and Φ



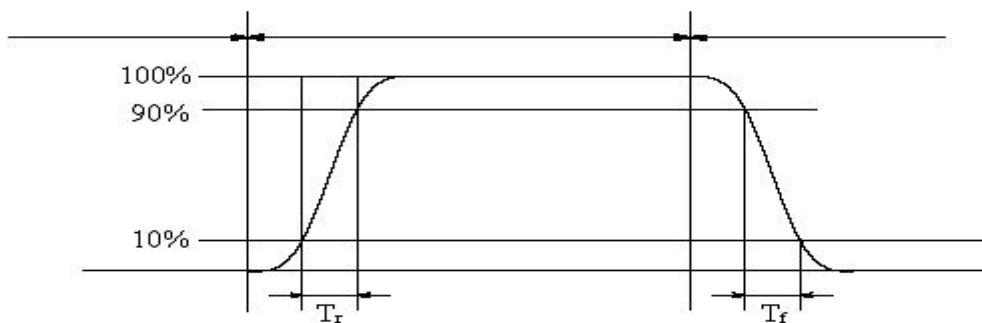
Note 4: Definition of contrast ratio.(Test LCD using DMS501)



$$\text{Contrast ratio}(Cr) = \frac{\text{Brightness of selected dots}}{\text{Brightness of non-selected dots}}$$

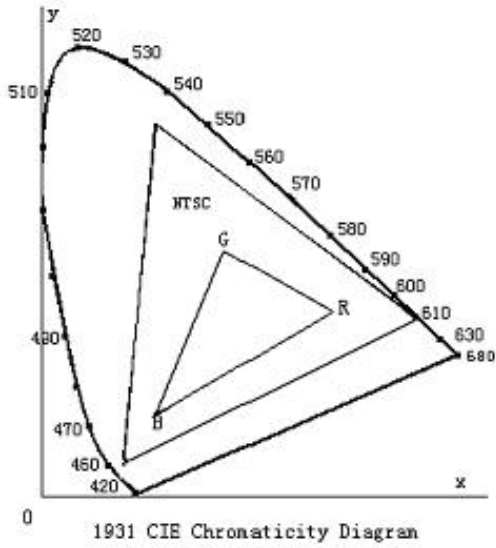
Note 5: Definition of Response time. (Test LCD using DMS501):

The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



The definition of response time

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.

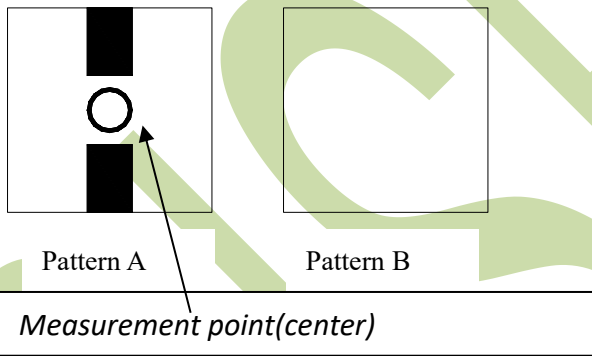


Color gamut:

$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 7: Definition of cross talk.

Cross talk ratio(%) = $\frac{|\text{pattern A Brightness} - \text{pattern B Brightness}|}{\text{pattern A Brightness}} \times 100$



Electric volume value = 3F+/-3Hex

8. Reliability Test Items and Criteria

No	Test Item	Test condition	Criterion
1	High Temperature Storage	80°C±2°C 96H Restore 2H at 25°C Power off	1. After testing, cosmetic and electrical defects should not happen. 2. Total current consumption should not be more than twice of initial value.
2	Low Temperature Storage	-30°C±2°C 96H Restore 2H at 25°C Power off	
3	High Temperature Operation	70°C±2°C 96H Restore 2H at 25°C Power on	
4	Low Temperature Operation	-20°C±2°C 96H Restore 4H at 25°C Power on	
5	High Temperature/Humidity Operation	60°C±2°C 90%RH 96H Power on	
6	Temperature Cycle	-30°C → 80°C 30min 5min 30min after 5 cycle, Restore 2H at 25°C Power off	

Note: Operation: Supply 3.3V for logic system.

The inspection terms after reliability test, as below

ITEM	Inspection
Contrast	CR>50%
IDD	IDD<200%
Brightness	Brightness>60%
Color Tone	Color Tone+/-0,05

9. Precautions for Use of LCD Modules

9.1 Handling Precautions

9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

9.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

9.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

9.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

9.1.6 Do not attempt to disassemble the LCD Module.

9.1.7 If the logic circuit power is off, do not apply the input signals.

9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

9.2 Storage precautions

9.2.1 *When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.*

9.2.2 *The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:*

Temperature : 0 °C ~ 40 °C

Relatively humidity: ≤80%

9.2.3 *The LCD modules should be stored in the room without acid, alkali and harmful gas.*

9.3 *The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.*

END