Application Note: SY98202

High Efficiency, Built-in Inductor, 1.7MHz, 2A, 23V Input Synchronous Step Down Regulator

General Description

The SY98202 is a high efficiency 1.7MHz synchronous step-down DC/DC converter capable of delivering 2A current, which integrates an inductor into a compact 3×3×2mm QFN package. The SY98202 operates over a wide input voltage range from 4.5V to 23V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

SY98202 features adjustable soft-start time, enable control and power good indicator for system sequence control. The device also provides cycle-by-cycle current limit, short circuit protection and thermal shutdown protection for reliable operation.

Ordering Information

SY98202□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY98202QNC	QFN3×3-10	--

Features

- low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 105mΩ/50mΩ
- 4.5-23V Input Voltage Range
- 2A Output Current Capability
- 1.7MHz Switching Frequency
- Instant PWM Architecture to Achieve Fast Transient Responses
- Cycle-by-cycle Peak Current Limitation
- Adjustable soft-start Time
- Hic-cup Mode Output Short Circuit Protection
- ±1.5% 0.6V Reference
- Power Good Indicator
- QFN3×3-10 Package

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Typical Applications

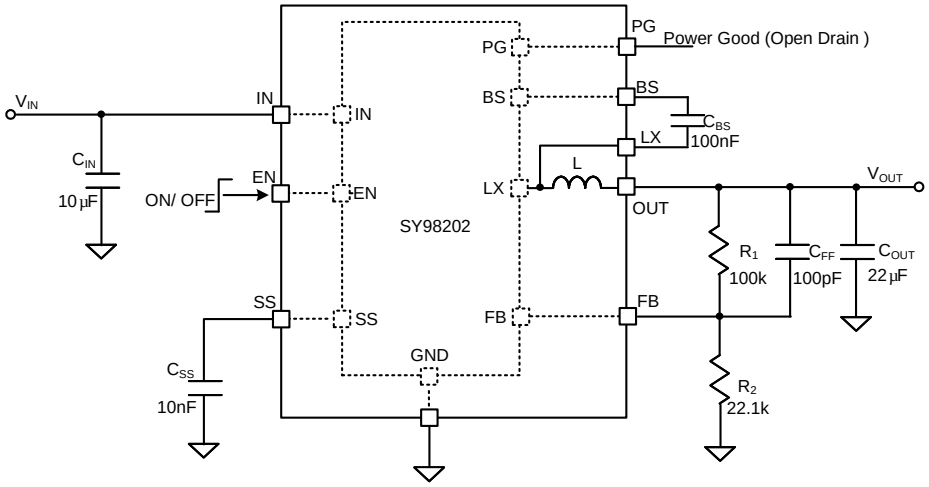

Figure1. Schematic Diagram

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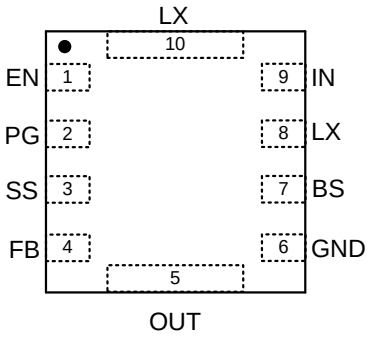
Pinout (top view)



(QFN3×3-10)

Top Mark: **BGB*xyz*** (Device code: **BGB**; ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
EN	1	Enable control. Pull high to turn on. Do not leave it floating.
PG	2	Open drain power good indicator. Externally pull high when the output is in regulation range. Otherwise pull low.
SS	3	Soft-start programming pin. Connect a capacitor from this pin to ground to program the soft-start time. $t_{SS}=C_{SS}\times0.6V/5\mu A$. Leave this pin open for default 1ms soft-start.
FB	4	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_1/R_2)$.
OUT	5	Output pin. Decouple this pin to ground with at least a 10μF MLCC.
GND	6	Ground pin.
BS	7	Boot-Strap Pin. Supply high side gate driver. Decouple this pin to LX pin with a 0.1μF ceramic cap.
LX	8,10	Inductor pin. Connect this pin to the switching node of inductor.
IN	9	Input pin. Decouple this pin to GND pin with at least a 1μF ceramic cap.

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Block Diagram

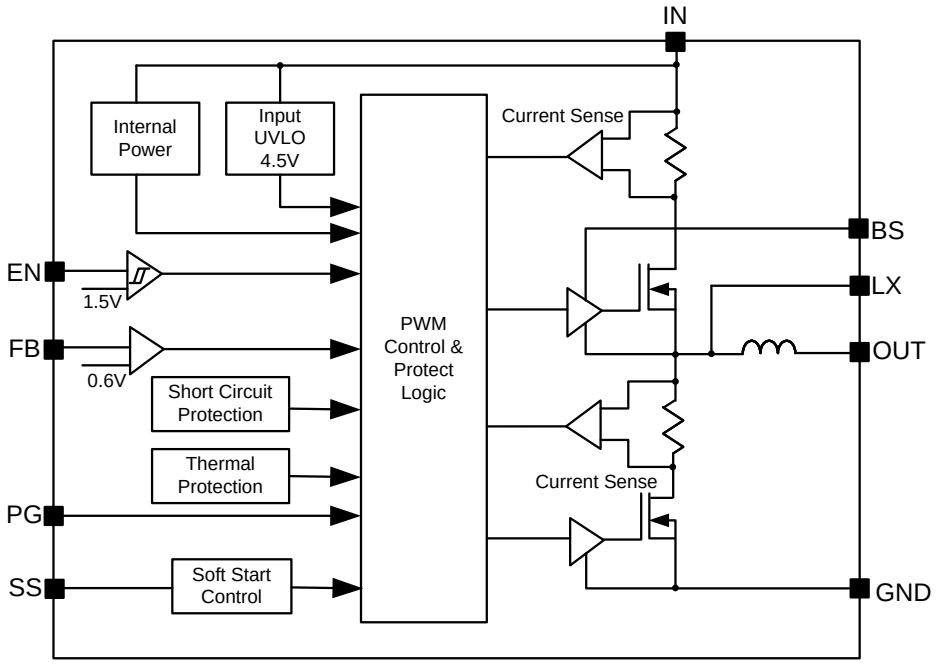

Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- 25V
BS-LX, SS ---------- 4V
All other pins ---------- VIN + 0.3V
Power Dissipation, P_D @ T_A = 25℃, QFN3×3-10(Note 2) ---------- 2.2W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 56℃/W
θ_{JC} ---------- 7.5℃/W
Junction Temperature Range ---------- 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4.5V to 23V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

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Electrical Characteristics

(V_{IN} = 12V, V_{OUT} =3.3V, C_{OUT} = 22μF, T_A = 25℃, I_{OUT} = 1A, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		23	V
Quiescent Current	IQ	I_{OUT}=0, V_{FB}=V_{REF}×105%		115		μA
Shutdown Current	ISHDN	EN=0		6.5	10	μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
Top FET RON	$R_{DS(ON)1}$			105		mΩ
Top FET Peak Current Limit	$I_{LIM,TOP}$	Note 4		4.5		A
Bottom FET RON	$R_{DS(ON)2}$			50		mΩ
Bottom FET Valley Current Limit	$I_{LIM,BOT}$		2.7	3.3	3.9	A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Power Good Threshold	V_{PG}	V_{FB} falling, PG from high to low		90		%V_{REF}
		V_{FB} rising, PG from low to high		95		%V_{REF}
		V_{FB} rising, PG from high to low		115		%V_{REF}
		V_{FB} falling, PG from low to high		110		%V_{REF}
Power Good Delay Time	t_{PG_F}	Note 4, PG falling edge		10		μs
	t_{PG_R}	Note 4, PG rising edge		60		μs
Oscillator Frequency	F_{OSC}			1.7		MHz
Soft-start Charging Current	I_{SS}			5		μA
Short Circuit Protection Wait Time	$t_{WAIT,SCP}$	Note 4		3		ms
Short Circuit Protection Off Time	$t_{OFF,SCP}$	Note 4		15		ms
Input UVLO Threshold	V_{UVLO}				4.5	V
Input UVLO Hysteresis	V_{HYS}			0.3		V
Min ON Time		Note 4		80		ns
Min OFF Time		Note 4		160		ns
Thermal Shutdown Temperature	T_{SD}	Note 4		150		℃
Thermal Shutdown Hysteresis	T_{HYS}	Note 4		15		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: P_D, θ_{JA}, θ_{JC} is measured in the natural convection at T_A = 25℃ on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Design Guarantee.

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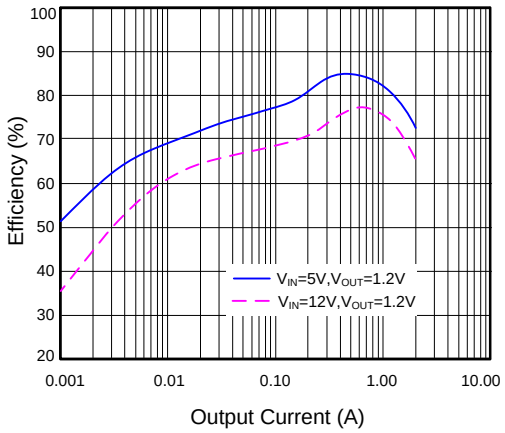
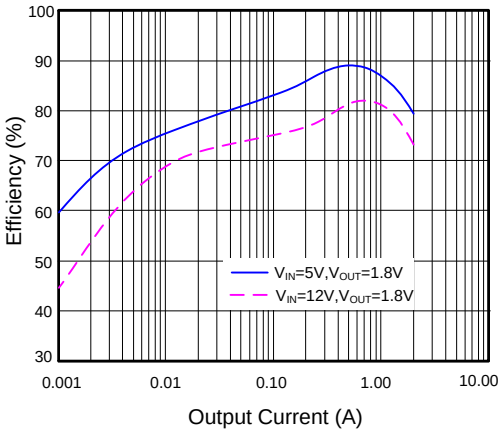
Typical Performance Characteristics

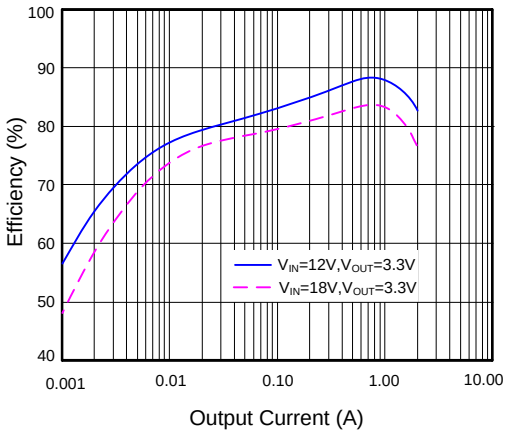
Efficiency vs. Output Current



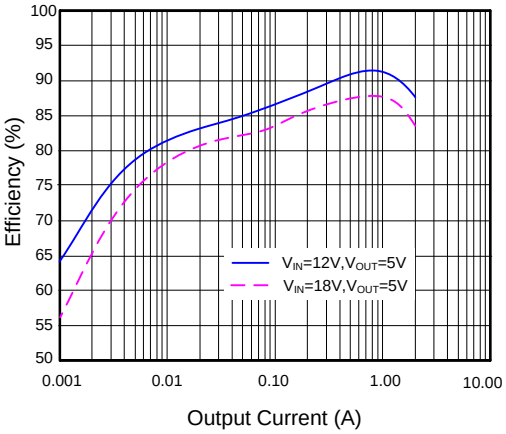
Efficiency vs. Output Current



Efficiency vs. Output Current

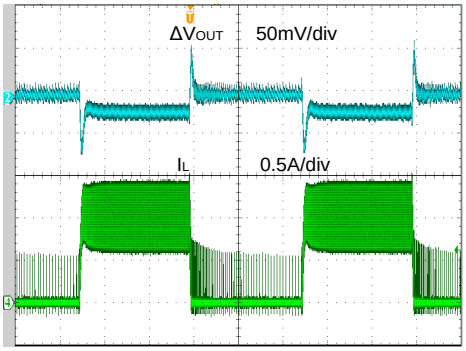


Efficiency vs. Output Current



Load Transient

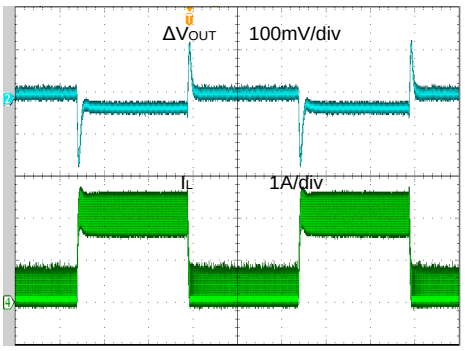
(V_{IN}=12V,V_{OUT}=3.3V,I_{OUT}=0-1A)



Time (200μs/div)

Load Transient

(V_{IN}=12V,V_{OUT}=3.3V,I_{OUT}=0.2-2A)



Time (200μs/div)

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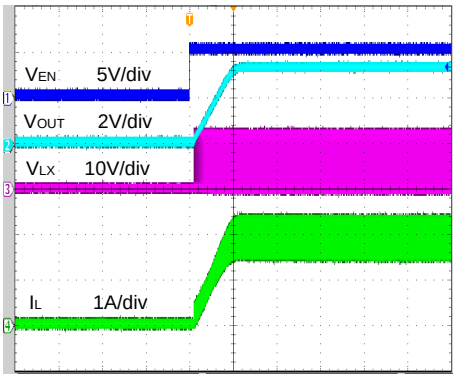
Startup from Enable

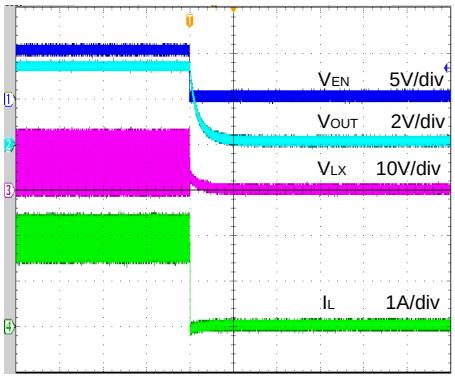
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=2A)



Time (800μs/div)

Shutdown from Enable

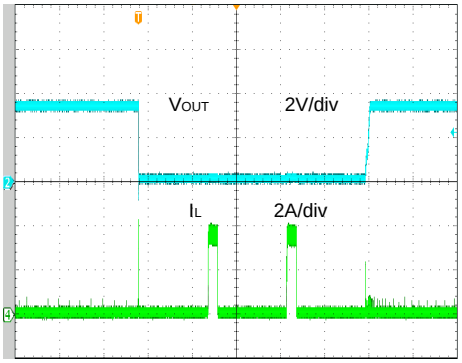
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=2A)



Time (200μs/div)

Short Circuit Protection

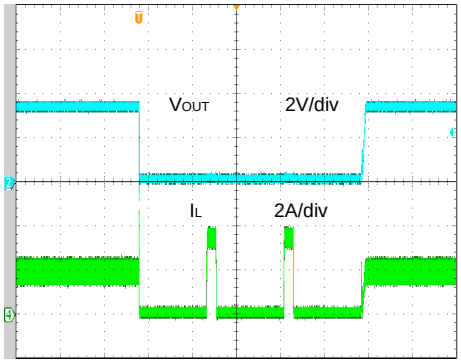
(V_{IN}=12V, V_{OUT}=3.3V, 0A to Short)



Time (10ms/div)

Short Circuit Protection

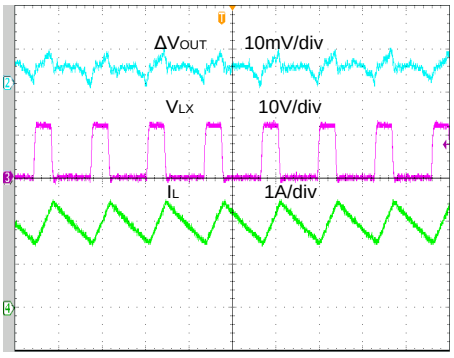
(V_{IN}=12V, V_{OUT}=3.3V, 2A to Short)



Time (10ms/div)

Output Ripple

(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=2A)



Time (400ns/div)

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Operation

The SY98202 is a high efficiency 1.7MHz synchronous step down DC/DC converter capable of delivering 2A current. The SY98202 operates over a wide input voltage range from 4.5V to 23V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

SY98202 features adjustable soft-start time, enable control and power good indicator for system sequence control. The device also provides cycle-by-cycle current limit, short circuit protection and thermal shutdown protection for reliable operation.

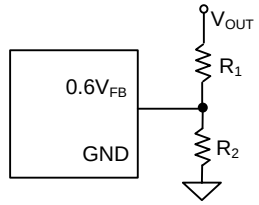
Applications Information

Because of the high integration in the SY98202, the application circuit based on this regulator is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT} and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 3.3V, R_1=100k is chosen, then using following equation, R_2 can be calculated to be 22.1k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1$$



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Input Capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)} \cdot$$

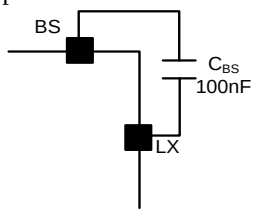
To minimize the potential noise problem, we place a typical X5R or a better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 10μF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or a better grade ceramic capacitor greater than 10μF capacitance.

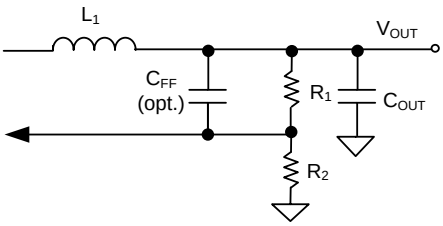
External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



Load Transient Considerations:

The SY98202 regulator integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic capacitor in parallel with R_1 may further speed up the load transient responses and it is recommended for applications with large load transient step requirements.



Soft-start:

The SY98202 provides programmable soft-start time feature. The minimum soft-start time is 1ms typically when SS pin is floating. Connect a capacitor across SS pin and GND to program the soft-start time.

t_{SS}(ms)=Css(nF)×0.6V/5μA

Power Good Indication

PG is an open-drain output pin. This pin will pull to ground if output voltage is lower than 95% or higher than 115% of regulation voltage. Otherwise this pin will go to a high impedance state.

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Layout Design:

The layout design of SY98202 regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{IN}, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connected to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The components R_1 and R_2, and the trace connected to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

PCB Layout Suggestion:

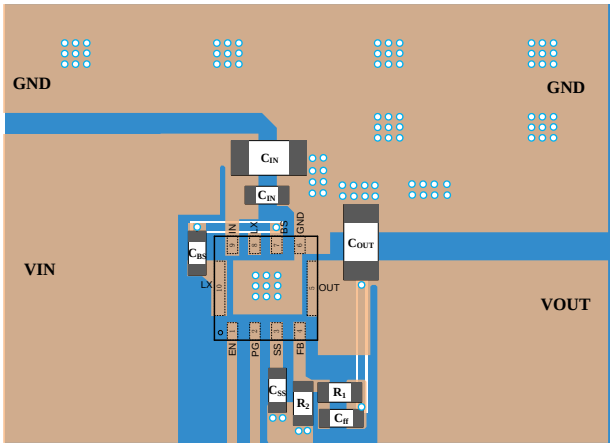

Figure3. PCB Layout Suggestion

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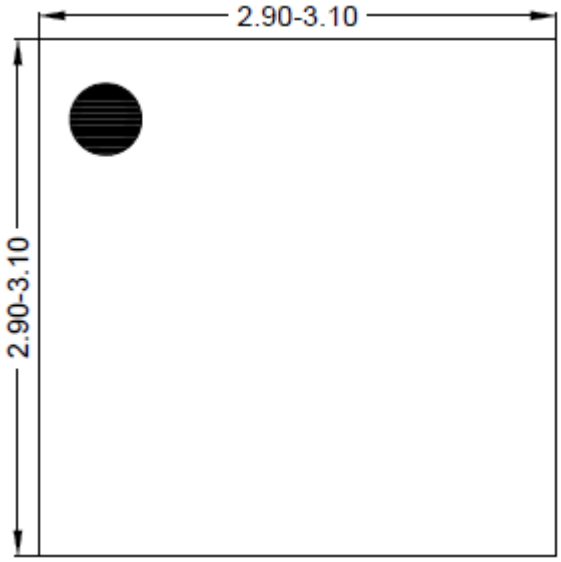
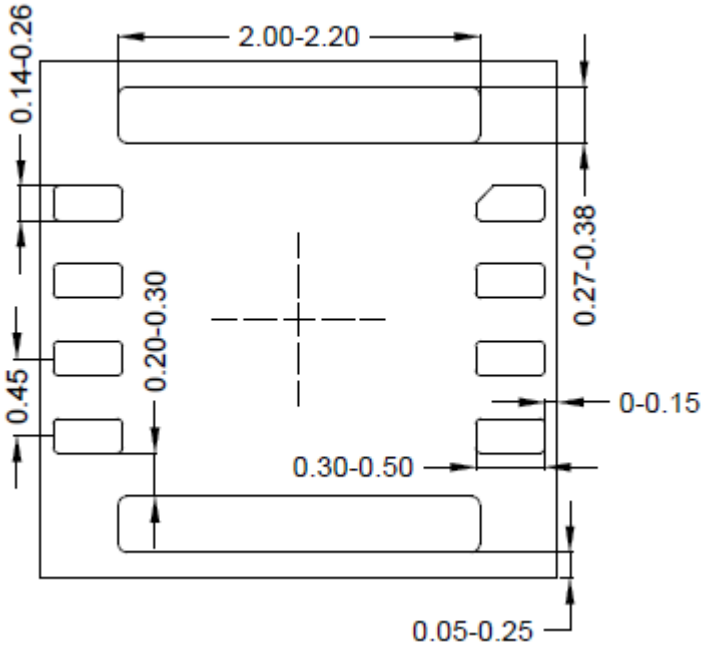
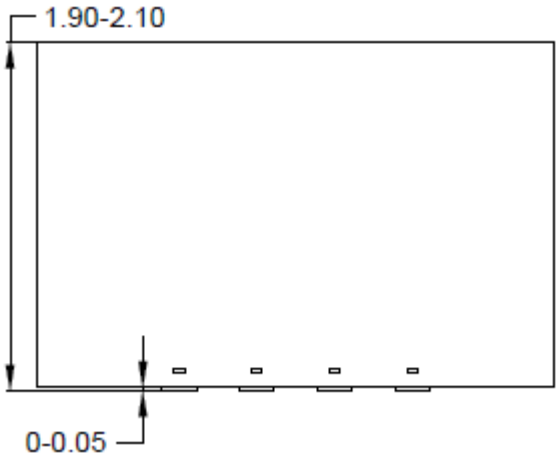
QFN3×3-10 Package Outline



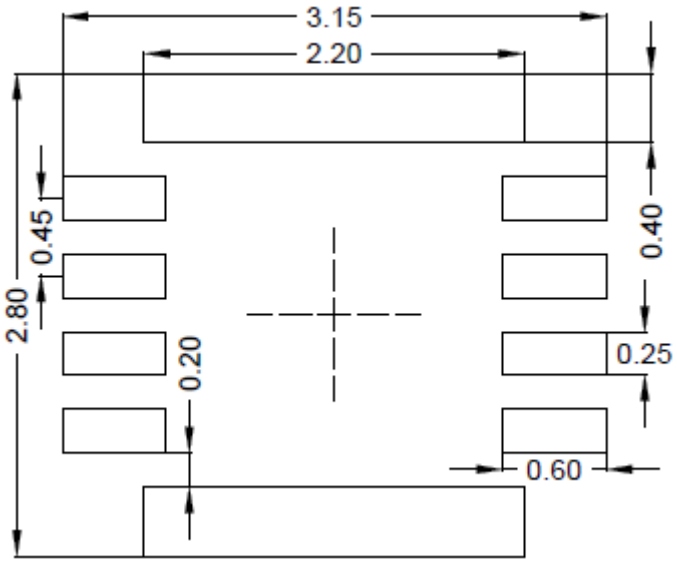
Top View



Bottom View



Side View



Recommended PCB Layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

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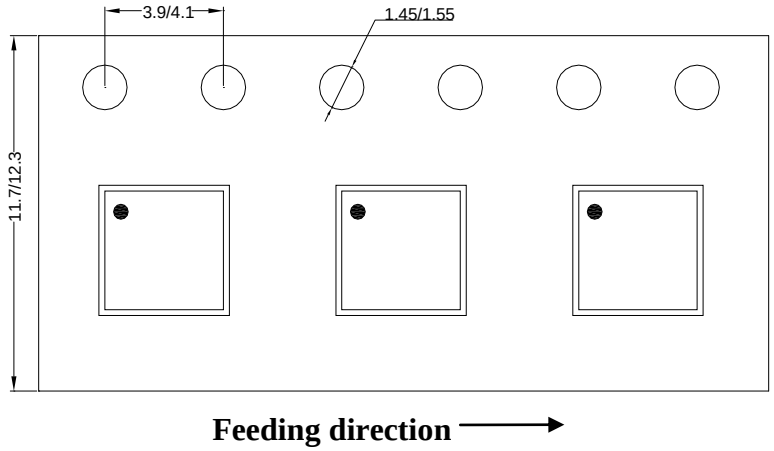
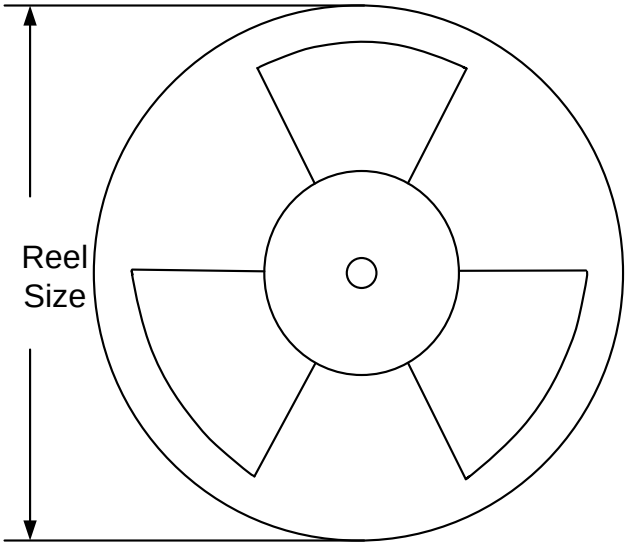
Taping & Reel Specification

1. QFN3×3 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	3000

3. Others: NA

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