Features

- power supplies：1.8 V and 3.3 V
- internal clock speed：1 GSPS (up to 400 MHz analog output)
- Integrated 1 GSPS, 14-bit DAC
- Frequency resolution: 0.23Hz or above
- Phase noise ≤ −125dBc/Hz (400 MHz carrier @ 1 kHz offset)
- Narrow-band SFDR: >80 dB
- Serial input/output (I/O) control
- Automatic linear or arbitrary frequency, phase, and amplitude sweep capability
- Inverse sinc correction filter
- 8 frequency and phase offset profiles
- Internal oscillator, can be driven by a single crystal
- Software and hardware-controlled power-down
- Integrated 1024 word × 32-bit RAM
- Parallel data path interface
- PLL REFCLK multiplier
- Phase modulation capability
- Amplitude modulation capability
- Multichip synchronization
- 100-lead TQFP_EP package

Applications

- Programmable clock generator
- FM chirp source for radar and scanning systems
- Test and measurement equipment
- Acousto-optic device drivers
- Polar modulator
- Fast frequency hopping

General Description

The CBM99D10 is a direct digital synthesizer (DDS) featuring an integrated 14-bit DAC and supporting sample rates up to 1 GSPS. It can generate a sinusoidal waveform of frequency 400MHz. The user has access to the three signal control parameters that control the DDS: Internal frequency, phase, and amplitude.

The DDS provides fast frequency hopping and frequency tuning resolution with its 32-bit accumulator. With a 1 GSPS sample rate, the tuning resolution is ~0.23 Hz. The DDS also enables fast phase and amplitude switching capability. The user can program its internal control registers via a serial I/O port to control the CBM99D10.

The CBM99D10 includes an integrated static RAM to support various combinations of frequency, phase, and/or amplitude modulation. The CBM99D10 also supports a user defined, digitally controlled, digital ramp mode of operation. In this mode, the frequency, phase, or amplitude can be varied linearly over time.

The CBM99D10 integral a high-speed parallel data input port to enable direct frequency, phase, amplitude, or polar modulation.

CATALOG

Functional Block Diagram

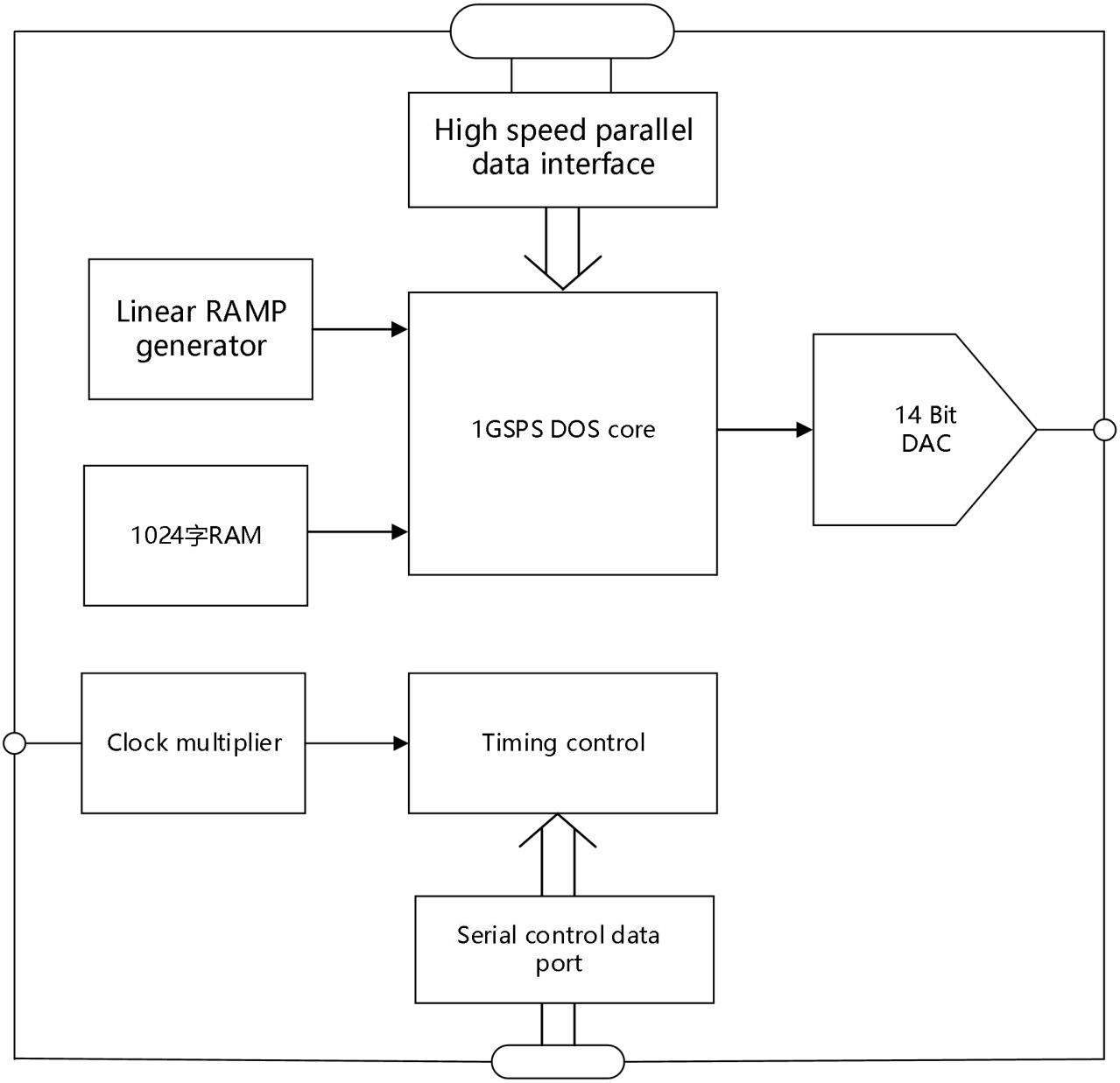


Figure 1. Functional Block Diagram

Specifications

AVDD (1.8 V) and DVDD (1.8 V) = 1.8 V ± 5%, AVDD (3.3 V) = 3.3 V ± 5%, DVDD_I/O = 3.3 V ± 5%, T = 25°C, R_{SET} = 10kΩ, I_{OUT} = 20 mA, external reference clock frequency = 1000 MHz with REFCLK multiplier disabled, unless otherwise noted.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
REF_CLK INPUT CHARACTERISTICS					
Frequency Range					
REFCLK Multiplier	Disabled	60		1000	MHz
	Enabled	3.2		60	MHz
Maximum REFCLK Input Divider Frequency	Full temperature range	1500	1900		MHz
Minimum REFCLK Input Divider Frequency	Full temperature range		25	35	MHz
External Crystal			25		MHz
Input Capacitance			3.2		pF
Input Impedance (Differential)			2.7		kΩ
Input Impedance (Single-ended)			1.35		kΩ
Duty Cycle	REFCLK multiplier disabled	45		55	%
	REFCLK multiplier enabled	40		60	%
REF_CLK Input level	Single-ended	50		1000	mV p-p
	Differential	100		2000	mV p-p
REFCLK MULTIPLIER VCO GAIN CHARACTERISTICS					
VCO Gain (KV) @ Center Frequency	VCO range Setting 0		435		MHz/V
	VCO range Setting 1		511		MHz/V
	VCO range Setting 2		559		MHz/V
	VCO range Setting 3		755		MHz/V
	VCO range Setting 4		793		MHz/V
	VCO range Setting 5		854		MHz/V
REFCLK_OUT CHARACTERISTICS					
Maximum Capacitive Load			18		pF

Maximum Frequency			25		MHz
DAC OUTPUT CHARACTERISTICS					
Full-Scale Output Current		8.8	20	31.7	mA
Gain Error		-10		+10	%FS
Output Offset				3.4	uA
Differential Nonlinearity			0.9		LSB
Integral Nonlinearity			1.7		LSB
Output Capacitance			4		pF
Residual Phase Noise	@ 1 kHz offset, 20 MHz A_{OUT}				
REFCLK Multiplier	Disabled		-150		dBc/Hz
	Enabled @ 20×		-141		dBc/Hz
	Enabled @ 100×		-139		dBc/Hz
Voltage Compliance Range		-0.5		0.5	V
Wideband SFDR(See the Typical Performance Characteristics section)					
SFDR Narrow-Band SFDR					
f_{OUT}=50.1MHz	±500kHz		-85		dBc
	±125kHz		-85		dBc
	±12.5kHz		-93		dBc
f_{OUT}=101.3MHz	±500kHz		-85		dBc
	±125kHz		-85		dBc
	±12.5kHz		-92		dBc
f_{OUT}=201.1MHz	±500kHz		-85		dBc
	±125kHz		-85		dBc
	±12.5kHz		-89		dBc
f_{OUT}=301.1MHz	±500kHz		-84		dBc
	±125kHz		-84		dBc
	±12.5kHz		-86		dBc
f_{OUT}=401.3MHz	±500kHz		-82		dBc
	±125kHz		-82		dBc
	±12.5kHz		-84		dBc
SERIAL PORT TIMING CHARACTERISTICS					
Maximum SCLK Frequency			65		Mbps

Minimum SCLK Clock Pulse Width	Low	3.8			ns
	High	3.8			ns
Maximum SCLK Rise/Fall Time			2.2		ns
Minimum Data Setup Time to SCLK		4.5			ns
Minimum Data Hold Time to SCLK		0			ns
Maximum Data Valid Time in Read Mode				11.3	ns
I/O_UPDATE/PROFILE<2:0>/RT TIMING CHARACTERISTICS					
Profile Minimum switching time	High	2			SYNC_CLK cycle
I/O_UPDATE Pulse Width		>1			SYNC_CLK cycle
Minimum Setup Time to SYNC_CLK		1.78			ns
Minimum Hold Time to SYNC_CLK		0			ns
Tx_ENABLE and 16-BIT PARALLEL (DATA) BUS TIMING					
Maximum PDCLK Frequency			250		MHz
Tx_ENABLE/Data Setup Time (to PDCLK)		1.7			ns
Tx_ENABLE/Data Hold Time (to PDCLK)		0			ns
OTHER TIMING CHARACTERISTICS					
Wake-Up Time					
Fast Recovery Mode			8		SYSCLK cycles
Full Sleep Mode	REFCLK Multiplier Enable		1.2		ms
	REFCLK MultiplierDisable			153	us
Minimum Reset Pulse Width High			5		SYSCLK cycles
DATA LATENCY (PIPE_LINE DELAY)					
Data Latency, Single Tone or using Profiles					
Frequency, Phase, Amplitude-to-DAC Output	Matched latency enabled		91		SYSCLK cycles
Frequency, Phase-to-DAC Output	Matched latency enabled		79		SYSCLK

	and OSK disabled				cycles
	Matched latency disabled		79		SYSCLK cycles
Amplitude-to-DAC Output	Matched latency disabled		47		SYSCLK cycles
Data Latency using RAM Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled/disabled		94		SYSCLK cycles
Amplitude-to-DAC Output	Matched latency enabled		106		SYSCLK cycles
	Matched latency disabled		58		SYSCLK cycles
Scan mode data delay					
Frequency, Phase-to-DAC Output	Matched latency enabled/disabled		91		SYSCLK cycles
Amplitude-to-DAC Output	Matched latency enabled		91		SYSCLK cycles
	Matched latency disabled		47		SYSCLK cycles
Data Latency, 16-Bit Input Modulation Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled		103		SYSCLK cycles
	Matched latency disabled		91		SYSCLK cycles
CMOS LOGIC INPUTS					
Logic 1 Voltage		2.0			V
Logic 0 Voltage				0.8	V
Logic 1 Current			94	158	uA
Logic 0 Current			94	158	uA
Input Capacitance			2.2		pF
XTAL_SEL INPUT					
Logic 1 Voltage		1.25			V
Logic 0 Voltage				0.6	V

Input Capacitance			2		pF
CMOS LOGIC OUTPUT	1mA load 1 mA load				
Logic 1		2.8			V
Logic 0				0.4	V
POWER SUPPLY CURRENT					
I_{AVDD} (1.8 V)			115		mA
I_{AVDD} (3.3 V)			35		mA
I_{DVDD}(1.8V)			225		mA
I_{DVDD}(3.3 V)			13		mA
TOTAL POWER CONSUMPTION					
Single Tone Mode			723	961	mW
Rapid Power-Down Mode			336	459	mW
Full Sleep Mode			21	43	mW

Pin Configuration and Function Descriptions

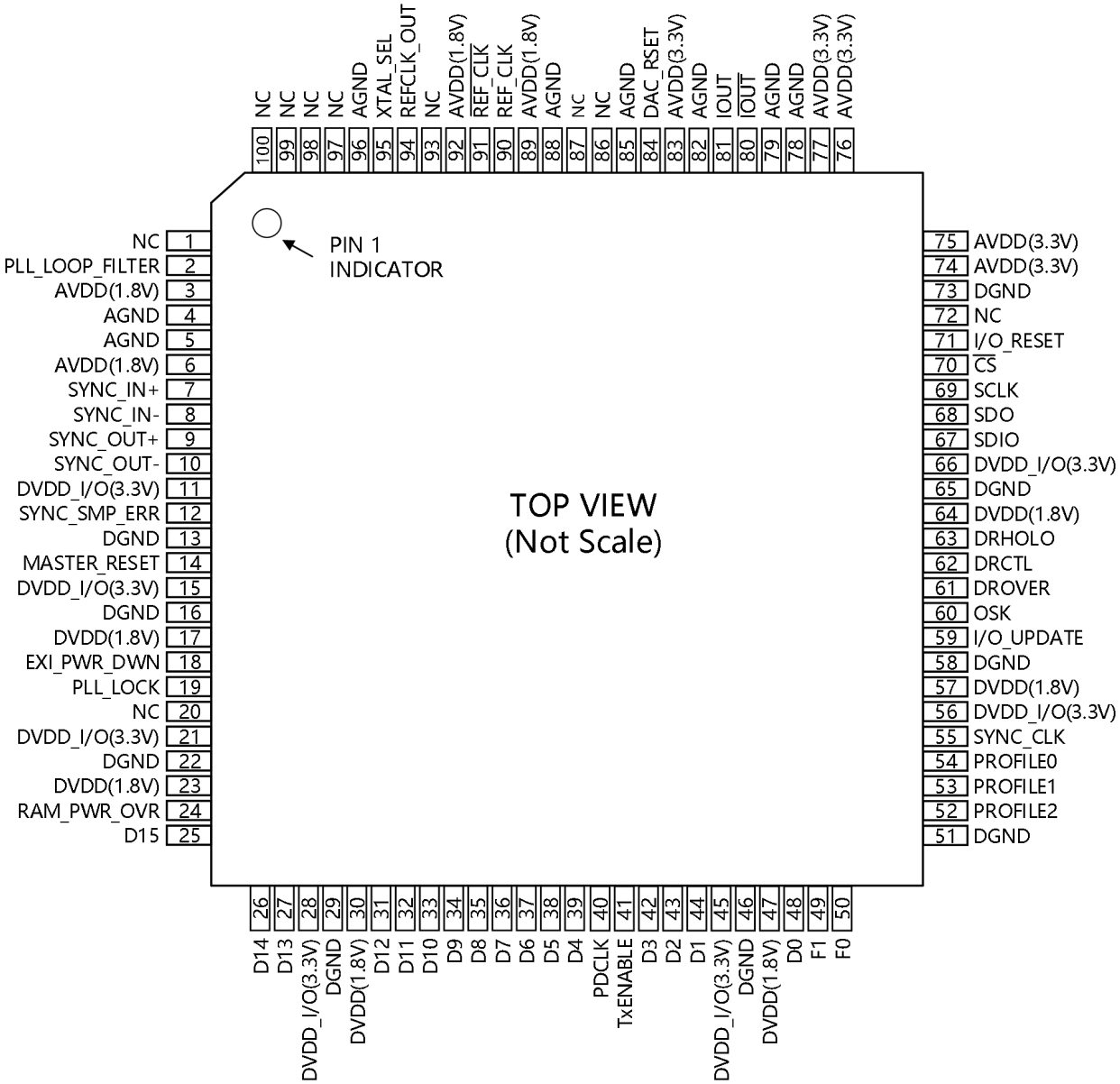


Figure 2. Pin Configuration

Pin Descriptions

Pin No.	Mnemonic	I/O	Description
1,20,72,86,87,93,97 to 100	NC		Not Connected. Allow device pins to float.
2	PLL_LOOP_FILTER	I	PLL Loop Filter Compensation Pin.
3/6/89/92	AVDD (1.8V)	I	Analog Core VDD, 1.8 V Analog Supplies.
74 to 77/83	AVDD (3.3V)	I	Analog DAC VDD, 3.3 V Analog Supplies.
17/23/30/47/57/64	DVDD (1.8V)	I	Digital Core VDD, 1.8 V Digital Supplies.
11/15/21/28/45/56/66	DVDD_I/O (3.3V)	I	Digital Input/Output VDD, 3.3 V Digital Supplies.
4/5/73/78/79/82/85/88/96	AGND	I	Analog Ground.
13/16/22/29/46/51/58/65	DGND	I	Digital Ground.
7	SYNC_IN+	I	Synchronization Signal, Digital Input (Rising Edge Active). The synchronization signal from the external master to synchronize internal sub clocks.
8	SYNC_IN-	I	Synchronization Signal, Digital Input (Rising Edge Active). The synchronization signal from the external master to synchronize internal sub clocks.
9	SYNC_OUT+	O	Synchronization Signal, Digital Output (Rising Edge Active). The synchronization signal from the internal device sub clocks to synchronize external slave devices.
10	SYNC_OUT-	O	Synchronization Signal, Digital Output (Rising Edge Active). The synchronization signal from the internal device sub clocks to synchronize external slave devices.
12	SYNC_SMP_ERR	O	Synchronization Sample Error, Digital Output (Active High). Sync sample error: a high on this pin indicates that the chip did not receive a valid sync signal on SYNC_IN+/SYNC_IN−.
14	MASTER_RESET	I	Master Reset, Digital Input (Active High). Master reset: clears all memory elements and sets registers to default values.
18	EXT_PWR_DWN	I	External Power-Down, Digital Input (Active High). A high level on this pin initiates the currently programmed power-down mode. See the Power-Down Control section of this document for further details. If unused, connect to ground.
19	PLL_LOCK	O	Clock Multiplier PLL Lock, Digital Output (Active High). A high on this pin indicates the Clock Multiplier PLL has acquired lock to the reference clock input.
24	RAM SWP OVR	O	RAM Sweep Over, Digital Output (Active High). A high on this pin indicates the RAM sweep profile has completed.

25 to 27 、 31 to 39、42 to 44、48	D<15:0>	I	Parallel Input Bus (Active High).
49,50	F[1 :0]	I	Modulation Format Pin. Digital input to determine the modulation format.
40	PDCLK	O	Parallel Data Clock. This is the digital output (clock).
41	TxENABLE	I	Transmit Enable. Digital input (active high).
52 to 54	PROFILE<2:0>	I	Profile Select Pins. Digital inputs (active high). Use these pins to select one of eight phase/frequency profiles for the DDS. Changing the state of one of these pins transfers the current contents of all I/O buffers to the corresponding registers. State changes should be set up on the SYNC_CLK pin.
55	SYNC_CLK	O	Output Clock Divided-By-Four. A digital output (clock). Many of the digital inputs on the chip, such as I/O_UPDATE and PROFILE<2:0> need to be set up on the rising edge of this signal.
59	I/O_UPDATE	I/O	Input/Output Update. Digital input (active high). A high on this pin transfers the contents of the I/O buffers to the corresponding internal registers.
60	OSK	I	Output Shift Keying. Digital input (active high). When the OSK features are placed in either manual or automatic mode, this pin controls the OSK function. If unused, this pin connects to high.
61	DROVER	O	Digital Ramp Over. Digital output (active high). This pin switches to Logic 1 whenever the digital ramp generator reaches its programmed upper or lower limit.
62	DRCTL	I	Digital Ramp Control. Digital input (active high). This pin controls the slope polarity of the digital ramp generator. See the Digital Ramp Generator (DRG) section for more details. If not using the digital ramp generator, connect this pin to Logic 0.
63	DRHOLD	I	Digital Ramp Hold. Digital input (active high). This pin stalls the digital ramp generator in its present state. If not using digital ramp generator, connect this pin to Logic 0.
67	SDIO	I/O	Serial Data Input/Output. Digital input/output (active high). This pin can be either uni-directional or bidirectional (default), depending on the configuration settings. In bidirectional serial port mode, this pin acts as the serial data input and output. In unidirectional mode, it is an input only.
68	SDO	O	Serial Data Output. Digital output (active high). This pin is only active in unidirectional serial data mode. In this mode, it functions as the output. In bidirectional mode, this pin is not operational and should be left floating.
69	SCLK	I	Serial Data Clock. Digital clock (rising edge on write,

			falling edge on read). This pin provides the serial data clock for the control data path. Write operations to the CBM97D79TQ use the rising edge. Readback operations from the CBM97D79TQ use the falling edge.
70	CS	I	Chip Select. Digital input (active low). This pin allows the AD9910 to operate on a common serial bus for the control data path. Bringing this pin low enables the AD9910 to detect serial clock rising/falling edges. Bringing this pin high causes the CBM97D79TQ to ignore input on the serial data pins.
71	I/O_RESET	I	Input/Output Reset. Digital input (active high). When the communication cycle goes high during a failure, this pin does not reset the entire device, but resets the state machine of the serial port controller and clears any I / O buffers written since the last I / O update. When not used, connect this pin to ground.
80	IOUT	O	Open-Source DAC Complementary Output Source. Analog output (current mode). Connect through a 50 Ω resistor to AGND.
81	IOUT	O	Open-Source DAC Output Source. Analog output (current mode). Connect through a 50 Ω resistor to AGND.
84	DAC_RSET	O	Analog Reference Pin. This pin programs the DAC output full-scale reference current. Attach a 10 kΩ resistor to AGND.
90	REF_CLK	I	Reference Clock Input. Analog input.
91	REF_CLK	I	Complementary reference Clock Input. Analog input.
94	REFCLK_OUT	O	Reference Clock Input. Analog input.
95	XTAL_SEL	I	Crystal selection
96	EPAD		EPAD shall be grounded by welding

1. 1. I = Input，O = Output。

Typical Performance Characteristics

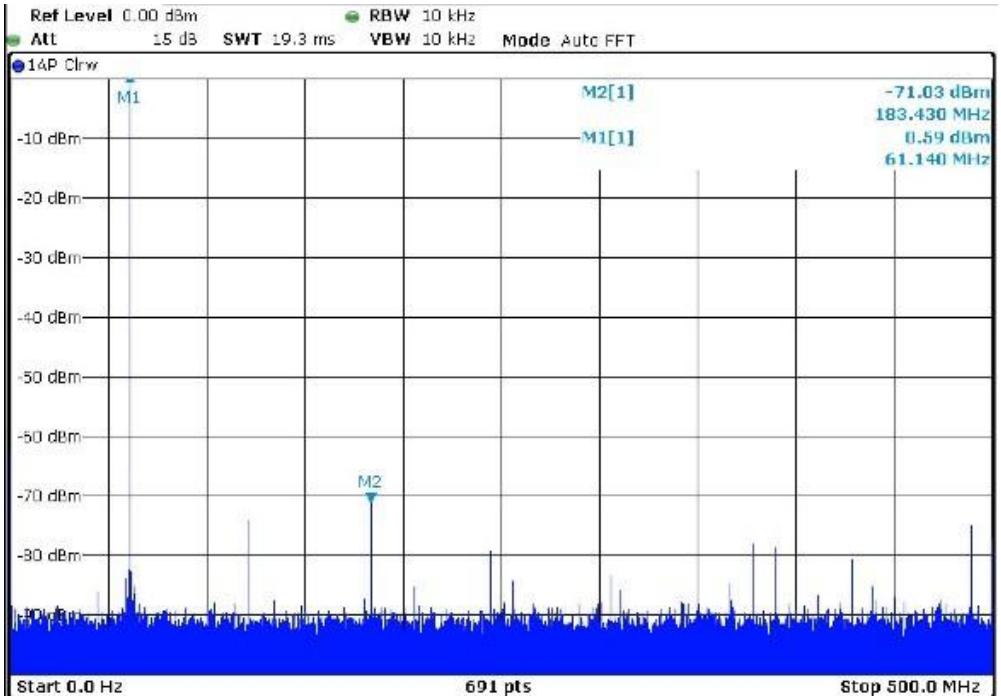


Figure 3. Wideband SFDR at 61.1 MHz, REFCLK=1GHZ

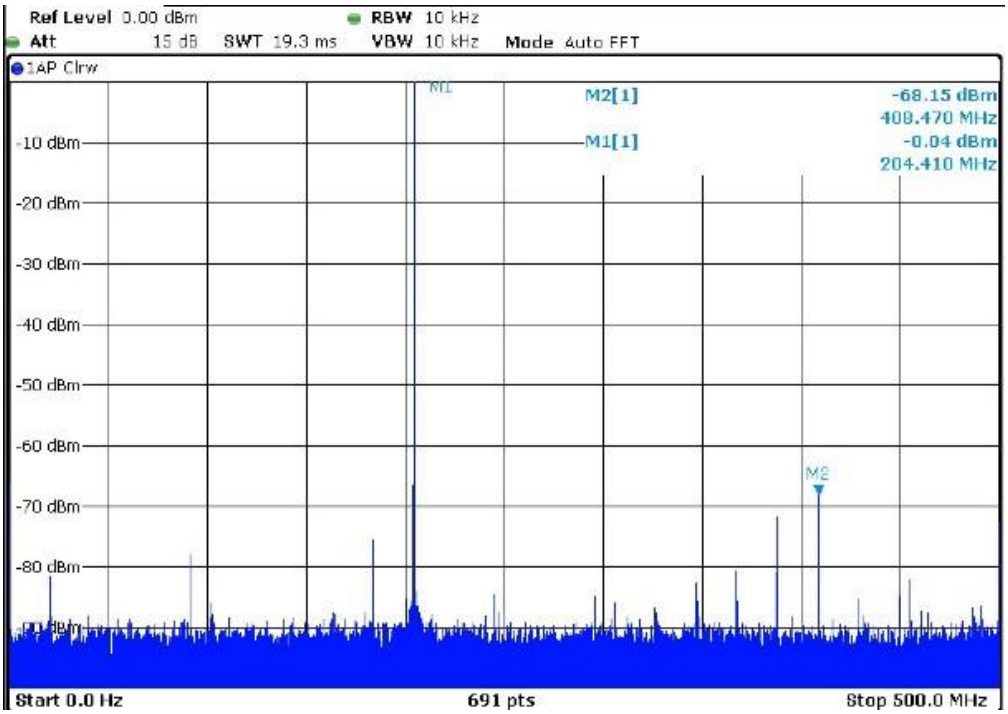


Figure 4. Wideband SFDR at 204.1 MHz, REFCLK=1GHZ

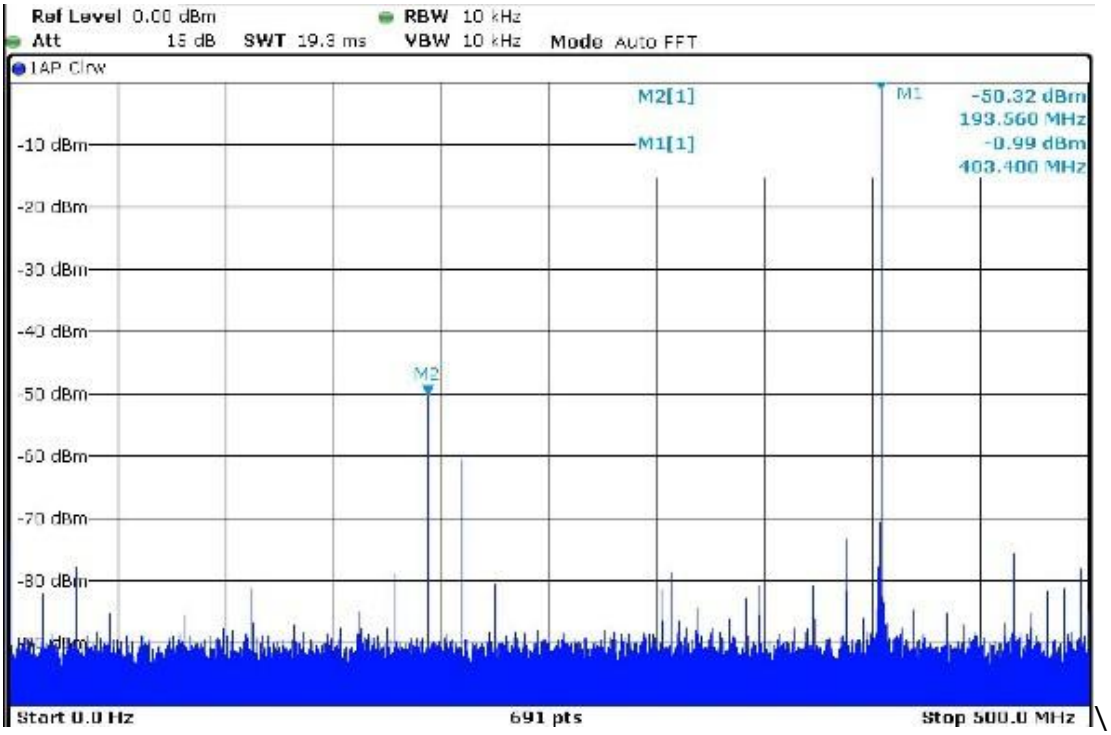


Figure 5. Wideband SFDR at 403.1MHz, REFCLK=1GHZ

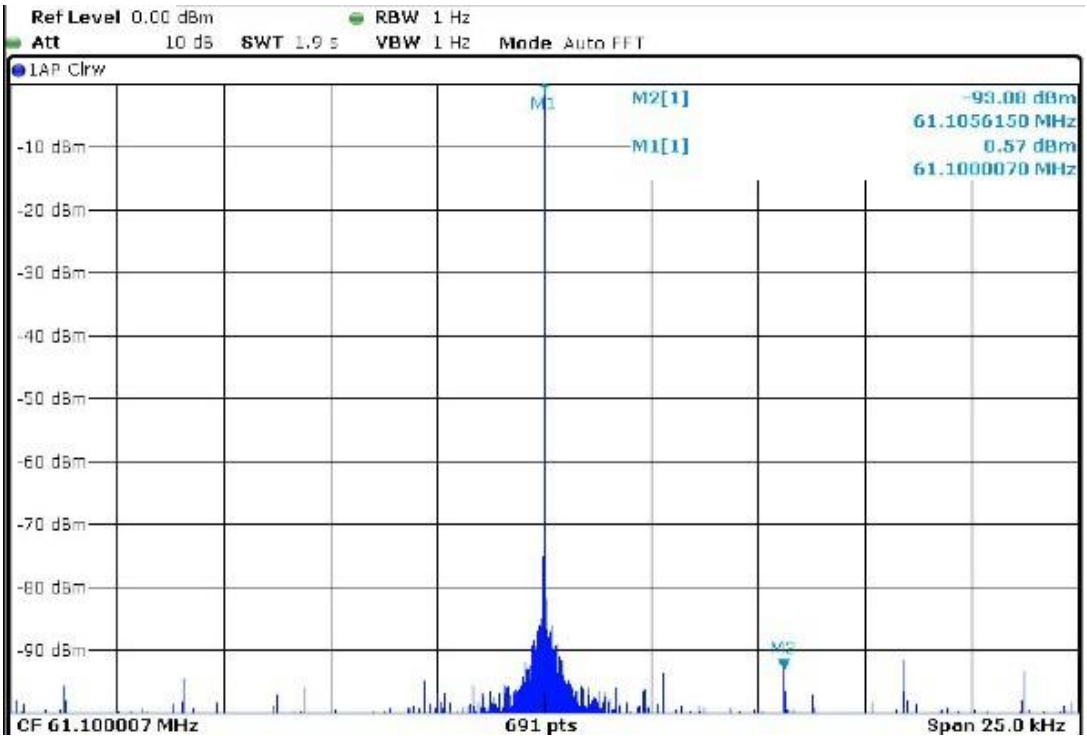


Figure 6. Narrowband view of Fig. 3 (with carrier and lower sideband suppression)

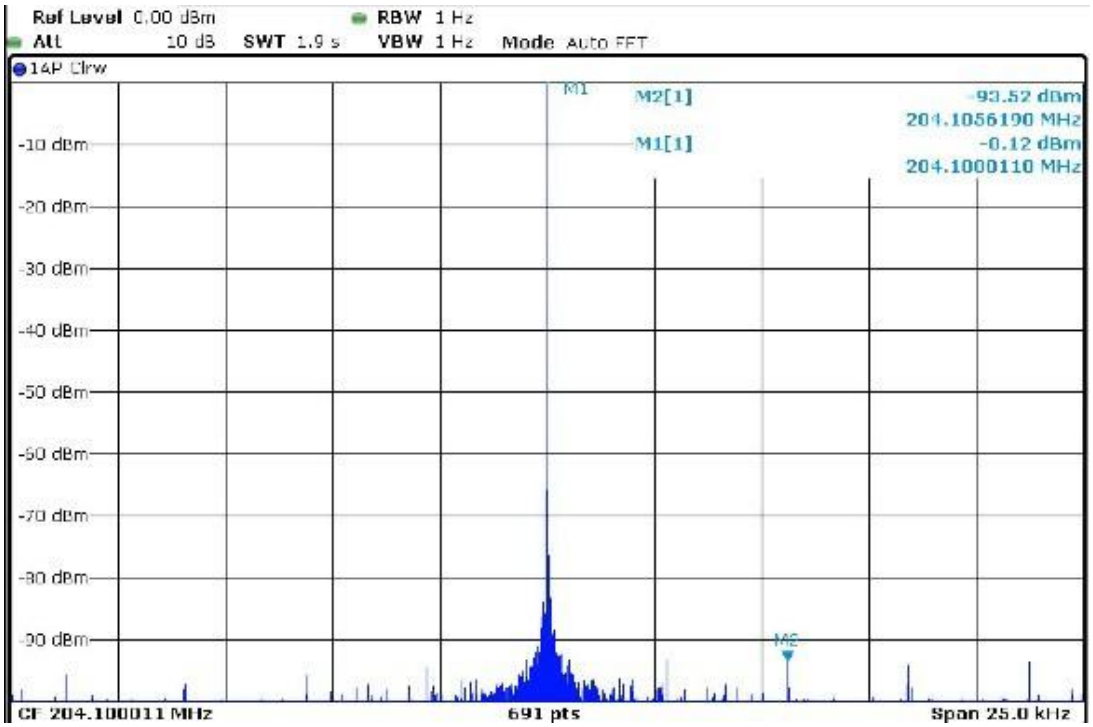


Figure 7. Narrowband view of Fig. 4 (with carrier and lower sideband suppression)

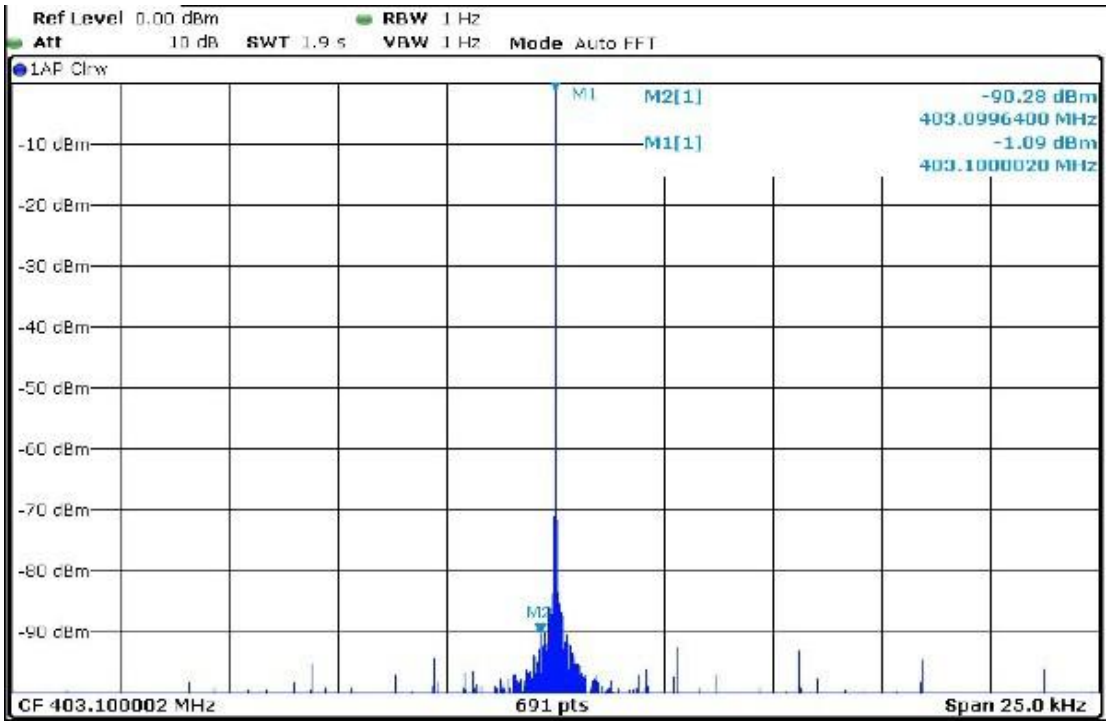


Figure 8. Narrowband view of Fig. 5 (with carrier and lower sideband suppression)

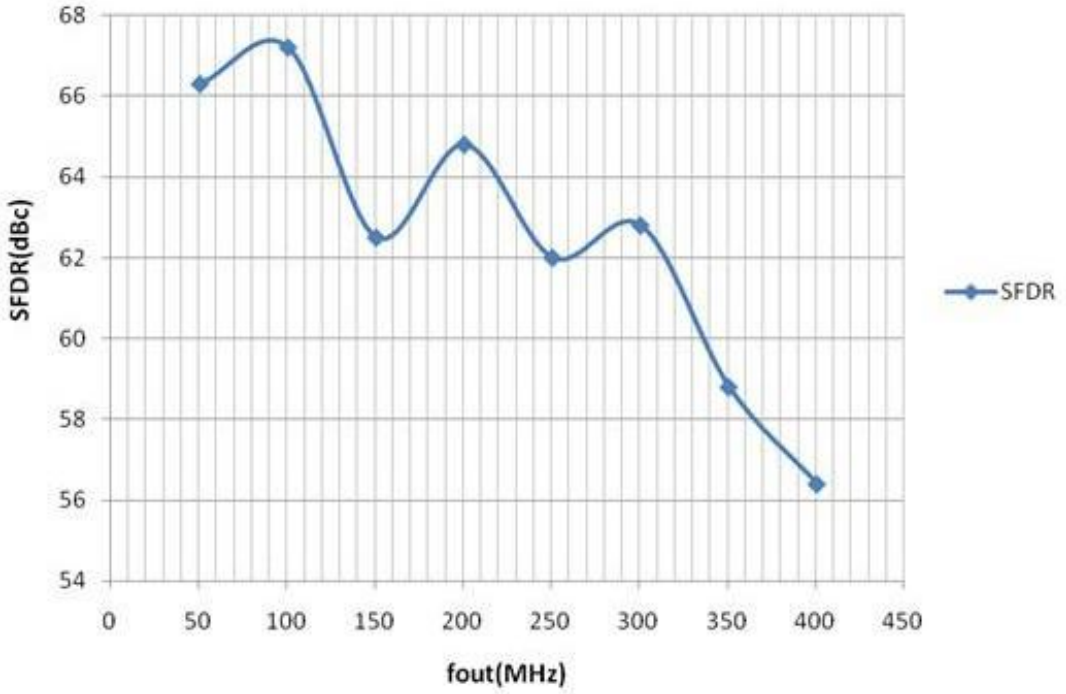


Figure 9. Wideband SFDR vs. Output Frequency

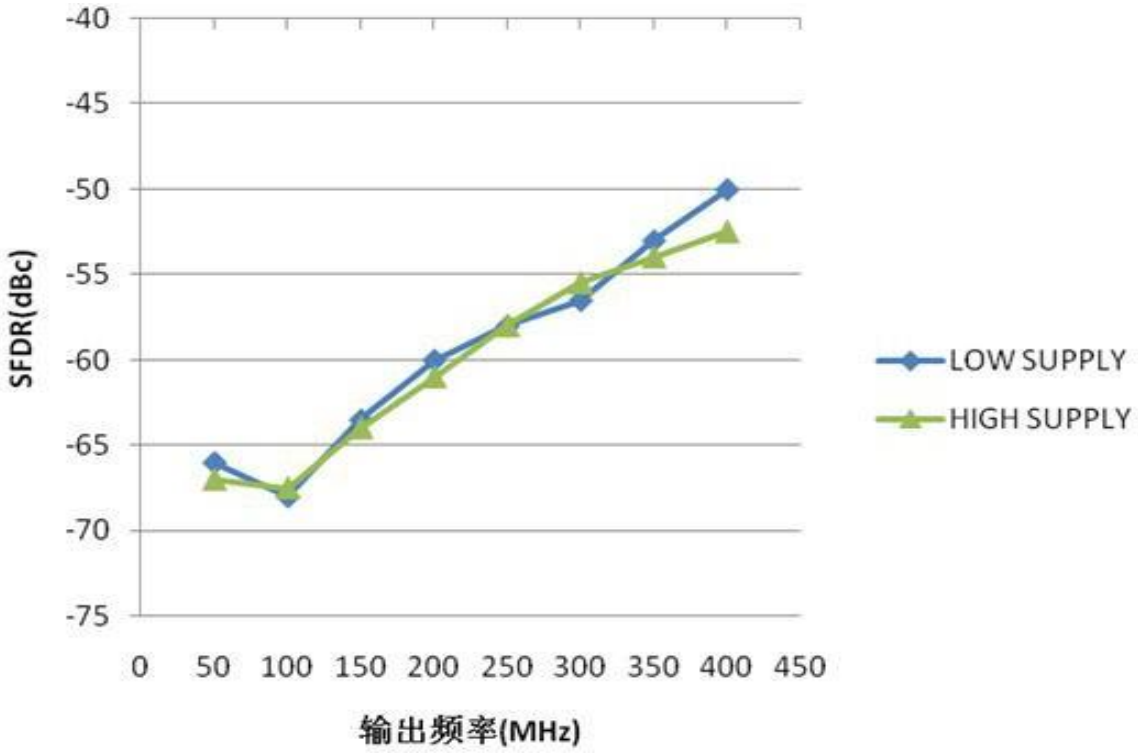


Figure 10. Wideband SFDR Output Frequency vs. Supply (±5%), REFCLK = 1 GHz

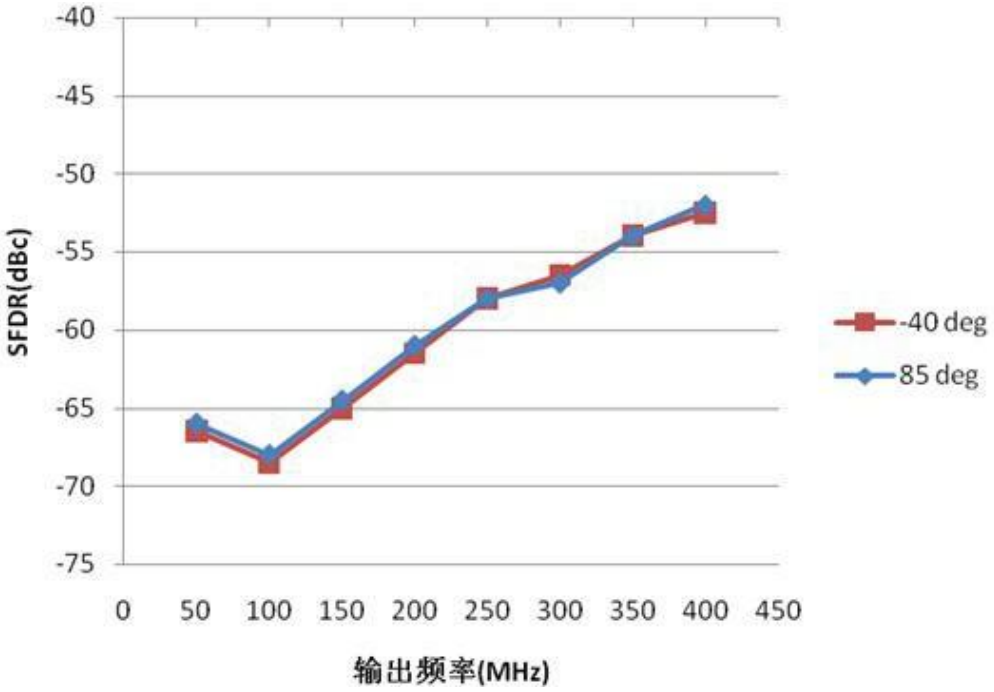


Figure 11. Wideband SFDR vs. Frequency and temperature, REFCLK = 1 GHz

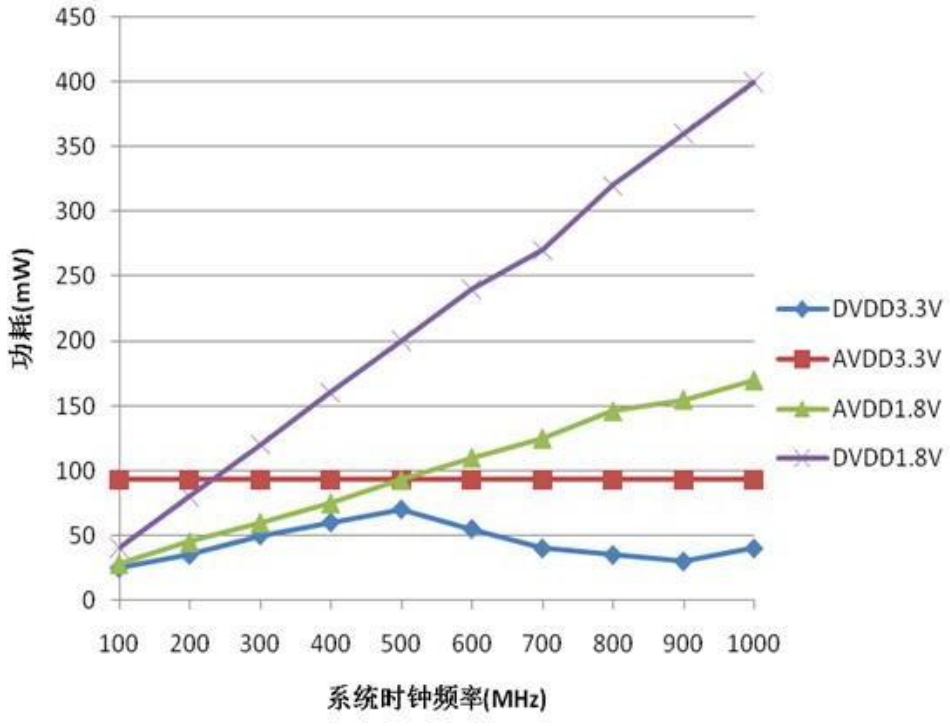


Figure 12. Power Dissipation vs. System Clock (PLL disabled)

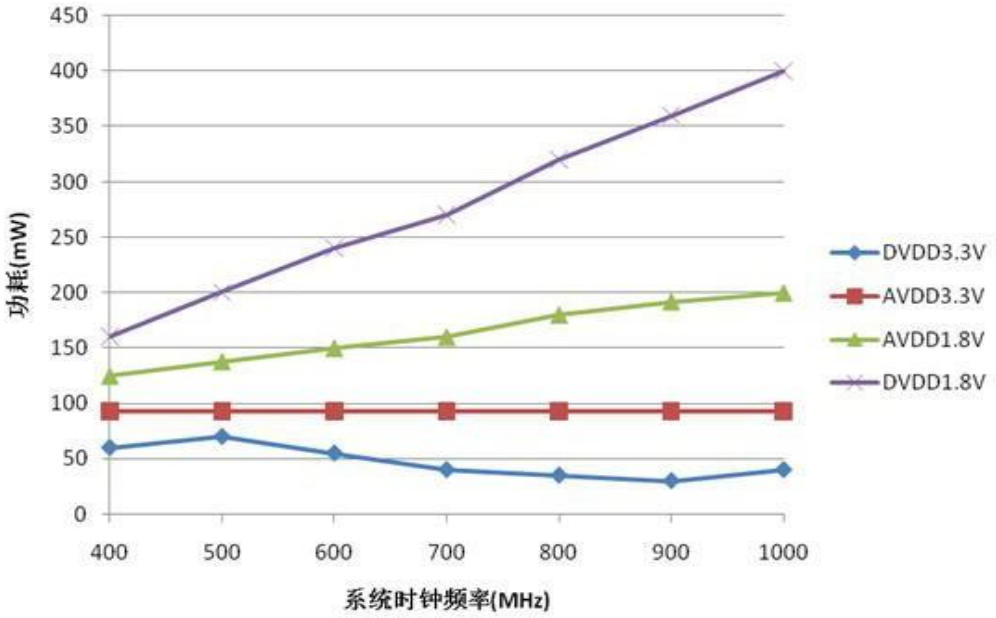


Figure 13. Power Dissipation vs. System Clock (PLL Enabled)

Table 1. Residual phase noise, system clock = 1GHz

frequency offset (Hz) / fout(Hz)	@10	@100	@1k	@10k	@100k	@1M	@10M
20.1M	-135	-145	-155	-161	-167	-167	-167
98.6M	-120	-131	-140	-150	-160	-161	-161
201.1M	-115	-125	-135	-145	-155	-158	-158
397.8M	-108	-117	-125	-135	-142	-150	-150

Table 2. Residual phase noise,using EFCLK multiplier, REFCLK=50MHz×20 and system clock=1GHz

frequency offset (Hz) / fout(Hz)	@10	@100	@1k	@10k	@100k	@1M	@10M
20.1M	-120	-131	-140	-150	-152	-145	-152
98.6M	-109	-118	-126	-136	-139	-131	-148
201.1M	-100	-110	-119	-130	-132	-125	-140
397.8M	-91	-101	-110	-120	-123	-115	-131

Serial I/O Timing Diagrams

The diagrams below provide basic examples of the timing relationships between the various control signals of the serial I/O port.

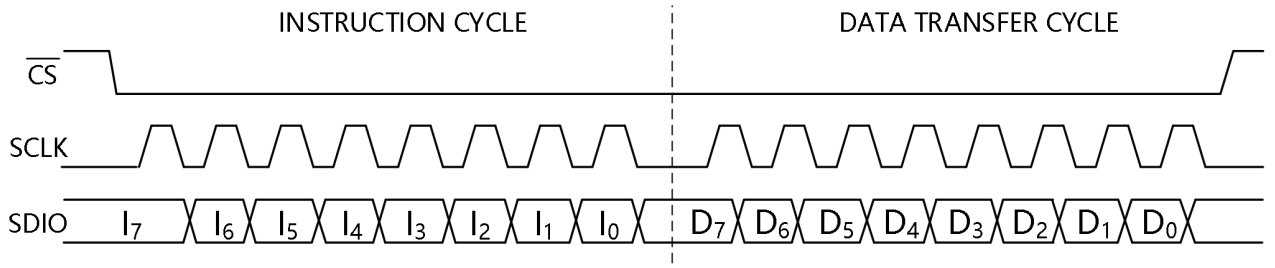
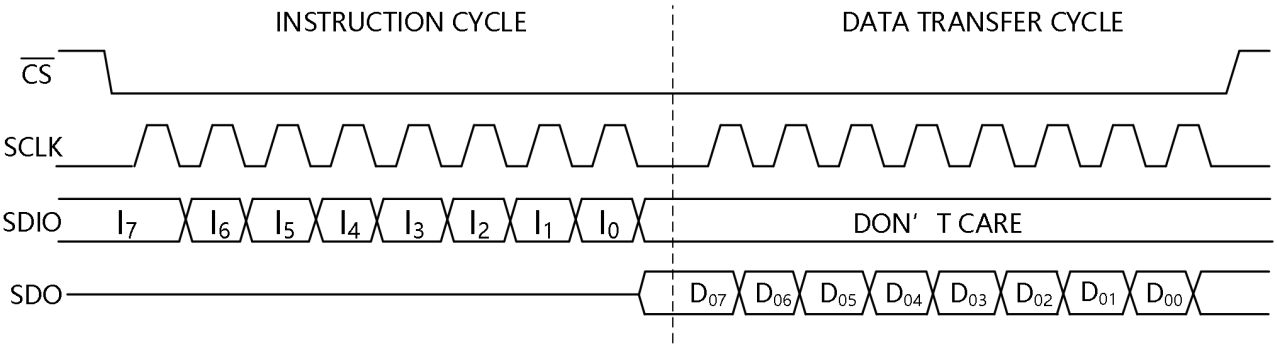


Figure 14. Serial Port Write Timing, Clock Stall Low



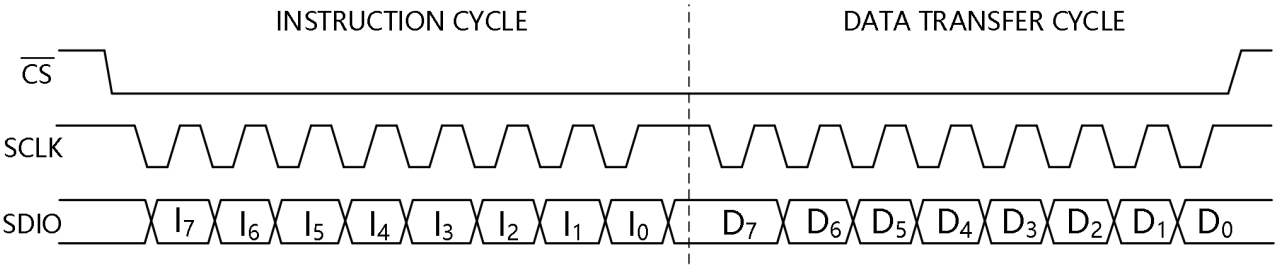


Figure 16. 3-Wire Serial Port Read Timing, Clock Stall High

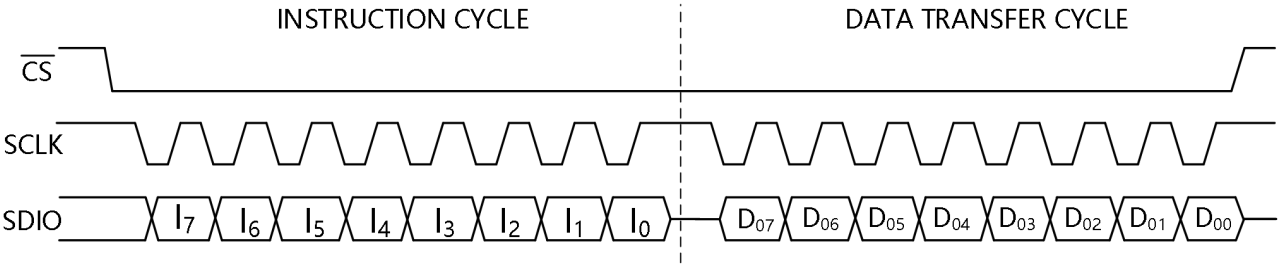


Figure 17. 2-Wire Serial Port Read Timing, Clock Stall High

Register Map and Bit Descriptions

Register Map

Note that the highest number found in the Bit Range column for each register in the following tables is the MSB and the lowest number is the LSB for that register.

Register Name and Address	Bit Address	Bit 7(MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0(LSB)	Default Value
CFR1—Control Function Register 1 (0x00)	31:24	RAM Enable	RAM Playback Destination		Open					0x00
	23:16	Manual OSK External Control	Inverse Sinc Filter Enable	Open	Internal Profile Control				Select DDS Sine Output	0x00
	15:8	Load LRR @ I/O Update	Auto clear Digital Ramp Accum.	Autoclear Phase Accum.	Clear Digital Ramp Accum.	Clear Phase Accum.	Load ARR @ I/O Update	OSK Enable	Select Auto OSK	0x00
	7:0	Digital Power-Down	DAC Power-Down	REFCLK Input Power-Down	Aux DAC Power-Down	External Power-Down Control	Open	SDIO Input Only	LSB First	0x00
CFR2—Control Function Register 2(0x01)	31:24	Open							Enable Amplitude Scale from Single Tone Profiles	0x00
	23:16	Internal I/O Update Active	SYNC_CLK Enable	Digital Ramp Destination		Digital Ramp Enable	Digital Ramp No-Dwell High	Digital Ramp No-Dwell Low	FTW Read Effective FTW	0x40

	15:08	I/O Update Rate Control		Open		PDCLK Enable	PDCLK Invert	TxEnable Invert	Open	0x08
	7:0	Matched Latency Enable	Data Assembler Hold Last Value	Sync Sample Error Mask	Parallel Data Port Enable	FM Gain				0x20
CFR3—Control Function Register 3 (0x01)	31:24	Open		DRV0[1:0]		Open	VCO SEL<2:0>			0x1F
	23:16	Open		ICP[2:0]			Open			0x3F
	15:8	REFCLK Input Divider Bypass	REFCLK Input Divider ResetB	Open			PFD Reset	Open	PLL Enable	0x40
	7:0	N [6:0]							开路	0x00
Auxiliary DAC Control (0x03)	31:24	Open								0x00
	23:16	Open								0x00
	15:8	Open								0x00
	7:0	FSC [7:0]								0x7F
	31:24	I/O Update Rate<31:24>								0xFF
I/O Update Rate (0x04)	23:16	I/O Update Rate [23:16]								0xFF
	15:8	I/O Update Rate [15:8]								0xFF
	7:0	I/O Update Rate [7:0]								0xFF
FTW—Frequency Tuning Word (0x07)	31:24	Frequency Tuning Word [31:24]								0x00
	23:16	Frequency Tuning Word [23:16]								0x00
	15: 8	Frequency Tuning Word [15:8]								0x00
	7:0	Frequency Tuning Word [7:0]								0x00
POW—Phase	15: 8	Phase Offset Word [15:8]								0x00

Offset Word (0x08)	7:0	Phase Offset Word [7:0]				0x00
ASF—Amplitude Scale Factor (0x09)	31:24	Amplitude Ramp Rate<15:8>				0x00
	23:16	Amplitude Ramp Rate<7:0>				0x00
	15: 8	Amplitude Scale Factor<13:6>				0x00
	7:0	Amplitude Scale Factor<5:0>			Amplitude Step Size<1:0>	0x00
Multichip Sync (0x0A)	31:24	Sync Validation Delay<3:0>	Sync Receiver Enable	Sync Generator Enable	Sync Generator Polarity	Open	0x00
	23:16	Sync State Preset Value<5:0>			Open		0x00
	15:08	Output Sync Generator Delay [4:0]		Open			0x00
	7:0	Output Sync Generator Delay [4:0]		Open			0x00
Digital Ramp Limit (0x0B)	63:56	Digital Ramp Upper Limit [31:24]					N/A
	55:48	Digital Ramp Upper Limit [23:16]					N/A
	47:40	Digital Ramp Upper Limit [15:8]					N/A
	39:32	Digital Ramp Upper Limit [7:0]					N/A
	31:24	Digital Ramp Lower Limit [31:24]					N/A
	23:16	Digital Ramp Lower Limit [23:16]					N/A
	15:08	Digital Ramp Lower Limit [15:8]					N/A
	7:0	Digital Ramp Lower Limit [7:0]					N/A
Digital Ramp Step Size (0x0C)	63:56	Digital Ramp Decrement Step Size [31:24]					N/A
	55:48	Digital Ramp Decrement Step Size [23:16]					N/A
	47:40	Digital Ramp Decrement Step Size [15:8]					N/A
	39:32	Digital Ramp Decrement Step Size [7:0]					N/A

	31:24	Digital Ramp Increment Step Size [31:24]			N/A
	23:16	Digital Ramp Increment Step Size [23:16]			N/A
	15:08	Digital Ramp Increment Step Size [15:8]			N/A
	7:0	Digital Ramp Increment Step Size [7:0]			N/A
Digital Ramp Rate (0x0D)	31:24	Digital Ramp Negative Slope Rate [15:8]			N/A
	23:16	Digital Ramp Negative Slope Rate [7:0]			N/A
	15:8	Digital Ramp Positive Slope Rate [15:8]			N/A
	7:0	Digital Ramp Positive Slope Rate [7:0]			N/A
Single Tone Profile 0(0x0E)	63:56	Open	Amplitude Scale Factor 0 [13:8]		0x08
	55:48	0Amplitude Scale Factor 0 [7:0]			0xB5
	47:40	Phase Offset Word 0[15:8]			0x00
	39:32	Phase Offset Word 0[7:0]			0x00
	31:24	Frequency Tuning Word 0[31:24]			0x00
	23:16	Frequency Tuning Word 0[23:16]			0x00
	15:8	Frequency Tuning Word 0[15:8]			0x00
	7:0	Frequency Tuning Word 0[7:0]			0x00
RAM Profile 0 (0x0E)	63:56	Open			0x00
	55:48	RAM Profile 0 Address Step Rate [15:8]			0x00
	47:40	RAM Profile 0 Address Step Rate [7:0]			0x00
	39:32	RAM Profile 0 Waveform End Address [9:2]			0x00
	31:24	RAM Profile 0 Waveform End Address [1:0]	Open		0x00
	23:16	RAM Profile 0 Waveform Start Address [9:2]			0x00
	15:8	RAM Profile 0 Waveform	Open		0x00

		Start Address [1:0]					
	7:0	Open	No-Dwell High	Open	Zero- Crossing	RAM Profile 0 Model Control 模式控制[2:0]	0x00
Single Tone Profile1(0x0F)	63:56	Open	Amplitude Scale Factor 1 [13:8]				0x00
	55:48	Amplitude Scale Factor 1[7:0]					0x00
	47:40	Phase Offset Word 1[15:8]					0x00
	39:32	Phase Offset Word 1[7:0]					0x00
	31:24	Frequency Tuning Word 1[31:24]					0x00
	23:16	Frequency Tuning Word 1[23:16]					0x00
	15:8	Frequency Tuning Word 1[15:8]					0x00
	7:0	Frequency Tuning Word 1[7:0]					0x00
RAM Profile1(0x0F)	63:56	Open					0x00
	55:48	RAM Profile1 Address Step Rate [15:8]					0x00
	47:40	RAM Profile1 Address Step Rate [7:0]					0x00
	39:32	RAM Profile1 Waveform End Address [9:2]					0x00
	31:24	RAM Profile1 Waveform End Address [1:0]	Open				0x00
	23:16	RAM Profile1 Waveform Start Address [9:2]					0x00
	15:8	RAM Profile1 Waveform Start Address [1:0]	Open				0x00
	7:0	Open	No-Dwell High	Open	Zero-Crossing	RAM Profile1 Model Contro [2:0]	0x00
Single Tone Profile	63:56	Open	Amplitude Scale Factor 2[13:8]				0x00
	55:48	Amplitude Scale Factor 2[7:0]					0x00

2(0x10)	47:40	Phase Offset Word 2[15:8]					0x00
	39:32	Phase Offset Word 2[7:0]					0x00
	31:24	Frequency Tuning Word 2[31:24]					0x00
	23:16	Frequency Tuning Word 2[23:16]					0x00
	15:8	Frequency Tuning Word 2[15:8]					0x00
	7:0	Frequency Tuning Word 2[7:0]					0x00
RAM Profile2(0x10)	63:56	Open					0x00
	55:48	RAM Profile2 Address Step Rate [15:8]					0x00
	47:40	RAM Profile2 Address Step Rate [7:0]					0x00
	39:32	RAM Profile2 Waveform End Address [9:2]					0x00
	31:24	RAM Profile2 Waveform End Address [1:0]	Open				0x00
	23:16	RAM Profile2 Waveform Start Address [9:2]					0x00
	15:8	RAM Profile2 Waveform Start Address [1:0]	Open				0x00
	7:0	Open	No-Dwell High	Open	Zero-Crossing	RAM Profile2 Mode Control [2:0]	0x00
Single Tone Profile 3(0x11)	63:56	Open	Amplitude Scale Factor 3[13:8]				0x00
	55:48	Amplitude Scale Factor 3[7:0]					0x00
	47:40	Phase Offset Word 3[15:8]					0x00
	39:32	Phase Offset Word 3[7:0]					0x00
	31:24	Frequency Tuning Word 3[31:24]					0x00
	23:16	Frequency Tuning Word 3[23:16]					0x00
	15:8	Frequency Tuning Word 3[15:8]					0x00
	7:0	Frequency Tuning Word 3[7:0]					0x00
RAM	63:56	Open					0x00

Profile3(0x11)	55:48	RAM Profile3 Address Step Rate [15:8]					0x00
	47:40	RAM Profile3 Address Step Rate [7:0]					0x00
	39:32	RAM Profile3 Waveform End Address [9:2]					0x00
	31:24	RAM Profile3 Waveform End Address [1:0]	Open				0x00
	23:16	RAM Profile3 Waveform Start Address [9:2]					0x00
	15:8	RAM Profile3 Waveform Start Address [1:0]	Open				0x00
	7:0	Open	No-Dwell High	Open	Zero-Crossing	RAM Profile3 Mode Control [2:0]	0x00
Single Tone Profile 4(0x12)	63:56	Open	Amplitude Scale Factor 4[13:8]				0x00
	55:48	Amplitude Scale Factor 4[7:0]					0x00
	47:40	Phase Offset Word 4[15:8]					0x00
	39:32	Phase Offset Word 4[7:0]					0x00
	31:24	Frequency Tuning Word 4[31:24]					0x00
	23:16	Frequency Tuning Word 4[23:16]					0x00
	15:8	Frequency Tuning Word 4[15:8]					0x00
	7:0	Frequency Tuning Word 4[7:0]					0x00
RAM Profile4(0x12)	63:56	Open					0x00
	55:48	RAM Profile4 Address Step Rate [15:8]					0x00
	47:40	RAM Profile4 Address Step Rate [7:0]					0x00
	39:32	RAM Profile4 Waveform End Address [9:2]					0x00
	31:24	RAM Profile4 Waveform End Address 波 [1:0]	Open				0x00
	23:16	RAM Profile4 Waveform Start Address [9:2]					0x00
	15:8	RAM Profile4 Waveform Start Address [1:0]	Open				0x00

	7:0	Open	No-Dwell High	Open	Zero-Crossing	RAM Profile4 Mode Control [2:0]	0x00
单频调制 Single Tone Profile 5(0x13)	63:56	Open	Amplitude Scale Factor 5[13:8]				0x00
	55:48	Amplitude Scale Factor 5[7:0]					0x00
	47:40	Phase Offset Word 5[15:8]					0x00
	39:32	Phase Offset Word 5[7:0]					0x00
	31:24	Frequency Tuning Word 5[31:24]					0x00
	23:16	Frequency Tuning Word 5[23:16]					0x00
	15:8	Frequency Tuning Word 5[15:8]					0x00
	7:0	Frequency Tuning Word 5[7:0]					0x00
RAM Profile5(0x13)	63:56	Open					0x00
	55:48	RAM Profile5 Address Step Rate [15:8]					0x00
	47:40	RAM Profile5 Address Step Rate [7:0]					0x00
	39:32	RAM Profile5 Waveform End Address [9:2]					0x00
	31:24	RAM Profile5 Waveform End Address [1:0]	Open				0x00
	23:16	RAM Profile5 Waveform Start Address [9:2]					0x00
	15:8	RAM Profile5 Waveform Start Address [1:0]	Open				0x00
	7:0	Open	No-Dwell High	Open	Zero-Crossing	RAM Profile5 Mode Control [2:0]	0x00

单频调制 Single Tone Profile 6(0x14)	63:56	Open	Amplitude Scale Factor 6[13:8]				0x00
	55:48	Amplitude Scale Factor 6[7:0]					0x00
	47:40	Phase Offset Word 6[15:8]					0x00
	39:32	Phase Offset Word 6[7:0]					0x00
	31:24	Frequency Tuning Word 6[31:24]					0x00
	23:16	Frequency Tuning Word 6[23:16]					0x00
	15:8	Frequency Tuning Word 6[15:8]					0x00
	7:0	Frequency Tuning Word 6[7:0]					0x00
RAM Profile6(0x14)	63:56	Open					0x00
	55:48	RAM Profile6 Address Step Rate [15:8]					0x00
	47:40	RAM Profile6 Address Step Rate [7:0]					0x00
	39:32	RAM Profile6 Waveform End Address [9:2]					0x00
	31:24	RAM Profile6 Waveform End Address [1:0]	Open				0x00
	23:16	RAM Profile6 Waveform Start Address [9:2]					0x00
	15:8	RAM Profile6 Waveform Start Address [1:0]	Open				0x00
	7:0	Open	No-Dwell High	Open	Zero-Crossing	RAM Profile6 Mode Control [2:0]	0x00
单频调制 Single Tone Profile 7(0x15)	63:56	Open	Amplitude Scale Factor 7[13:8]				0x00
	55:48	Amplitude Scale Factor 7[7:0]					0x00
	47:40	Phase Offset Word 7[15:8]					0x00
	39:32	Phase Offset Word 7[7:0]					0x00

	31:24	Frequency Tuning Word 7[31:24]					0x00
	23:16	Frequency Tuning Word 7[23:16]					0x00
	15:8	Frequency Tuning Word 7[15:8]					0x00
	7:0	Frequency Tuning Word 7[7:0]					0x00
RAM Profile7(0x15)	63:56	Open					0x00
	55:48	RAM Profile7 Address Step Rate [15:8]					0x00
	47:40	RAM Profile7 Address Step Rate [7:0]					0x00
	39:32	RAM Profile7 Waveform End Address [9:2]					0x00
	31:24	RAM Profile7 Waveform End Address [1:0]	Open				0x00
	23:16	RAM Profile7 Waveform Start Address [9:2]					0x00
	15:8	RAM Profile7 Waveform Start Address [1:0]	Open				0x00
	7:0	Open	No-Dwell High	Open	Zero-Crossing	RAM Profile7 Mode Control [2:0]	0x00
RAM(0x16)	31:00:00	RAM Control word [31:0]					0x00

Register Bit Descriptions

The serial I/O port registers span an address range of 0 to 23 (0x00 to 0x16 in hexadecimal notation). This represents a total of 24 registers. However, two of these registers are unused yielding a total of 22 available registers. The unused registers are Register 5 and Register 6 (0x05 and 0x06, respectively). Unless otherwise stated, programmed bits are not transferred to their internal destinations until the assertion of the I/O_UPDATE pin or a profile change.

Control Function Register 1 (CFR1) - Address 0x00, four bytes are assigned to this register.

Bit (s)	Mnemonic	Description
31	RAM Enable	0 = disables RAM functionality (default). 1 = enables RAM functionality (required for both load/retrieve and playback operation).
30:29	RAM Playback Destination	See Table 4 for details; default is 00b.
28:24	Open	
23	Manual OSK External Control	Ineffective unless Bits<9:8> = 102. Manual OSK External Control 0 = OSK pin inoperative (default). 1 = OSK pin enabled for manual OSK control.
22	Inverse Sinc Filter Enable	0 = Inverse sinc filter bypassed (default). 1 = Inverse sinc filter active.
21	Open	
20:17	Internal Profile Control	Ineffective unless CFR1[31]= 1. These bits are effective without the need for an I/O update. See Table 6, for details. Default is 0000b
16	Select DDS Sine Output	0 = cosine output of the DDS is selected (default). 1 = sine output of the DDS is selected.
15	Load LRR @ I/O Update	Ineffective unless CFR2<19> = 1. 0 = normal operation of the digital ramp timer (default). 1 = digital ramp timer loaded any time I/O_UPDATE is asserted or a PROFILE[2:0] change occurs.
14	Auto clear Digital Ramp Accumulator	0 = normal operation of the DRG accumulator (default). 1 = the ramp accumulator is reset for one cycle of the DDS clock after which the accumulator automatically resumes normal operation. As long as this bit remains set, the ramp accumulator is momentarily reset each time an I/O update is asserted or a PROFILE[2:0] change occurs. This bit is synchronized with either an I/O update or a PROFILE[2:0] change and the next rising edge of SYNC_CLK.
13	Clear Digital Ramp	0 = normal operation of the DRG accumulator (default).

	Accumulator	1 = In I / O_ After the update is set or the profile is changed, the DDS phase accumulator is reset synchronously.
12	Autoclear Digital Ramp Accumulator	0 = normal operation of the DRG accumulator (default). 1=asynchronous, static reset of the DRG accumulator. The ramp accumulator remains reset as long as this bit remains set. This bit is synchronized with either an I/O update or a PROFILE[2:0] change and the next rising edge of SYNC_CLK.
11	Autoclear Phase Accumulator	0 = normal operation of the DDS phase accumulator (default). 1 = asynchronous, static reset of the DRG accumulator.
10	Load ARR @ I/O Update	Ineffective unless CFR1[9:8]= 11b. 0 = normal operation of the OSK amplitude ramp rate timer (default). 1 = OSK amplitude ramp rate timer reloaded anytime I/O_UPDATE is asserted or a PROFILE[2:0] change occurs.
9	OSK Enable	The Output Shift Keying Enable bit. 0 = OSK disabled (default). 1 = OSK enabled.
8	Select Auto OSK	Ineffective unless CFR1 [9] = 1. 0 = manual OSK enabled (default). 1 = automatic OSK enabled.
7	Digital Power-Down	This bit is effective without the need for an I/O update. 0 = clock signals to the digital core are active (default). 1 = clock signals to the digital core are disabled.
6	DAC Power-Down	0 = DAC clock signals and bias circuits are active (default). 1 = DAC clock signals and bias circuits are disabled.
5	REFCLK Input Power-Down	This bit is effective without the need for an I/O update. 0 = REFCLK input circuits and PLL are active (default). 1 = REFCLK input circuits and PLL are disabled.
4	Auxiliary DAC Power-Down	0 = auxiliary DAC clock signals and bias circuits are active (default). 1 = auxiliary DAC clock signals and bias circuits are disabled.
3	External Power-Down Control	0 = assertion of the EXTPWRDN pin effects full power-down (default). 1 = assertion of the EXTPWRDN pin effects fast recovery power-down.
2	Open	
1	SDIO Input Only	0 = configures the SDIO pin for bidirectional operation; 2-wire serial programming mode (default). 1 = configures the serial data I/O pin (SDIO) as an input only pin; 3-wire serial programming mode.
0	LSB First	0 = configures the serial I/O port for MSB-first format (default) 1 = configures the serial I/O port for LSB-first format.

Control Function Register 2 (CFR2)-Address 0x01, four bytes are assigned to this register.

Bit (s)	Mnemonic	Description
31:25	Open	
24	Enable Amplitude Scale from Single Tone profile	Ineffective if Bit CFR2[19]=1 or CFR1[31]=1 or CFR1<9> = 1. 0 = the amplitude scaler is bypassed and shut down for power conservation (default). 1 = the amplitude is scaled by the ASF from the active profile.
23	Internal I/O Update Active	This bit is effective without the need for an I/O update. 0 = serial I/O programming is synchronized with the external assertion of the I/O_UPDATE pin, which is configured as an input pin (default). 1 = serial I/O programming is synchronized with an internally generated I/O update signal (the internally generated signal appears at the I/O_UPDATE pin, which is configured as an output pin).
22	SYNC_CLK Enable	0 = The SYNC_CLK pin is disabled; static Logic 0 output. 1 = the SYNC_CLK pin generates a clock signal at ¼ f_{SYSCLK}; used for synchronization of the serial I/O port (default).
21:20	Digital Ramp Destination	See Table 3 for details. Default is 00b.
19	Digital Ramp Enable	0 = disables digital ramp generator functionality (default). 1 = enables digital ramp generator functionality.
18	Digital Ramp No-Dwell High	0 = disables no-dwell high functionality (default). 1 = enables no-dwell high functionality.
17	Digital Ramp No-Dwell Low	0 = disables no-dwell low functionality (default). 1 = enables no-dwell low functionality.
16	Read Effective FTW	0 = a serial I/O port read operation of the FTW register reports the contents of the FTW register (default). 1 = a serial I/O port read operation of the FTW register reports the actual 32-bit word appearing at the input to the DDS phase accumulator.
15:14	I/O Update Rate Control	Ineffective unless CFR2[23]= 1. Sets the prescale ratio of the divider that clocks the auto I/O update timer as follows: 00 = divide-by-1 (default). 01 = divide-by-2. 10 = divide-by-4. 11 = divide-by-8.
13:12	Open	
11	PDCLK Enable	0 = the PDCLK pin is disabled and forced to a static Logic 0 state; the internal clock signal continues to operate and provide timing to the data assembler.

		1 = the internal PDCLK signal appears at the PDCLK pin (default).
10	PDCLK Invert	0 = normal PDCLK polarity; Q-data associated with Logic 1, I-data with Logic 0 (default). 1 = inverted PDCLK polarity.
9	TxEnable Invert	0 = no inversion. 1 = inversion.
8	Open	
7	Matched Latency Enable	0 = simultaneous application of amplitude, phase, and frequency changes to the DDS arrive at the output in the order listed (default). 1 = simultaneous application of amplitude, phase, and frequency changes to the DDS arrive at the output simultaneously.
6	Data Assembler Hold Last Value	Ineffective unless CFR2[4]= 1. 0 = the data assembler of the parallel data port internally forces zeros on the data path and ignores the signals on the D<15:0> and F<1:0> pins while the TxENABLE pin is Logic 0 (default). This implies that the destination of the data at the parallel data port is amplitude when TxENABLE is Logic 0. 1 = the data assembler of the parallel data port internally forces the last value received on the D<15:0> and F<1:0> pins while the TxENABLE pin is Logic 1.
5	Sync Sample Error Mask	0 = enables the SYNC_SMP_ERR pin to indicate (active high) detection of a synchronization pulse sampling error. 1 = the SYNC_SMP_ERR pin is forced to a static Logic 0 condition (default).
4	Parallel Data Port Enable	0 = disables parallel data port modulation functionality (default). 1 = enables parallel data port modulation functionality.
3:0	FM Gain	Default is 0000b.

Control Function Register 3 (CFR3)-Address 0x02, four bytes are assigned to this register.

Bit (s)	Mnemonic	Description
31:30	Open	
29:28	DRVO	Controls the REFCLK_OUT pin, (see Table 7 for details); default is 00b.
27	Open	
26:24	VCO SEL	Selects frequency band of the REFCLK PLL VCO, (see Table 8 for details); default is 111b.
23:22	Open	
21:19	ICP	Selects the charge pump current in the REFCLK PLL (see Table 9 for details); default is 111b.
18:16	Open	
15	REFCLK Input Divider Bypass	0 = input divider is selected (default). 1 = input divider is bypassed.
14	REFCLK Input Divider Reset B	0 = input divider is reset. 1 = input divider operates normally (default).
13:11	Open	
10	PFD Reset	0= Normal operation (default). 1= Phase discriminator disabled.
9	Open	
8	PLL Enable	0 = REFCLK PLL bypassed (default). 1 = REFCLK PLL enabled.
7:1	N	This 7-bit number is divide modulus of the REFCLK PLL feedback divider; default is 0000000b.
0	Open	

Auxiliary DAC Control Register-Address 0x03, four bytes are assigned to this register**.**

Bit (s)	Mnemonic	Description
31:8	Open	
7:0	FSC	This 8-bit number controls the full-scale output current of the main DAC (see the Auxiliary DAC section); default is 0x7F.

I/O Update Rate Register-Address 0x04, four bytes are assigned to this register. This register is effective without the need for an I/O update.

Bit (s)	Mnemonic	Description
31:0	I/O Update Rate	Ineffective unless CFR2[23] = 1. This 32-bit number controls the automatic I/O update rate (see the Automatic I/O Update section for details). Default is 0xFFFFFFFF.

Frequency Tuning Word Register (FTW) - Address 0x07, 4 bytes are assigned to this register.

Bit(s)	Descriptor	Description
31:0	Frequency Tuning Word	32-bit frequency tuning word.

Phase offset word register - Address 0x08, 2 bytes are assigned to this register.

Bit(s)	Descriptor	Description
15:0	Phase offset word	16 bits Phase offset word

Amplitude Scale Factor (ASF) Register-Address 0x09, four bytes are assigned to this register.

Bit (s)	Mnemonic	Description
31:16	Amplitude Ramp Rate	16-bit amplitude ramp rate value. Effective only if CFR1<9:8> = 11b.
15:2	Amplitude Scale Factor	14-bit amplitude scale factor.
1:0	Amplitude Step Size	Effective only if CFR1[9:8]=11b.

Multichip Sync Register-Address 0x0A, four bytes are assigned to this register.

Bit (s)	Mnemonic	Description
31:28	Sync Validation Delay	Default is 0000b. This 4-bit number sets the timing skew (in ~150 ps increments) between SYSCLK and the delayed sync-in signal for the synchronization validation block in the synchronization receiver.
27	Sync Receiver Enable	0 = synchronization clock receiver disabled (default). 1 = synchronization clock receiver enabled.
26	Sync Generator Enable	0: synchronization clock generator disabled (default). 1: synchronization clock generator enabled.
25	Sync Generator Polarity	0: synchronization clock generator coincident with the rising edge of the system clock (default). 1: synchronization clock generator coincident with the falling edge of the system clock.
24	Open	
23:18	Sync State Preset Value	This 6-bit number is the state that the internal clock generator assumes when it receives a sync pulse. Default is 000000b.
17:16	Open	
15:11	Output Sync Generator Delay	This 5-bit number sets the output delay (in ~150ps increments) of the sync generator. Default is 00000b.
10:8	Open	
7:3	Input Sync Receiver Delay	This 5-bit number sets the input delay (in ~150 ps increments) of the sync receiver. Default is 00000b.
2:0	Open	

Digital Ramp Limit Register - Address 0x0B, 8 bytes are assigned to this register. This register is only effective if CFR2[19] = 1.

Bit (s)	Mnemonic	Description
63:32	Digital Ramp Upper Limit	32-bit digital ramp upper limit value.
31:0	Digital Ramp Lower Limit	32-bit digital ramp lower limit value.

Digital Ramp Step Size Register - Address 0x0C, 8 bytes are assigned to this register. This register is only effective if CFR2[19] = 1.

Bit (s)	Mnemonic	Description
63:32	Digital Ramp Decrement Step Size	32-bit digital ramp decrement step size value.
31:0	Digital Ramp Increment Step Size	32-bit digital ramp increment step size value.

Digital Ramp Rate Register - Address 0x0D, 4 bytes are assigned to this register. This register is only effective if CFR2[19] = 1.

Bit (s)	Mnemonic	Description
31:16	Digital Ramp Negative Slope Rate	16-bit digital ramp negative slope value that defines the time interval between decrement values.
15:0	Digital Ramp Positive Slope Rate	16-bit digital ramp positive slope value that defines the time interval between increment values.

Profile Registers

There are eight consecutive serial I/O addresses (Address 0x0E to Address 0x015) dedicated to device profiles. All eight profile registers are either single tone profiles or RAM profiles. RAM profiles are in effect when CFR1<31> = 1. Single tone profiles are in effect when CFR1<31> = 0, CFR2<19> = 0, and CFR2<4> = 0. In normal operation, the active profile register is selected using the external PROFILE<2:0> pins. However, in the specific case when CFR1<31> = 1 and CFR1<20:17> ≠ 00002, the active profile is selected automatically (see the RAM Ramp Up Internal Profile Control Mode section).

Profile 0 to Profile 7—Single Tone Register - Address 0x0E to Address 0x15, 8 bytes are assigned to this register.

Bit (s)	Mnemonic	Description
63:56	Open	
55:40	Address Step Rate	16-bit address step rate value.
39:30	Waveform End Address	10-bit waveform end address.
29:24	Open	
23:14	Waveform Start Address	10-bit waveform start address.
13:6	Open	
5	No-Dwell High	Effective only when the RAM mode is in ramp up. 0 = when the RAM state machine reaches the end address, it halts. 1 = when the RAM state machines reaches the end address, it jumps to the start address and halts.
4	Open	
3	Zero-Crossing	Effective only when in RAM mode, direct switch. 0 = zero-crossing function disabled. 1 = zero-crossing function enabled.
2:0	RAM Mode Control	See Table 5 for details.

RAM Register - Address 0x16, 4 bytes are assigned to this register.

Bit (s)	Mnemonic	Description
31:0	RAM word	The start and end addresses in the RAM profile 0 to RAM profile 7 control registers define the 32-bit words written to the ram register(1 to 1024).

Table 3. Purpose of Digital Ramp

Purpose bit of Digital Ramp CFR2[21:20]	DDS Signal control parameters	DDS Parameter Bits
00	Frequency	31:0
01	Phase	31:16
1x	Range	31:18

Table 4. RAM Playback purpose

RAM Playback purpose CFR1[30:29]	DDS signal control parameters	DDS Parameter Bits
00	Frequency	31:0
01	Phase	31:16
10	Range	31:18
11	Polarity (Phase and Range)	31:16（Phase）
		15:2（Range）

Table 5. RAM operation mode

RAM Profile Control word	RAM operation mode
000、101、110、111	Direct conversion mode
001	Up ramp mode
010	Bidirectional ramp mode
011	Continuous bidirectional ramp mode
100	Continuous cycle mode

Table 6. RAM internal profile control mode

Internal profile control bit CFR1[20:17]	Waveform type	Internal profile control description
0000		Internal profile control disabled.
0001	Burst	Execute profile 0, profile 1, and abort
0010	Burst	Execute profile 0, profile 2, and abort
0011	Burst	Execute profile 0, profile 3, and abort
0100	Burst	Execute profile 0, profile 4, and abort
0101	Burst	Execute profile 0, profile 5, and abort
0110	Burst	Execute profile 0, profile 6, and abort
0111	Burst	Execute profile 0, profile 7, and abort
1000	continuity	Execute profile 0, profile 1, continuous
1001	continuity	Execute profile 0, profile 2, continuous
1010	continuity	Execute profile 0, profile 3, continuous
1011	continuity	Execute profile 0, profile 4, continuous
1100	continuity	Execute profile 0, profile 5, continuous
1101	continuity	Execute profile 0, profile 6, continuous
1110	continuity	Execute profile 0, profile 7, continuous
1111		Invalid

Table 7. REFCLK_OUT Buffer Control

DRV0 Bit (CFR3[29:28])	REFCLK_OUT Buffer
00	Disabled (Three states)
01	Low output current
10	Medium output current
11	High output current

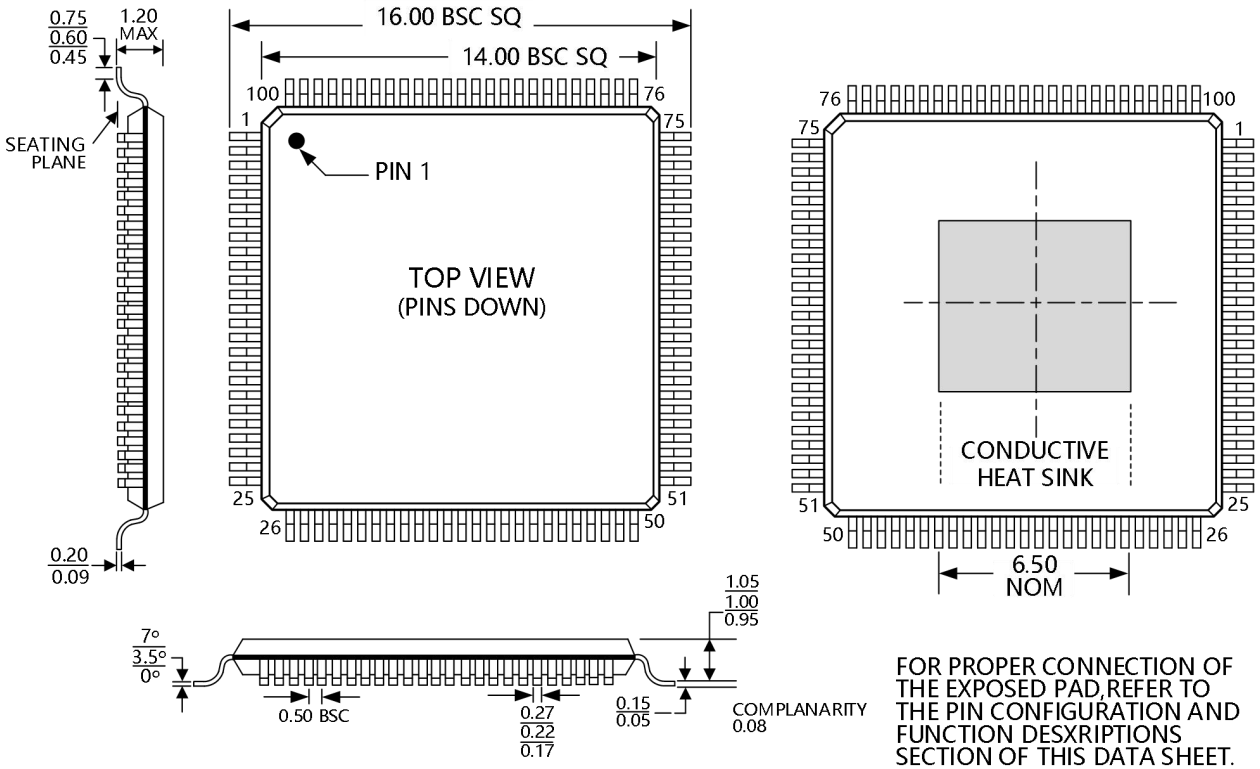
Table 8. VCO Range Bit Settings

VCO SEL Bits (CFR3[26:24])	VCO Range
000	VCO0
001	VCO1
010	VCO2
011	VCO3
100	VCO4
101	VCO5
110	PLL Bypassed
111	PLL Bypassed

Table 9. PLL Charge Pump Current

ICP set up bits (CFR3[21:19])	Charge Pump Current, I_{CP} (μA)
000	212
001	237
010	262
011	287
100	312
101	337
110	363
111	387

Outline Dimensions



COMPLIANT TO JEDEC STANDARDS MS-026-AED-HDT

Unit: millimeter（mm）

100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP] (SV-100-4) Dimensions in mm

YMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.60
A1	0.05	-	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.19	-	0.27
b1	0.18	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.13	0.14

D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	-	15.35
e	0.50 BSC		

L/F Carrier size（mil）	D2	E2
155×186	4352 REF	3.74 REF

Package/Ordering Information

PRODUCT TYPE	OPERATING TEMPERTURE	PACKAGE	PAKEAGE MARKING	NUMBER OF PACKAGES
CBM99D10BQ	-45℃ ~ 85℃	TQFP-100	CBM99D10BQ	Tray，90