ALPHA & OMEGA SEMICONDUCTOR

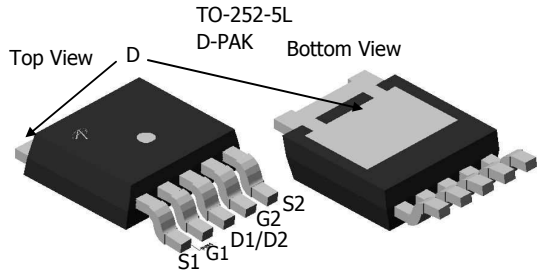
AOD604
Complementary Enhancement Mode Field Effect Transistor

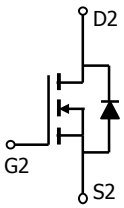
General Description
The AOD604 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

-RoHS Compliant
-Halogen Free*

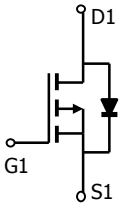
Features
n-channel	p-channel
V_{DS} (V) = 40V	-40V
I_D = 8A (V_{GS}=10V)	-8A (V_{GS} = -10V)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 33 mΩ (V_{GS}=10V)	< 50 mΩ (V_{GS} = -10V)
< 47 mΩ (V_{GS}=4.5V)	< 70 mΩ (V_{GS} = -4.5V)

100% UIS Tested!





n-channel



p-channel

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage		V_{DS}	40	-40	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	8	-8	A
	T_C=100°C		6.3	-6.3	
Pulsed Drain Current [C]		I_{DM}	30	-30	
Avalanche Current [C]		I_{AR}	8	-8	A
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	20	30	mJ
Power Dissipation [B]	T_C=25°C	P_D	20	30	W
	T_C=100°C		10	15	
Power Dissipation [A]	T_A=25°C	P_{DSM}	1.6	1.7	W
	T_A=70°C		1	1.1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	-55 to 175	°C

Thermal Characteristics: n-channel and p-channel

Parameter		Symbol	Device	Typ	Max	
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	n-ch	25	30	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		n-ch	66	80	°C/W
Maximum Junction-to-Case [B]	Steady-State	$R_{\theta JC}$	n-ch	7	7.5	°C/W
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	p-ch	17	25	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		p-ch	60	75	°C/W
Maximum Junction-to-Case [B]	Steady-State	$R_{\theta JC}$	p-ch	4	5	°C/W

N-Channel MOSFET Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=10mA, V_{GS}=0V	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=32V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250µA	1	2.3	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=8A		25	33	mΩ
		T_J=125°C		39	52	
		V_{GS}=4.5V, I_D=6A		34	47	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=8A		25		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				8	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=20V, f=1MHz		404		pF
C_{oss}	Output Capacitance			95		pF
C_{rss}	Reverse Transfer Capacitance			37		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		2.7		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=20V, I_D=8A		9.2		nC
Q_g(4.5V)	Total Gate Charge			4.5		nC
Q_{gs}	Gate Source Charge			1.6		nC
Q_{gd}	Gate Drain Charge			2.6		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=20V, R_L=2.5Ω, R_{GEN}=3Ω		3.5		ns
t_r	Turn-On Rise Time			6		ns
$t_{D(off)}$	Turn-Off DelayTime			13.2		ns
t_f	Turn-Off Fall Time			3.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=8A, dI/dt=100A/µs		22.9		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=8A, dI/dt=100A/µs		18.3		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev3: Sep. 2008

N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

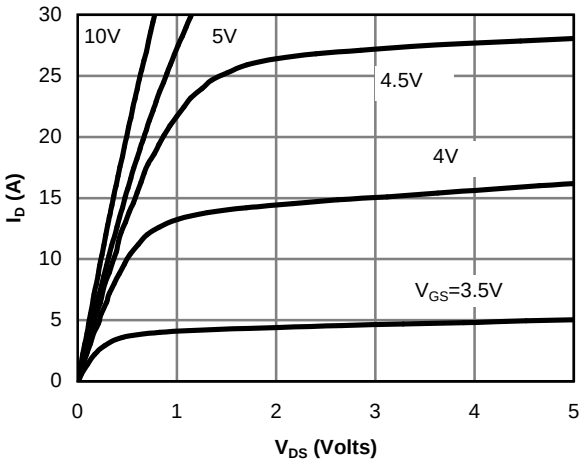


Fig 1: On-Region Characteristics

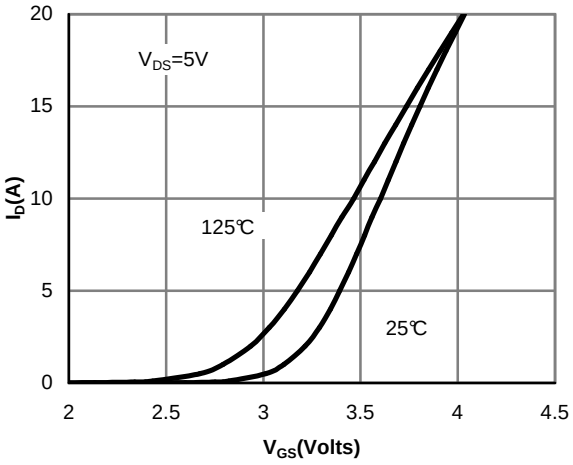


Figure 2: Transfer Characteristics

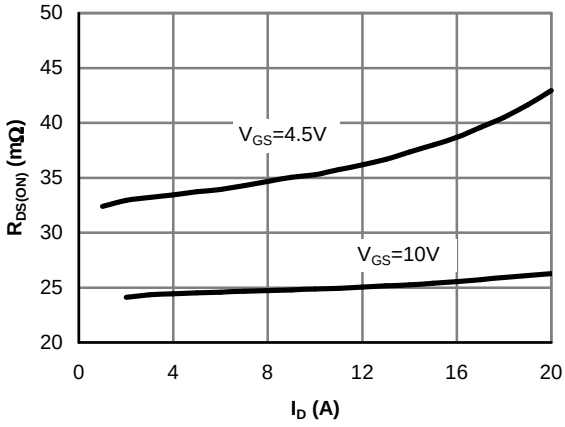


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

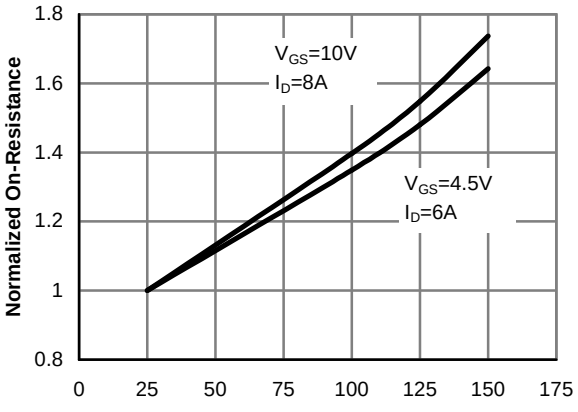


Figure 4: On-Resistance vs. Junction Temperature

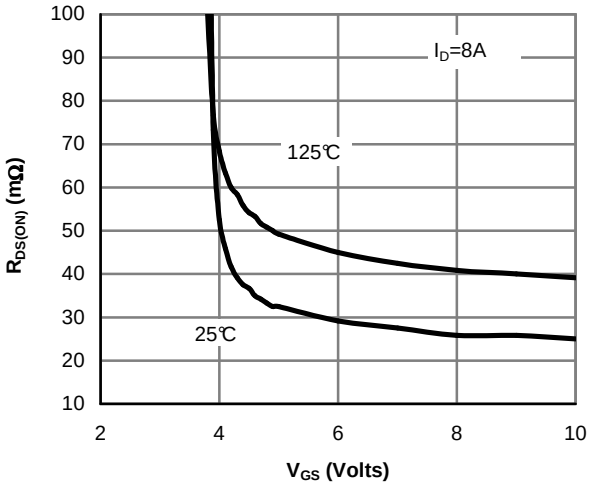


Figure 5: On-Resistance vs. Gate-Source Voltage

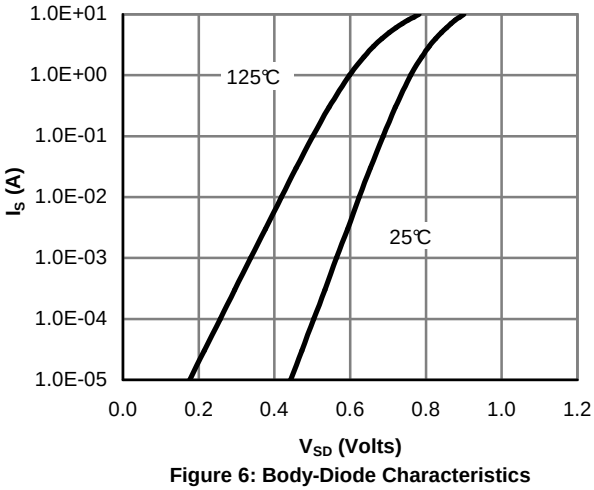


Figure 6: Body-Diode Characteristics

N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

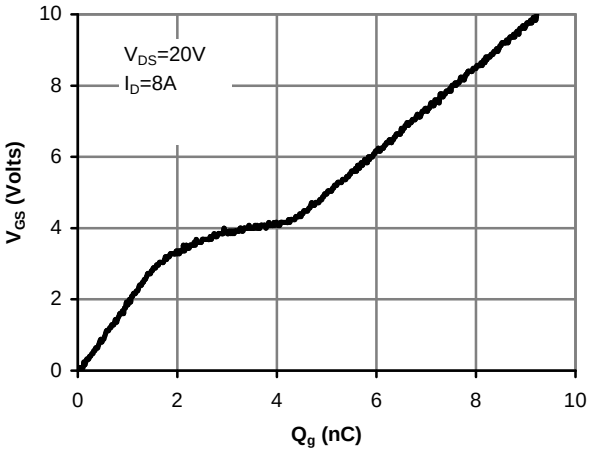


Figure 7: Gate-Charge Characteristics

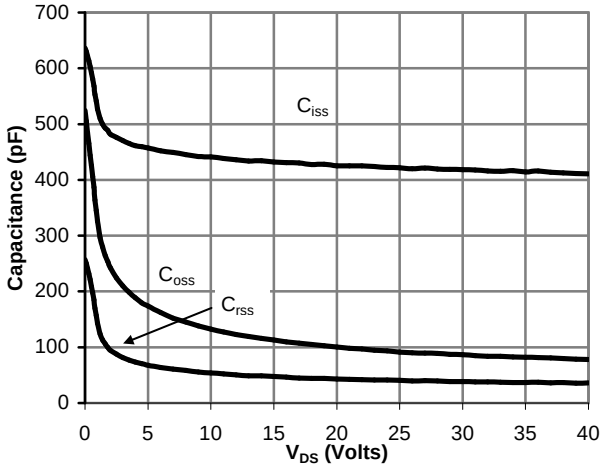


Figure 8: Capacitance Characteristics

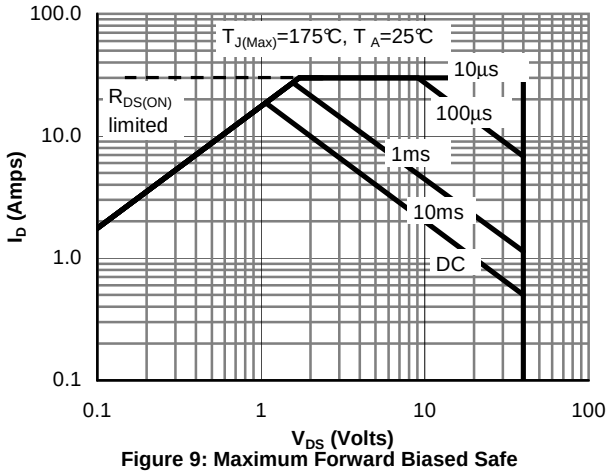


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

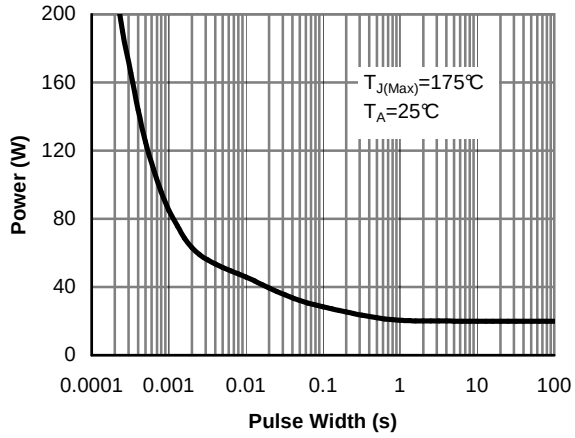


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

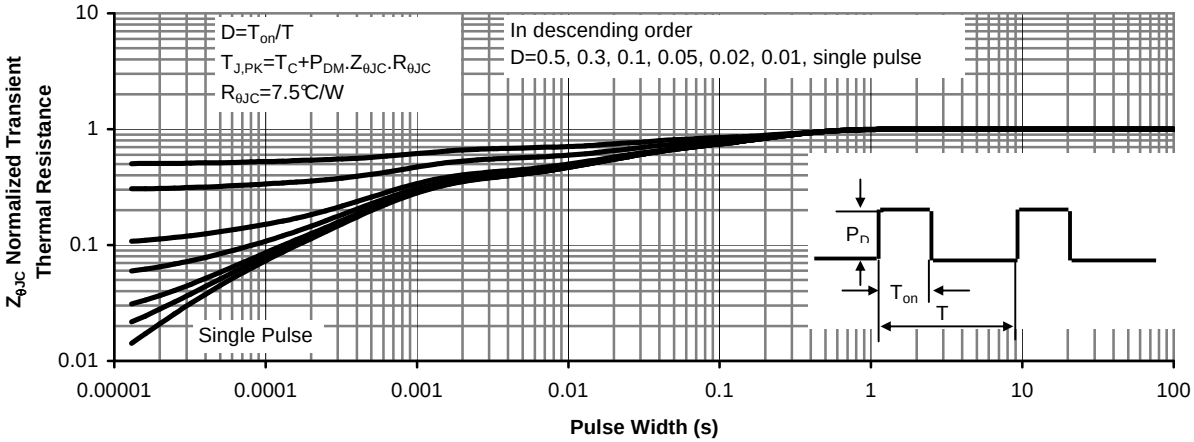


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

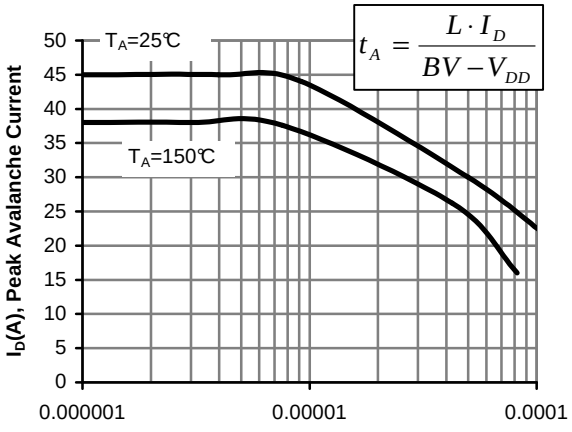


Figure 12: Single Pulse Avalanche capability

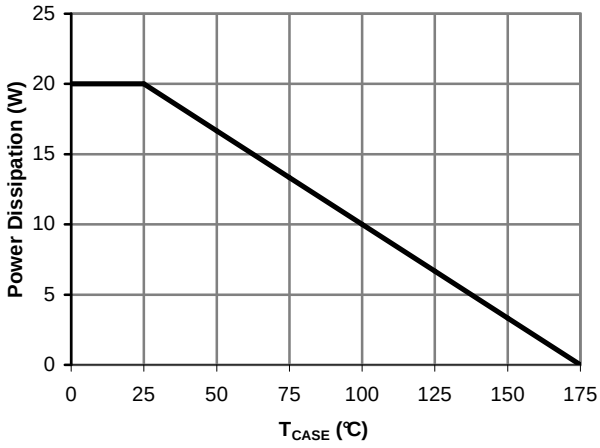


Figure 13: Power De-rating (Note B)

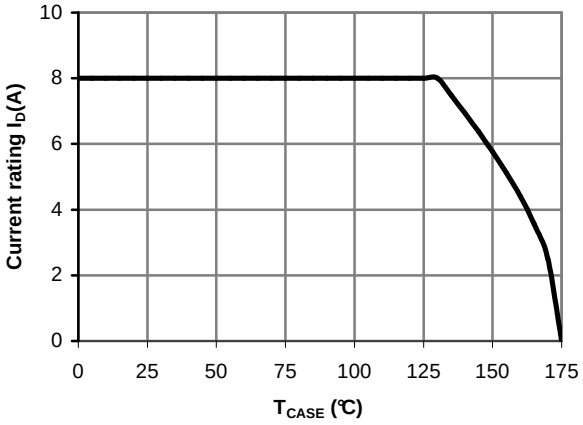


Figure 14: Current De-rating (Note B)

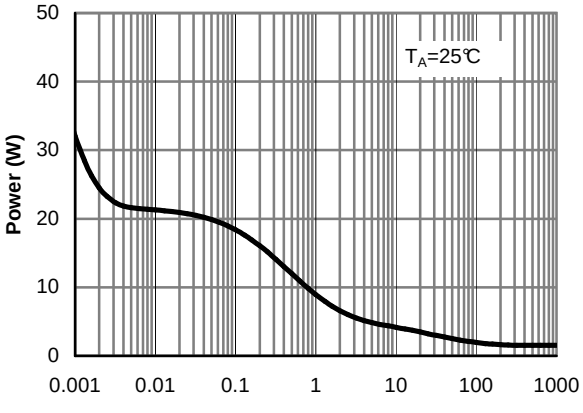


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

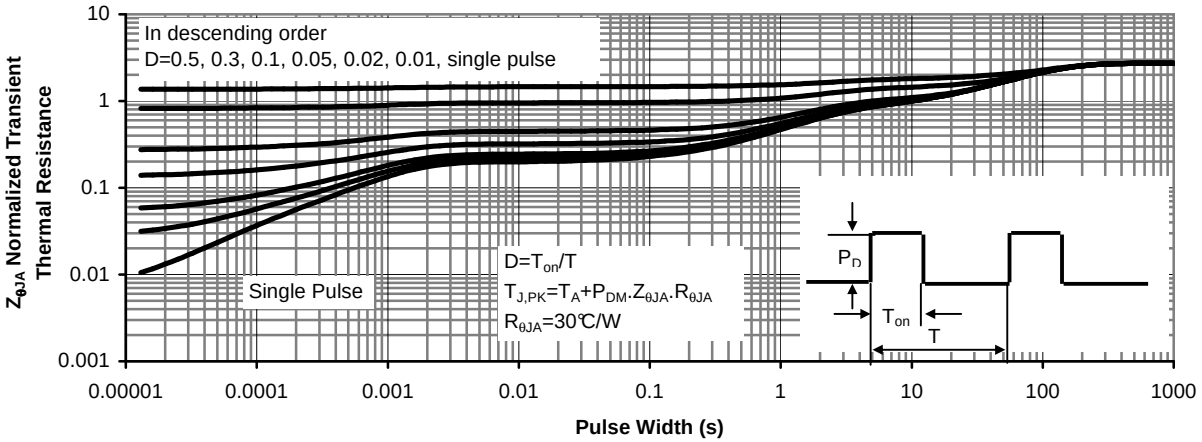


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

P-Channel MOSFET Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-10mA, V_{GS}=0V	-40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-32V, V_{GS}=0V			-1	µA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-1	-1.8	-3	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	-30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-8A		41	50	mΩ
		T_J=125°C		62		
		V_{GS}=-4.5V, I_D=-4A		57	70	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-8A		16		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.75	-1	V
I_S	Maximum Body-Diode Continuous Current				-8	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-20V, f=1MHz		657		pF
C_{oss}	Output Capacitance			143		pF
C_{rss}	Reverse Transfer Capacitance			63		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		6.5		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge (10V)	V_{GS}=-10V, V_{DS}=-20V, I_D=-8A		14.1		nC
Q_g(4.5V)	Total Gate Charge (4.5V)			7		nC
Q_{gs}	Gate Source Charge			2.2		nC
Q_{gd}	Gate Drain Charge			4.1		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-20V, R_L=2.5Ω, R_{GEN}=3Ω		8		ns
t_r	Turn-On Rise Time			12.2		ns
$t_{D(off)}$	Turn-Off DelayTime			24		ns
t_f	Turn-Off Fall Time			12.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-8A, dI/dt=100A/µs		23.2		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-8A, dI/dt=100A/µs		18.2		nC

A: The value of R qJA is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation PDSM is based on R qJA and the maximum allowed junction temperature of 150°C. The va lue in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the P CB allows it.
B. The power dissipation PD is based on TJ(MAX)=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C: Repetitive rating, pulse width limited by junction temperature TJ(MAX)=175°C.
D. The R qJA is the sum of the thermal impedence from junction to case R qJC and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300 ms pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of TJ(MAX)=175°C.
G. The maximum current rating is limited by bond-wires.
H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C. The SOA curve provides a single pulse rating.
*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).
Rev3: Sep. 2008

P-Channel MOSFET Electrical Characteristics (T_J=25°C unless otherwise noted)

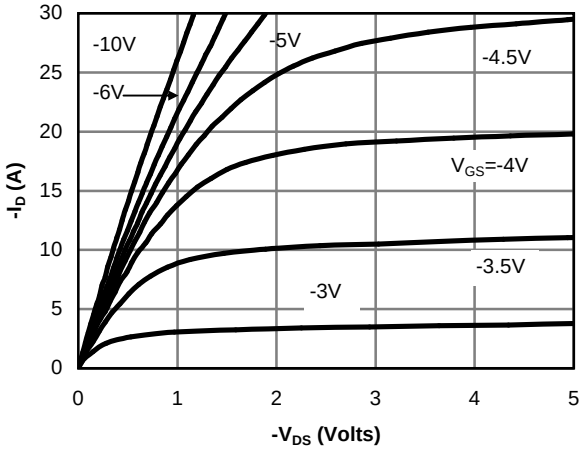


Fig 1: On-Region Characteristics

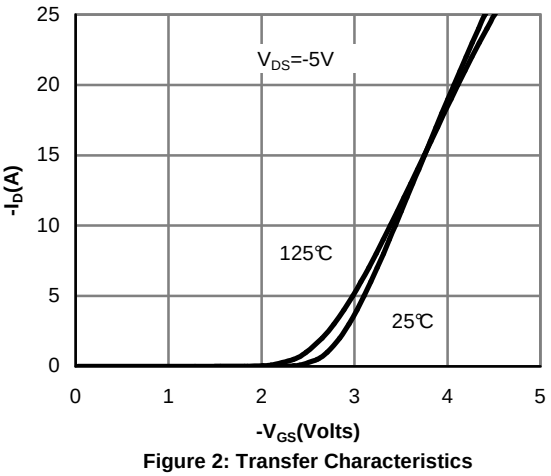


Figure 2: Transfer Characteristics

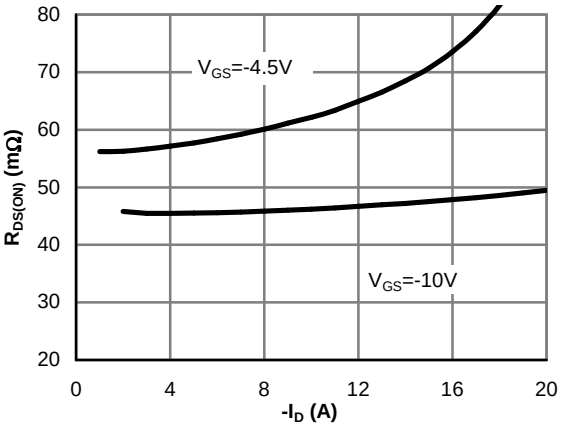


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

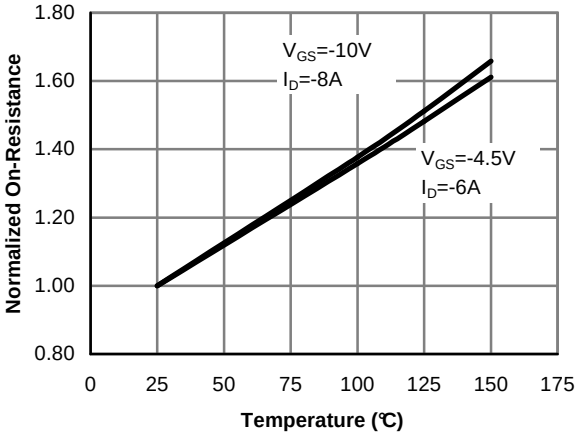


Figure 4: On-Resistance vs. Junction Temperature

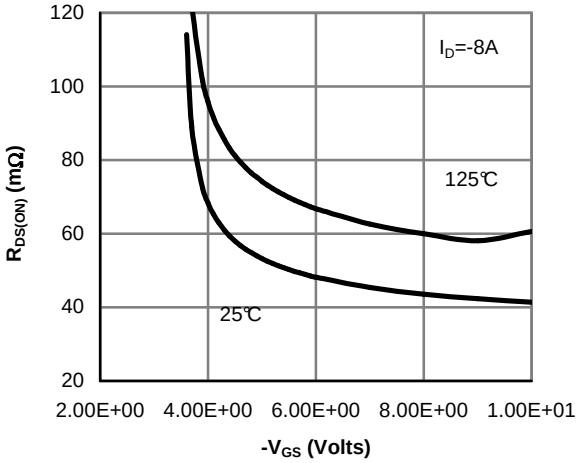


Figure 5: On-Resistance vs. Gate-Source Voltage

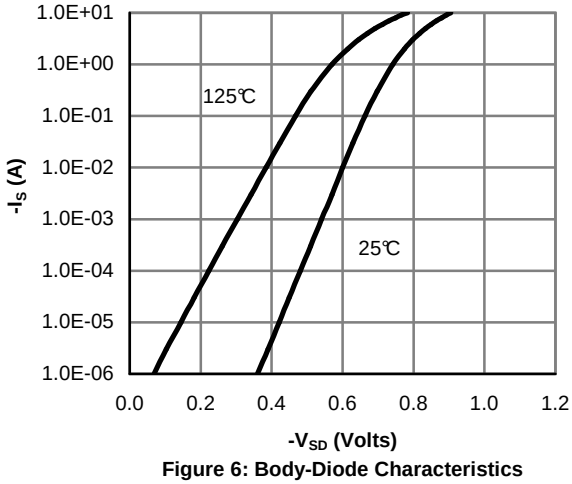


Figure 6: Body-Diode Characteristics

P-Channel MOSFET Electrical Characteristics (T_J=25°C unless otherwise noted)

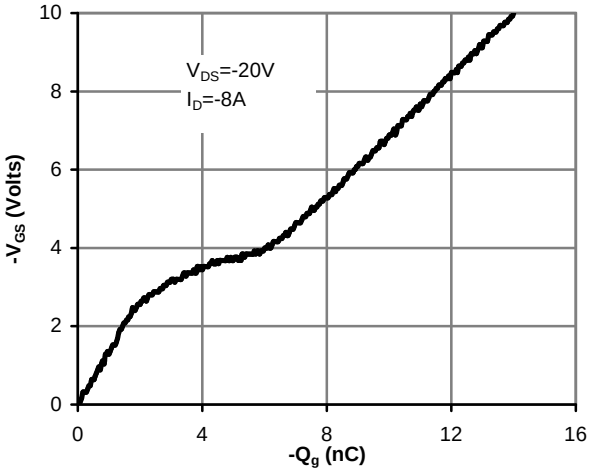


Figure 7: Gate-Charge Characteristics

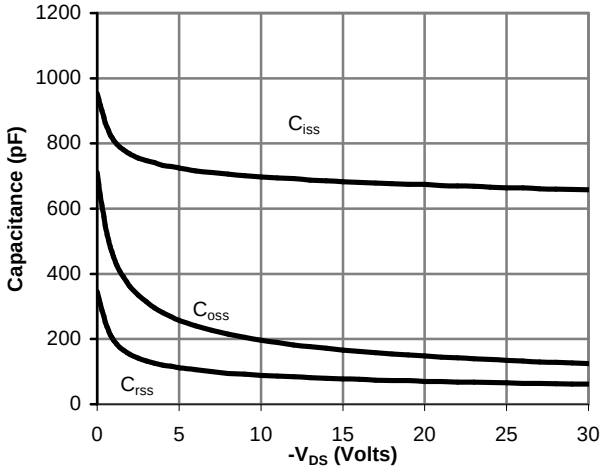


Figure 8: Capacitance Characteristics

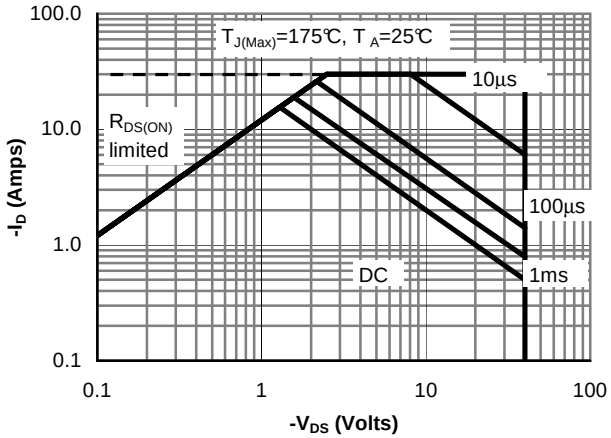


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

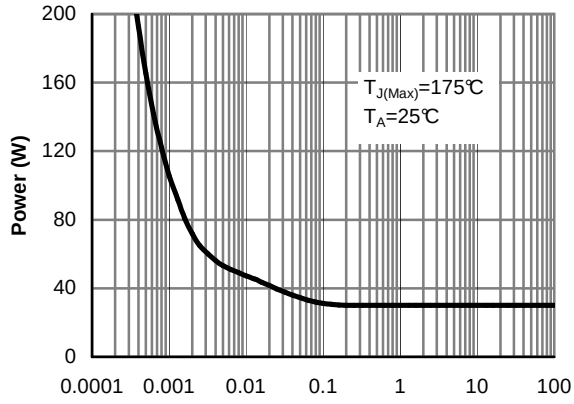


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

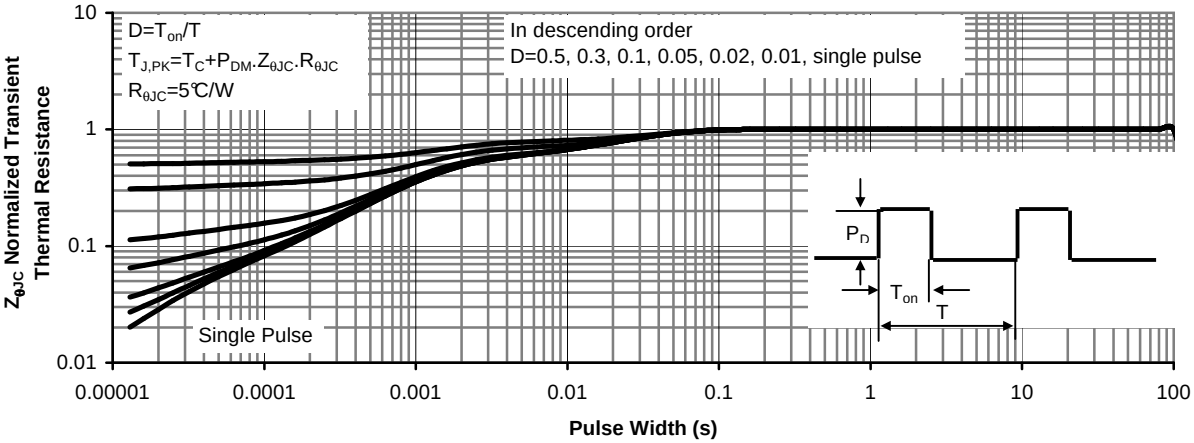


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

P-Channel MOSFET Electrical Characteristics (T_J=25°C unless otherwise noted)

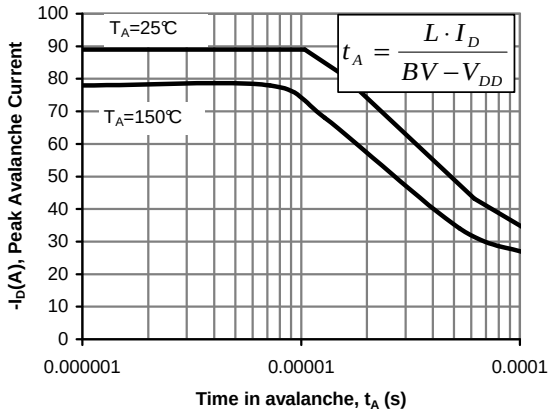


Figure 12: Single Pulse Avalanche capability

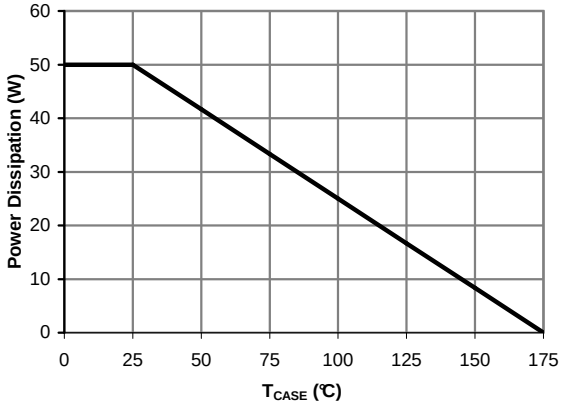


Figure 13: Power De-rating (Note B)

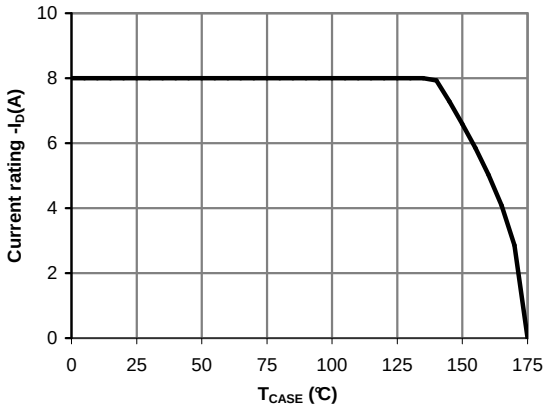


Figure 14: Current De-rating (Note B)

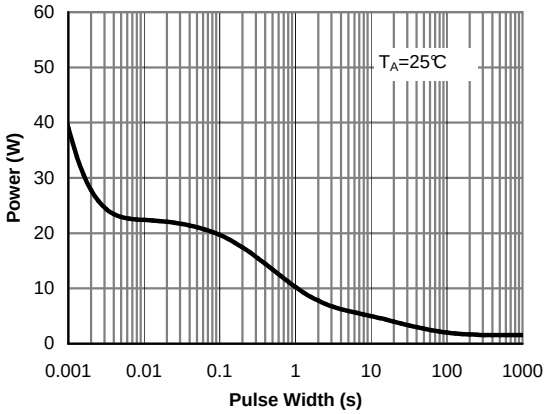


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

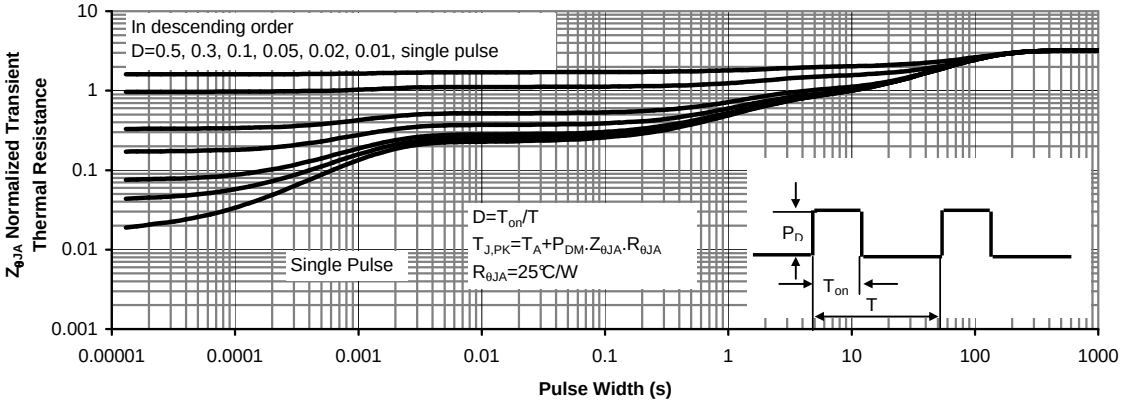
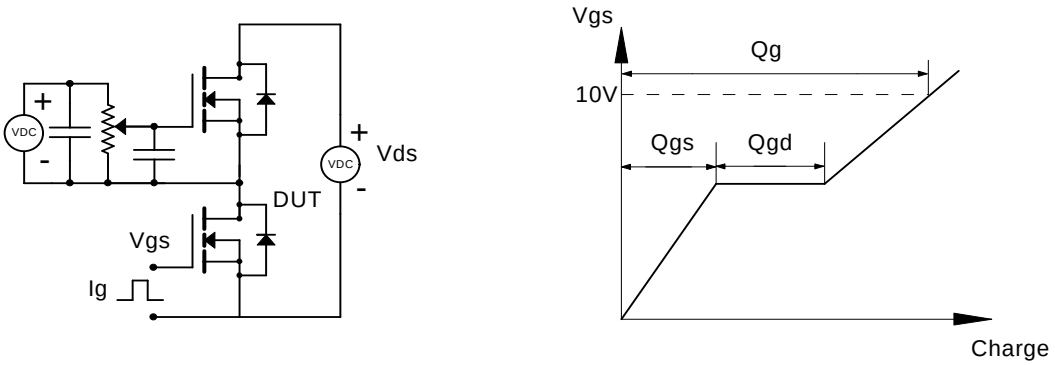
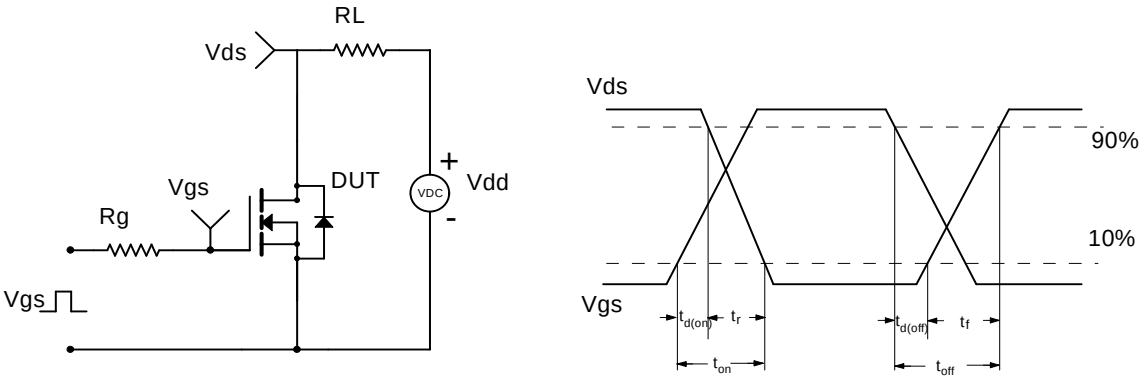


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

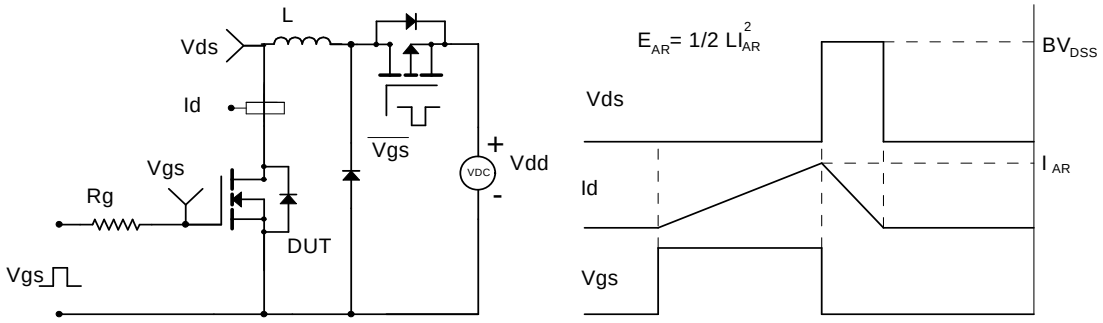
Gate Charge Test Circuit & Waveform



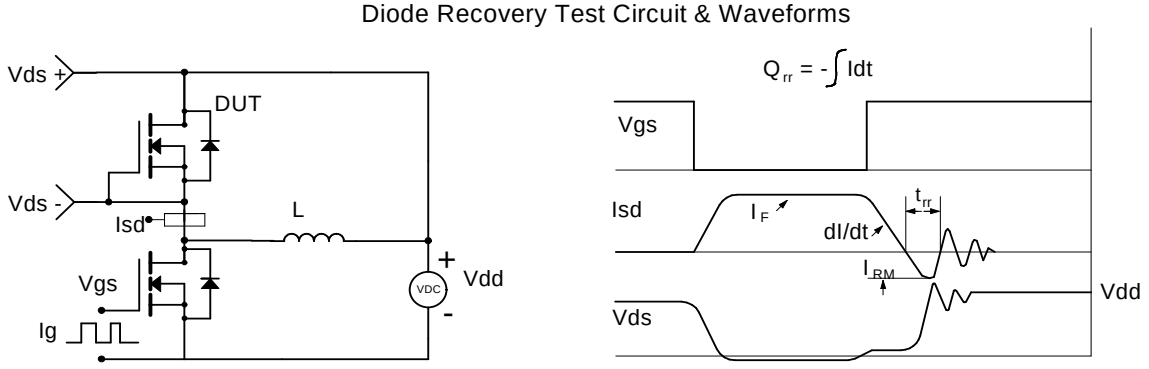
Resistive Switching Test Circuit & Waveforms



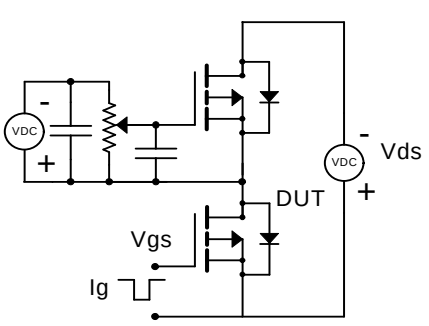
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

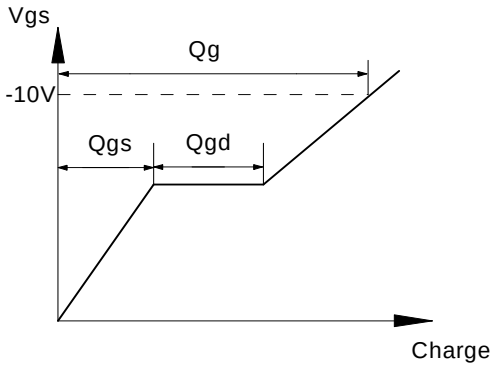


Diode Recovery Test Circuit & Waveforms

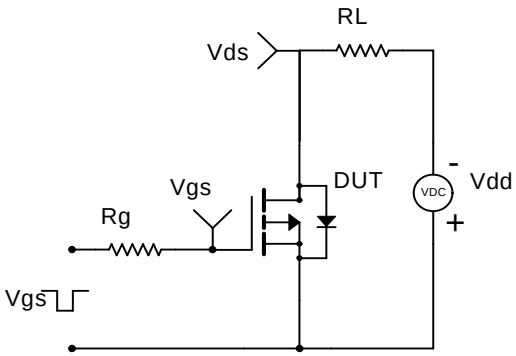


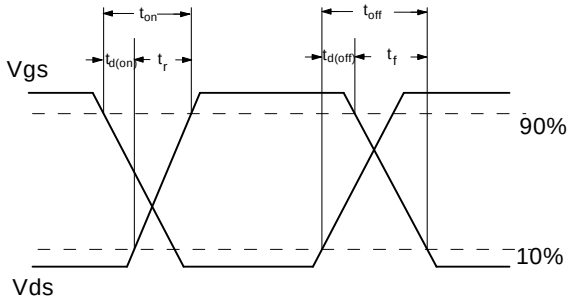
Gate Charge Test Circuit & Waveform



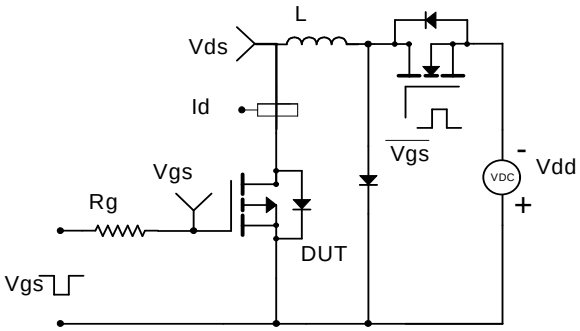


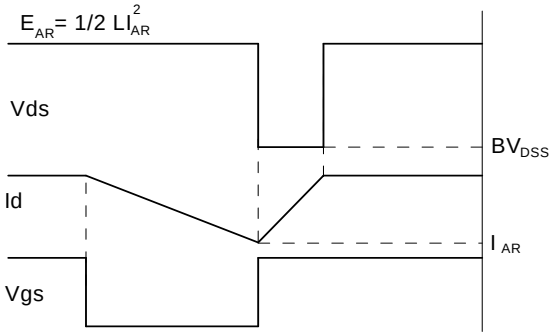
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms