

CM1213A

1, 2 and 4-Channel Low Capacitance ESD Protection Arrays

Product Description

The CM1213A family of diode arrays has been designed to provide ESD protection for electronic components or subsystems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail. A Zener diode is embedded between V_P and V_N , offering two advantages. First, it protects the V_{CC} rail against ESD strikes, and second, it eliminates the need for a bypass capacitor that would otherwise be needed for absorbing positive ESD strikes to ground. The CM1213A will protect against ESD pulses up to 8 kV per the IEC 61000-4-2 standard.

These devices are particularly well-suited for protecting systems using high-speed ports such as USB 2.0, IEEE1394 (Firewire[®], iLink[™]), Serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

Features

- One, Two, and Four Channels of ESD Protection
Note: For 6 and 8-channel Devices, See the CM1213 Datasheet
- Provides ESD Protection to IEC61000-4-2 Level 4
 - ± 8 kV Contact Discharge
- Low Channel Input Capacitance of 0.85 pF Typical
- Minimal Capacitance Change with Temperature and Voltage
- Channel Input Capacitance Matching of 0.02 pF Typical is Ideal for Differential Signals
- Zener Diode Protects Supply Rail and Eliminates the Need for External By-pass Capacitors
- Each I/O Pin Can Withstand Over 1000 ESD Strikes*
- These Devices are Pb-Free and are RoHS Compliant

Applications

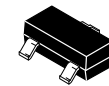
- USB2.0 Ports at 480 Mbps in Desktop PCs, Notebooks and Peripherals
- IEEE1394 Firewire[®] Ports at 400 Mbps/800 Mbps
- DVI Ports, HDMI Ports in Notebooks, Set Top Boxes, Digital TVs, LCD Displays
- Serial ATA Ports in Desktop PCs and Hard Disk Drives
- PCI Express Ports
- General Purpose High-Speed Data Line ESD Protection

*Standard test condition is IEC61000-4-2 level 4 test circuit with each pin subjected to ± 8 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

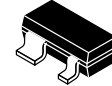


ON Semiconductor[®]

<http://onsemi.com>



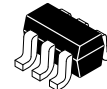
SOT23-3
SO SUFFIX
CASE 318



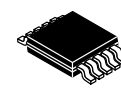
SOT143
SR SUFFIX
CASE 527AF



SC-74
SO SUFFIX
CASE 318F

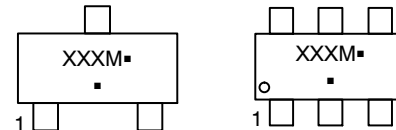


SC70-6
S7 SUFFIX
CASE 419AD



MSOP-10
MR SUFFIX
CASE 846AE

MARKING DIAGRAM



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

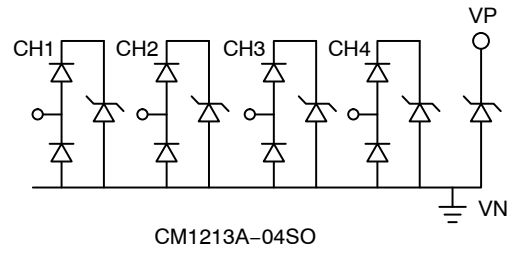
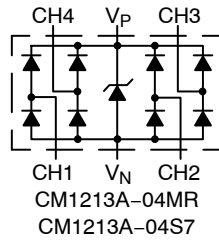
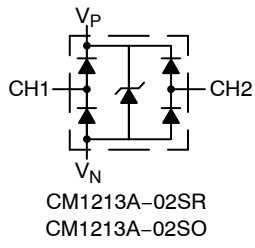
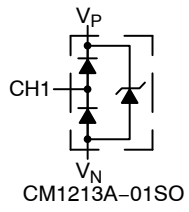
ORDERING INFORMATION

| Device | Package | Shipping [†] |
|--------------|--------------------|-----------------------|
| CM1213A-01SO | SOT23-3 (Pb-Free) | 3000/Tape & Reel |
| CM1213A-02SR | SOT143-4 (Pb-Free) | 3000/Tape & Reel |
| CM1213A-02SO | SC-74 (Pb-Free) | 3000/Tape & Reel |
| CM1213A-04SO | SC-74 (Pb-Free) | 3000/Tape & Reel |
| CM1213A-04S7 | SC70-6 (Pb-Free) | 3000/Tape & Reel |
| CM1213A-04MR | MSOP-10 (Pb-Free) | 4000/Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

CM1213A

BLOCK DIAGRAM



CM1213A

Table 1. PIN DESCRIPTIONS

| 1-Channel, 3-Lead SOT23-3 Package (CM1213A-01SO) | | | |
|--|----------------|------|------------------------------|
| Pin | Name | Type | Description |
| 1 | CH1 | I/O | ESD Channel |
| 2 | V _P | PWR | Positive voltage supply rail |
| 3 | V _N | GND | Negative voltage supply rail |

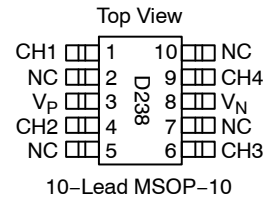
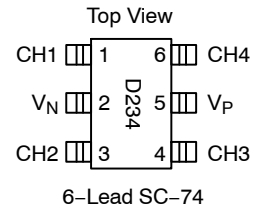
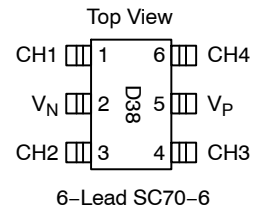
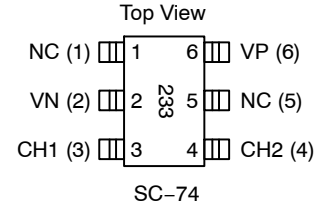
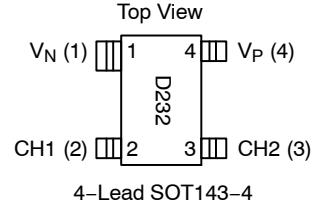
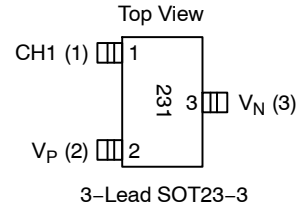
| 2-Channel, 4-Lead SOT143-4 Package (CM1213A-02SR) | | | |
|---|----------------|------|------------------------------|
| Pin | Name | Type | Description |
| 1 | V _N | GND | Negative voltage supply rail |
| 2 | CH1 | I/O | ESD Channel |
| 3 | CH2 | I/O | ESD Channel |
| 4 | V _P | PWR | Positive voltage supply rail |

| 2-Channel, SC-74 Package (CM1213A-02SO) | | | |
|---|----------------|------|------------------------------|
| Pin | Name | Type | Description |
| 1 | NC | - | No Connect |
| 2 | V _N | GND | Negative voltage supply rail |
| 3 | CH1 | I/O | ESD Channel |
| 4 | CH2 | I/O | ESD Channel |
| 5 | NC | - | No Connect |
| 6 | V _P | PWR | Positive voltage supply rail |

| 4-Channel, 6-Lead SC-74 (CM1213A-04SO) and SC70-6 (CM1213A-04S7) | | | |
|--|----------------|------|------------------------------|
| Pin | Name | Type | Description |
| 1 | CH1 | I/O | ESD Channel |
| 2 | V _N | GND | Negative voltage supply rail |
| 3 | CH2 | I/O | ESD Channel |
| 4 | CH3 | I/O | ESD Channel |
| 5 | V _P | PWR | Positive voltage supply rail |
| 6 | CH4 | I/O | ESD Channel |

| 4-Channel, 10-Lead MSOP-10 Package (CM1213A04MR) | | | |
|--|----------------|------|------------------------------|
| Pin | Name | Type | Description |
| 1 | CH1 | I/O | ESD Channel |
| 2 | NC | - | No Connect |
| 3 | V _P | PWR | Positive voltage supply rail |
| 4 | CH2 | I/O | ESD Channel |
| 5 | NC | - | No Connect |
| 6 | CH3 | I/O | ESD Channel |
| 7 | NC | - | No Connect |
| 8 | V _N | GND | Negative voltage supply rail |
| 9 | CH4 | I/O | ESD Channel |
| 10 | NC | - | No Connect |

PACKAGE / PINOUT DIAGRAMS



CM1213A

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

| Parameter | Rating | Units |
|--|--------------------------------|-------|
| Operating Supply Voltage ($V_P - V_N$) | 6.0 | V |
| Operating Temperature Range | -40 to +85 | °C |
| Storage Temperature Range | -65 to +150 | °C |
| DC Voltage at any channel input | $(V_N - 0.5)$ to $(V_P + 0.5)$ | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

| Parameter | Rating | Units |
|--|------------|-------|
| Operating Temperature Range | -40 to +85 | °C |
| Package Power Rating SOT23-3, SOT143-4, SC-74, and SC70-6 Packages MSOP-10 Package | 225 400 | mW |

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------|--|--|--------------|--------------|--------------|----------|
| V_P | Operating Supply Voltage ($V_P - V_N$) | | | 3.3 | 5.5 | V |
| I_P | Operating Supply Current | $(V_P - V_N) = 3.3$ V | | | 8.0 | μ A |
| V_F | Diode Forward Voltage Top Diode Bottom Diode | $I_F = 8$ mA; $T_A = 25^\circ$ C | 0.60 0.60 | 0.80 0.80 | 0.95 0.95 | V |
| I_{LEAK} | Channel Leakage Current | $T_A = 25^\circ$ C; $V_P = 5$ V, $V_N = 0$ V | | 0.1 | 1.0 | μ A |
| C_{IN} | Channel Input Capacitance | At 1 MHz, $V_P = 3.3$ V, $V_N = 0$ V, $V_{IN} = 1.65$ V (Note 2) | | 0.85 | 1.2 | pF |
| ΔC_{IN} | Channel Input Capacitance Matching | At 1 MHz, $V_P = 3.3$ V, $V_N = 0$ V, $V_{IN} = 1.65$ V (Note 2) | | 0.02 | | pF |
| V_{ESD} | ESD Protection – Peak Discharge Voltage at any channel input, in system Contact discharge per IEC 61000-4-2 standard | $T_A = 25^\circ$ C (Notes 2 and 3) | 8 | | | kV |
| V_{CL} | Channel Clamp Voltage Positive Transients Negative Transients | $T_A = 25^\circ$ C, $I_{PP} = 1$ A, $t_P = 8/20$ μ S (Note 2) | | +10 -1.7 | | V |
| R_{DYN} | Dynamic Resistance Positive Transients Negative Transients | $I_{PP} = 1$ A, $t_P = 8/20$ μ S Any I/O pin to Ground (Note 2) | | 0.9 0.5 | | Ω |

1. All parameters specified at $T_A = -40^\circ$ C to $+85^\circ$ C unless otherwise noted.
2. Standard IEC 61000-4-2 with $C_{Discharge} = 150$ pF, $R_{Discharge} = 330$ Ω , $V_P = 3.3$ V, V_N grounded.
3. These measurements performed with no external capacitor on V_P (V_P floating).

CM1213A

Table 5. ELECTRICAL OPERATING CHARACTERISTICS FOR CM1293A-04SO (Note1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-------------------|--|---|-----|--------------|------|-------|
| V _P | Operating Supply Voltage (V _P -V _N) | | | 3.3 | 5.5 | V |
| I _P | Operating Supply Current | (V _P -V _N) = 3.3 V | | | 8.0 | μA |
| V _F | Diode Forward Voltage | I _F = 8 mA; T _A = 25°C | | 0.90 | | V |
| I _{LEAK} | Channel Leakage Current | T _A = 25°C; V _P = 5 V, V _N = 0 V | | ±0.1 | ±1.0 | μA |
| C _{IN} | Channel Input Capacitance | At 1 MHz, V _{IN} = 0 V (Note 2) | | | 2.0 | pF |
| ΔC _{I/O} | Channel I/O to I/O Capacitance | | | 1.5 | | pF |
| V _{ESD} | ESD Protection Peak Discharge Voltage at any channel input, in system Contact discharge per IEC 61000-4-2 standard | T _A = 25°C (Notes 2 and 3) | | ±8 | | kV |
| V _{CL} | Channel Clamp Voltage Positive Transients Negative Transients | T _A = 25°C, I _{PP} = 1A, t _P = 8/20 μS (Note 2) | | +9.9 -1.6 | | V |
| R _{DYN} | Dynamic Resistance Positive Transients Negative Transients | T _A = 25°C, I _{PP} = 1A, t _P = 8/20 μS (Note 2) | | 0.96 0.5 | | Ω |

1. All parameters specified at T_A = -40°C to +85°C unless otherwise noted.
2. Standard IEC 61000-4-2 with C_{Discharge} = 150 pF, R_{Discharge} = 330 Ω, V_P = 3.3 V, V_N grounded.
3. These measurements performed with no external capacitor on V_P (V_P floating).

CM1213A

PERFORMANCE INFORMATION

Input Channel Capacitance Performance Curves

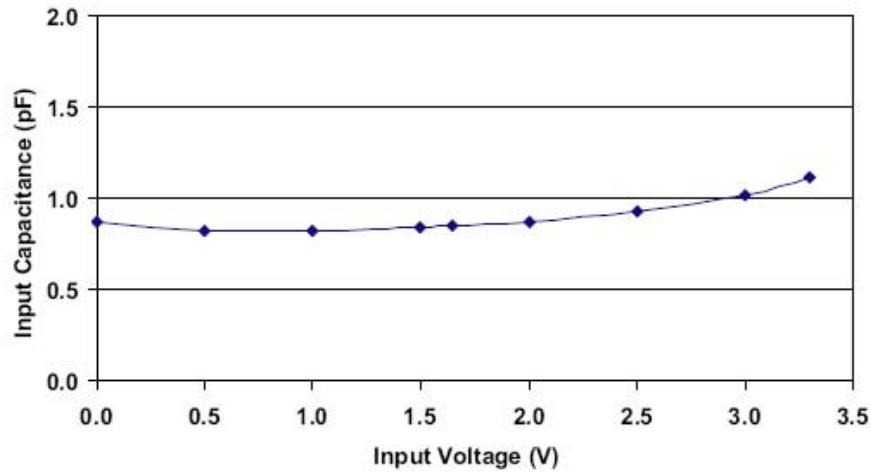


Figure 1. Typical Variation of C_{IN} vs. V_{IN}
($f = 1 \text{ MHz}$, $V_P = 3.3 \text{ V}$, $V_N = 0 \text{ V}$, $0.1 \mu\text{F}$ Chip Capacitor between V_P and V_N , 25°C)

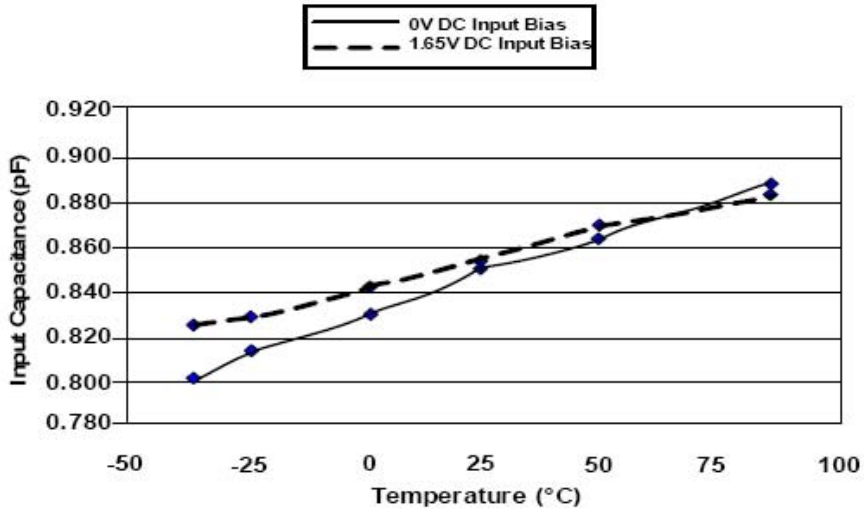


Figure 2. Typical Variation of C_{IN} vs. Temp
($f = 1 \text{ MHz}$, $V_{IN} = 30 \text{ mV}$, $V_P = 3.3 \text{ V}$, $V_N = 0 \text{ V}$, $0.1 \mu\text{F}$ Chip Capacitor between V_P and V_N)

CM1213A

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

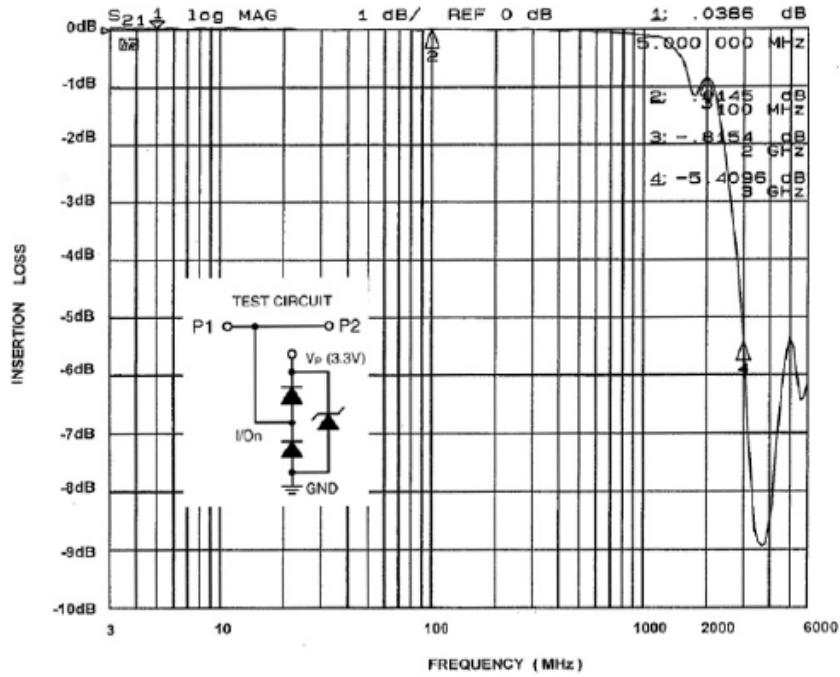


Figure 3. Insertion Loss (S₂₁) vs. Frequency (0 V DC Bias, V_p=3.3 V)

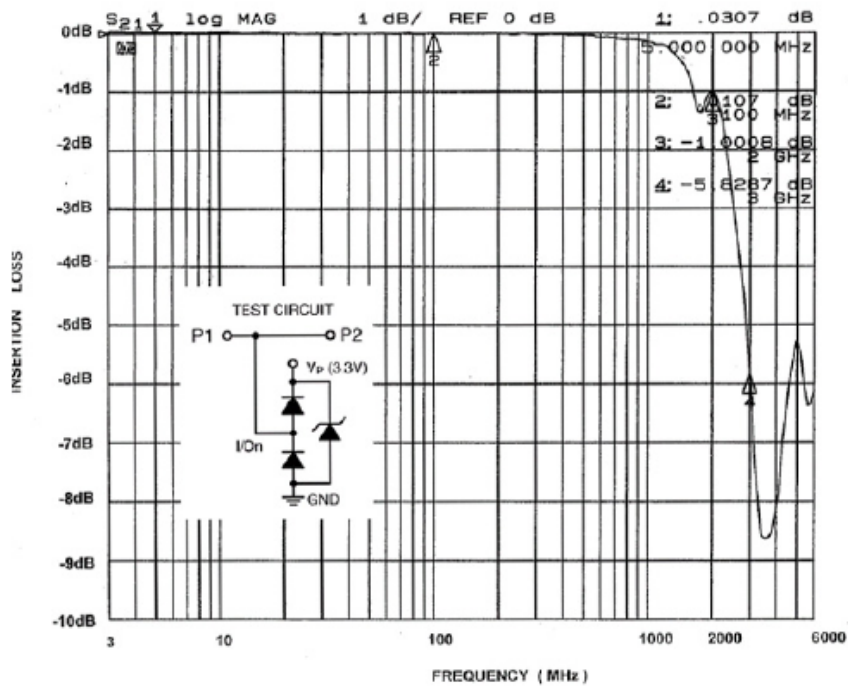


Figure 4. Insertion Loss (S₂₁) vs. Frequency (2.5 V DC Bias, V_p=3.3 V)

APPLICATION INFORMATION

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Application of Positive ESD Pulse between Input Channel and Ground, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L_1 and L_2 . The voltage V_{CL} on the line being protected is:

$$V_{CL} = \text{Fwd Voltage Drop of } D_1 + V_{\text{SUPPLY}} + L_1 \times d(I_{\text{ESD}}) / dt + L_2 \times d(I_{\text{ESD}}) / dt$$

where I_{ESD} is the ESD current pulse, and V_{SUPPLY} is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1 ns. Here $d(I_{\text{ESD}})/dt$ can be approximated by $\Delta I_{\text{ESD}}/\Delta t$, or $30/(1 \times 10^{-9})$. So just 10 nH of series inductance (L_1 and L_2 combined) will lead to a 300 V increment in V_{CL} !

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1213A has an integrated Zener diode between V_P and V_N . This greatly reduces the effect of supply rail inductance L_2 on V_{CL} by clamping V_P at the breakdown voltage of the Zener diode. However, for the lowest possible V_{CL} , especially when V_P is biased at a voltage significantly below the Zener breakdown voltage, it is recommended that a 0.22 μF ceramic chip capacitor be connected between V_P and the ground plane.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See also ON Semiconductor Application Note “Design Considerations for ESD Protection”, in the Applications section.

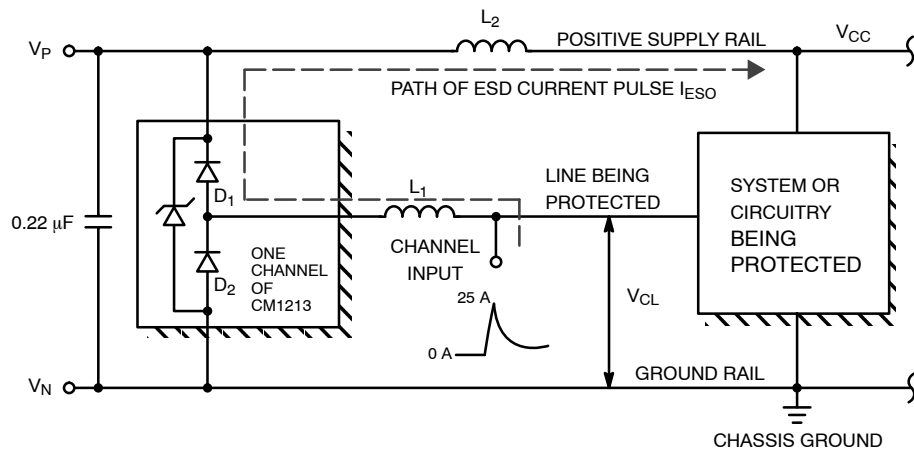
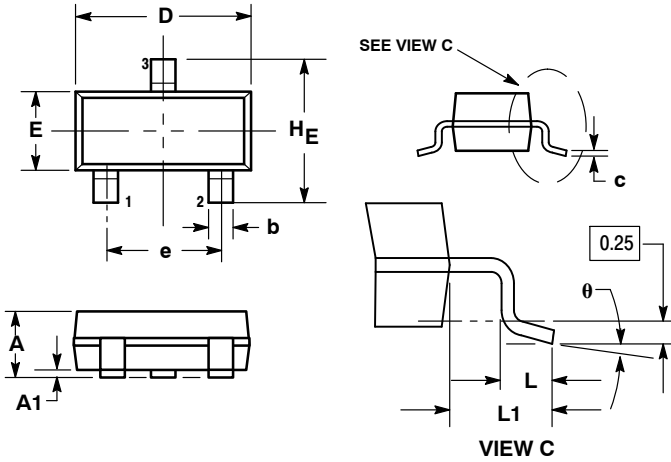


Figure 5. Application of Positive ESD Pulse between Input Channel and Ground

CM1213A

PACKAGE DIMENSIONS

SOT-23 (TO-236)
CASE 318-08
ISSUE AP

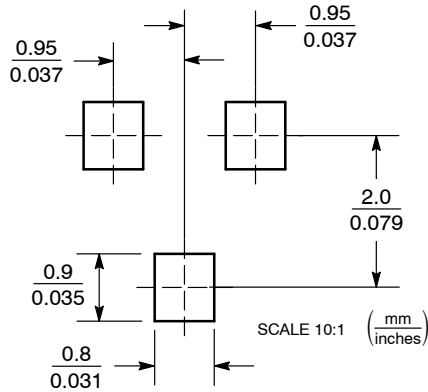


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | MILLIMETERS | | | INCHES | | |
|----------|-------------|------|------|--------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.89 | 1.00 | 1.11 | 0.035 | 0.040 | 0.044 |
| A1 | 0.01 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.37 | 0.44 | 0.50 | 0.015 | 0.018 | 0.020 |
| c | 0.09 | 0.13 | 0.18 | 0.003 | 0.005 | 0.007 |
| D | 2.80 | 2.90 | 3.04 | 0.110 | 0.114 | 0.120 |
| E | 1.20 | 1.30 | 1.40 | 0.047 | 0.051 | 0.055 |
| e | 1.78 | 1.90 | 2.04 | 0.070 | 0.075 | 0.081 |
| L | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| L1 | 0.35 | 0.54 | 0.69 | 0.014 | 0.021 | 0.029 |
| HE | 2.10 | 2.40 | 2.64 | 0.083 | 0.094 | 0.104 |
| θ | 0° | --- | 10° | 0° | --- | 10° |

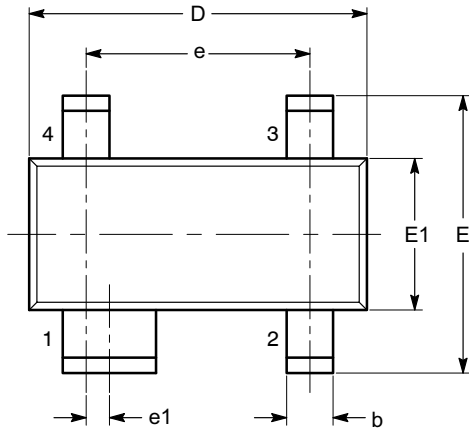
SOLDERING FOOTPRINT



CM1213A

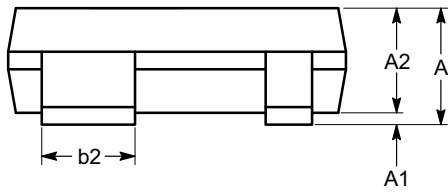
PACKAGE DIMENSIONS

SOT-143, 4 Lead
CASE 527AF-01
ISSUE A

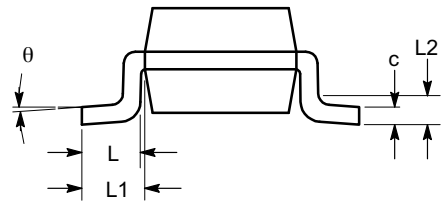


TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|----------|----------|------|------|
| A | 0.80 | | 1.22 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.75 | 0.90 | 1.07 |
| b | 0.30 | | 0.50 |
| b2 | 0.76 | | 0.89 |
| c | 0.08 | | 0.20 |
| D | 2.80 | 2.90 | 3.04 |
| E | 2.10 | | 2.64 |
| E1 | 1.20 | 1.30 | 1.40 |
| e | 1.92 BSC | | |
| e1 | 0.20 BSC | | |
| L | 0.40 | 0.50 | 0.60 |
| L1 | 0.54 REF | | |
| L2 | | 0.25 | |
| θ | 0° | | 8° |



SIDE VIEW



END VIEW

Notes:

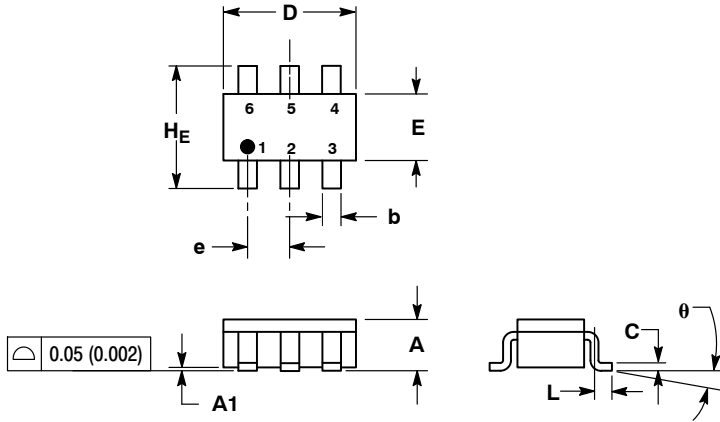
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC TO-253.

CM1213A

PACKAGE DIMENSIONS

SC-74
CASE 318F-05
ISSUE M

SCALE 2:1

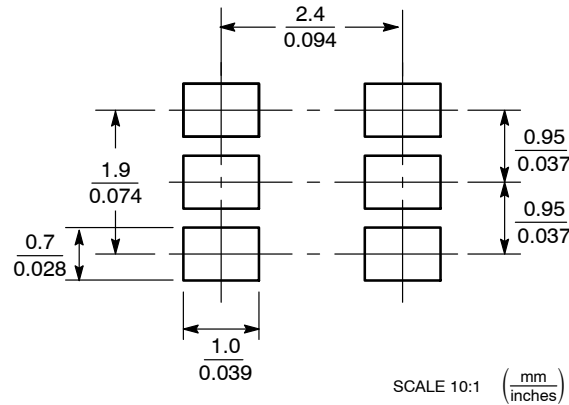


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F-01, -02, -03, -04 OBSOLETE. NEW STANDARD 318F-05.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|--------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 | 0.035 | 0.039 | 0.043 |
| A1 | 0.01 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.25 | 0.37 | 0.50 | 0.010 | 0.015 | 0.020 |
| c | 0.10 | 0.18 | 0.26 | 0.004 | 0.007 | 0.010 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 1.30 | 1.50 | 1.70 | 0.051 | 0.059 | 0.067 |
| e | 0.85 | 0.95 | 1.05 | 0.034 | 0.037 | 0.041 |
| L | 0.20 | 0.40 | 0.60 | 0.008 | 0.016 | 0.024 |
| HE | 2.50 | 2.75 | 3.00 | 0.099 | 0.108 | 0.118 |
| θ | 0° | - | 10° | 0° | - | 10° |

SOLDERING FOOTPRINT*

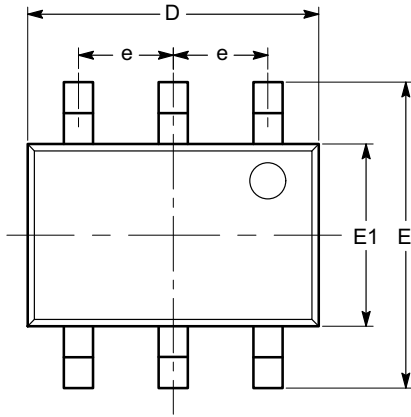


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

CM1213A

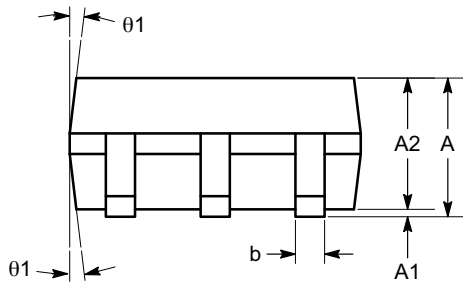
PACKAGE DIMENSIONS

SC-88 (SC-70 6 Lead), 1.25x2
 CASE 419AD-01
 ISSUE A

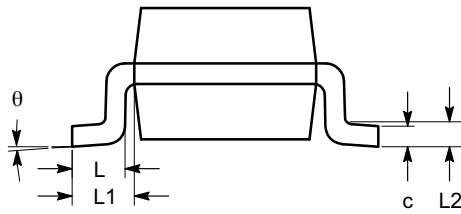


TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|-----------|----------|------|------|
| A | 0.80 | | 1.10 |
| A1 | 0.00 | | 0.10 |
| A2 | 0.80 | | 1.00 |
| b | 0.15 | | 0.30 |
| c | 0.10 | | 0.18 |
| D | 1.80 | 2.00 | 2.20 |
| E | 1.80 | 2.10 | 2.40 |
| E1 | 1.15 | 1.25 | 1.35 |
| e | 0.65 BSC | | |
| L | 0.26 | 0.36 | 0.46 |
| L1 | 0.42 REF | | |
| L2 | 0.15 BSC | | |
| θ | 0° | | 8° |
| $\theta1$ | 4° | | 10° |



SIDE VIEW



END VIEW

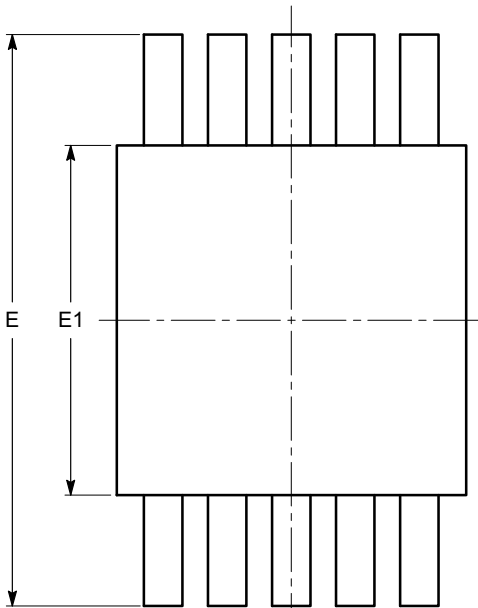
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

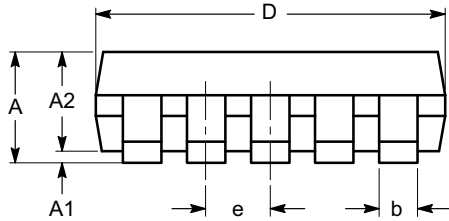
CM1213A

PACKAGE DIMENSIONS

MSOP 10, 3x3
CASE 846AE-01
ISSUE 0

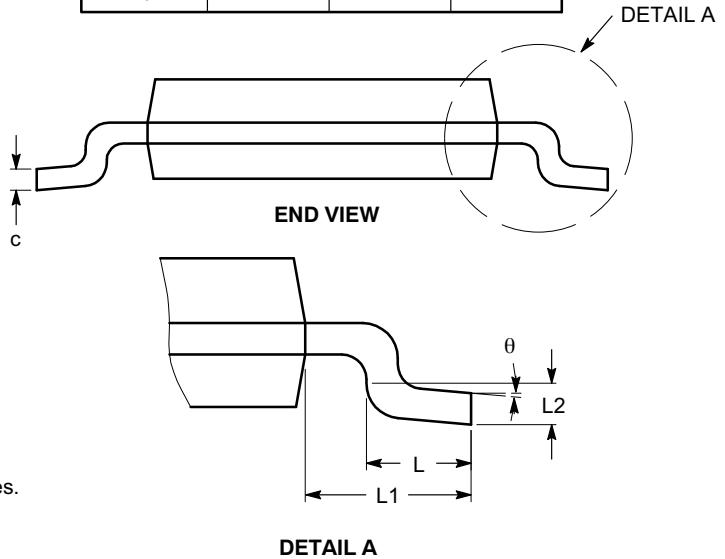


TOP VIEW



SIDE VIEW

| SYMBOL | MIN | NOM | MAX |
|----------|----------|------|------|
| A | | | 1.10 |
| A1 | 0.00 | 0.05 | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| b | 0.17 | | 0.27 |
| c | 0.13 | | 0.23 |
| D | 2.90 | 3.00 | 3.10 |
| E | 4.75 | 4.90 | 5.05 |
| E1 | 2.90 | 3.00 | 3.10 |
| e | 0.50 BSC | | |
| L | 0.40 | 0.60 | 0.80 |
| L1 | 0.95 REF | | |
| L2 | 0.25 BSC | | |
| θ | 0° | | 8° |



Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-187.

FireWire is a registered trademark of Apple Computer, Inc.
iLink is a trademark of S. J. Electro Systems, Inc.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative