P-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 60	0.015 at V_{GS} = - 10 V	- 50[d]
	0.020 at V_{GS} = - 4.5 V	- 50[d]

FEATURES

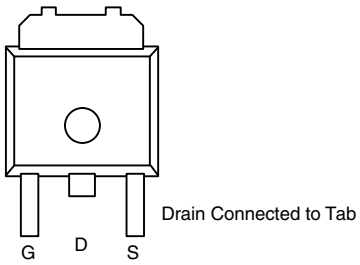
- TrenchFET® Power MOSFET
- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

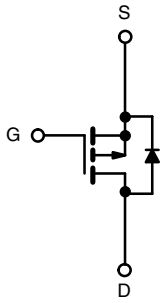
- Load Switch

TO-252



Top View

Ordering Information
SUD50P06-15-GE3 (Lead (Pb)-free and Halogen-free)
SUD50P06-15-T4-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)	T_C = 25 °C	I_D	- 50[d]	A
	T_C = 125 °C		- 27.5	
Pulsed Drain Current		I_{DM}	- 80	
Avalanche Current		I_{AS}	- 50	
Single Pulse Avalanche Energy[a]	L = 0.1 mH	E_{AS}	125	mJ
Power Dissipation	T_C = 25 °C	P_D	113[c]	W
	T_A = 25 °C		2.5[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Junction-to-Ambient[b]	t ≤ 10 s	R_{thJA}	15	18	°C/W
	Steady State		40	50	
Junction-to-Case		R_{thJC}	0.82	1.1	

Notes:
a. Duty cycle ≤ 1 %.
b. When mounted on 1" square PCB (FR-4 material).
c. See SOA curve for voltage derating.
d. Package limited.

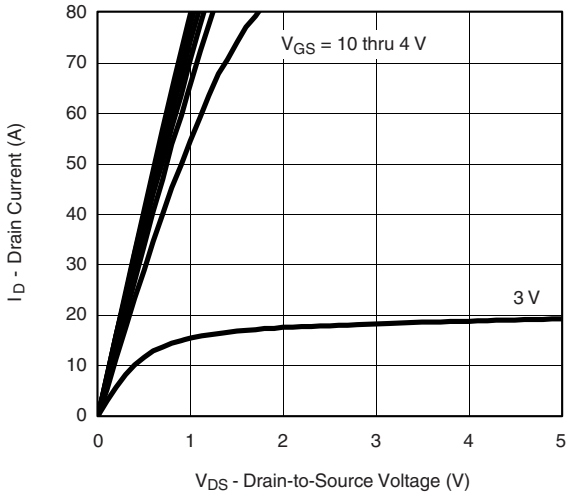
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1		- 3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 60 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 60 V, V_{GS} = 0 V, T_J = 125 °C			- 50	
		V_{DS} = - 60 V, V_{GS} = 0 V, T_J = 150 °C			- 100	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = - 5 V, V_{GS} = - 10 V	- 50			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 17 A		0.012	0.015	Ω
		V_{GS} = - 10 V, I_D = - 50 A, T_J = 125 °C			0.025	
		V_{GS} = - 10 V, I_D = - 50 A, T_J = 150 °C			0.028	
		V_{GS} = - 4.5 V, I_D = - 14 A			0.020	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 17 A		61		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = - 25 V, f = 1 MHz		4950		pF
Output Capacitance	C_{oss}			480		
Reverse Transfer Capacitance	C_{rss}			405		
Total Gate Charge[c]	Q_g	V_{DS} = - 30 V, V_{GS} = - 10 V, I_D = - 50 A		110	165	nC
Gate-Source Charge[c]	Q_{gs}			19		
Gate-Drain Charge[c]	Q_{gd}			28		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = - 30 V, R_L = 0.6 Ω $I_D \cong$ - 50 A, V_{GEN} = - 10 V, R_G = 6 Ω		15	23	ns
Rise Time[c]	t_r			70	105	
Turn-Off Delay Time[c]	$t_{d(off)}$			175	260	
Fall Time[c]	t_f			175	260	
Source-Drain Diode Ratings and Characteristics T_C = 25 °C[b]						
Continuous Current	I_S				- 50	A
Pulsed Current	I_{SM}				- 80	
Forward Voltage[a]	V_{SD}	I_F = - 50 A, V_{GS} = 0 V		- 1	- 1.6	V
Reverse Recovery Time	t_{rr}	I_F = - 50 A, dI/dt = 100 A/µs		45	70	ns

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

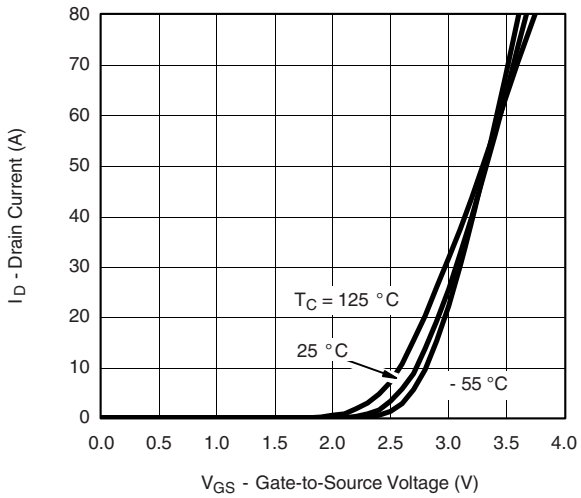
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For technical questions, contact: pmostechsupport@vishay.comm
Document Number: 68940
S12-2439 Rev. C, 15-Oct-12

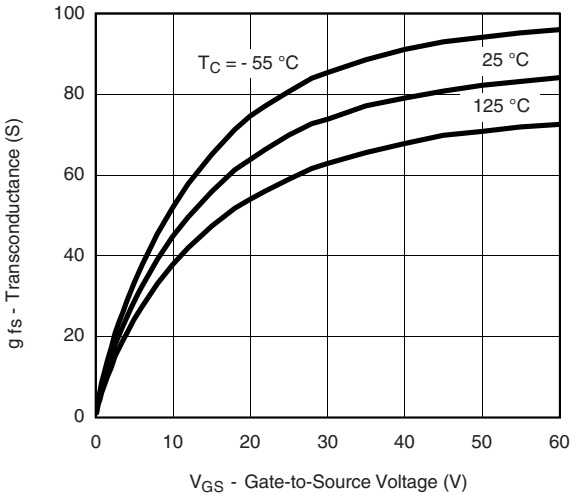
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



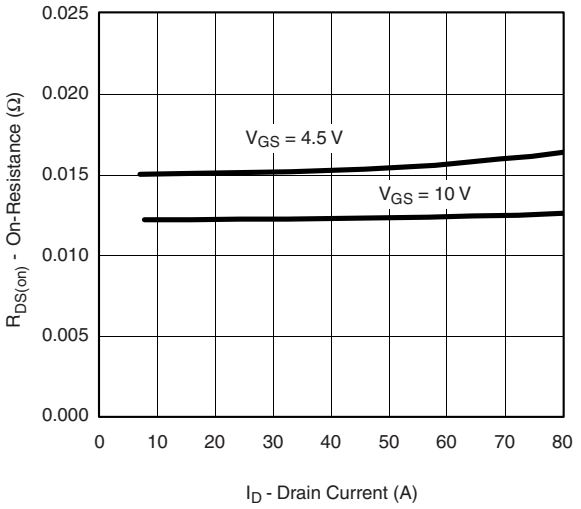
Output Characteristics



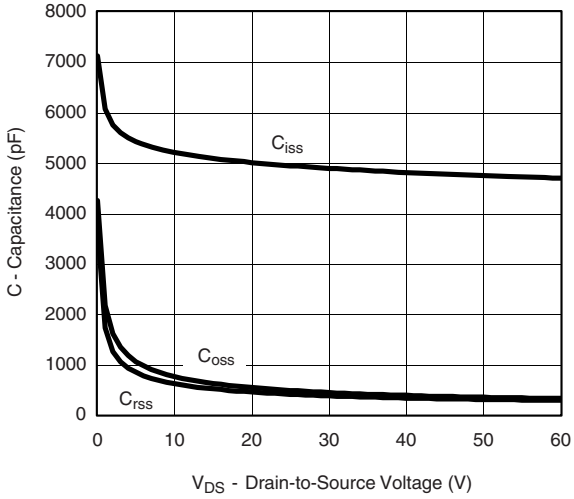
Transfer Characteristics



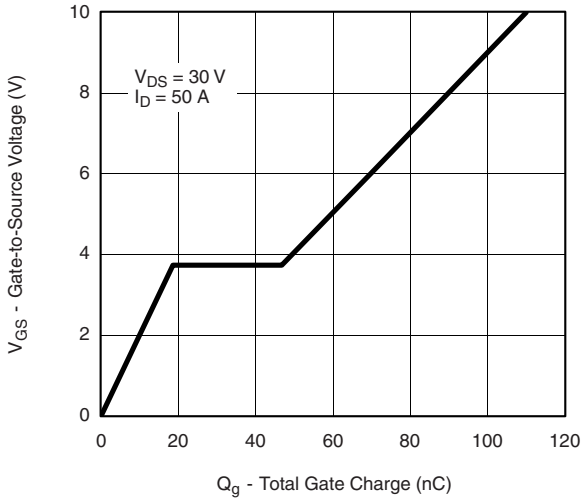
Transconductance



On-Resistance vs. Drain Current

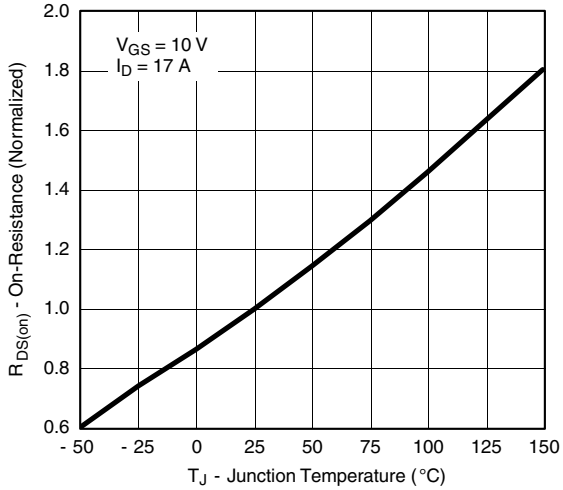


Capacitance

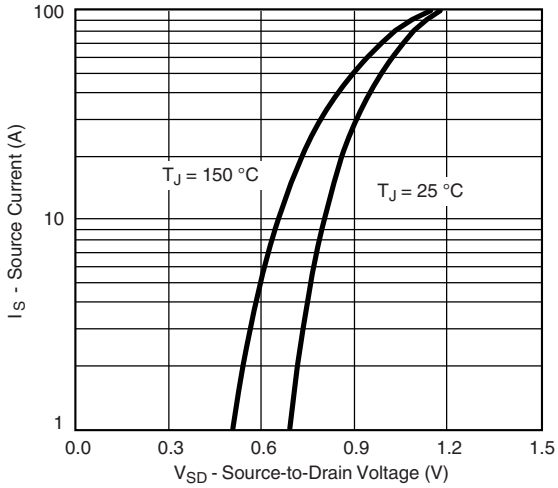


Gate Charge

TYPICAL CHARACTERISTICS

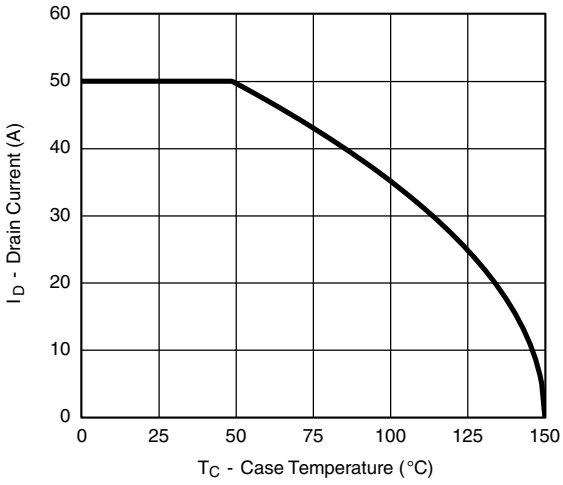


On-Resistance vs. Junction Temperature

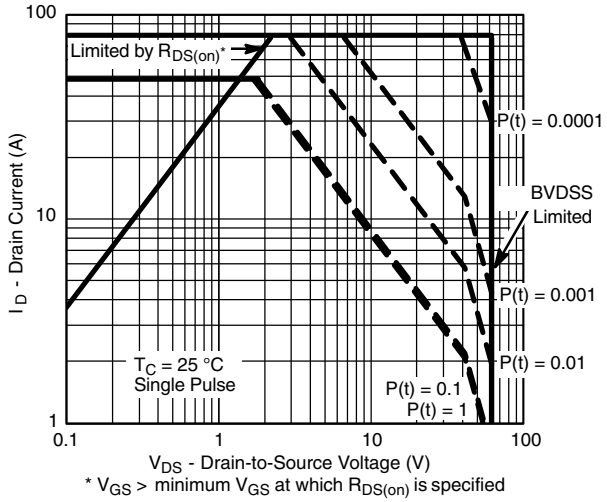


Source-Drain Diode Forward Voltage

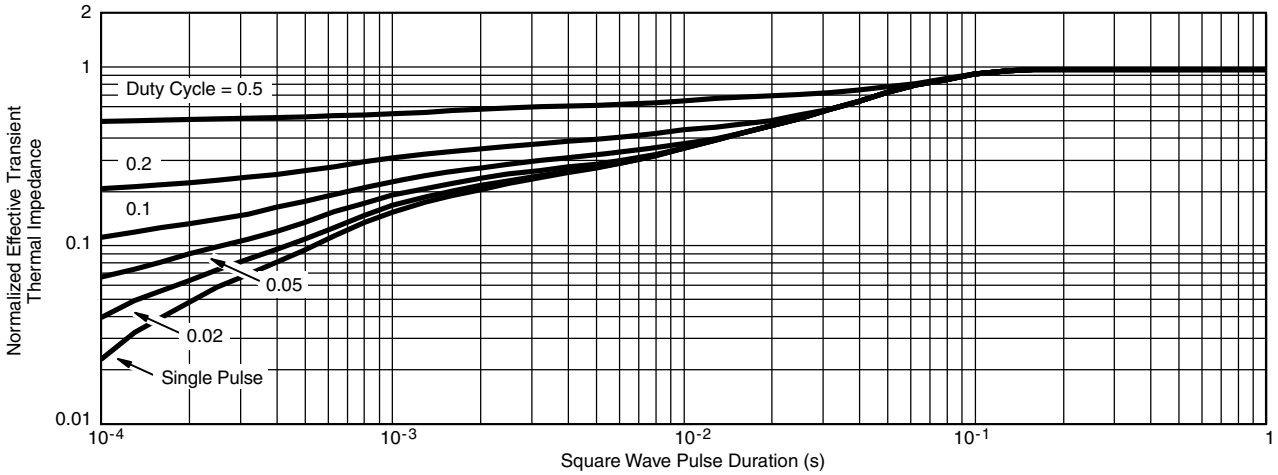
THERMAL RATINGS (25 °C, unless otherwise noted)



Drain Current vs. Case Temperature



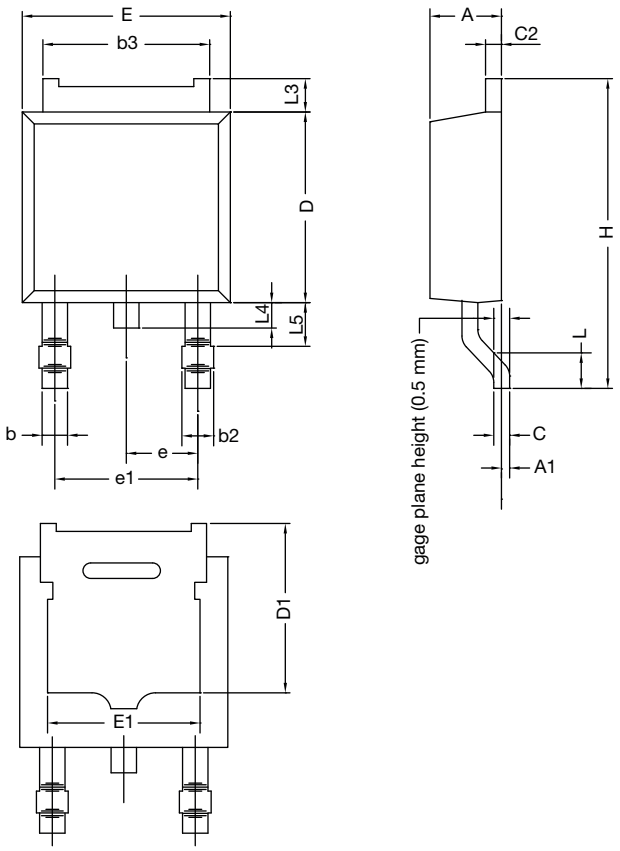
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68940.

TO-252AA Case Outline

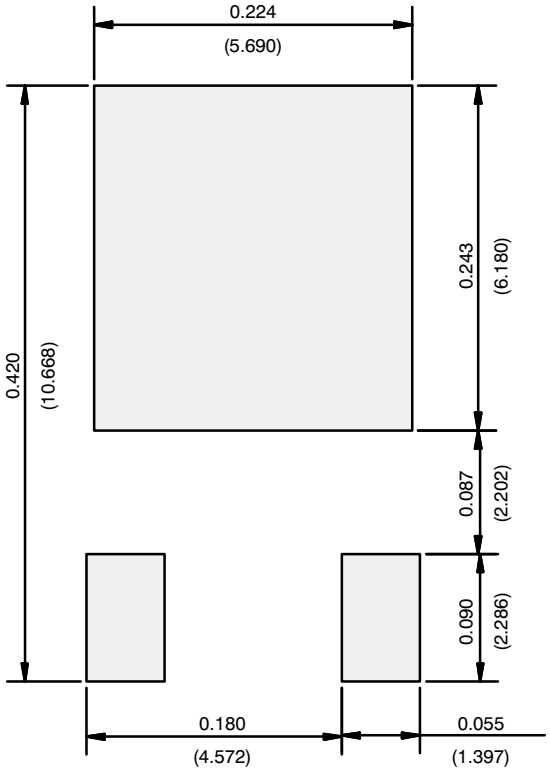


	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

Notes

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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