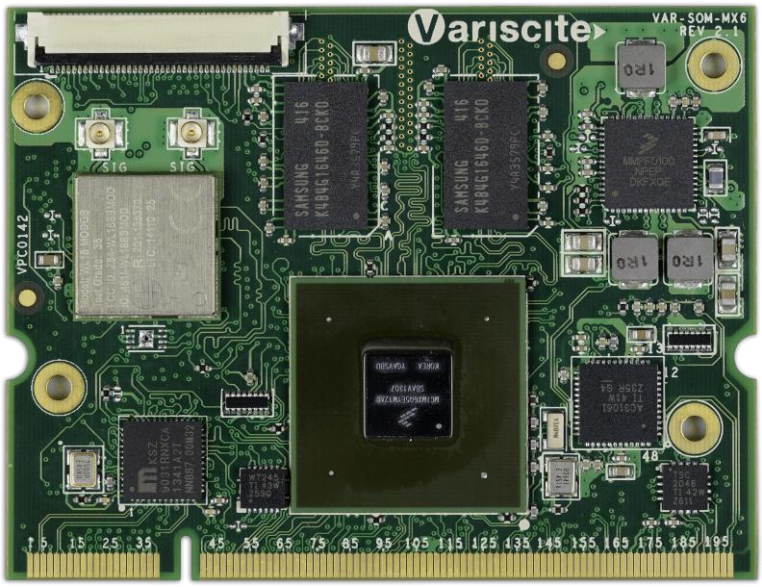
VARISCITE LTD.

VAR-SOM-MX6 v2.1 Datasheet

Freescale i.MX6™ - based System-on-Module



VARISCITE LTD.

VAR-SOM-MX6 Datasheet

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Document Revision History

Revision	Date	Notes
1.0	09/9/2014	Initial
1.01	22/10/2014	Section 4.19.1 - eMMC boot clarification
1.02	22/10/2014	Additional 200 pin connectors recommendations
1.03	25/12/2014	Section 3.2 - Updated: pins 16, 94, removed pin 70 Section 8 - Updated
1.04	05/02/2015	Section 9 - Updated Mechanical Drawing
1.05	25/12/2015	Section 8 -MTBF revised. Full report can be requested at support@variscite.com Section 6.2 - Power consumption @ suspend
1.06	11/01/2016	Section 3.1 - Updated Note [2] Section 4.10 - Corrected UART number, updated note Section 4.15 - Updated note
1.07	06/06/2016	Section 4.12 – Corrected ECSPI pinmux tables
1.08	14/09/2016	Section 4.8 – Updated Interface features Section 6.2 – Updated CPU Usage, Additional Peripherals
1.09	07/12/2016	Section 1.4 – Corrected pin 72 name typo (V2.X) Section 3.1 – Corrected pin 17 name typo Section 8 – Updated notes
1.10	25/12/2016	Section 6.2 – Updated CPU Usage table
1.11	02/02/2017	Section 4.8 – Updated interface features
1.12	26/06/2017	Section 3.1, 4.19 – Added notes on POR_B signal
1.13	02/11/2017	Section 1.2, 2.5, 4.5 – Updated Bluetooth features
1.14	21/12/2017	Section 3.1, 4.10 – Updated UART features, notes, pinmux tables
1.15	22/01/2018	Section 3.2 – Updated pins 42,60 68-73
1.16	14/03/2018	Section 3.1, 4.7 – Added note for USB_OTG design, updated pinmux table.
1.17	12/04/2018	Section 1.2, 2.1 – Added support for iMX6 QuadPlus
1.18	21/03/2019	Section 3.1,3.4 - Updated pinmux tables. Section 4.12 – Updated SPI pinmux table Section 6.2 – Updated suspend
1.19	30/08/2020	Section 4.9 – Renamed table heading from “AUDMUX4 Signals” to “Analog Signals”
1.20	20/10/2020	Section 1.3 – Updated Block Diagram
1.21	01/05/2022	Section 8 – Updated Table
1.22	17/5/2022	sections: 1.2,2.5,4.5 - Updated the BT

Document Revision History 3

1. Overview 6

1.1. General Information 6
1.2. Feature Summary 7
1.3. Block Diagram 8
1.4. VAR-SOM-MX6 V1.X vs V2.X 9

2. Main Hardware Components 9

2.1. Freescale i.MX6 9
2.2. Memory 14
2.3. 10/100/1000 Ethernet PHY 14
2.4. TLV320AIC3106 Audio 15
2.5. Wi-Fi + BT 15
2.6. PMIC 16

3. External Connectors 16

3.1. VAR-SOM-MX6 Connector Pin-out 17
3.2. SO-DIMM 200 Pin Mux 23
3.3. 40-pin FFC Connector Pin-out 26
3.4. 40-pin FFC Mux 27

4. SOM's interfaces 29

4.1. Display Interfaces 29
4.2. Touch Panel 31
4.3. Camera Interfaces 31
4.4. Gigabit Ethernet 34
4.5. Wi-Fi & Bluetooth 34
4.6. USB Host 2.0 35
4.7. USB 2.0 OTG 35
4.8. MMC/SD/SDIO 35
4.9. Audio 37
4.10. UART Interfaces 38
4.11. Flexible Controller Area Network (FLEXCAN) 40
4.12. SPI 40
4.13. PCIe 42
4.14. Serial ATA 42
4.15. I^2C 43
4.16. Local Bus 43
4.17. JTAG 45
4.18. General Purpose IOs 45
4.19. General System Control 45
4.20. Power 46

5. Absolute Maximum Characteristics 47

6. Operational Characteristics 47

6.1. Power supplies 47
6.2. Power Consumption 47

7. DC Electrical Characteristics 47

8. Environmental Specifications 48

9. Mechanical Drawings 48

10. Legal Notice 49

11. Warranty Terms 50
12. Contact Information 51

1. Overview

1.1. General Information

The VAR-SOM-MX6 is a high performance System-on-Module. It provides an ideal building block that easily integrates with a wide range of target markets requiring rich multimedia functionality, powerful graphics and video capabilities, as well as high-processing power. Compact, cost effective and with low power consumption, VAR-SOM-MX6 secures an Intel Atom performance level.

Supporting products:

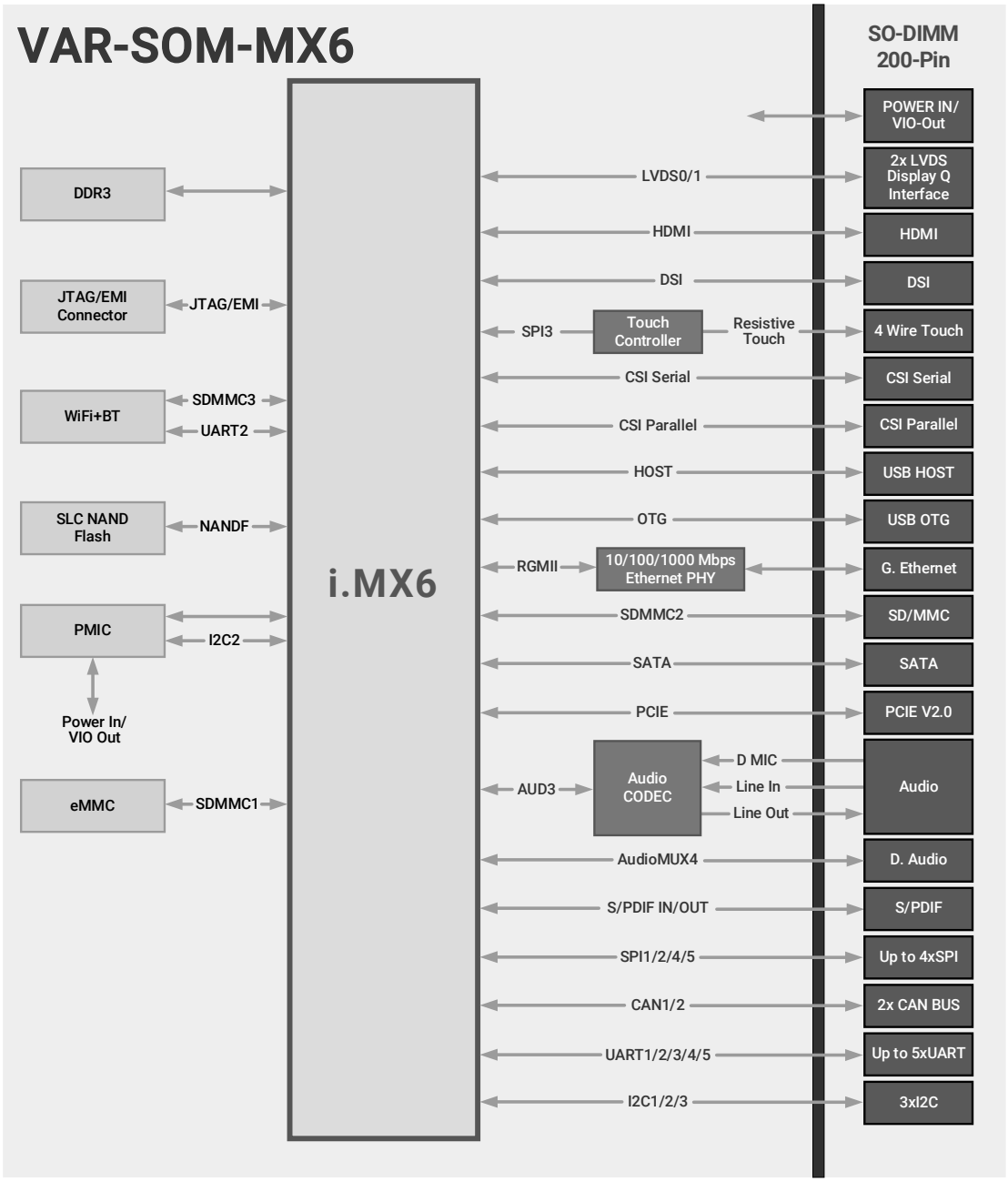
- VAR-MX6CustomBoard – evaluation board
  - ✓ Carrier -Board, compatible with VAR-SOM-MX6
  - ✓ Schematics
- VAR-EXT-CB402 – CSI2 Camera module
- O.S support
  - ✓ Linux BSP
  - ✓ Windows Embedded Compact 7
  - ✓ Android

Contact Variscite support services for further information: mailto:support@variscite.com.

1.2. Feature Summary

- Freescale i.MX6 series SoC (Single/Dual/Quad/QuadPlus ARM® Cortex™-A9 Core, 1.2 GHz)
- Up to 4GB DDR3 RAM
- Up to 1GB NAND Flash for storage memory / boot
- Up to 64GB eMMC storage
- 2 x LVDS display interface
- HDMI V1.4 interface
- 1 x MIPI DSI
- Touch panel interface
- Parallel & serial camera interface
- On-board 10/100/1000 Mbps Ethernet PHY
- TI WiLink8 2.4/5GHz WLAN (802.11 a/b/g/n) / BT-BLE 5.1 with CSA2 support and optional MIMO
- 1 x USB 2.0 host, 1 x OTG
- 1 x SD/MMC
- Serial interfaces (SPI , I2C, UART, I2S,)
- CAN Bus
- Stereo line-In / headphones out
- Digital microphone
- Single 3.3 V power supply
- 67mm x 51mm, 200 pin SO-DIMM Connector

1.3. Block Diagram



1.4. VAR-SOM-MX6 V1.X vs V2.X

a) Features differences summary:

Feature	V1.x	V2.x
WLAN module	LSR Tiwi-BLE	TI WLMOD183x
eMMC	NA	Up to 64GB
SDHC1 port	External pins 68-73 on 200 SODIMM connector	Internal

b) Pin-out changes are only on the 200 pin SODIMM connector:

Pin #	V1.X	V2.X
40	BOOT_SEL1 | Ball M23	BOOT_SEL1 | Ball L23
68	SD1_DATA0 | Ball A21	PWM1_OUT | Ball T2
69	SD1_CMD | Ball B21	PWM3_OUT | Ball B19
70	SD1_DATA2 | Ball E19	GPIO2_14 | Ball B20
71	SD1_DATA1 | Ball C20	GPIO1_2 | Ball T1
72	SD1_CLK | Ball D20	PWM2_OUT | Ball T4
73	SD1_DATA3 | Ball F18	GPIO2_11 | Ball A20

c) New boot strap pins. Refer to section 4.19.1

2. Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-MX6

2.1. Freescale i.MX6

2.1.1. Overview

The i.MX6 Dual/Quad/QuadPlus processors represent Freescale Semiconductor's latest achievement in integrated multimedia applications processors, optimized for lowest power consumption. The processors feature Freescale's advanced implementation of the quad ARM™ Cortex-A9 core, which operates at speeds of up to 1.2 GHz. They include 2D and 3D graphics processors, 3D 1080p video processing and integrated power management. Each processor provides a 64-bit DDR3/LVDDR3-1066 memory interface and a number of other interfaces such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

2.1.2. i.MX6 Block Diagram

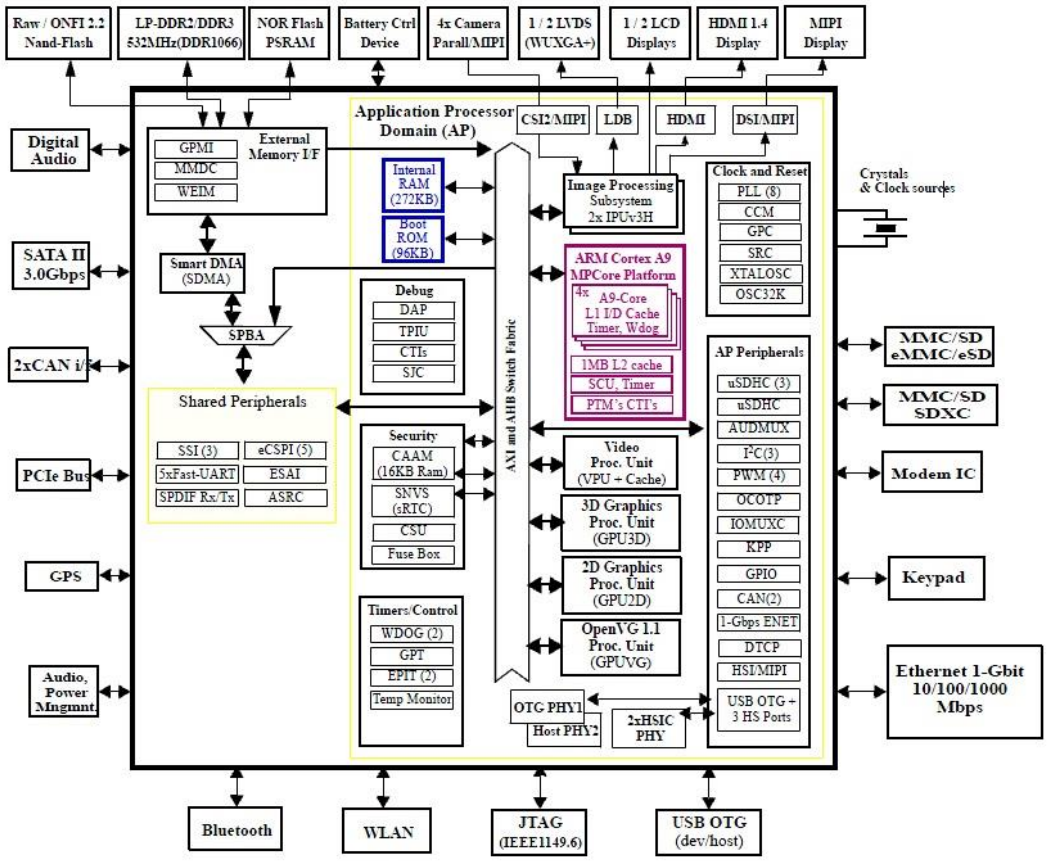


Figure 1. i.MX 6Dual/6Quad System Block Diagram

2.1.3. CPU Platform

The i.MX6 Dual/Quad/QuadPlus Application Processor (AP) is based on the ARM Cortex-A9 MPCore™ Platform, which has the following features:

- ARM Cortex A9 MPCore™ Dual or Quad core CPU configurations (with TrustZone)
- Symmetric CPU configuration where each CPU includes:
  - 32 Kbyte L1 Instruction Cache
  - 32 Kbyte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor.
- The ARM Cortex A9 MPCore™ complex includes:
- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 Megabyte unified L2 cache shared by all CPU cores (Dual or Quad)
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- NEON MPE coprocessor
  - SIMD Media Processing Architecture

  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline External
  - Supports single and double-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations as described in the ARM VFPv3 architecture.
- Provides conversions between 16-bit, 32-bit and 64-bit floating-point formats and ARM integer word formats.

2.1.4. Memory Interfaces

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (1 MByte)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 16-bit, 32-bit, and 64-bit DDR3-1066, LV-DDR3-1066, and 1/2 LPDDR2-1066 channels, supporting DDR interleaving mode, for 2x32 LPDDR2-1066
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size,
  - BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 32 bit.
- 16-bit NOR Flash. All WEIMv2 pins are muxed on other interfaces.
- 16-bit PSRAM, Cellular RAM

2.1.5. DMA engine

The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features:

- Powered by a 16-bit Instruction-Set micro-RISC engine
- Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels
- 48 events with total flexibility to trigger any combination of channels
- Memory accesses including linear, FIFO, and 2D addressing
- Shared peripherals between ARM and SDMA
- Very fast Context-Switching with 2-level priority based preemptive multi-tasking
- DMA units with auto-flush and prefetch capability
- Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address)
- DMA ports can handle unit-directional and bi-directional flows (copy mode)
- Up to 8-word buffer for configurable burst transfers
- Support of byte-swapping and CRC calculations

- Library of Scripts and API is available

2.1.6. Display Subsystem

The i.MX6Dual/6Quad/6QuadPlus video graphics subsystem consists of the following dedicated modules:

- Video Processing Unit (VPU): a multi-standard high performance video/image CODEC
- Three Graphics Processing Units (GPUs):
  - 3D GPU: accelerating the generation of 3D graphics (OpenGL/ES) and vector graphics (OpenVG)
  - 2D GPU: acceleration the generation of 2D graphics (BitBLT).
  - OpenVG: acceleration of vector graphics (OpenVG).
- Two (identical) Image Processing Units (IPUs): providing connectivity to cameras and displays, related processing, synchronization and control.
- Display interface bridges: providing optional translation from the digital display interface supported by the IPU to other interfaces:
  - LVDS bridge (LDB): providing up to two LVDS interfaces
  - HDMI transmitter
  - MIPI/DSI transmitter
- MIPI/CSI-2 receiver
- Two (identical) Display Content Integrity Checker (DCIC) are used to authenticate sensitive displayed data.
- A Video Data Order Adapter (VDOA): used to re-order video data from the "tiled" order used by the VPU to the conventional raster-scan order needed by the IPU.

2.1.7. MIPI - Camera Serial Interface Host Controller

The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2), Version 1.00 - 29 November 2005
- Optional support for Camera Control Interface (CCI) through the use of DesignWare Core (DW_apb_i2c)
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009
- Supports up to 4 D-PHY Rx Data Lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets; Support for several frame formats such as:
  - General Frame or Digital Interlaced Video with or without accurate sync timing
  - Data type (Packet or Frame level) and Virtual Channel interleaving
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification
- Supports all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions
  - From 24-bit down to 6-bit per pixel

- Generic or user-defined byte-based data types
- Error detection and correction
- PHY level
- Packet level
- Line level
- Frame level

2.1.8. 2D and 3D Graphics Processing Unit (GPU)

The GPU2D module has two independent sub-modules: R2D and V2D GPUs. Both GPU were designed to display on a variety of consumer devices. Addressable screen sizes range from small displays featured on cell phones to large 1080p high definition displays.
The GPU2D cores provide powerful graphics at low power consumption, utilizing the smallest silicon footprints. Dynamic power consumption is minimized by extensive use of localized clock gating.
Hardware acceleration is brought to numerous 2D and VG applications including graphical user interfaces (GUI), menu displays, flash animation and gaming.
The GPU3D is a high-performance core that delivers hardware acceleration for 3D graphics display. Addressable screen sizes range from the smallest cell phones to HD 1080p displays. It provides high performance, high quality graphics, low power consumption and the smallest silicon footprint.
GPU3D accelerates numerous 3D graphics applications, including Graphical User Interfaces (GUI), menu displays, flash animation, and gaming. This module supports the following graphics APIs:

- OpenGL ES 1.1, 2.0, and 3.0
- OpenVG 1.1
- EGL 1.4
- OpenGL 2.1
- OpenCL 1.1 EP (Not supported in iMX6 SOLO/DL)
- DirectX 11 (9_3)

2.1.9. Audio Back End

The AUDMUX provides flexible, programmable routing of the serial interfaces (SSI1 or SSI2) to and from off-chip devices. The AUDMUX routes audio data (and even splices together multiple time-multiplexed audio streams) but does not decode or process audio data itself. The AUDMUX is controlled by the ARM but can route data even when the ARM is in a low-power mode.
The ESAI (Enhanced Serial Audio Interface) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The ESAI is connected to the IOMUX and to the ESAI_BIFIFO module.
The ESAI_BIFIFO (ESAI Bus Interface and FIFO) is the interface between the ESAI module and the shared peripheral bus. It contains the FIFOs used to buffer data to and from the ESAI, as well as providing the data word alignment and padding necessary to match the 24-bit data bus of the ESAI to the 32-bit data bus of the shared peripheral bus.
The SPDIF (Sony/Philips Digital Interface) audio module is a stereo transceiver that allows the processor to receive and transmit digital audio over it. The SPDIF receiver section

includes a frequency measurement block that allows the precise measurement of incoming sampling frequency. A recovered clock is provided by the SPDIF receiver section and may be used to drive both internal and external components in the system. The SPDIF is connected to the shared peripheral bus.
The ASRC (Asynchronous Sample Rate Converter) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversions of up to 10 channels of over 120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs. The ASRC is connected to the shared peripheral bus.

2.1.10. 10/100/1000 Ethernet Controller

The MAC-NET core, in conjunction with a 10/100/1000 MAC, implements layer 3 network acceleration functions. These functions are designed to accelerate the processing of various common networking protocols, such as IP, TCP, UDP and ICMP, providing wire speed services to client applications. The MAC operation is fully programmable and can be used in NIC (Network Interface Card), bridging, or switching applications. The core implements the remote network monitoring (RMON) counters according to IETF RFC 2819. The core also implements a hardware acceleration block to optimize the performance of network controllers providing IP and TCP, UDP, ICMP protocol services. The acceleration block performs critical functions in hardware, which are typically implemented with large software overhead. The core implements programmable embedded FIFOs that can provide buffering on the receive path for loss-less flow control .Advanced power management features are available with magic packet detection and programmable power-down modes.

2.2. Memory

2.2.1. RAM

The VAR-SOM-MX6 is available with up to 4 GB of DDR3 memory.

2.2.2. Non-volatile Storage Memory

- NAND flash: The VAR-SOM-MX6 is available with up to 1GB of SLC NAND FLASH memory. The NAND flash is used for Flash Disk purposes, O.S. run-time-image and the Boot-loader (Boot from NAND).
- eMMC : Up to 64GB of storage. Boot from eMMC is not possible, therefore minimal NAND-flash of 128MB is required.

2.3. 10/100/1000 Ethernet PHY

The VAR-SOM-MX6 features the Micrel KSZ9031 gigabit Ethernet PHY. The KSZ9031RN is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable. The KSZ9031RN provides the Reduced Gigabit Media Independent Interface (RGMII) for direct connection to RGMII MACs in Gigabit Ethernet processors and switches for data transfer at 10/100/1000 Mbps speed.

2.4. TLV320AIC3106 Audio

The Texas Instrument's TLV320AIC3106 is a low-power, highly integrated stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single-ended or fully differential configurations. Extensive register-based power control is included, enabling stereo 48-kHz DAC playback as low as 15mW. The VAR-SOM-MX6 exposes the following interface of the TLV320AIC3106:

- Headphone
- Line-in
- Digital microphone

2.5. Wi-Fi + BT

The VAR-SOM-MX6 contains TI's WL183xMOD WiLink, a high performance 2.4/5 GHz IEEE 802.11 a/b/g/n Bluetooth 5.1/BLE with CSA2 support radio module, with optional Dual Band and MIMO support.
The modules support improved performance over WiFi in bit rates reaching 100Mbps (UDP) and 80Mbps (TCP).
The module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The module also provides a Bluetooth platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

- IEEE 802.11 b,g,n or Dual Band 2.4/5GHz 802.11 a/b/g/n with optional MIMO
- Bluetooth 5.1/BLE with CSA2 support
- U.FL connectors for external antennas
- Integrated band-pass filter
- Operating Temperature Range:
  Dual Band 2.4/5GHz Modules: -40 to +85
  2.4GHz Modules: -20 to +70

2.6. PMIC

The VAR-SOM-MX6 features Freescale's PMPF0100 as a Power Management Integrated circuit (PMIC) designed specifically for use with Freescale's i.MX6 series of application processors. The PMPF0100 regulates all power rails required on SoM from a single 3.3 V power supply.
The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

3. External Connectors

The VAR-SOM-MX6 exposes a 200-pin SO–DIMM mechanical standard interface. The recommended mating connector for baseboard interfacing are:

1. CONCRAFT - 0701A0BE52E
2. Tyco Electronics -1565917-4

In addition to the 200-pin SO-DIMM interface VAR-SOM-MX6 exposes a 40-pin FFC connector. The recommended mating cable is Molex 21020-0427 or equivalent

Pin#:
Pin number on the SO-DIMM200 connector

Pin Name:
Default VAR-SOM-MX6 pin name

Type:
Pin type & direction:

- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin

Pin Group:
Pin functionality group

i.MX6 Ball:
Ball number

Mode (Tables 3.2 & 3.4):
Pin mux mode option

3.1. VAR-SOM-MX6 Connector Pin-out

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
1	GND	POWER	Digital GND		
2	GND	POWER	Digital GND		
3	MDI_A+	DS	Gigabit Ethernet		
4	MDI_C+	DS	Gigabit Ethernet		
5	MDI_A-	DS	Gigabit Ethernet		
6	MDI_C-	DS	Gigabit Ethernet		
7	GND	POWER	Digital GND		
8	GND	POWER	Digital GND		
9	MDI_B+	DS	Gigabit Ethernet		
10	MDI_D+	DS	Gigabit Ethernet		
11	MDI_B-	DS	Gigabit Ethernet		
12	MDI_D-	DS	Gigabit Ethernet		
13	GND	POWER	Digital GND		
14	GND	POWER	Digital GND		
15	GETH_LED2	O	Gigabit Ethernet LED		
16	GETH_LED1	O	Gigabit Ethernet LED		
17	PWM2	IO	Pulse width modulation	GPIO4[30]	T25
18	DMIC_CLK	O	Digital microphone interface		
19	GND	POWER	Digital GND		
20	DMIC_DATA	I	Digital microphone interface		
21	AUDMUX4_RXD	IO	Digital audio mux	GPIO5[17]	W24
22	AUDMUX4_RXC	IO	Digital audio mux	GPIO5[13]	U23
23	AUDMUX4_RXFS	IO	Digital audio mux	GPIO5[12]	V25
24	AUDMUX4_TXFS	IO	Digital audio mux	GPIO5[16]	V24
25	AUDMUX4_TXC	IO	Digital audio mux	GPIO5[14]	U22
26	AUDMUX4_TXD	IO	Digital audio mux	GPIO5[15]	T20
27	GND	POWER	Digital GND		
28	GND	POWER	Digital GND		
29	CLKO2	O	Reference clock out		
30	NC		Leave not connected		
31	GND	POWER	Digital GND		
32	VIN_3V3	POWER	3.3 V power supply IN		
33	GND	POWER	Digital GND		
34	VIN_3V3	POWER	3.3 V power supply IN		
35	GND	POWER	Digital GND		
36	VIN_3V3	POWER	3.3 V power supply IN		
37	GND	POWER	Digital GND		
38	VIN_3V3	POWER	3.3 V power supply IN		

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
39	CSPI1_CS0	IO	Configurable SPI	GPIO4[9]	U6
40	BOOT_SEL1	IO	EIM_DA05	GPIO3[5]	L23
41	CSPI1_MISO	IO	Configurable SPI	GPIO4[8]	U7
42	BOOT_SEL0	IO	EIM_DA7	GPIO3[7]	L25
43	CSPI1_CLK	IO	Configurable SPI	GPIO4[6]	W5
44	CAN1_TX	IO	Controller area network	GPIO1[7]	R3
45	CSPI1_MOSI	IO	Configurable SPI	GPIO4[7]	V6
46	CAN1_RX	IO	Controller area network	GPIO1[8]	R5
47	GND	POWER	Digital GND		
48	CSPI1_CS1	IO	Configurable SPI	GPIO4[10]	W6
49	3V3_PER	POWER	Power good indication		
50	UART2_CTS	IO	UART2 port[2]	GPIO3[28]	G23
51	UART2_RTS	IO	UART2 port[2]	GPIO3[29]	J19
52	UART2_TXD	IO	UART2 port[2]	GPIO3[26]	E24
53	UART2_RXD	IO	UART2 port[2]	GPIO3[27]	E25
54	UART3_RXD	IO	UART3 port	GPIO3[25]	G22
55	UART3_CTS	IO	UART3 port	GPIO3[23]	D25
56	UART3_TXD	IO	UART3 port	GPIO3[24]	F22
57	UART3_RTS	IO	UART3 port[3]	GPIO2[31]	F23
58	GND	POWER	Digital GND		
59	GND	POWER	Digital GND		
60	SD2_CLK	IO	SD/MMC and SDXC	GPOP1[10]	C21
61	SD2_DATA2	IO	SD/MMC and SDXC	GPIO1[13]	A23
62	SD2_DATA0	IO	SD/MMC and SDXC	GPIO1[15]	A22
63	SD2_DATA1	IO	SD/MMC and SDXC	GPIO1[14]	E20
64	SD2_CMD	O	SD/MMC and SDXC	GPIO1[11]	F19
65	SD2_DATA3	IO	SD/MMC and SDXC	GPIO1[12]	B22
66	GND	POWER	Digital GND		
67	GND	POWER	Digital GND		
68	PWM1_OUT	IO	General purpose	GPIO1[9]	T2
69	PWM3_OUT	IO	General purpose	GPIO2[9]	B19
70	GPIO2_14	IO	General purpose	GPIO2[14]	B20
71	GPIO1_2	IO	General purpose	GPIO1[2]	T1
72	PWM2_OUT	IO	General purpose	GPIO1[1]	T4
73	GPIO2_11	IO	General purpose	GPIO2[11]	A20
74	NC		Leave not connected		
75	SPDIFIN	IO	SPDIF	GPIO3[21]	H20
76	GND	POWER	Digital GND		
77	SPDIFOUT	IO	SPDIF	GPIO3[22]	E23

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
78	GND	POWER	Digital GND		
79	USB_H1_OC	IO	USB host	GPIO3[30]	J20
80	CAN2_TX_OTG_OC	IO	FlexCAN-2	GPIO4[14]	T6
81	CSI0_HSYNCH	IO	Camera interface	GPIO5[19]	P4
82	CAN2_RX	IO	FlexCAN-2	GPIO4[15]	V5
83	UART1_RX	IO	UART1 port	GPIO5[29]	M3
84	UART1_RTS	IO	UART1 port	GPIO3[20]	G20
85	UART1_TX	IO	UART1 port	GPIO5[28]	M1
86	UART1_CTS	IO	UART1 port	GPIO3[19]	G21
87	I2C1_SDA	IO	I2C interface	GPIO5[26]	N6
88	I2C1_SCL	IO	I2C interface	GPIO5[27]	N5
89	GND	POWER	Digital GND		
90	I2C3_SDA	IO	I2C interface	GPIO7[11]	R2
91	SATA_RXN	DS	Serial ATA		A14
92	I2C3_SCL	IO	I2C interface	GPIO1[5]	R4
93	SATA_RXP	DS	Serial ATA		B14
94	USB_OTG_ID	IO	USB on-the-go [5]	GPIO1[4]	R6
95	GND	POWER	Digital GND		
96	CSI0_DAT19	IO	Camera interface	GPIO6[5]	L6
97	SATA_TXP	DS	Serial ATA		A12
98	POR_B	I O	iMX6 Power on Reset Input signal, [4] PMIC Reset open drain output signal		C11, PMIC.3
99	SATA_TXN	DS	Serial ATA		B12
100	CLK1_N	DS	PCIE clock		C7
101	GND	POWER	Digital GND		
102	CLK1_P	DS	PCIE clock		D7
103	VIN_3V3	POWER	Main power supply		G15
104	USB_H1_VBUS	I	USB 2.0 5V indication		D10
105	VIN_3V3	POWER	Main power supply		G15
106	USB_OTG_VBUS	I	OTG 5V indication		E9
107	VIN_3V3	POWER	Main power supply		G15
108	USB_HOST_DN	DS	USB host		F10
109	VIN_3V3	POWER	Main power supply		G15
110	USB_HOST_DP	DS	USB host		E10
111	VIN_3V3	POWER	Main power supply		G15
112	GND	POWER	Digital GND		
113	CSI0_DAT18	IO	Camera interface	GPIO6[4]	M6
114	USB_OTG_DN	DS	USB on-the-go		B6
115	CSI0_DAT15	IO	Camera interface	GPIO6[1]	M5
116	USB_OTG_DP	DS	USB on-the-go		A6

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
117	CSI0_DAT17	IO	Camera interface	GPIO6[3]	L3
118	GND	POWER	Digital GND		
119	CSI_D0P	DS	Camera serial interface		E3
120	CSI0_VSYNC	IO	Camera interface	GPIO5[21]	N2
121	CSI_D0M	DS	Camera serial interface		E4
122	CSI0_DATA_EN	IO	Camera interface	GPIO5[20]	P3
123	CSI_D1M	DS	Camera serial interface		D1
124	CSI0_DAT12	IO	Camera interface	GPIO5[30]	M2
125	CSI_D1P	DS	Camera serial interface		D2
126	GND	POWER	Digital GND		
127	CSI_D2P	DS	Camera serial interface		E2
128	PCIE_TXM	DS	PCI express interface		A3
129	CSI_D2M	DS	Camera serial interface		E1
130	PCIE_TXP	DS	PCI express interface		B3
131	CSI_D3M	DS	Camera serial interface		F2
132	GND	POWER	Digital GND		
133	CSI_D3P	DS	Camera serial interface		F1
134	PCIE_RXP	DS	PCI express interface		B2
135	CSI_CLK0P	DS	Camera serial interface		F3
136	PCIE_RXM	DS	PCI express interface		B1
137	CSI_CLK0M	DS	Camera serial interface		F4
138	GND	POWER	Digital GND		
139	GND	POWER	Digital GND		
140	DSI_CLK0P	DS	Display serial interface		H4
141	DSI_D0M	DS	Display serial Interface		G2
142	DSI_CLK0M	DS	Display serial interface		H3
143	DSI_D0P	DS	Display serial interface		G1
144	GND	POWER	Digital GND		
145	DSI_D1M	DS	Display serial interface		H2
146	HDMI_D1P	DS	HDMI		J4
147	DSI_D1P	DS	Display serial interface		H1
148	HDMI_D1M	DS	HDMI		J3
149	GND	POWER	Digital GND		
150	HDMI_CLKM	DS	HDMI		J5
151	HDMI_D2P	DS	HDMI		K4
152	HDMI_CLKP	DS	HDMI		J6
153	HDMI_D2M	DS	HDMI		K3
154	HDMI_HPD	DS	HDMI		K1
155	HDMI_D0P	DS	HDMI		K6
156	HDMI_DDCCEC	IO	HDMI		K2

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
157	HDMI_D0M	DS	HDMI		K5
158	GND	POWER	Digital GND		
159	GND	POWER	Digital GND		
160	LVDS0_TX1_N	DS	LVDS display bridge		U4
161	LVDS0_TX0_N	DS	LVDS display bridge		U2
162	LVDS0_TX1_P	DS	LVDS display bridge		U3
163	LVDS0_TX0_P	DS	LVDS display bridge		U1
164	LVDS0_TX2_N	DS	LVDS display bridge		V2
165	LVDS0_TX3_N	DS	LVDS display bridge		W2
166	LVDS0_TX2_P	DS	LVDS display bridge		V1
167	LVDS0_TX3_P	DS	LVDS display bridge		W1
168	LVDS0_CLK_N	DS	LVDS display bridge		V4
169	GND	POWER	Digital GND		
170	LVDS0_CLK_P	DS	LVDS display bridge		V3
171	CSI0_DAT14	IO	Camera interface	GPIO6[0]	M4
172	GND	POWER	Digital GND		
173	CSI0_DAT16	IO	Camera interface	GPIO6[2]	L4
174	I2C2_SCL	IO	I2C interface[1]		U5
175	CSI0_DAT13	IO	Camera interface	GPIO5[31]	L1
176	I2C2_SDA	IO	I2C interface[1]		T7
177	CSI0_PIXCLK	I	Camera interface	GPIO5[18]	P1
178	GND	POWER	Digital GND		
179	GND	POWER	Digital GND		
180	LVDS1_CLK_N	DS	LVDS display bridge		Y3
181	LVDS1_TX3_P	DS	LVDS display bridge		AA4
182	LVDS1_CLK_P	DS	LVDS display bridge		Y4
183	LVDS1_TX3_N	DS	LVDS display bridge		AA3
184	LVDS1_TX0_N	DS	LVDS display bridge		Y1
185	GND	POWER	Digital GND		
186	LVDS1_TX0_P	DS	LVDS display bridge		Y2
187	TS_X-	AI	Touch screen interface		
188	LVDS1_TX1_N	DS	LVDS display bridge		AA1
189	TS_X+	AI	Touch screen interface		
190	LVDS1_TX1_P	DS	LVDS display bridge		AA2
191	TS_Y+	AI	Touch screen interface		
192	LVDS1_TX2_N	DS	LVDS display bridge		AB1
193	TS_Y-	AI	Touch screen interface		
194	LVDS1_TX2_P	DS	LVDS display bridge		AB2
195	AGND	POWER	Audio GND		
196	AGND	POWER	Audio GND		

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
197	LINEIN1_LP	AI			
198	HPLOUT	AO			
199	LINEIN1_RP	AI			
200	HPROUT	AO			

Notes:

[1] I2C2 Interface is used on-som. Pin mode can't be changed.

[2] UART2 interface is used for on SOM Bluetooth connectivity. Interface cannot be used if using Bluetooth. UART2 Pins marked with * are shared with WiFi/Bluetooth module. Pins can't be used and mode can't be altered if the WiFi/Bluetooth module is assembled.

[3] UART3 RTS pin is being latched at boot to determine boot sequence. Use with OE# buffer, and enable only after SOM is powered-up. Use reference schematics as example.

[4] A Delay should be added on POR_B to ensure POR_B is released after SOM voltage rails have stabilized. Use a voltage supervisor, see reference schematics.

[5] The VAR-MX6Customboard schematics design supports either Client or Host mode but not OTG functionality. 'USB_OTG_ID' naming of pin 94 follows the VAR-MX6Customboard schematics design naming, however, this SoC ball does not have the alternate function of USB_OTG_ID required for OTG implementation.
For implementing full native OTG functionality SoC 'USB_OTG_ID' and 'USB_OTG_PWR' alternate functions should be utilized. Please see sections 3.2, 4.7 for pin mux options And VAR-SOLOCustomBoard schematics for implementation.

3.2. SO-DIMM 200 Pin Mux

The table below summarizes the additional available functionality for each pin-in SO-DIMM 200 connector.

PIN	ball	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
16	V21		ENET_TX_EN	ESAI_TX3_RX2			GPIO1[28]		
17	T25	IPU1_DISP0_DAT[9]	IPU2_DISP0_DAT[9]	PWM2_PWMO	WDOG2_WDOG_B		GPIO4[30]		
21	W24	IPU1_DISP0_DAT[23]	IPU2_DISP0_DAT[23]	ECSPI1_SS0	AUDMUX_AUD4_RXD		GPIO5[17]		
22	U23	IPU1_DISP0_DAT[19]	IPU2_DISP0_DAT[19]	ECSPI2_SCLK	AUDMUX_AUD5_RXD	AUDMUX_AUD4_RXC	GPIO5[13]		WEIM_CS[3]
23	V25	IPU1_DISP0_DAT[18]	IPU2_DISP0_DAT[18]	ECSPI2_SS0	AUDMUX_AUD5_TXFS	AUDMUX_AUD4_RXFS	GPIO5[12]		WEIM_CS[2]
24	V24	IPU1_DISP0_DAT[22]	IPU2_DISP0_DAT[22]	ECSPI1_MISO	AUDMUX_AUD4_TXFS		GPIO5[16]		
25	U22	IPU1_DISP0_DAT[20]	IPU2_DISP0_DAT[20]	ECSPI1_SCLK	AUDMUX_AUD4_TXC		GPIO5[14]		
26	T20	IPU1_DISP0_DAT[21]	IPU2_DISP0_DAT[21]	ECSPI1_MOSI	AUDMUX_AUD4_TXD		GPIO5[15]		
39	U6	ECSPI1_SS0	ENET_COL	AUDMUX_AUD5_RXD	KPP_ROW[1]	UART5_RXD_MUX	GPIO4[9]	USDHC2_VSELECT	
40	L23	WEIM_DA_A[5]	IPU1_DISP1_DATA04	IPU2_CSI1_DATA04			GPIO3[5]		SRC_BOOT_CFG05
41	U7	ECSPI1_MISO	ENET_MDIO	AUDMUX_AUD5_TXFS	KPP_COL[1]	UART5_TXD_MUX	GPIO4[8]	USDHC1_VSELECT	
42	L25	WEIM_DA_A[7]	IPU1_DISP1_DATA02	IPU2_CSI1_DATA02			GPIO3[7]		SRC_BT_CFG[07]
43	W5	ECSPI1_SCLK	ENET_RDATA[3]	AUDMUX_AUD5_TXC	KPP_COL[0]	UART4_TXD_MUX	GPIO4[6]	DCIC1_DCIC_OUT	
44	R3	ESAI_TX4_RX1	ECSPI5_RDY	EPIT1_EPITO	CAN1_TXCAN	UART2_TXD_MUX	GPIO1[7]	SPDIF_PLOCK	USBOH3_OTGUSB_HOST_MODE
45	V6	ECSPI1_MOSI	ENET_TDATA[3]	AUDMUX_AUD5_TXD	KPP_ROW[0]	UART4_RXD_MUX	GPIO4[7]	DCIC2_DCIC_OUT	
46	R5	ESAI_TX5_RX0	ANATOP_ANATOP_32K_OUT	EPIT2_EPITO	CAN1_RXCAN	UART2_RXD_MUX	GPIO1[8]	SPDIF_SRCLK	USBOH3_OTGUSB_PWRCTL_WAKEUP
48	W6	ECSPI1_SS1	ENET_RDATA[2]	CAN1_TXCAN	KPP_COL[2]	ENET_MDC	GPIO4[10]	USBOH3_H1USB_PWRCTL_WAKEUP	
50	G23	WEIM_D[28]	I2C1_SDA	ECSPI4_MOSI	IPU2_CSI1_D[12]	UART2_CTS	GPIO3[28]	IPU1_EXT_TRIG	IPU1_DI0_PIN13
51	J19	WEIM_D[29]	IPU1_DI1_PIN15	ECSPI4_SS0		UART2_RTS	GPIO3[29]	IPU2_CSI1_VSYNC	IPU1_DI0_PIN14
52	E24	WEIM_D[26]	IPU1_DI1_PIN11	IPU1_CSI0_D[1]	IPU2_CSI1_D[14]	UART2_TXD_MUX	GPIO3[26]	IPU1_SISG[2]	IPU1_DISP1_DATA22

PIN	ball	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
53	E25	WEIM_D[27]	IPU1_DI1_PIN13	IPU1_CSI0_D[0]	IPU2_CSI1_D[13]	UART2_RXD_MUX	GPIO3[27]	IPU1_SISG[3]	IPU1_DISP1_DATA23
54	G22	WEIM_D[25]	ECSPI4_SS3	UART3_RXD_MUX	ECSPI1_SS3	ECSPI2_SS3	GPIO3[25]	AUDMUX_AUD5_RXC	UART1_DSR
55	D25	WEIM_D[23]	IPU1_DI0_D0_CS	UART3_CTS	UART1_DCD	IPU2_CSI1_DATA_EN	GPIO3[23]	IPU1_DI1_PIN2	IPU1_DI1_PIN14
56	F22	WEIM_EB[24]	ECSPI4_SS2	UART3_TXD_MUX	ECSPI1_SS2	ECSPI2_SS2	GPIO3[24]	AUDMUX_AUD5_RXFS	UART1_DTR
57	F23	WEIM_EB[3]	ECSPI4_RDY	UART3_RTS	UART1_RI	IPU2_CSI1_HSYNC	GPIO2[31]	IPU1_DI1_PIN3	SRC_BT_CFG[31]
60	C21	USDHC2_CLK	ecspi5_ECSPI5_SCLK	KPP_COL[5]	AUDMUX_AUD4_RXFS		GPIO1[10]		
61	A23	USDHC2_DAT2	ECSPI5_SS1	WEIM_CS[3]	AUDMUX_AUD4_TXD	KPP_ROW[6]	GPIO1[13]		
62	A22	USDHC2_DAT0	ECSPI5_MISO		AUDMUX_AUD4_RXD	KPP_ROW[7]	GPIO1[15]	DCIC2_DCIC_OUT	
63	E20	USDHC2_DAT1	ECSPI5_SS0	WEIM_CS[2]	AUDMUX_AUD4_TXFS	KPP_COL[7]	GPIO1[14]		
64	F19	USDHC2_CMD	ECSPI5_MOSI	KPP_ROW[5]	AUDMUX_AUD4_RXC		GPIO1[11]		
65	B22	USDHC2_DAT3	ECSPI5_SS3		AUDMUX_AUD4_TXC		GPIO1[12]		
68	T2	ESAI_RX_FS	WDOG1_B	KPP_COL[6]	CCM_REF_EN_B	PWM1_OUT	GPIO1[9]	USDHC1_WP	
69	B19		USDHC4_DAT1	PWM3_OUT			GPIO2[9]		
70	B20		USDHC4_DAT6	UART2_CTS_B			GPIO2[14]		
71	T1	ESAI_TX_FS		KPP_ROW[6]			GPIO1[2]	USDHC2_WP	MLB_DATA
72	T4	ESAI_RX_CLK	WDOG2_B	KPP_ROW[5]	USB_OTG_ID	PWM2_OUT	GPIO1[1]	USDHC1_CD_B	
73	A20		USDHC4_DAT3				GPIO2[11]		
75	H20	WEIM_D[21]	ECSPI4_SCLK	IPU1_DI0_PIN17	IPU2_CSI1_D[11]	USBOH3_USBOTG_OC	GPIO3[21]	I2C1_SCL	SPDIF_IN1
77	E23	WEIM_D[22]	ECSPI4_MISO	IPU1_DI0_PIN1	IPU2_CSI1_D[10]	USBOH3_USBOTG_PWR	GPIO3[22]	SPDIF_OUT1	
79	J20	WEIM_D[30]	IPU1_DISP1_DAT[21]	IPU1_DI0_PIN11	IPU1_CSI0_D[3]	UART3_CTS	GPIO3[30]	USBOH3_USBH1_OC	
80	T6	CAN2_TXCAN	IPU1_SISG[4]	USBOH3_USBOTG_OC	KPP_COL[4]	UART5_RTS	GPIO4[14]		
81	P4	IPU1_CSI0_HSYNC			CCM_CLKO		GPIO5[19]		CHEETAH_TRCTL
82	V5	CAN2_RXCAN	IPU1_SISG[5]	USBOH3_USBOTG_PWR	KPP_ROW[4]	UART5_CTS	GPIO4[15]		

PIN	ball	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
83	M3	IPU1_CSI0_D[11]	AUDMUX_AUD3_RXFS	ECSPI2_SS0	UART1_RXD_MUX		GPIO5[29]		CHEETAH_TRACE[8]
84	G20	WEIM_D[20]	ECSPI4_SS0	IPU1_DI0_PIN16	IPU2_CSI1_D[15]	UART1_RTS	GPIO3[20]	EPIT2_EPITO	
85	M1	IPU1_CSI0_D[10]	AUDMUX_AUD3_RXC	ECSPI2_MISO	UART1_TXD_MUX		GPIO5[28]		CHEETAH_TRACE[7]
86	G21	WEIM_D[19]	ECSPI1_SS1	IPU1_DI0_PIN8	IPU2_CSI1_D[16]	UART1_CTS	GPIO3[19]	EPIT1_EPITO	
87	N6	IPU1_CSI0_D[8]	WEIM_D[6]	ECSPI2_SCLK	KPP_COL[7]	I2C1_SDA	GPIO5[26]		CHEETAH_TRACE[5]
88	N5	IPU1_CSI0_D[9]	WEIM_D[7]	ECSPI2_MOSI	KPP_ROW[7]	I2C1_SCL	GPIO5[27]		CHEETAH_TRACE[6]
90	R2	ESAI_TX3_RX2	ENET_1588_EVENT2_IN	ENET_ANATOP_ETHERNET_REF_OUT	USDHC1_LCTL	SPDIF_IN1	GPIO7[11]	I2C3_SDA	SJC_DE_B
92	R4	ESAI_TX2_RX3		KPP_ROW[7]	CCM_CLKO		GPIO1[5]	I2C3_SCL	CHEETAH_EVENTI
94	R6	ESAI_TX_HF_CLK		KEY_COL7			GPIO1[4]	USDHC2_CD_B	
96	L6	IPU1_CSI0_D[19]	WEIM_D[15]		UART5_CTS		GPIO6[5]		
113	M6	IPU1_CSI0_D[18]	WEIM_D[14]		UART5_RTS		GPIO6[4]		CHEETAH_TRACE[15]
115	M5	IPU1_CSI0_D[15]	WEIM_D[11]		UART5_RXD_MUX		GPIO6[1]		CHEETAH_TRACE[12]
117	L3	IPU1_CSI0_D[17]	WEIM_D[13]		UART4_CTS		GPIO6[3]		CHEETAH_TRACE[14]
120	N2	IPU1_CSI0_VSYNC	WEIM_D[1]				GPIO5[21]		CHEETAH_TRACE[0]
122	P3	IPU1_CSI0_DATA_EN	WEIM_D[0]				GPIO5[20]		CHEETAH_TRCLK
124	M2	IPU1_CSI0_D[12]	WEIM_D[8]		UART4_TXD_MUX		GPIO5[30]		CHEETAH_TRACE[9]
171	M4	IPU1_CSI0_D[14]	WEIM_D[10]		UART5_TXD_MUX		GPIO6[0]		CHEETAH_TRACE[11]
173	L4	IPU1_CSI0_D[16]	WEIM_D[12]		UART4_RTS		GPIO6[2]		CHEETAH_TRACE[13]
174	U5	ECSPI1_SS3	ENET_CRS	HDMI_TX_DDC_SCL	KEY_COL3	I2C2_SCL	GPIO4[12]	SPDIF_IN	
175	L1	IPU1_CSI0_D[13]	WEIM_D[9]		UART4_RXD_MUX		GPIO5[31]		CHEETAH_TRACE[10]
176	T7		ASRC_EXT_CLK	HDMI_TX_DDC_SDA	KEY_ROW3	I2C2_SDA	GPIO4[13]	SD1_VSELECT	
177	P1	IPU1_CSI0_PIXCLOCK					GPIO5[18]		ARM_EVENTO

Note [1]: ECSPI5 Alternate function is available only on i.MX6 Quad/Dual SoC CPU variants

3.3. 40-pin FFC Connector Pin-out

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
1	JTAG_TDI	I	JTAG data-in		G5
2	EIM_A16	IO	WEIM A16 signal	GPIO2[22]	H25
3	JTAG_NTRST	I	JTAG reset		C2
4	JTAG_TMS	I	JTAG test mode select		C3
5	JTAG_TCK	O	JTAG test clock		H5
6	EIM_A17	IO	WEIM A17 signal	GPIO2[21]	G24
7	JTAG_TDO	O	JTAG data-out		G6
8	DGND	POWER	Digital GND		
9	EIM_WAIT	IO	WEIM wait signal	GPIO5[0]	M25
10	EIM_A18	IO	WEIM A18 signal	GPIO2[20]	J22
11	EIM_A24	IO	WEIM A24 signal	GPIO5[4]	F25
12	EIM_CS0	IO	WEIM CS0 signal	GPIO2[23]	H24
13	EIM_CS1	IO	WEIM CS1 signal	GPIO2[24]	J23
14	EIM_A22	IO	WEIM A22 signal	GPIO2[16]	F24
15	EIM_OE	IO	WEIM OE signal	GPIO2[25]	J24
16	EIM_EB1	IO	WEIM EB1 signal	GPIO2[29]	K23
17	EIM_DA3	IO	WEIM DA3 signal	GPIO3[3]	K24
18	EIM_DA6	IO	WEIM DA6 signal	GPIO3[6]	K25
19	EIM_DA1	IO	WEIM DA1 signal	GPIO3[10]	J25
20	EIM_A20	IO	WEIM A20 signal	GPIO2[18]	H22
21	EIM_DA5	IO	WEIM DA5 signal	GPIO3[5]	L23
22	EIM_DA7	IO	WEIM DA7 signal	GPIO3[7]	L25
23	EIM_DA8	IO	WEIM DA8 signal	GPIO3[8]	L24
24	EIM_A19	IO	WEIM A19 signal	GPIO2[19]	G25
25	EIM_LBA	IO	WEIM LBA signal	GPIO2[27]	K22
26	EIM_EB0	IO	WEIM EB0 signal	GPIO2[28]	K21
27	EIM_DA12	IO	WEIM DA12 signal	GPIO3[12]	M24
28	EIM_DA14	IO	WEIM DA14 signal	GPIO3[14]	N23
29	EIM_BCLK	IO	WEIM BCLK signal	GPIO6[31]	N22
30	EIM_DA0	IO	WEIM DA0 signal	GPIO3[0]	L20
31	EIM_DA15	IO	WEIM DA15 signal	GPIO3[15]	N24
32	EIM_DA2	IO	WEIM DA2 signal	GPIO3[2]	L21
33	EIM_DA9	IO	WEIM DA9 signal	GPIO3[9]	M21
34	EIM_DA4	IO	WEIM DA4 signal	GPIO3[4]	L22
35	EIM_DA10	IO	WEIM DA10 signal	GPIO3[10]	M22
36	DGND	POWER	Digital GND		
37	EIM_DA13	IO	WEIM DA13 signal	GPIO3[13]	M23
38	EIM_DA11	IO	WEIM DA11 signal	GPIO3[11]	M20

Pin #	Pin Name	Type	Pin Group	GPIO	i.MX6 Ball
39	EIM_A23	IO	WEIM A23 signal	GPIO6[6]	J21
40	EIM_RW	IO	WEIM RW signal	GPIO2[26]	K20

3.4. 40-pin FFC Mux

The table below summarizes the additional available functionality for each pin in the 40pin FFC connector.

Pin #	Ball	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
1	G5								
2	H25	EIM_ADDR16	IPU1_DI1_DISP_CLK	IPU2_CSI1_PIXCLK			GPIO2_IO22		SRC_BOOT_CFG16
3	C2								
4	C3								
5	H5								
6	G24	EIM_ADDR17	IPU1_DISP1_DATA12	IPU2_CSI1_DATA12			GPIO2_IO21		SRC_BOOT_CFG17
7	G6								
9	M25	EIM_WAIT	EIM_DTACK_B				GPIO5_IO00		SRC_BOOT_CFG25
10	J22	EIM_ADDR18	IPU1_DISP1_DATA13	IPU2_CSI1_DATA13			GPIO2_IO20		SRC_BOOT_CFG18
11	F25	EIM_ADDR24	IPU1_DISP1_DATA19	IPU2_CSI1_DATA19	IPU2_SISG2	IPU1_SISG2	GPIO5_IO04		SRC_BOOT_CFG24
12	H24	EIM_CS0	IPU1_DI1_PIN05	ECSPI2_SCLK			GPIO2_IO23		
13	J23	EIM_CS1	IPU1_DI1_PIN06	ECSPI2_MOSI			GPIO2_IO24		
14	F24	EIM_ADDR22	IPU1_DISP1_DATA17	IPU2_CSI1_DATA17			GPIO2_IO16		SRC_BOOT_CFG22
15	J24	EIM_OE	IPU1_DI1_PIN07	ECSPI2_MISO			GPIO2_IO25		
16	K23	EIM_EB1	IPU1_DISP1_DATA10	IPU2_CSI1_DATA10			GPIO2_IO29		SRC_BOOT_CFG28
17	K24	EIM_AD03	IPU1_DISP1_DATA06	IPU2_CSI1_DATA06			GPIO3_IO03		SRC_BOOT_CFG03
18	K25	EIM_AD06	IPU1_DISP1_DATA03	IPU2_CSI1_DATA03			GPIO3_IO06		SRC_BOOT_CFG06
19	J25	EIM_AD01	IPU1_DISP1_DATA08	IPU2_CSI1_DATA08			GPIO3_IO01		SRC_BOOT_CFG01
20	H22	EIM_ADDR20	IPU1_DISP1_DATA15	IPU2_CSI1_DATA15			GPIO2_IO18		SRC_BOOT_CFG20
21	L23	EIM_AD05	IPU1_DISP1_DATA04	IPU2_CSI1_DATA04			GPIO3_IO05		SRC_BOOT_CFG05
22	L25	EIM_AD07	IPU1_DISP1_DATA02	IPU2_CSI1_DATA02			GPIO3_IO07		SRC_BOOT_CFG07
23	L24	EIM_AD08	IPU1_DISP1_DATA01	IPU2_CSI1_DATA01			GPIO3_IO08		SRC_BOOT_CFG08
24	G25	EIM_ADDR19	IPU1_DISP1_DATA14	IPU2_CSI1_DATA14			GPIO2_IO19		SRC_BOOT_CFG19
25	K22	EIM_LBA	IPU1_DI1_PIN17	ECSPI2_SS1			GPIO2_IO27		SRC_BOOT_CFG26
26	K21	EIM_EB0	IPU1_DISP1_DATA11	IPU2_CSI1_DATA11		CCM_PMIC_READY	GPIO2_IO28		SRC_BOOT_CFG27
27	M24	EIM_AD12	IPU1_DI1_PIN03	IPU2_CSI1_VSYNC			GPIO3_IO12		SRC_BOOT_CFG12
28	N23	EIM_AD14	IPU1_DI1_D1_CS				GPIO3_IO14		SRC_BOOT_CFG14
29	N22	EIM_BCLK	IPU1_DI1_PIN16				GPIO6_IO31		
30	L20	EIM_AD00	IPU1_DISP1_DATA09	IPU2_CSI1_DATA09			GPIO3_IO00		SRC_BOOT_CFG00
31	N24	EIM_AD15	IPU1_DI1_PIN01	ipu1.IPU1_DI1_PIN04			GPIO3_IO15		SRC_BOOT_CFG15
32	L21	EIM_AD02	IPU1_DISP1_DATA07	IPU2_CSI1_DATA07			GPIO3_IO02		SRC_BOOT_CFG02

Pin #	Ball	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
33	M21	EIM_AD09	IPU1_DISP1_DATA00	IPU2_CSI1_DATA00			GPIO3_IO09		SRC_BOOT_CFG09
34	L22	EIM_AD04	IPU1_DISP1_DATA05	IPU2_CSI1_DATA05			GPIO3_IO04		SRC_BOOT_CFG04
35	M22	EIM_AD10	IPU1_DI1_PIN15	IPU2_CSI1_DATA_EN			GPIO3_IO10		SRC_BOOT_CFG10
37	M23	EIM_AD13	IPU1_DI1_D0_CS				GPIO3_IO13		SRC_BOOT_CFG13
38	M20	EIM_AD11	IPU1_DI1_PIN02	IPU2_CSI1_HSYNC			GPIO3_IO11		SRC_BOOT_CFG11
39	J21	EIM_ADDR23	IPU1_DISP1_DATA18	IPU2_CSI1_DATA18	IPU2_SISG3	IPU1_SISG3	GPIO6_IO06		SRC_BOOT_CFG23
40	K20	EIM_RW	IPU1_DI1_PIN08	ECSPI2_SS0			GPIO2_IO26		SRC_BOOT_CFG29

4. SOM's interfaces

4.1. Display Interfaces

4.1.1. Overview

The VAR-SOM-MX6 consists of the following display interfaces:

- Two LVDS channels, driven by the LDB; pixel clock up to 170 MHz
- One HDMI port (ver. 1.4) - driven by the HDMI transmitter: Pixel clock up to 266 MHz (gated by the IPU capabilities)
- One MIPI/DSI port - driven by the MIPI/DSI transmitter; two data lanes @ 1 GHz
- Each IPU has two display ports. Up to four external ports can be active at any given time (additional asynchronous data flows can be sent though the parallel ports and the MIPI/DSI port).

4.1.2 DSI

VAR-SOM-MX6 MIPI DSI Host Controller supports up to 2 D-PHY data lanes:

- Bidirectional communication and escape mode support through the data lane
- Programmable display resolutions, from 160 x 120(QQVGA) to 1024 x 768(XVGA)
- Multiple peripheral support capability, configurable virtual channels
- Video mode pixel formats, 16 bpp (5,6,5 RGB), 18 bpp (6,6,6,RGB) packed, 18 bpp (6,6,6,RGB) loosely, 24 bpp (8,8,8,RGB)

DSI signals:

Signal	Pin #	Type	Description
DSI_CLK0M	142	ODS	Negative DSI clock differential
DSI_CLK0P	140	ODS	Positive DSI clock differential
DSI_D0M	141	ODS	Negative DSI data 0 differential
DSI_D0P	143	ODS	Positive DSI data 0 differential
DSI_D1M	145	ODS	Negative DSI data 1 differential
DSI_D1P	147	ODS	Positive DSI data 1 differential

4.1.3 HDMI

The HDMI module provides an HDMI standard interface port to an HDMI 1.4 compliant display

HDMI Signals:

Signal	Pin #	Type	Description
HDMI_CLKM	150	ODS	Negative HDMI clock differential
HDMI_CLKP	152	ODS	Positive HDMI clock differential
HDMI_D0M	157	ODS	Negative HDMI data 0 differential

HDMI_D0P	155	ODS	Positive HDMI data 0 differential
HDMI_D1M	148	ODS	Negative HDMI data 1 differential
HDMI_D1P	146	ODS	Positive HDMI data 1 differential
HDMI_D2M	153	ODS	Negative HDMI data 2 differential
HDMI_D2P	151	ODS	Positive HDMI data 2 differential
HDMI_DDCCEC	156	IO	One wire bidirectional CEC
HDMI_HPD	154	I	Hot plug detect

4.1.4 LVDS Interface

LVDS Display Bridge (LDB) will be used to connect the IPU (Image Processing Unit) to the External LVDS display interface.
There are 2 LVDS channels. These outputs are used to communicate RGB data and controls to external LCD displays.
The LVDS ports may be used as follows:

- Single channel output
- Dual channel output (one input source, two channel outputs for two displays)
- Split channel output (one input source, split to two channels on output)
- Separate two channel output (two input sources from IPU)

LVDS0 Signals:

Signal	Pin #	Type	Description
LVDS0_TX0_N	161	ODS	Negative data 0 differential
LVDS0_TX0_P	163	ODS	Positive data 0 differential
LVDS0_TX1_N	160	ODS	Negative data 1 differential
LVDS0_TX1_P	162	ODS	Positive data 1 differential
LVDS0_TX2_N	164	ODS	Negative data 2 differential
LVDS0_TX2_P	166	ODS	Positive data 2 differential
LVDS0_TX3_N	165	ODS	Negative data 3 differential
LVDS0_TX3_P	167	ODS	Positive data 3 differential
LVDS0_CLK_N	168	ODS	Negative clock differential
LVDS0_CLK_P	170	ODS	Positive clock differential

Table 4-1 LVDS Signals

LVDS1 Signals:

Signal	Pin #	Type	Description
LVDS1_TX0_N	184	ODS	Negative data 0 differential
LVDS1_TX0_P	186	ODS	Positive data 0 differential
LVDS1_TX1_N	188	ODS	Negative data 1 differential
LVDS1_TX1_P	190	ODS	Positive data 1 differential
LVDS1_TX2_N	192	ODS	Negative data 2 differential
LVDS1_TX2_P	194	ODS	Positive data 2 differential
LVDS1_TX3_N	183	ODS	Negative data 3 differential
LVDS1_TX3_P	181	ODS	Positive data 3 differential
LVDS1_CLK_N	180	ODS	Negative clock differential
LVDS1_CLK_P	182	ODS	Positive clock differential

4.2. Touch Panel

The VAR-SOM-MX6 features a 4-wire resistive touch panel interface:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

Touch-screen Controller Signals:

Signal	Pin #	Type	Description
TS_X-	187	AI	Touch screen X minus
TS_Y-	193	AI	Touch screen Y minus
TS_X+	189	AI	Touch screen X plus
TS_Y+	191	AI	Touch screen Y plus

4.3. Camera Interfaces

4.3.1. MIPI CSI-2

The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between the system and the MIPI D-PHY, allowing communication with an MIPI CSI-2 compliant camera sensor.

The MIPI CSI-2 host controller supports the following features:

- Compliance with MIPI Alliance standard for camera serial interface 2 (CSI-2), version 1.00 29th November, 2005
- Optional support for Camera Control Interface (CCI) through the use of DesignWare Core (DW_apb_i2c)
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, version 1.00.00 14th May, 2009
- Supports up to 4 D-PHY Rx data lanes
- Dynamically configurable multi-lane merging
- Long and short packet decoding
- Timing accurate signaling of frame and line synchronization packets
- Support for several frame formats such as:
  - General frame or digital interlaced video with or without accurate sync timing
  - Data type (packet or frame level) and virtual channel interleaving
- 32-bit image data interface delivering data formatted as recommended in CSI-2 specification
- Supports all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types
  - Error detection and correction:
    - PHY level
    - Packet level
    - Line level

- Frame level

MIPI CSI-2 signals:

Signal	Pin #	Type	Description
CSI_CLK0M	137	IDS	Negative CSI-2 clock differential
CSI_CLK0P	135	IDS	Positive CSI-2 clock differential
CSI_D0M	121	IDS	Negative CSI-2 data 0 differential
CSI_D0P	119	IDS	Positive CSI-2 data 0 differential
CSI_D1M	123	IDS	Negative CSI-2 data 1 differential
CSI_D1P	125	IDS	Positive CSI-2 data 1 differential
CSI_D2M	129	IDS	Negative CSI-2 data 2 differential
CSI_D2P	127	IDS	Positive CSI-2 data 2 differential
CSI_D3M	131	IDS	Negative CSI-2 data 3 differential
CSI_D3P	133	IDS	Positive CSI-2 data 3 differential

4.3.2. Parallel CSIx

Based on i.MX6 IPU, the VAR-SOM-MX6 supports two camera ports - each controlled by a CSI sub-block, providing a connection to image sensors and related devices.

CSI0 can implement 12bit CSI interface.

CSI0 Signals on 200 pin SO-DIMM connector:

Signal	Pin #	Type	Description
CSI0_DAT8	87	IO	Camera data line
CSI0_DAT9	88	IO	Camera data line
CSI0_DAT10	85	IO	Camera data line
CSI0_DAT11	83	IO	Camera data line
CSI0_DAT12	124	IO	Camera data line
CSI0_DAT13	175	IO	Camera data line
CSI0_DAT14	171	IO	Camera data line
CSI0_DAT15	115	IO	Camera data line
CSI0_DAT16	173	IO	Camera data line
CSI0_DAT17	117	IO	Camera data line
CSI0_DAT18	113	IO	Camera data line
CSI0_DAT19	96	IO	Camera data line
CSI0_DATA_EN	122	IO	Camera data enable
CSI0_HSYNCH	81	IO	Camera horizontal sync
CSI0_PIXCLK	177	IO	Camera pixel clock
CSI0_VSYNC	120	IO	Camera vertical sync

CSI1 Signals:

CSI1 can implement 20bit CSI interface.

CSI1 Signals that are exposed by the 40-pin FFC connector

Signal	Pin #	Type	Description
IPU2.CSI1_D[0]	33	IO	Camera data 0 line
IPU2.CSI1_D[1]	23	IO	Camera data 1 line
IPU2.CSI1_D[2]	22	IO	Camera data 2 line
IPU2.CSI1_D[3]	18	IO	Camera data 3 line
IPU2.CSI1_D[4]	21	IO	Camera data 4 line
IPU2.CSI1_D[5]	34	IO	Camera data 5 line
IPU2.CSI1_D[6]	17	IO	Camera data 6 line
IPU2.CSI1_D[7]	32	IO	Camera data 7 line
IPU2.CSI1_D[8]	19	IO	Camera data 8 line
IPU2.CSI1_D[9]	30	IO	Camera data 9 line
IPU2.CSI1_D[10]	16	IO	Camera data 10 line
IPU2.CSI1_D[11]	26	IO	Camera data 11 line
IPU2.CSI1_D[12]	6	IO	Camera data 12 line
IPU2.CSI1_D[13]	10	IO	Camera data 13 line
IPU2.CSI1_D[14]	24	IO	Camera data 14 line
IPU2.CSI1_D[15]	20	IO	Camera data 15 line
IPU2.CSI1_D[17]	14	IO	Camera data 17 line
IPU2.CSI1_D[18]	39	IO	Camera data 18 line
IPU2.CSI1_D[19]	11	IO	Camera data 19 line
IPU2.CSI1_DATA_EN	35	IO	Camera data enable
IPU2.CSI1_HSYNC	38	IO	Camera horizontal sync
IPU2.CSI1_PIXCLK	2	IO	Camera pixel clock
IPU2.CSI1_VSYNC	27	IO	Camera vertical sync

CSI1 Signals that are exposed by the 200-pin connector

IPU2.CSI1_D[16]	86	IO	Camera data 16 line

4.4. Gigabit Ethernet

Gigabit Ethernet Features:

The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external Gigabit magnetics is required to complete the interface to the media. The i.MX6 processor also consists of HW assist for IEEE1588 standard. See the IEEE1588 section for more details.

Gigabit Ethernet Magnetics:

In order to utilize the VAR-SOM-MX6 Gigabit Ethernet interface, compatible magnetics should be used on the carrier board.

Vendor	Part Number	Package	Cores	Configuration
Pulse	H5007NL	Transformer	8	Auto-MDX
TDK	TLA-7T101LF	Transformer	8	Auto-MDX
Pulse	J0G-0009NL	Integrated RJ45	8	Auto-MDX

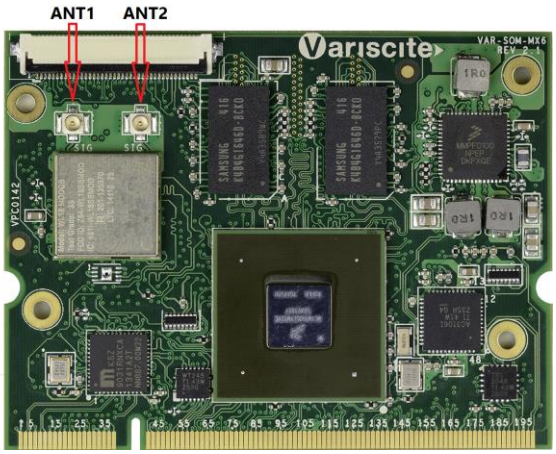
Gigabit Ethernet Signals:

Signal	Pin #	Type	Description
MDI_A+	3	DS	Positive A differential lane
MDI_A-	5	DS	Negative A differential lane
MDI_B+	9	DS	Positive B differential lane
MDI_B-	11	DS	Negative B differential lane
MDI_C+	4	DS	Positive C differential lane
MDI_C-	6	DS	Negative C differential lane
MDI_D+	10	DS	Positive D differential lane
MDI_D-	12	DS	Negative D differential lane

4.5. Wi-Fi & Bluetooth

The VAR-SOM-MX6 contains TI's WL183xMOD WiLink, a high performance 2.4/5 GHz IEEE 802.11 a/b/g/n Bluetooth 5.1/BLE with CSA2 support radio module, with optional Dual Band and MIMO support.
The modules support improved performance over WiFi in bit rates reaching 100Mbps (UDP) and 80Mbps (TCP).
The module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The module also provides a Bluetooth platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

- IEEE 802.11 b,g,n or Dual Band 2.4/5GHz 802.11 a/b/g/n with optional MIMO
- Bluetooth 5.1/BLE with CSA2 support
- U.FL connectors for external antennas
- Integrated band-pass filter
- Operating Temperature Range:
  Dual Band 2.4/5GHz Modules: -40 to +85
  2.4GHz Modules: -20 to +70



WL1831 – Populate ANT1 only

4.6. USB Host 2.0

The USB controller block provides high performance USB functionality that conforms to the USB 2.0 specification.

USB Host1 Signals:

Signal	Pin #	Type	Description
USB_HOST_DP	110	IODS	Positive USB host data
USB_HOST_DN	108	IODS	Negative USB host data
USB_H1_VBUS	104	I	USB 2.0 VBUS indicator (5V)
USB_H1_OC	79	I	USB host over current indicator , Active low 3.3v digital

4.7. USB 2.0 OTG

USB 2.0 On-the-go Features:

High-speed OTG core

- HS/FS/LS UTMI compliant interface
- High speed, full speed and low speed operation in host mode (with UTMI transceiver)
- High speed, and full speed operation in peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Up to 8 bidirectional endpoints
- Integrated HS USB PHY

OTG Signals:

Signal	Pin #	Type	Description
USB_OTG_DN	114	IODS	Negative USB OTG data
USB_OTG_DP	116	IODS	Positive USB OTG data
USB_OTG_VBUS	106	I	USB 2.0 OTG VBUS indicator (5V)
USB_OTG_ID	94	I	Low : Host mode Float: Client mode

Note:

The VAR-MX6Customboard schematics design supports either Client or Host mode but not OTG functionality. 'USB_OTG_ID' naming of pin 94 follows the VAR-MX6Customboard schematics design naming, however, this SoC ball does not have the alternate function of USB_OTG_ID required for OTG implementation.
For implementing full native OTG functionality SoC 'USB_OTG_ID' and 'USB_OTG_PWR' alternate functions should be utilized. Please see below for pin mux options and VAR-SOLOCustomBoard schematics for implementation.

Signal	Pin #	Type	Description
USB_OTG_ID	72	I	USB OTG host/client ID Low : Host mode Float: Client mode
USB_OTG_PWR	77, 82	O	USB OTG Port power enable

4.8. MMC/SD/SDIO

MX6 MMC interface features:

- Fully compliant with MMC command/response sets and physical layer as defined in the Multimedia Card System specification v4.2/4.3/4.4/.41, including high-capacity (size > 2 GB) cards HC MMC.
- Fully compliant with SD command/response sets and physical layer as defined in the SD Memory Card specifications v2.0, including high-capacity SDHC and extended-capacity SDXC cards.
- Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card specification, Part E1 v1.10
- Fully compliant with SD Card specification, Part A2, SD Host Controller Standard specification v2.00
- 1-bit or 4-bit transfer mode specifications for MMC/SD/SDIO cards up to HS mode (25MB/s max)

SDMMC2 Signals:

Signal	Pin #	Type	Description
SD2_CLK	60	O	Clock for MMC/SD/SDIO card
SD2_CMD	64	IO	CMD line connect to card
SD2_DATA0	62	IO	DAT0 line in all modes (also used to detect busy state)
SD2_DATA1	63	IO	DAT1 line-in
SD2_DATA2	61	IO	DAT2 line
SD2_DATA3	65	IO	DAT3 line-in

4.9. Audio

The VAR-SOM-MX6 features three audio interfaces:

- TLV320AIC3106 Audio codec interfaces
    1. Analog outputs / inputs:
        - stereo line-in
        - Stereo HP out
    2. Digital microphone input
- SSI Digital audio interface
- S/PDIF in/out

Analog audio signals are featured by the on-SOM TLV320AIC3106 audio codec. Refer to the data sheet for detailed electrical characteristics of the relevant interfaces http://www.ti.com/product/tlv320aic3106.

Analog Signals:

Signal	Pin #	Type	Description
HP_LOUT	198	AO	Headphones out - left
HP_ROUT	200	AO	Headphones out - right
LINEIN1_LP	197	AI	Line-in - Right
LINEIN1_RP	199	AI	Line-in - Left

Digital AUDMUX:

Key features of the block include:

- Full 6-wire SSI interfaces for asynchronous receive and transmit
- Configurable 4-wire (synchronous) or 6-wire (asynchronous) peripheral interfaces
- Independent Tx/Rx frame sync and clock direction selection for host or peripheral
- Each host interface's capability to connect to any other host or peripheral interface in a point-to-point or point-to-multipoint (network mode)
- Transmit and receive data switching to support external network mode

AUDMUX4 Signals:

Signal	Pin #	Type	Description
AUDMUX4_TXD	26	IO	Transmit data from pin
AUDMUX4_RXD	21	IO	Receive data at pin
AUDMUX4_TXC	25	IO	Transmit clock input/output at pin
AUDMUX4_RXC	22	IO	Receive clock input/output at pin
AUDMUX4_TXFS	24	IO	Transmit frame sync input/output at pin
AUDMUX4_RXFS	23	IO	Receive frame sync input/output at pin

S/PDIF (Sony Phillips Digital Interface) In/Out:

S/PDIF is a standard audio file transfer format, developed jointly by the Sony and Phillips corporations.

SPIDF Signals:

Signal	Pin #	Type	Description
SPDIFIN	75		In
SPDIFOUT	77		Out

Spdif.plock	44(MUXED)		
Spdif.srclk	46(MUXED)		Clock

4.10. UART Interfaces

All 5 UART interfaces are supported, refer to Table 3.2 for pin mux configurations of the UART interface.

UART Features:

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection)
- 7 or 8 data bits for RS-232 characters, or 9 bit RS-485 format
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
- RS-485 driver direction control via CTS_B signal
- Auto baud rate detection (up to 115.2 Kbit/s)
- DCE/DTE capability
- Two independent, 32-entry FIFOs for transmit and receive

UART1 Signals:

Signal	Pin #	Type	Description
UART1_CTS	86	O	UART HW flow control RTS
UART1_RTS	84	I	UART HW flow control CTS
UART1_TX	85	O	UART transmit
UART1_RX	83	I	UART receive

Note: UART1 is used as default boot debug port.

UART2 Signals:

Signal	Pin #	Type	Description
UART2_TXD	44 52	O	UART transmit
UART2_RXD	46 53	I	UART receive
UART2_RTS	51*	I	UART HW flow control RTS
UART2_CTS	50* 70	O	UART HW flow control CTS

Note:
UART2 is used for by on SOM Bluetooth. Interface cannot be used if using Bluetooth.
Pins marked with * are shared with WiFi/Bluetooth module. Pins can't be used and mode can't be altered if the WiFi/Bluetooth module is assembled.

UART3 Signals:

Signal	Pin #	Type	Description
UART3_TXD	56	O	UART transmit
UART3_RXD	54	I	UART receive
UART3_RTS[1]	57	I	UART HW flow control RTS

UART3_CTS	55 79	O	UART HW flow control CTS

[1] UART3 RTS pin is being latched at boot to determine boot sequence. Use with OE# buffer, and enable only after SOM is powered-up. Use reference schematics as example.

UART4 Signals:

Signal	Pin #	Type	Description
UART4_TXD	43 124	O	UART transmit
UART4_RXD	45 175	I	UART receive
UART4_RTS	173	I	UART HW flow control RTS
UART4_CTS	117	O	UART HW flow control CTS

UART5 Signals:

Signal	Pin #	Type	Description
UART5_TXD	41 171	O	UART transmit
UART5_RXD	39 115	I	UART receive
UART5_RTS	80 113	I	UART HW flow control RTS
UART5_CTS	82 96	O	UART HW flow control CTS

4.11. Flexible Controller Area Network (FLEXCAN)

The CAN protocol was primarily, but not exclusively, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: Real-time processing, reliable operation in the Electromagnetic Interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, version 2.0 B, which supports both standard and extended message frames.

CAN1 Signals:

Signal	Pin #	Type	Description
CAN1_RX	46	I	CAN BUS receive
CAN1_TX	44	O	CAN BUS transmit

CAN2 Signals:

Signal	Pin #	Type	Description
CAN2_TX	80	O	CAN BUS receive
CAN2_RX	82	I	CAN BUS transmit

Signal Descriptions
CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

4.12. SPI

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous 4-wire serial communication block. The ECSPI contains a 64 x 32 receive buffer (RXFIFO) and a 64 x 32 transmit buffer (TXFIFO). With data FIFOs, the ECSPI allows rapid data communication with fewer software interruptions.

4.12.1. eCSPI Key Features:

- Full-duplex synchronous serial interface
- Master/slave configurable
- Four chip select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmitting and receiving data
- 32-bit wide by 16-entry FIFO for HT message data
- Polarity and phase of the chip select (SS) and SPI clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Max operation frequency up to the reference clock frequency

ECSPI1 Signals:

Signal	Pin #	Type	Description
cSPI1_CLK	25, 43	IO	SPI1 clock
cSPI1_MOSI	26, 45	IO	SPI1 MOSI signal
cSPI1_MISO	24, 41	IO	SPI1 SOMI signal

cSPI1_CS0	39, 21	IO	SPI1 chip select 0 signal
cSPI1_CS1	48, 86	IO	SPI1 chip select 1 signal
cSPI1_CS2	56	IO	SPI1 chip select 2 signal
cSPI1_CS3	54, 174	IO	SPI1 chip select 3 signal

ECSPI2 Signals:

Signal	Pin #	Type	Description
cSPI2_CLK	22, 87	IO	SPI2 clock
cSPI2_MOSI	88	IO	SPI2 MOSI signal
cSPI2_MISO	85	IO	SPI2 SOMI signal
cSPI2_CS0	23, 83	IO	SPI2 Chip select 0 signal
cSPI2_CS2	56	IO	SPI2 Chip select 2 signal
cSPI2_CS3	54	IO	SPI2 Chip select 3 signal

ECSPI4 Signals:

Signal	Pin #	Type	Description
cSPI4_CLK	75	IO	SPI4 clock
cSPI4_MOSI	50	IO	SPI4 MOSI signal
cSPI4_MISO	77	IO	SPI4 SOMI signal
cSPI4_CS0	51, 84	IO	SPI4 Chip select 0 signal
cSPI4_CS2	56	IO	SPI4 Chip select 2 signal
cSPI4_CS3	54	IO	SPI4 Chip select 3 signal
cSPI4_RDY	57	IO	SPI4 ready signal

ECSPI5 Signals:

Signal	Pin #	Type	Description
cSPI5_CLK	60	IO	SPI5 clock
cSPI5_MOSI	64	IO	SPI5 MOSI signal
cSPI5_MISO	62	IO	SPI5 SOMI signal
cSPI5_CS0	63	IO	SPI5 Chip select 0 signal
cSPI5_CS1	61	IO	SPI5 Chip select 1 signal
cSPI5_CS3	65	IO	SPI5 Chip select 3 signal
cSPI5_RDY	44	IO	SPI5 ready signal

Note: ECSPI5 Alternate function is available only on i.MX6 Quad/Dual SoC CPU variants

4.13. PCIe

VAR-SOM-MX6 PCI Express functionality has the following parts:

PCI Express includes the following cores:

- PCI Express Dual Mode (DM) core
- PCI Express Root Complex (RC) core
- PCI Express Endpoint (EP) core

PCI Express 2.0 PHY:

- PCIe 2.0 PHY is a complete mixed-signal semiconductor intellectual property (IP) solution, designed for single-chip integration into computer applications
- The PCIe 2.0 PHY supports both the 5 Gbps data rate of the PCI Express Gen 2.0 specifications as well as being backwards compatible to the 2.5Gb/s Gen 1.1 specification

PCIE Signals:

Signal	Pin #	Type	Description
PCIE_TXP	130	DS	Positive PCI TX differential
PCIE_TXM	128	DS	Negative PCI TX differential
PCIE_RXP	134	DS	Positive PCI RX differential
PCIE_RXM	136	DS	Negative PCI RX differential
CLK1_P	102	DS	Positive PCI clock differential
CLK1_N	100	DS	Negative PCI clock differential

4.14. Serial ATA

VAR-SOM-MX6 includes an integrated Serial Advanced Technology Attachment (SATA) controller that is compatible with the Advanced Host Controller Interface (AHCI) specification.
The SATA Controller block (SATA) along with integrated physical link hardware (SATA PHY) provide one SATA port for the attachment of external SATA compliant storage devices.

SATA Signals:

Signal	Pin #	Type	Description
SATA_RXN	91	DS	Negative SATA RX differential
SATA_RXP	93	DS	Positive SATA RX differential
SATA_TXN	99	DS	Negative SATA TX differential
SATA_TXP	97	DS	Positive SATA TX differential

4.15. I²C

I2C-1, 2, 3 Interface connectivity peripherals provide serial interface for external devices. Data rates of up to 400 kbps are supported.

I2C1 Signals:

Signal	Pin #	Type	Description
I2C1_SCL	88,75	IO	I2C1 I²C clock, open drain
I2C1_SDA	87,50	IO	I2C1 I²C data, open drain

I2C2 Signals:

Signal	Pin #	Type	Description
I2C2_SCL	174	IO	I²C clock, open drain, internally PU
I2C2_SDA	176	IO	I²C data, open drain, internally PU

Note: I2C2 interface is used by PMIC, CODEC and EEPROM on-som devices (I2C ADDR =0x1B, 0x8, 0x56 & 0x57). Pin configuration for I2C2 signal can't be changed.

I2C3 Signals:

Signal	Pin #	Type	Description
I2C3_SCL	92	IO	I2C3 I²C clock, open drain
I2C3_SDA	90	IO	I2C3 I²C data, open drain

4.16. Local Bus

The EIM handles the interface to devices external to the chip, including generation of chip selects, clock and control for external peripherals and memory. It provides asynchronous access to devices with a SRAM-like interface and synchronous access to devices with Nor-Flash-like or PSRAM-like interfaces.
The local bus signals are split between two connectors: SODIMM 200 connector and 40-pin FFC connector.

Local Bus Signals on SODIMM Connector:

Signal	Pin #	Type	Description
WEIM_D[19]	86	IO	Local Bus D[19] signal
WEIM_D[20]	84	IO	Local Bus D[20] signal
WEIM_D[21]	75	IO	Local Bus D[21] signal
WEIM_D[22]	77	IO	Local Bus D[22] signal
WEIM_D[23]	55	IO	Local Bus D[23] signal
WEIM_D[26]	52	IO	Local Bus D[24] signal
WEIM_D[25]	54	IO	Local Bus D[25] signal
WEIM_D[27]	53	IO	Local Bus D[27] signal
WEIM_D[28]	50	IO	Local Bus D[28] signal
WEIM_D[29]	51	IO	Local Bus D[29] signal
WEIM_D[30]	79	IO	Local Bus D[30] signal
WEIM_DA_A[13]	40	IO	Local Bus DA[13] signal
WEIM_D[24]	56	IO	Local Bus EB[2] signal
WEIM_EB[3]	57	IO	Local Bus EB[3] signal
WEIM_D[8]	124	IO	Local Bus D[8] signal
WEIM_D[9]	175	IO	Local Bus D[9] signal
WEIM_D[10]	171	IO	Local Bus D[10] signal
WEIM_D[11]	115	IO	Local Bus D[11] signal
WEIM_D[12]	173	IO	Local Bus D[12] signal

Signal	Pin #	Type	Description
WEIM_D[13]	117	IO	Local Bus D[13] signal
WEIM_D[14]	113	IO	Local Bus D[14] signal
WEIM_D[15]	96	IO	Local Bus D[15] signal
WEIM_D[6]	87	IO	Local Bus D[6] signal
WEIM_D[7]	88	IO	Local Bus D[7] signal
WEIM_D[0]	122	IO	Local Bus D[0] signal
WEIM_D[1]	120	IO	Local Bus D[1] signal
WEIM_CS[2]	63	IO	Local Bus CS[2] signal
WEIM_CS[3]	61	IO	Local Bus CS[3] signal
WEIM_CS[2]	23	IO	Local Bus CS[2] signal
WEIM_CS[3]	22	IO	Local Bus CS[3] signal
WEIM_DA_A[7]	42	IO	Local Bus DA[7] signal
WEIM_DA_A[13]	37	IO	Local Bus DA[13] signal

Local Bus Signals 40 Pin FFC connector:

Signal	Pin #	Type	Description
WEIM_A[16]	2	IO	Local Bus A[16] signal
WEIM_A[17]	6	IO	Local Bus A[17] signal
WEIM_WAIT	9	IO	Local Bus Wait signal
WEIM_A[18]	10	IO	Local Bus A[18] signal
WEIM_A[24]	11	IO	Local Bus A[24] signal
WEIM_CS[0]	12	IO	Local Bus CS[0] signal
WEIM_CS[1]	13	IO	Local Bus CS[1] signal
WEIM_A[22]	14	IO	Local Bus A[22] signal
WEIM_OE	15	IO	Local Bus OE signal
WEIM_EB[1]	16	IO	Local Bus EB[1] signal
WEIM_DA_A[3]	17	IO	Local Bus DA[3] signal
WEIM_DA_A[6]	18	IO	Local Bus DA[6] signal
WEIM_DA_A[1]	19	IO	Local Bus DA[10] signal
WEIM_A[20]	20	IO	Local Bus A[20] signal
WEIM_DA_A[5]	21	IO	Local Bus DA[5] signal
WEIM_DA_A[8]	23	IO	Local Bus DA[8] signal
WEIM_A[19]	24	IO	Local Bus A[19] signal
WEIM_LBA	25	IO	Local Bus LBA signal
WEIM_EB[0]	26	IO	Local Bus EB[0] signal
WEIM_DA_A[12]	27	IO	Local Bus DA[12] signal
WEIM_DA_A[14]	28	IO	Local Bus DA[14] signal
WEIM_BCLK	29	IO	Local Bus BCLK signal
WEIM_DA_A[0]	30	IO	Local Bus DA[0] signal
WEIM_DA_A[15]	31	IO	Local Bus DA[15] signal
WEIM_DA_A[2]	32	IO	Local Bus DA[2] signal
WEIM_DA_A[9]	33	IO	Local Bus DA[9] signal
WEIM_DA_A[4]	34	IO	Local Bus DA[4] signal
WEIM_DA_A[10]	35	IO	Local Bus DA[10] signal
WEIM_DA_A[11]	38	IO	Local Bus DA[11] signal
WEIM_A[23]	39	IO	Local Bus A[23] signal
WEIM_RW	40	IO	Local Bus RW signal

4.17. JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals.

JTAG signals 40-pin FFC Connector:

Signal	Pin #	Type	Description
JTAG_TDI	1	I	JTAG data-in
JTAG_NTRST	3	I	JTAG reset
JTAG_TMS	4	I	JTAG test mode select
JTAG_TCK	5	O	JTAG test clock
JTAG_TDO	7	O	JTAG data-out

4.18. General Purpose IOs

Most of the SoM's IO pins can be used as GPIOs.
See Chapter 3, Table 3.1 and 3.2 for a complete SoM connectors signal list and GPIO multiplexing.

4.19. General System Control

4.19.1. Boot Options

Below you can find the MX6 boot options

8	7	6	5	4	3	2	1
BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG2_6	BT_CFG2_5	BT_CFG2_4	BT_CFG2_3
1XXX = NANDF Boot							
011X = MMC/eMMC Boot				X0 = 1-bit X1 = 4-bit 10 = 8-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
010X = SD/eSD Boot				X0 = 1-bit X1 = 4-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
0011 = Serial ROM (SPINOR) Boot							
0010 = SATA Boot							

The boot-select pin configures the boot sequence of the VAR-SOM-MX6:
BOOT_CFG = X1X00101

Pin Name	Pin Number	MX6 BOOT_CFG	Internally pulled
BOOT_SEL0	42	BT_CFG1_7	Pulled-up 10K
BOOT_SEL1	40	BT_CFG1_5	Pulled-down 10K

Use cases:
BOOT_SEL [1:0] = [0:1] => BOOT_CFG = 11000101 => NAND Boot
BOOT_SEL [1:0] = [0:0] => BOOT_CFG = 01000101 => SD2 boot, SD-Card, 4 bit bus
BOOT_SEL [1:0] = [1:0] => BOOT_CFG = 01100101 => SD2 boot, eMMC (external, on carrier board) ,4 bit bus
Note: boot from on-SOM eMMC is not possible

4.19.2. Reset

'0' logic will reset VAR-SOM-MX6.

A Delay should be added on POR_B to ensure POR_B is released after SOM voltage rails have stabilized. Use a voltage supervisor, see reference schematics.

4.19.3. Reference Clock Out

VAR-SOM-MX6 output clock (CLKO2) is controlled by the i.MX6 CCM module. Please refer to the i.MX6 user manual regarding the configuration option for this clock.

4.19.4. General System Control Signals

Signal	Pin #	Type	Description
CLKO	29	O	Clock out
BOOT_SEL0	42	I	Refer to section 4.19.1
BOOT_SEL1	40	I	Refer to section 4.19.1
POR_B	98	I O	iMX6 Power on Reset Input signal, PMIC Reset open drain output signal '0' logic will reset the system

4.20. Power

4.20.1. Power Supply

Signal	Pin #	Type	Description
VIN_3V3	32, 34, 36, 38, 103, 105, 107, 109, 111	Power In	VAR-SOM-OMX6 Single DC-IN Supply voltage. Voltage range: 3.3 +/- 5%

4.20.2. Ground

Signal	Pin #	Type	Description
GND	13, 14, 19, 27, 28, 31, 33, 35, 37, 47, 58, 59, 66, 67, 76, 78, 89, 95, 101, 112, 118, 126, 132, 138, 139, 144, 149, 158, 159, 169, 172, 178, 179, 185	Power	Digital ground
AGND	195,196	Power	Analog GND

5. Absolute Maximum Characteristics

Power Supply	Min	Max	Unit
Main Power Supply, DC-IN	-0.3	3.5	V

6. Operational Characteristics

6.1. Power supplies

	Min	Typical	Max	Unit
Main Power Supply, DC-IN	-5%	3.3	+5%	V

6.2. Power Consumption

CPU usage:

Task	SOM VBAT current draw in ma @3.3v
Suspend	17.2mA@3.7v (Only "L" revisions can be operated at 3.7V Contact support for further information)
Idle (~10% CPU) @ 400mhz	380mA
FHD Video playback	750mA
100% CPU Dhrystone test – Dual core	630mA
100% CPU Dhrystone test – Quad core	900mA
4 cores 100% utilization with graphics	1370mA

Additional peripherals:

Task	SOM VBAT current draw in ma @3.3v
WLAN transmission 2.4Ghz 802.11(b/g/n)	~(570-630)mA
WLAN transmission 5Ghz 802.11(a)	~640mA
Gbit Ethernet	~710mA

7. DC Electrical Characteristics

Parameter	Min	Typical	Max	Unit
Digital 3.3V				
V_{IH}	0.7x VIN_3V3		VIN_3V3	V
V_{IL}	0		0.3x VIN_3V3	V
V_{OH}	VIN_3V3- 0.15			V
V_{OL}			0.15	V

Table 7-1 DC Electrical Characteristics

8. Environmental Specifications

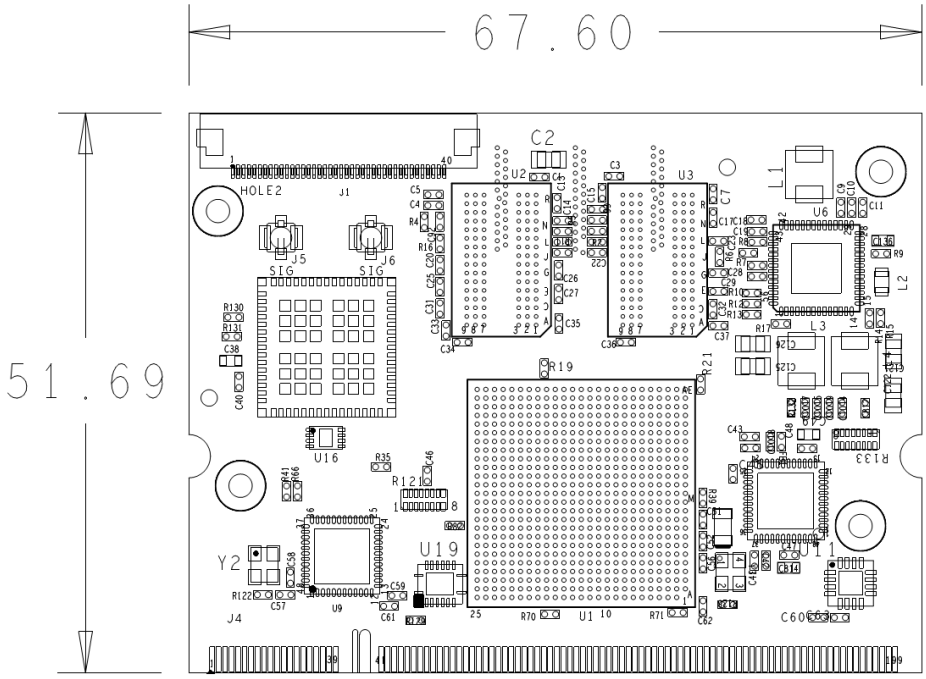
	Min	Max
Commercial Operating Temperature Range	0 ^{0}C	+70 ^{0}C
Extended Operating Temperature Range	-20 ^{0}C	+70 ^{0}C
Industrial Operating Temperature Range	-40 ^{0}C	+85 ^{0}C
Referring MIL-HDBK-217F-2 Parts Count Reliability Prediction Method Model: 25Deg Celsius, Class B-1, GM 25Deg Celsius, Class B-1, GB	 374 Khrs > 2668 Khrs >	

Notes:

1. Extended and Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.
2. The 1GHz Dual/Quad IT variants of the VAR-SOM-MX6 are based on the automotive grade of the i.MX6 processor. For detailed lifetime usage estimates of this processor, please refer to NXP application note # AN4724 http://www.nxp.com/assets/documents/data/en/application-notes/AN4724.pdf?fsrch=1&sr=1&pageNum=1.

9. Mechanical Drawings

Top View [mm



CAD files are available for download at http://www.variscite.com/

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