2-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Application

1 FEATURES

- **No Direction-Control**
- **Data Rates**
  24Mbps (Push-Pull)
  2Mbps (Open-Drain)
- **1.65V to 5.5V on A ports and 2.3V to 5.5V on B Ports (V_{CCA}≤V_{CCB})**
- **V_{CC} Isolation: If Either V_{CC} is at GND, Both Ports are in the High-Impedance State**
- **No Power-Supply Sequencing Required: Either V_{CCA} or V_{CCB} can be Ramped First**
- **I_{OFF}: Supports Partial-Power-Down Mode Operation**
- **ESD Protection Exceeds JESD 22**
  - **5000-V Human-Body Model**
  - **400-V Machine Model (A115)**
  - **1000-V Charged-Device Model (JS-002)**
- **Extended Temperature: -40°C to +85°C**

2 APPLICATIONS

- **I²C/ SMBus**
- **UART**
- **GPIO**

3 DESCRIPTIONS

This two-bit non-inverting translator is a bidirectional voltage-level translator and can be used to establish digital switching compatibility between mixed-voltage systems. It uses two separate configurable power-supply rails, with the A ports supporting operating voltages from 1.65V to 5.5V while it tracks the V_{CCA} supply, and the B ports supporting operating voltages from 2.3V to 5.5V while it tracks the V_{CCB} supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.8V, 2.5V, 3.3V and 5V voltage nodes.

When the output-enable (OE) input is low, all I/Os are placed in the high-impedance state, which significantly reduces the power-supply quiescent current consumption. OE has an internal pull-down current source, as long as V_{CCA} is powered.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

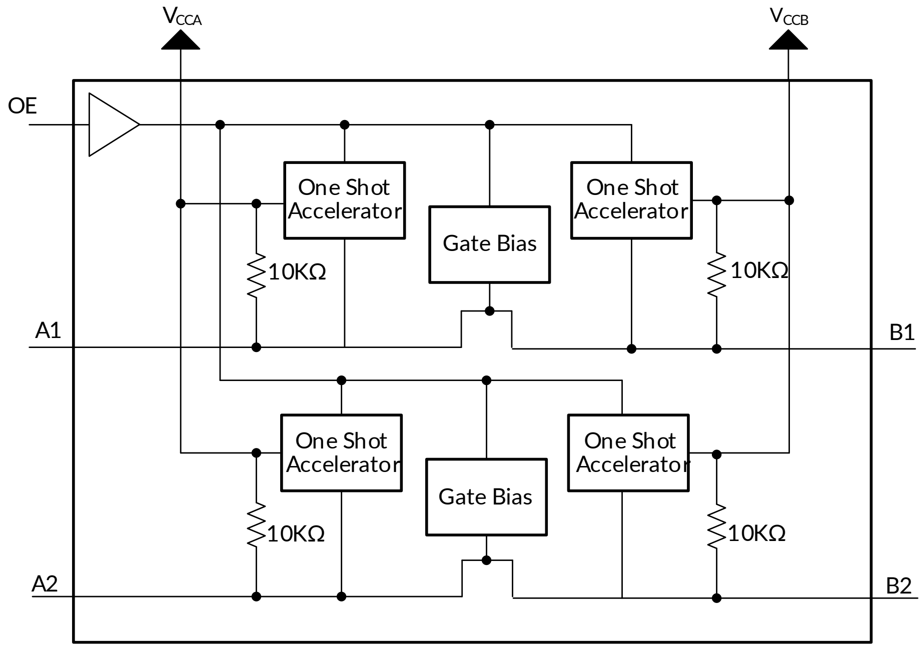
The RS0102 is available in Green SOT-23-8 packages. It operates over an ambient temperature range of -40°C to +85°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS0102	SOT23-8	2.92mm×1.60mm
	DFN1.4x1-8L	1.40mm×1.00mm
	VSSOP8	2.00mm×2.30mm
	DFN2x3-8L	2.00mm×3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Functional Block Diagram



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5 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

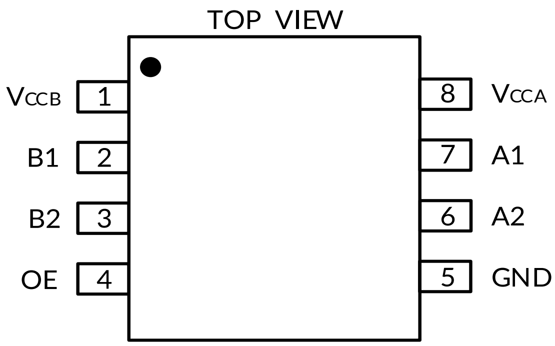
VERSION	Change Date	Change Item
A.1	2020/10/15	Initial version completed
A.2	2021/01/09	Add Moisture Sensitivity Level information Fix mistake in RS0102YVS8 PACKAGE value from 4000 to 3000
A.3	2021/08/16	Add “Typical Characteristics” Page 14
A.4	2021/11/01	1.Change Recommended Operating Conditions in Page 7@A.3Version. 2.Add TAPE AND REEL INFORMATION
A.5	2024/01/19	1.Update FEATURES on Page 1@RevA.4 2.Change the Voltage Waveforms Enable and Disable diagram in Page 18@ A.4 Version 3.Update Package thermal impedance and ESD Ratings on Page 4@RevA.4

6 PACKAGE/ORDERING INFORMATION (1)

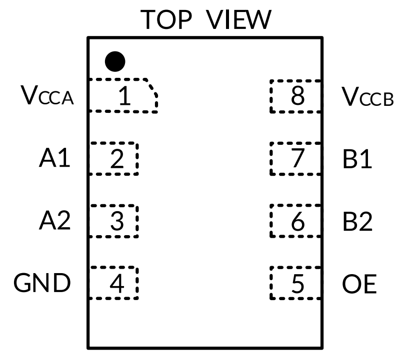
PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS0102	RS0102YH8	-40°C ~+85°C	SOT23-8	0102	MSL3	Tape and Reel,3000
	RS0102YUTDS8	-40°C ~+85°C	DFN1.4x1-8L	0102	MSL3	Tape and Reel,5000
	RS0102YVS8	-40°C ~+85°C	VSSOP8	0102	MSL3	Tape and Reel,3000
	RS0102YTDB8	-40°C ~+85°C	DFN2x3-8L	0102	MSL3	Tape and Reel,3000

NOTE:
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
(2) There may be additional marking, which relates to the lot trace code information(data code and vendor code)，the logo or the environmental category on the device.
(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

7 PIN CONFIGURATIONS



SOT-23-8



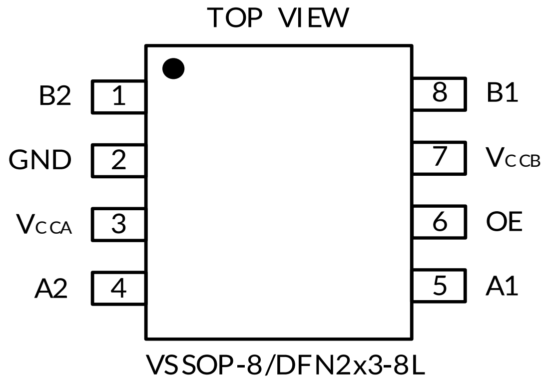
DFN-1.4X1-8L

PIN DESCRIPTION

PIN		NAME	TYPE [1]	FUNCTION
SOT-23-8	DFN-1.4X1-8L			
1	8	V_{CCB}	P	B Ports Supply Voltage.2.3V ≤ V_{CCB} ≤ 5.5V.
2	7	B1	I/O	Input/output B1. Reference to V_{CCB}.
3	6	B2	I/O	Input/output B2. Reference to V_{CCB}.
4	5	OE	I	Output Enable (Active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
5	4	GND	–	Ground.
6	3	A2	I/O	Input/output A2. Reference to V_{CCA}.
7	2	A1	I/O	Input/output A1. Reference to V_{CCA}.
8	1	V_{CCA}	P	A Port Supply Voltage.1.65V ≤ V_{CCA} ≤ 5.5V and V_{CCA} ≤ V_{CCB}.

(1) I=input, O=output, I/O=input and output, P=power.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	TYPE [1]	FUNCTION
VSSOP-8/DFN2×3-8L			
1	B2	I/O	Input/output B2. Reference to V_{CCB}.
2	GND	–	Ground.
3	V_{CCA}	P	A Port Supply Voltage.1.65V ≤ V_{CCA} ≤ 5.5V and V_{CCA} ≤ V_{CCB}
4	A2	I/O	Input/output A2. Reference to V_{CCA}.
5	A1	I/O	Input/output A1. Reference to V_{CCA}.
6	OE	I	Output Enable (Active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
7	V_{CCB}	P	B Ports Supply Voltage.2.3V ≤ V_{CCB} ≤ 5.5V.
8	B1	I/O	Input/output B1. Reference to V_{CCB}.

(1) I=input, O=output, I/O=input and output, P=power.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{CCA}	Supply Voltage Range		-0.3	6.0	V
V_{CCB}	Supply Voltage Range		-0.3	6.0	V
V_I (2)	Input Voltage Range	A port	-0.3	6.0	V
		B port	-0.3	6.0	
V_O (2)	Voltage range applied to any output in the high-impedance or power-off state	A port	-0.3	6.0	V
		B port	-0.3	6.0	
V_O (2)(3)	Voltage range applied to any output in the high or low state	A port	-0.3	V_{CCA}+0.3	V
		B port	-0.3	V_{CCB}+0.3	
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB} or GND			±100	mA
θ_{JA}	Package thermal impedance (4)	SOT23-8		184	°C/W
		DFN1.4x1-8L		199	
		VSSOP8		199	
		DFN2x3-8L		TBD	
T_J	Junction Temperature (5)		-40	150	°C
T_{stg}	Storage temperature		-65	+150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD-51.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±5000	V
		Charged-device model (CDM)	±1000	V
		Machine model (MM)	±400	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Supply voltage (1)	V_{CCA}		1.65		5.5	V
	V_{CCB}		2.3		5.5	
High-level input voltage (V_{IH})	A-port I/Os	V_{CCA} = 1.65 V to 1.95 V V_{CCB} = 2.3 V to 5.5 V	V_{CCI} – 0.2		V_{CCI}	V
		V_{CCA} = 2.3 V to 5.5 V V_{CCB} = 2.3 V to 5.5 V	V_{CCI} – 0.4		V_{CCI}	V
	B-port I/Os	V_{CCA} = 1.65 V to 5.5 V V_{CCB} = 2.3 V to 5.5 V	V_{CCI} – 0.4		V_{CCI}	V
	OE input	V_{CCA} = 1.65 V to 5.5 V V_{CCB} = 2.3 V to 5.5 V	V_{CCA} × 0.8		5.5	V
Low-level input voltage (V_{IL})	A-port I/Os	V_{CCA} = 1.65 V to 5.5 V V_{CCB} = 2.3 V to 5.5 V	0		0.15	V
	B-port I/Os	V_{CCA} = 1.65 V to 5.5 V V_{CCB} = 2.3 V to 5.5 V	0		0.15	V
	OE input	V_{CCA} = 1.65 V to 5.5 V V_{CCB} = 2.3 V to 5.5 V	0		V_{CCA} × 0.25	V
Input transition rise or fall rate(Δt/Δv)		A-port I/Os push-pull driving			10	ns/V
		B-port I/Os push-pull driving			10	ns/V
		Control input			10	ns/V
T_A Operating free-air temperature			-40		85	°C

(1) V_{CCA} must be less than or equal to V_{CCB}.

(2) The maximum V_{IL} value is provided to ensure that a valid V_{OL} is maintained. The V_{OL} value is V_{IL} plus the voltage drop across the pass gate transistor.

8.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1) (2) (3)

PARAMETER		CONDITIONS	V_{CCA}	V_{CCB}	TEMP	MIN(4)	TYP(5)	MAX(4)	UNITS
V_{OHA}	Port A output high voltage	I_{OH} = −20 µA $V_{IB} \geq V_{CCB}$ – 0.4V	1.65V to 5.5V	2.3V to 5.5V	Full	V_{CCA} × 0.7		5.5	V
V_{OLA}	Port A output low voltage	I_{OL} = 1mA $V_{IB} \leq$ 0.15 V	1.65V to 5.5V	2.3V to 5.5V	Full			0.3	
V_{OHB}	Port B output high voltage	I_{OH} = −20 µA $V_{IA} \geq V_{CCA}$ – 0.4 V	1.65V to 5.5V	2.3V to 5.5V	Full	V_{CCB} × 0.7			
V_{OLB}	Port B output low voltage	I_{OL} = 1mA $V_{IA} \leq$ 0.15 V	1.65V to 5.5V	2.3V to 5.5V	Full			0.3	
I_I	Input leakage current	OE	1.65V to 5.5V	2.3V to 5.5V	+25°C			±1	µA
					Full			±1.5	
I_{off}	Partial power down current	A Ports	0V	0V to 5.5V	+25°C			±0.5	µA
					Full			±1	
		B Ports	0V to 5.5V	0V	+25°C			±0.5	µA
					Full			±1	
I_{OZ}(6)	High-impedance State output current	A or B port OE=0V	1.65V to 5.5V	2.3V to 5.5V	+25°C			±0.5	µA
					Full			±1	
I_{CCA}	V_{CCA} supply current	$V_I = V_O$ = open I_O = 0	1.65V to V_{CCB}	2.3V to 5.5V	Full			2.5	µA
			5.5V	0V	Full			2.5	
			0V	5.5V	Full			-1	
I_{CCB}	V_{CCB} supply current	$V_I = V_O$ = open I_O = 0	1.65V to V_{CCB}	2.3V to 5.5V	Full			10	µA
			5.5V	0V	Full			-1	
			0V	5.5V	Full			1	
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_O$ = open I_O = 0	1.65V to V_{CCB}	2.3V to 5.5V	Full			13	µA
I_{CCZA}	V_{CCA} supply current	$V_I = V_{CCI}$ or 0V I_O = 0, OE=0V	1.65V to V_{CCB}	2.3V to 5.5V	Full			1	µA
I_{CCZB}	V_{CCB} supply current	$V_I = V_{CCI}$ or 0V I_O = 0, OE=0V	2.3V to 5.5V	2.3V to 5.5V	Full			1	µA
C_I	Input capacitance	OE	3.3V	3.3V	+25°C		2.5		pF
C_{IO}	Input-to-output internal capacitance	A port	3.3V	3.3V	+25°C		5		pF
		B port	3.3V	3.3V	+25°C		5		

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port
(3) V_{CCA} must be less than or equal to V_{CCB}.
(4) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(5) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(6) For I/O ports, the parameter I_{OZ} includes the input leakage current.

8.5 Timing Requirements

8.5.1 V_{CCA}=1.8V±0.15 V

		V_{CCB}=2.5V ±0.2V	V_{CCB}=3.3V ±0.2V	V_{CCB}=5V ±0.2V	UNIT
		TYP	TYP	TYP	
Data rate	Push-pull driving	21	22	24	Mbps
	Open-drain driving	2	2	2	
Pulse duration(t_w)	Push-pull driving (data inputs)	47	45	41	ns
	Open-drain driving (data inputs)	500	500	500	

8.5.2 V_{CCA}=2.5V±0.15 V

		V_{CCB}=2.5V ±0.2V	V_{CCB}=3.3V ±0.2V	V_{CCB}=5V ±0.2V	UNIT
		TYP	TYP	TYP	
Data rate	Push-pull driving	20	22	24	Mbps
	Open-drain driving	2	2	2	
Pulse duration(t_w)	Push-pull driving (data inputs)	50	45	41	ns
	Open-drain driving (data inputs)	500	500	500	

8.5.3 V_{CCA}=3.3V±0.15 V

		V_{CCB}=3.3V ±0.2V	V_{CCB}=5V ±0.2V	UNIT
		TYP	TYP	
Data rate	Push-pull driving	23	24	Mbps
	Open-drain driving	2	2	
Pulse duration(t_w)	Push-pull driving (data inputs)	43	41	ns
	Open-drain driving (data inputs)	500	500	

8.5.4 V_{CCA}=5V±0.15 V

		V_{CCB}=5V ±0.2V	UNIT
		TYP	
Data rate	Push-pull driving	24	Mbps
	Open-drain driving	2	
Pulse duration(t_w)	Push-pull driving (data inputs)	41	ns
	Open-drain driving (data inputs)	500	

8.6 Switching Characteristics: V_{CCA}=1.8V ± 0.15V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		V_{CCB}=2.5V±0.2V	V_{CCB}=3.3V±0.2V	V_{CCB}=5V±0.2V	UNITS
				TYP	TYP	TYP	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving	2.5	3.1	4.5	ns
			Open-drain driving	26.1	26.4	26.6	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving	4.2	3.7	3.6	ns
			Open-drain driving	221	183	143	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving	2.1	2.0	2.2	ns
			Open-drain driving	26.1	26.1	26.2	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving	1.8	1.6	1.5	ns
			Open-drain driving	173	89	66	
t_{en}	Enable time	OE-to-A or B		25	21	19	ns
t_{dis}	Disable time	OE-to-A or B		1250	1250	1250	ns
t_{rA}	Input rise time	A port rise time	Push-pull driving	6.9	6.1	5.6	ns
			Open-drain driving	118	39	13	
t_{rB}	Input rise time	B port rise time	Push-pull driving	5.8	4.8	4.1	ns
			Open-drain driving	166	127	75	
t_{fA}	Input fall time	A port fall time	Push-pull driving	3.0	2.8	2.7	ns
			Open-drain driving	1.9	1.7	1.6	
t_{fB}	Input fall time	B port fall time	Push-pull driving	4.8	6.2	8.4	ns
			Open-drain driving	2.3	2.4	2.8	
$t_{SK(O)}$	Skew(time), output	Channel-to-Channel Skew		0.5	0.5	0.5	ns
Maximum data rata		Push-pull driving		21	22	24	Mbps
		Open-drain driving		2	2	2	

8.7 Switching Characteristics: V_{CCA}=2.5V ± 0.15V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		V_{CCB}=2.5V±0.2V TYP	V_{CCB}=3.3V±0.2V TYP	V_{CCB}=5V±0.2V TYP	UNITS
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving	2.8	3.4	5.0	ns
			Open-drain driving	26.3	26.5	26.6	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving	2.7	2.5	2.4	ns
			Open-drain driving	198	169	131	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving	2.5	2.4	2.5	ns
			Open-drain driving	26.4	26.5	26.6	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving	2.1	2.0	1.9	ns
			Open-drain driving	196	138	63	
t_{en}	Enable time	OE-to-A or B		24	20	17	ns
t_{dis}	Disable time	OE-to-A or B		1250	1250	1250	ns
t_{rA}	Input rise time	A port rise time	Push-pull driving	3.4	2.9	2.7	ns
			Open-drain driving	156	92	13	
t_{rB}	Input rise time	B port rise time	Push-pull driving	4.7	3.5	2.7	ns
			Open-drain driving	160	124	81	
t_{fA}	Input fall time	A port fall time	Push-pull driving	5.1	5.2	5.0	ns
			Open-drain driving	2.1	2.0	1.8	
t_{fB}	Input fall time	B port fall time	Push-pull driving	5.0	6.4	8.7	ns
			Open-drain driving	2.0	2.2	2.8	
$t_{SK(O)}$	Skew(time), output	Channel-to-channel skew		0.5	0.5	0.5	ns
Maximum data rata		Push-pull driving		20	22	24	Mbps
		Open-drain driving		2	2	2	

8.8 Switching Characteristics: V_{CCA}=3.3V ± 0.3V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		V_{CCB}=3.3V±0.2V	V_{CCB}=5V±0.2V	UNITS
				TYP	TYP	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving	3.6	5.1	ns
			Open-drain driving	26.4	26.6	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving	2.3	2.1	ns
			Open-drain driving	155	109	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving	3.1	3.3	ns
			Open-drain driving	26.5	26.7	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving	1.9	1.8	ns
			Open-drain driving	158	87	
t_{en}	Enable time	OE-to-A or B		19	15	ns
t_{dis}	Disable time	OE-to-A or B		1250	1250	ns
t_{rA}	Input rise time	A port rise time	Push-pull driving	2.3	2.1	ns
			Open-drain driving	117	48	
t_{rB}	Input rise time	B port rise time	Push-pull driving	3.0	2.4	ns
			Open-drain driving	117	75	
t_{fA}	Input fall time	A port fall time	Push-pull driving	8.0	7.6	ns
			Open-drain driving	2.2	2.1	
t_{fB}	Input fall time	B port fall time	Push-pull driving	8.2	10.8	ns
			Open-drain driving	2.1	2.4	
$t_{SK(O)}$	Skew(time), output	Channel-to-channel skew		0.5	0.5	ns
Maximum data rata		Push-pull driving		23	24	Mbps
		Open-drain driving		2	2	

8.9 Switching Characteristics: V_{CCA}=5.0V ± 0.35V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		V_{CCB}=5V±0.2V TYP	UNITS
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving	5.6	ns
			Open-drain driving	26.8	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving	2.0	ns
			Open-drain driving	155	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving	5.8	ns
			Open-drain driving	27.5	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving	1.8	ns
			Open-drain driving	160	
t_{en}	Enable time	OE-to-A or B		17	ns
t_{dis}	Disable time	OE-to-A or B		1250	ns
t_{rA}	Input rise time	A port rise time	Push-pull driving	1.9	ns
			Open-drain driving	105	
t_{rB}	Input rise time	B port rise time	Push-pull driving	2.3	ns
			Open-drain driving	95	
t_{fA}	Input fall time	A port fall time	Push-pull driving	9.0	ns
			Open-drain driving	2.6	
t_{fB}	Input fall time	B port fall time	Push-pull driving	8.9	ns
			Open-drain driving	2.5	
$t_{SK(O)}$	Skew(time), output	Channel-to-channel skew		0.5	ns
Maximum data rata		Push-pull driving		24	Mbps
		Open-drain driving		2	

8.10 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

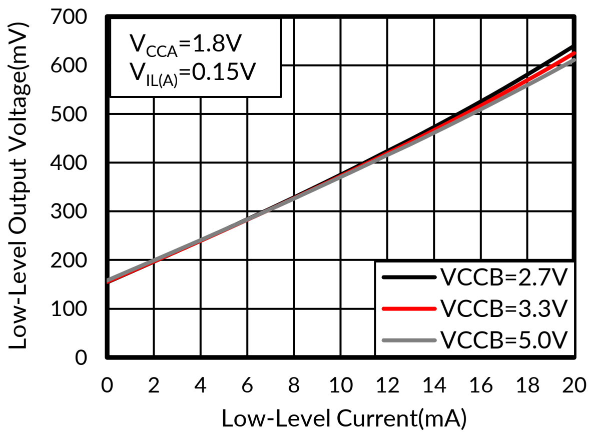


Figure1: Low-Level Output Voltage vs Low-Level Current

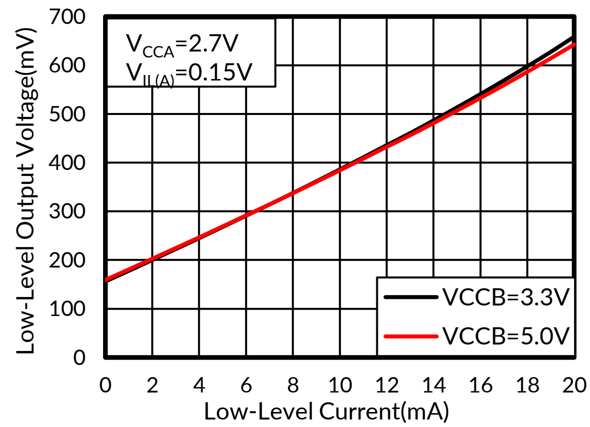


Figure2: Low-Level Output Voltage vs Low-Level Current

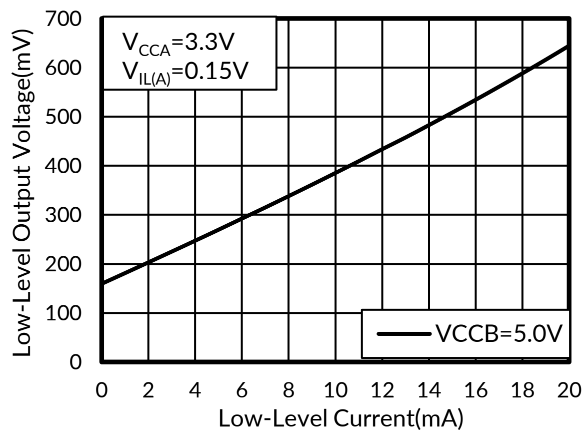


Figure3: Low-Level Output Voltage vs Low-Level Current

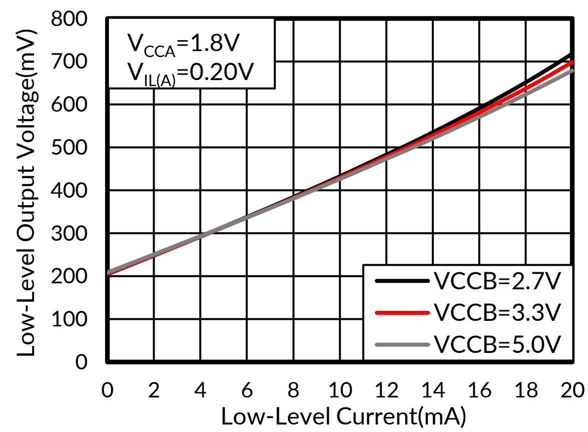


Figure4: Low-Level Output Voltage vs Low-Level Current

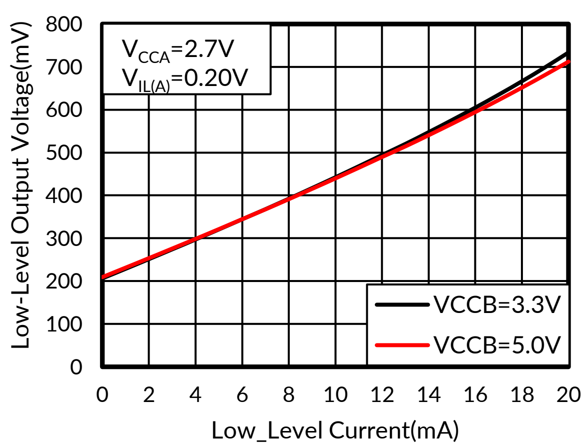


Figure5: Low-Level Output Voltage vs Low-Level Current

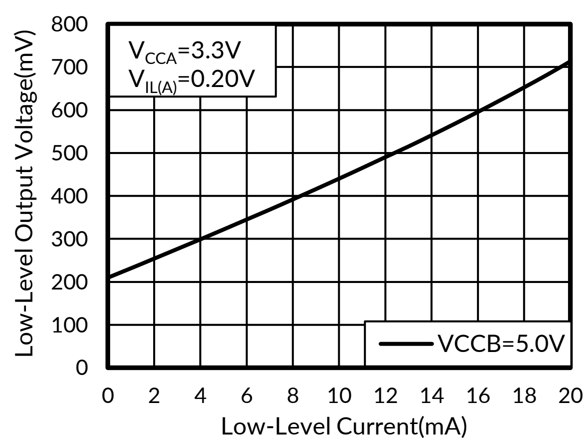


Figure6: Low-Level Output Voltage vs Low-Level Current

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

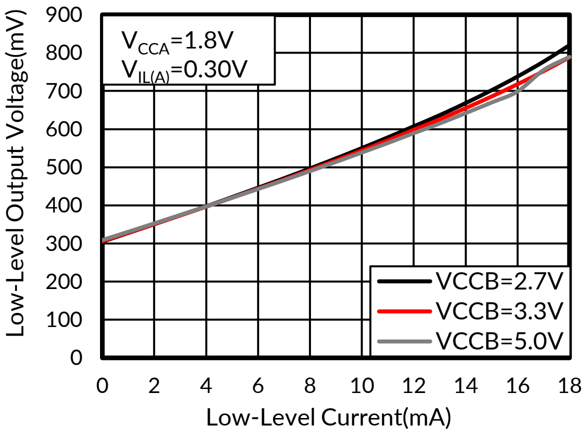


Figure7: Low-Level Output Voltage vs Low-Level Current

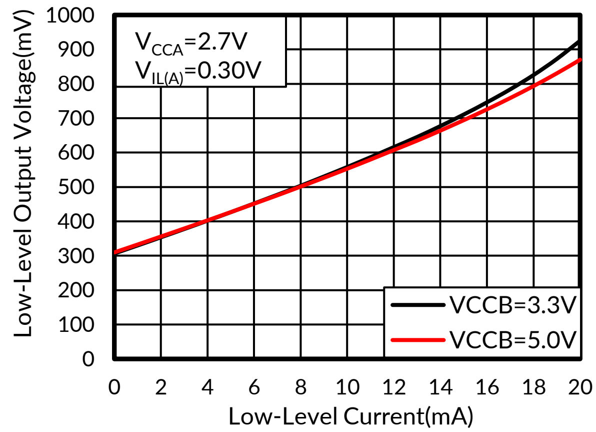


Figure8: Low-Level Output Voltage vs Low-Level Current

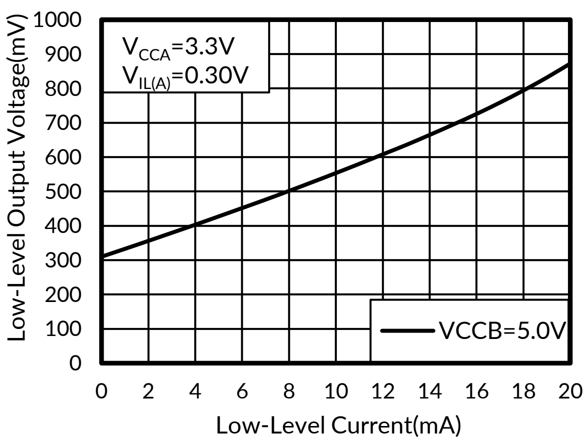


Figure9: Low-Level Output Voltage vs Low-Level Current

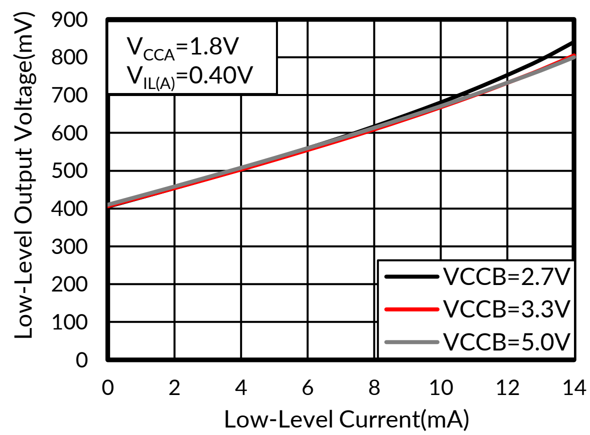


Figure10: Low-Level Output Voltage vs Low-Level Current

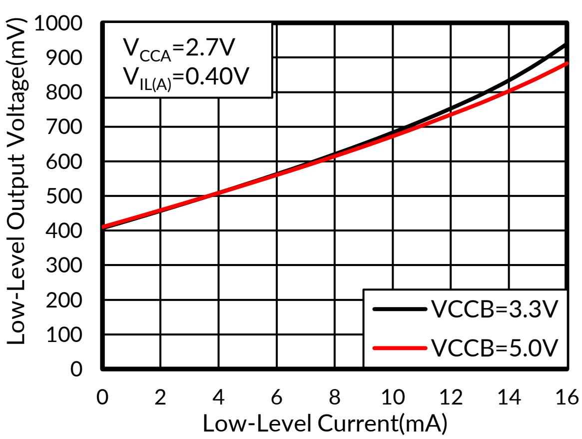


Figure11: Low-Level Output Voltage vs Low-Level Current

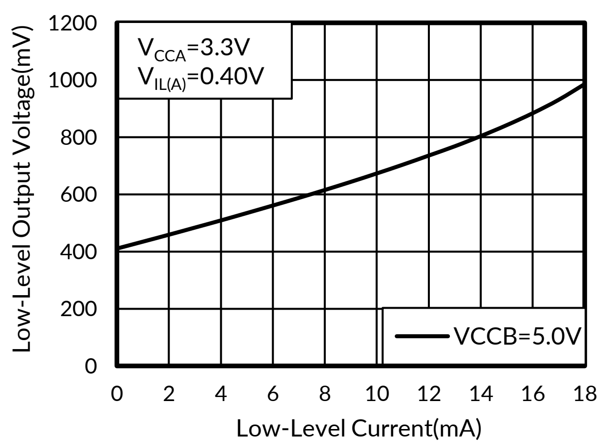


Figure12: Low-Level Output Voltage vs Low-Level Current

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

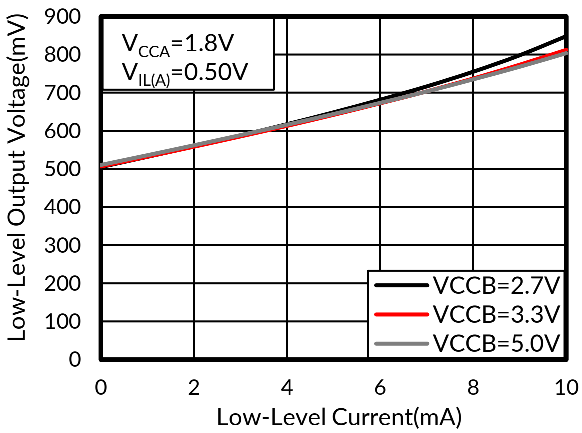


Figure13: Low-Level Output Voltage vs Low-Level Current

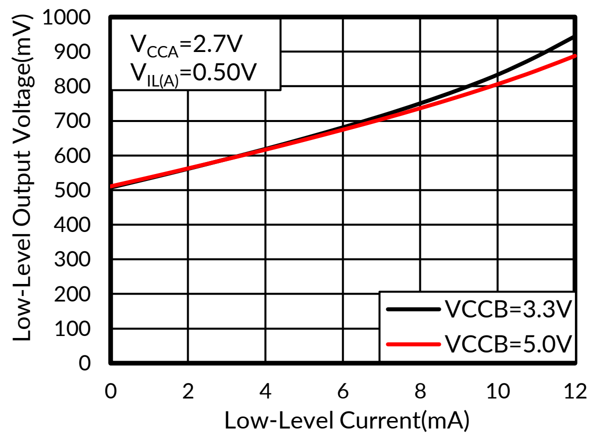


Figure14: Low-Level Output Voltage vs Low-Level Current

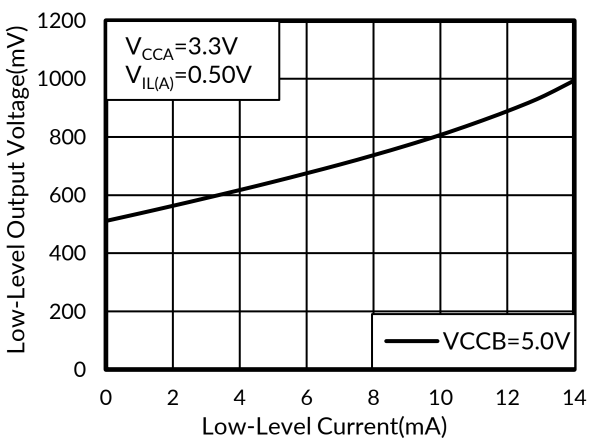


Figure15: Low-level Output Voltage vs Low-Level Current

9 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- PRR 10 MHz
- Z_O = 50 Ω
- dv/dt ≥ 1 V/ns

Note: All input pulses are measured one at a time, with one transition per measurement.

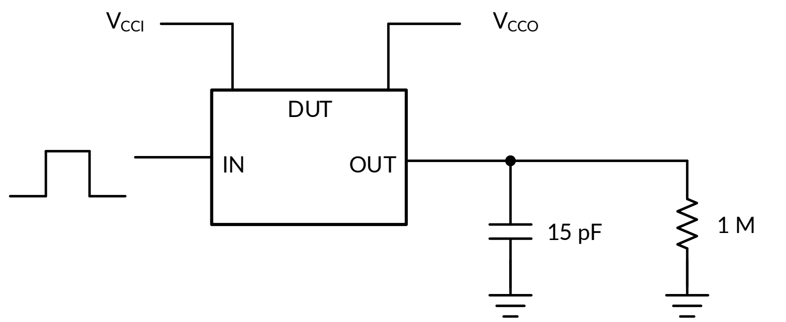


Figure 16. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using A Push-Pull Driver

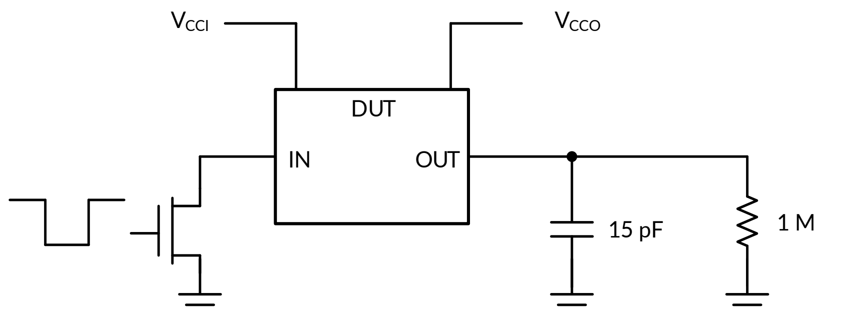


Figure 17. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using An Open-Drain Driver

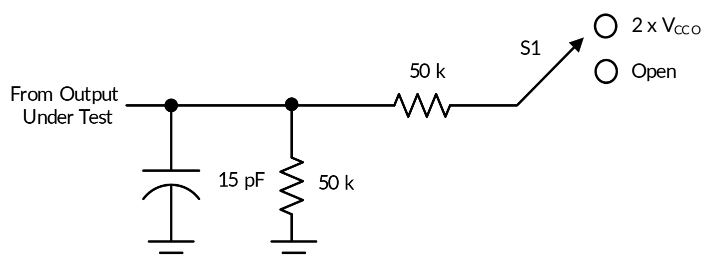
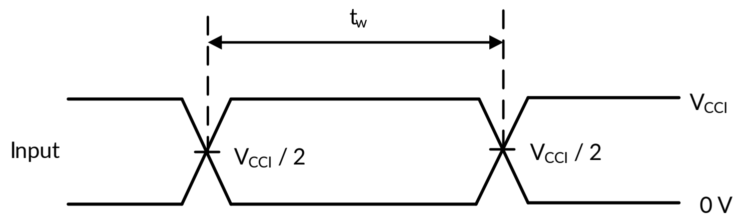


Figure 18. Load Circuit For Enable/Disable Time Measurement

Table 1. Switch Configuration For Enable/Disable Timing

TEST	S1
t_{PZL}(1), t_{PLZ}(2)	2 × V_{CCO}
t_{PHZL}(1), t_{PZH}(2)	Open

(1) t_{PZL} and t_{PZH} are the same as t_{en}.
(2) t_{PLZ} and t_{PHZ} are the same as t_{dis}.



(1) All input pulses are measured one at a time, with one transition per measurement.

Figure 19. Voltage Waveforms Pulse Duration

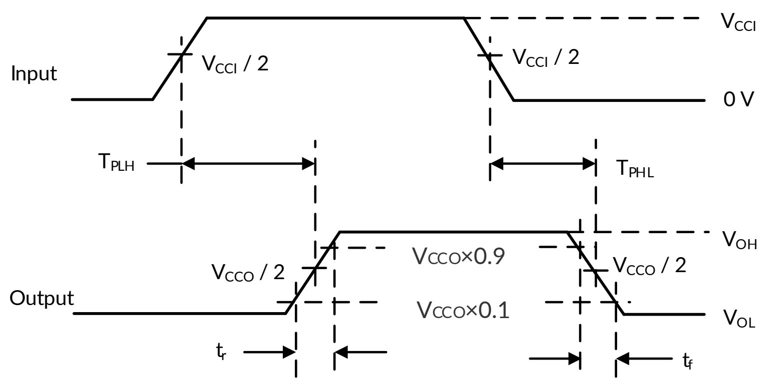
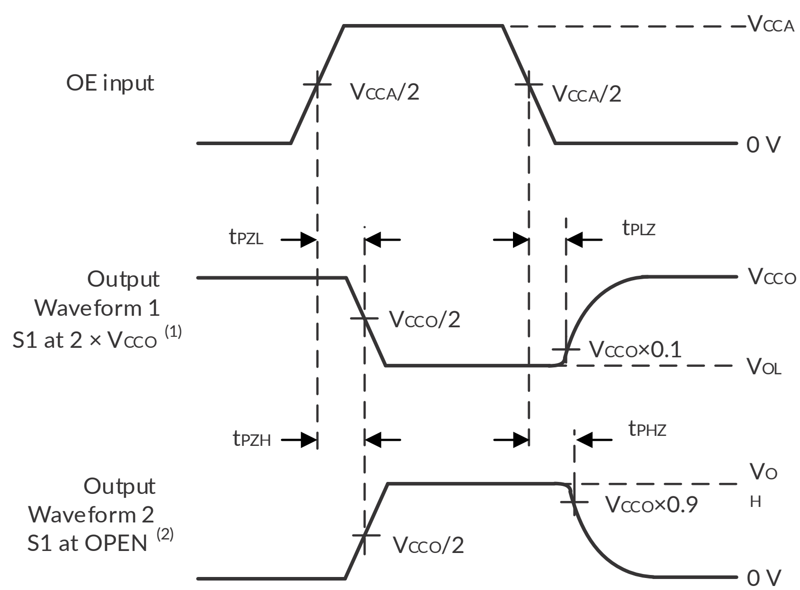


Figure 20. Voltage Waveforms Propagation Delay Times



A. Waveform 1 is for an output with internal such that the output is high, except when OE is high.
B. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Figure 21. Voltage Waveforms Enable and Disable

10 Feature Description

10.1 Overview

The RS0102 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.65 V to 5.5 V, while the B port can accept I/O voltages from 2.3 V to 5.5 V. The device is a pass-gate architecture with edge-rate accelerators (one-shots) to improve the overall data rate. 10-kΩ pullup resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

10.2 Architecture

The RS0102 architecture (see Figure 22) is an auto-direction-sensing based translator that does not require a direction-control signal to control the direction of data flow from A to B or from B to A. These two bidirectional channels independently determine the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

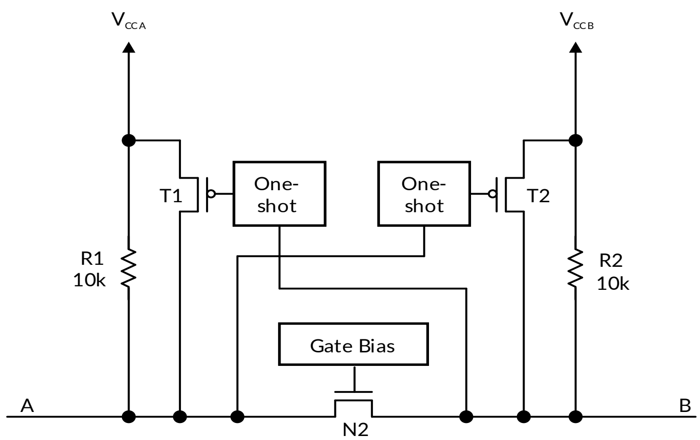


Figure 22. Architecture of a RS0102 Cell

The RS0102 employs two key circuits to enable this voltage translation:

1) An N-channel pass-gate transistor topology that ties the A-port to the B-port
2) Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B Ports.

10.3 Input Driver Requirements

The continuous dc-current "sinking" capability is determined by the external system-level open-drain (or push - pull) drivers that are interfaced to the RS0102 I/O pins. Since the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest dc-current "sourcing" capability of hundreds of micro-Amps, as determined by the internal 10-kΩ pullup resistors.

The fall time (t_{fA}, t_{fB}) of a signal depends on the edge-rate and output impedance of the external device driving RS0102 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the t_{PHL} and max data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL} and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω.

Feature Description

10.4 Output Load Considerations

We recommend careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths should be kept short enough such that the round-trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the RS0102 device output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

10.5 Enable and Disable

The RS0102 device has an OE input that is used to disable the device by setting OE low, which places all I/Os in the Hi-Z state. The disable time (t_{dis}) indicates the delay between the time when OE goes low and when the outputs are disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

10.6 Pullup or Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10-kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10-kΩ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10-kΩ resistors). Adding lower value pull-up resistors will affect V_{OL} levels, however. The internal pull-ups of the RS0102 are disabled when the OE pin is low.

11 Application and Implementation

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The RS0102 device can be used to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels found in electronic systems. It should be used in a point-to-point topology for interfacing devices or systems operating at different interface voltages with one another. Its primary target application use is for interfacing with open-drain drivers on the data I/Os such as I_2C or 1-wire, where the data is bidirectional and no control signal is available. The device can also be used in applications where a push-pull driver is connected to the data I/Os, but the RS0102 might be a better option for such push-pull applications.

11.2 Typical Application

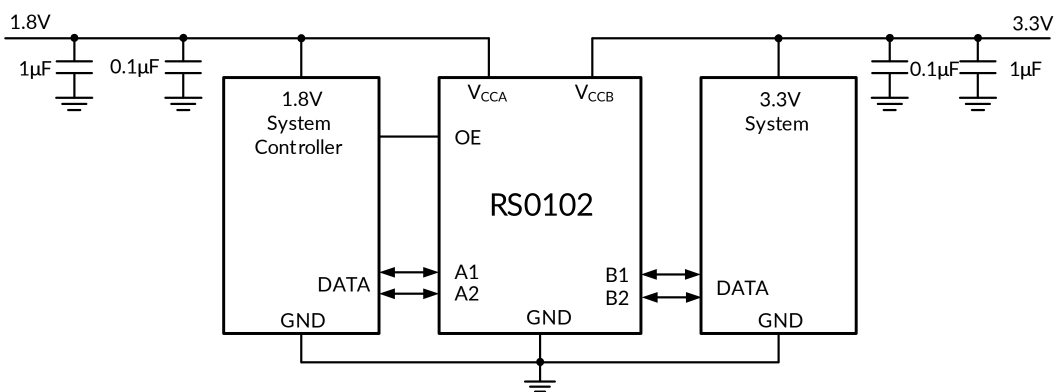
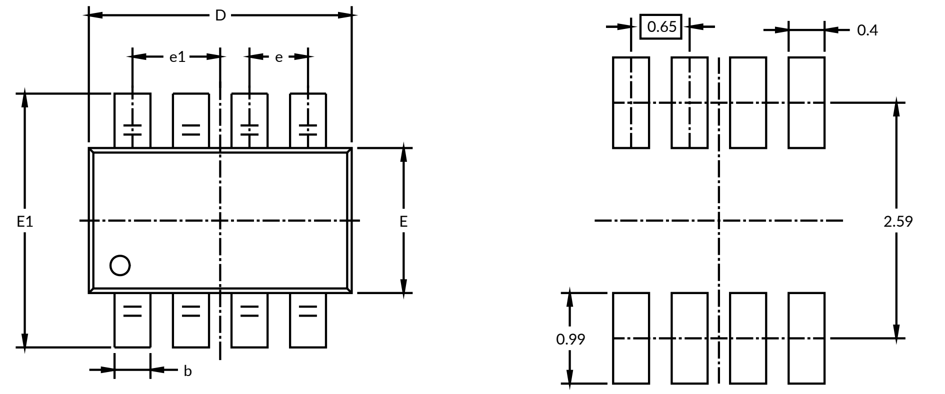


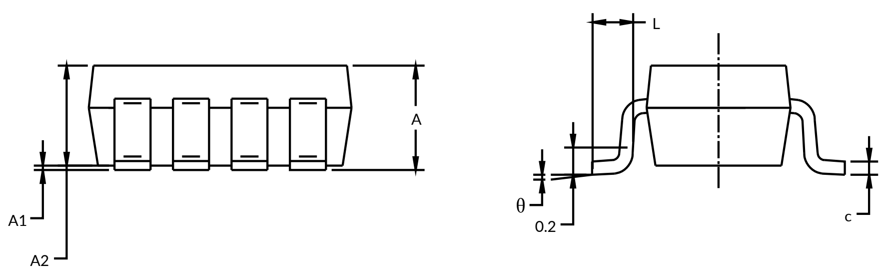
Figure 23. Typical Application Circuit

12 PACKAGE OUTLINE DIMENSIONS

SOT-23-8 (3)



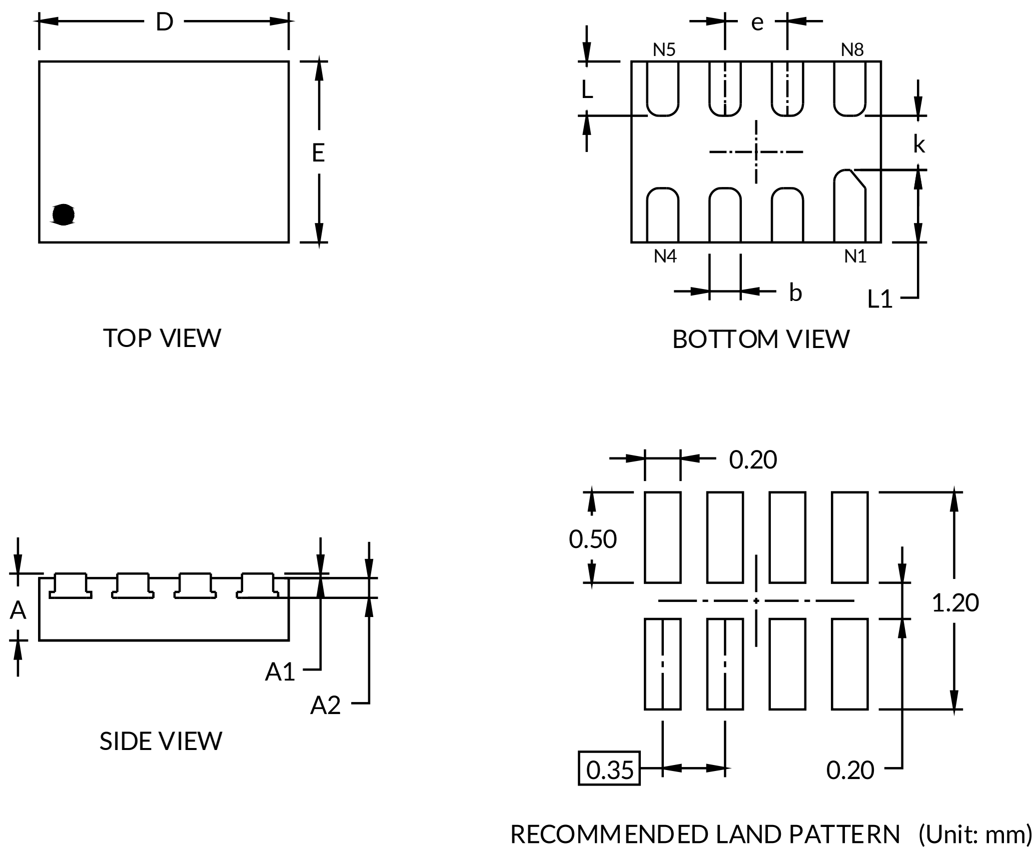
RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D (1)	2.820	3.020	0.111	0.119
E (1)	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.650(BSC) (2)		0.026(BSC) (2)	
e1	0.975(BSC) (2)		0.038(BSC) (2)	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

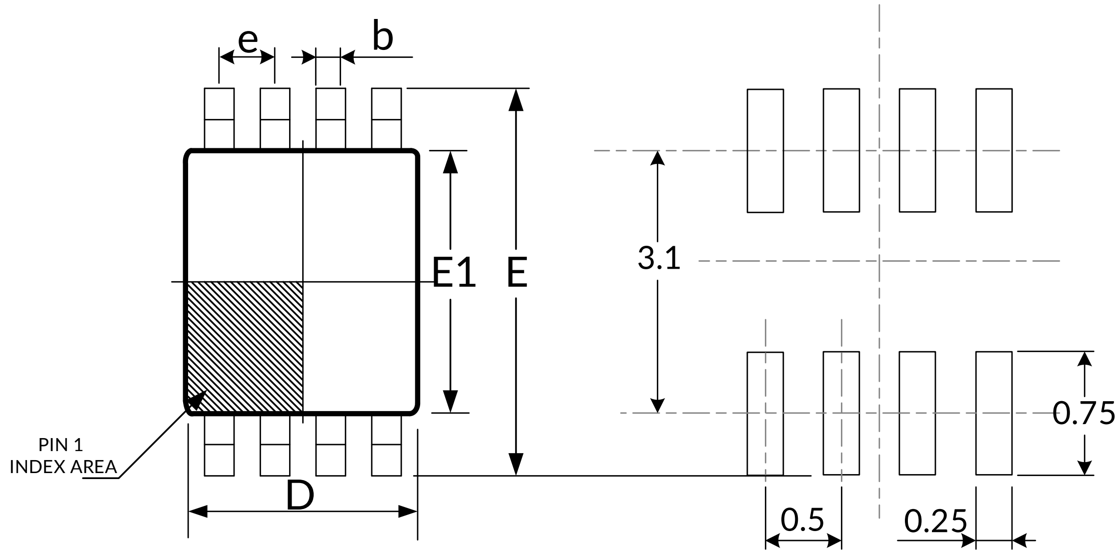
XTDFN-1.4x1-8L (3)



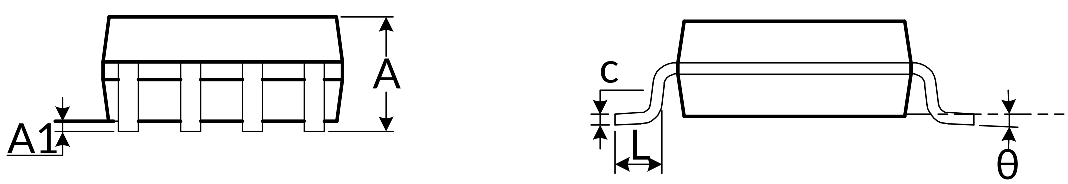
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.340	0.400	0.013	0.016
A1	0.000	0.050	0.000	0.002
A2	0.110 REF (2)		0.004 REF (2)	
D (1)	1.350	1.450	0.053	0.057
E (1)	0.950	1.050	0.037	0.041
k	0.200 MIN		0.008 MIN	
b	0.150	0.200	0.006	0.008
e	0.350 TYP		0.014 TYP	
L	0.250	0.350	0.010	0.014
L1	0.350	0.450	0.014	0.018

NOTE:
1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. This drawing is subject to change without notice.

VSSOP-8 (3)



RECOMMENDED LAND PATTERN (Unit: mm)

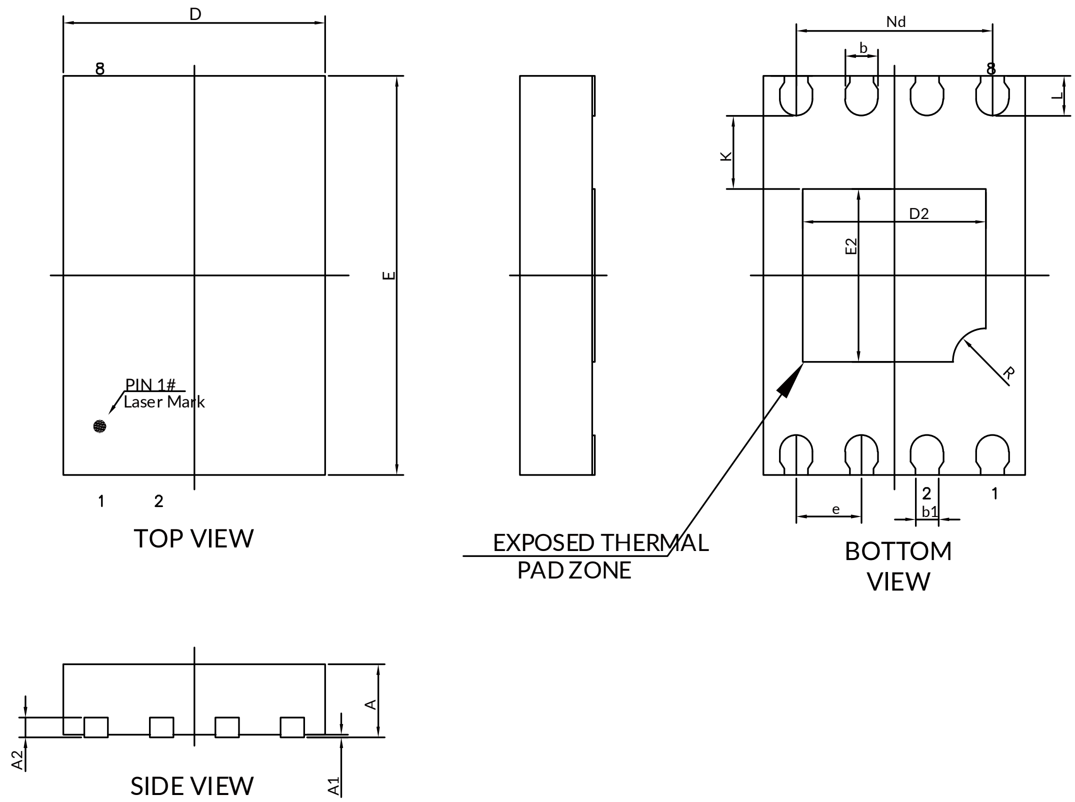


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.600	0.900	0.024	0.085
A1	0.000	0.100	0.000	0.004
b	0.170	0.250	0.007	0.010
c	0.100	0.200	0.004	0.008
D (1)	1.900	2.100	0.075	0.083
e	0.500(BSC) (2)		0.020(BSC) (2)	
E	3.000	3.200	0.118	0.126
E1 (1)	2.200	2.400	0.087	0.095
L	0.200	0.350	0.008	0.014
θ	0°	6°	0°	6°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

DFN2x3-8L (4)

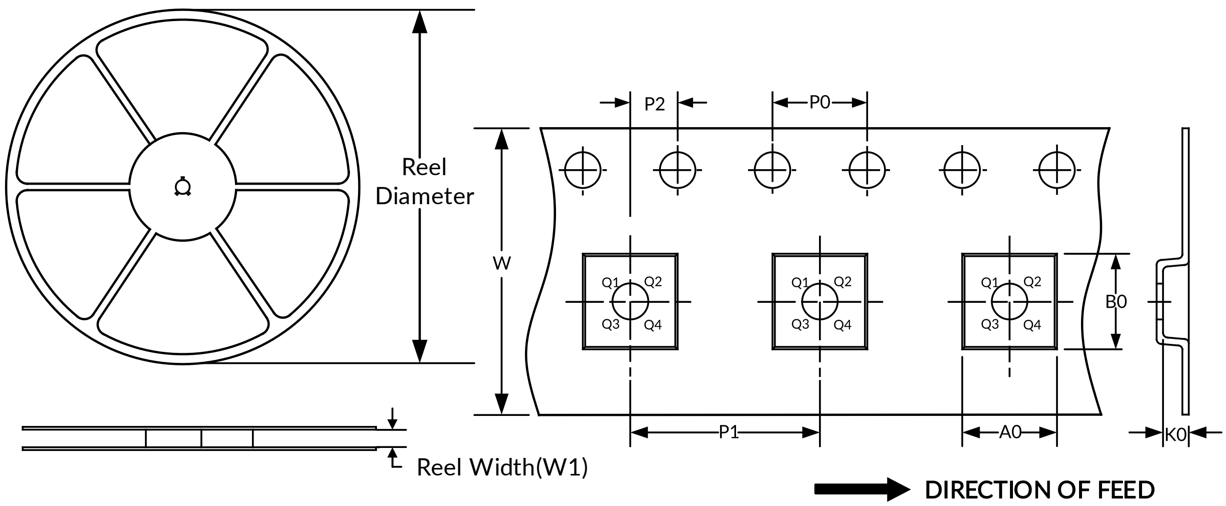


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A2	0.152 REF (3)		0.006 REF (3)	
D (1)	1.900	2.100	0.075	0.083
E (1)	2.900	3.100	0.114	0.122
D2	1.300	1.500	0.051	0.059
E2	1.200	1.400	0.047	0.055
e	0.500 BSC (2)		0.020 BSC (2)	
Nd	1.500 BSC (2)		0.059 BSC (2)	
b	0.200	0.300	0.008	0.012
b1	0.180 REF (3)		0.007 REF (3)	
L	0.250	0.350	0.010	0.014
R	0.200	0.300	0.008	0.012
K	0.500	0.600	0.020	0.024

NOTE:
1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

13 TAPE AND REEL INFORMATION

REEL DIMENSIONS TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-8	7"	9.5	3.17	3.23	1.37	4.0	4.0	2.0	8.0	Q3
DFN1.4×1.0-8L	7"	9.5	1.2	1.6	0.5	4.0	4.0	2.0	8.0	Q1
VSSOP8	7"	9.5	2.25	3.35	1.40	4.0	4.0	2.0	8.0	Q3
DFN2*3-8L	7"	9.5	2.30	3.30	0.95	4.0	4.0	2.0	8.0	Q2

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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