TC4420/TC4429

6A High-Speed MOSFET Drivers

Features

- Latch-Up Protected: will withstand >1.5A Reverse Output Current
- Logic Input will withstand Negative Swing Up to 5V
- ESD Protected: 4 kV
- Matched Rise and Fall Times:
  - 25 nsec (2500 pF load)
- High Peak Output Current: 6A Peak
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- High Capacitive Load Drive Capability: 10,000 pF
- Short Delay Time: 55 nsec (typ.)
- Logic High Input, Any Voltage: 2.4V to V_{DD}
- Low Supply Current With Logic '1' Input:
  - 450 µA (typ.)
- Low Output Impedance: 2.5Ω
- Output Voltage Swing to Within 25 mV of Ground or V_{DD}

Applications

- Switch-Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class D Switching Amplifiers

General Description

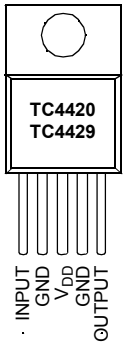
The TC4420/TC4429 are 6A (peak), single output MOSFET drivers. The TC4429 is an inverting driver (pin-compatible with the TC429), while the TC4420 is a non-inverting driver. These drivers are fabricated in CMOS for lower power, more efficient operation versus bipolar drivers.

Both devices have TTL-compatible inputs, which can be driven as high as V_{DD} + 0.3V or as low as -5V without upset or damage to the device. This eliminates the need for external level-shifting circuitry and its associated cost and size. The output swing is rail-to-rail, ensuring better drive voltage margin, especially during power-up/power-down sequencing. Propagational delay time is only 55 nsec (typ.) and the output rise and fall times are only 25 nsec (typ.) into 2500 pF across the usable power supply range.

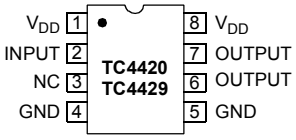
Unlike other drivers, the TC4420/TC4429 are virtually latch-up proof. They replace three or more discrete components, saving PCB area, parts and improving overall system reliability.

Package Types:

5-Pin TO-220

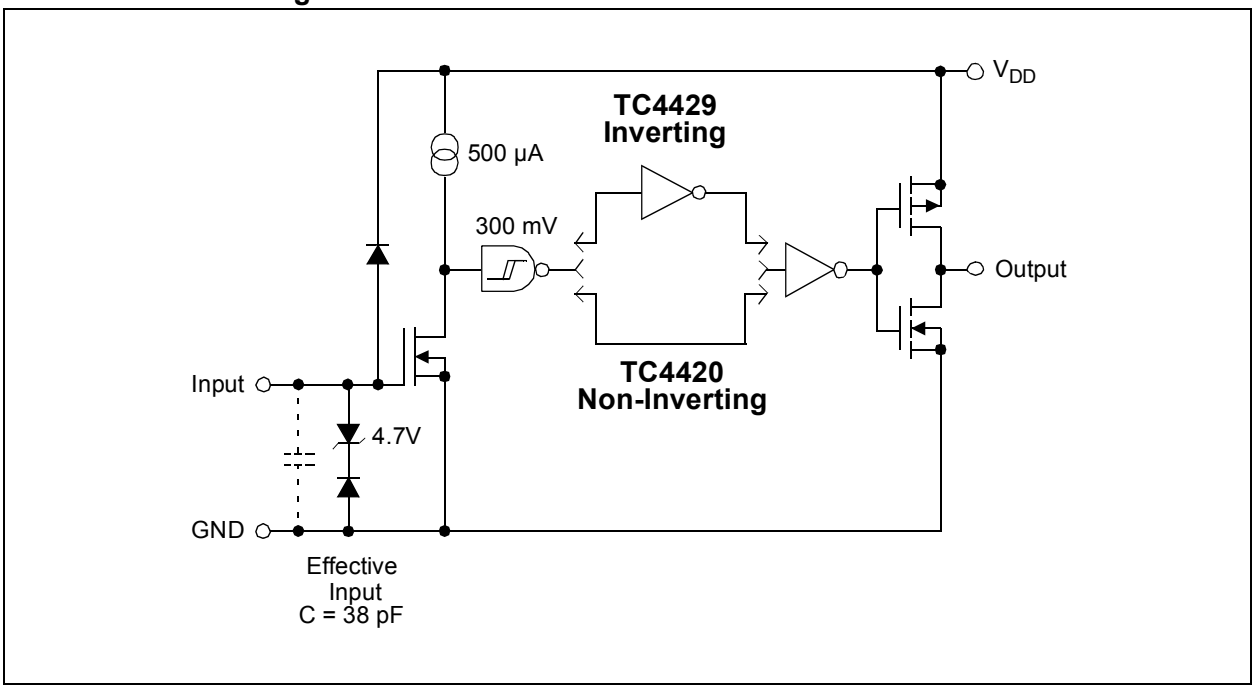


8-Pin PDIP/SOIC/CERDIP



Note: Duplicate pins must both be connected for proper operation.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage ..... +20V
Input Voltage ..... – 5V to V_{DD} + 0.3V
Input Current (V_{IN} > V_{DD}) ..... 50 mA
Power Dissipation ($T_A \leq 70°C$)
PDIP ..... 730 mW
SOIC ..... 470 mW
CERDIP ..... 800 mW
5-Pin TO-220 ..... 1.6W
Package Power Dissipation ($T_A \leq 25°C$)
5-Pin TO-220 (With Heatsink) 12.5W
Derating Factors (To Ambient)
PDIP ..... 8 mW/°C
SOIC ..... 4 mW/°C
CERDIP ..... 6.4 mW/°C
5-Pin TO-220 ..... 12 mW/°C
Thermal Impedances (To Case)
5-Pin TO-220 $R_{\theta J-C}$ ..... 10°C/W

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25ºC with 4.5V $\leq V_{DD} \leq$ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	1.8	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	1.3	0.8	V	
Input Voltage Range	V_{IN}	- 5	—	V_{DD}+0.3	V	
Input Current	I_{IN}	-10	—	+10	µA	$0V \leq V_{IN} \leq V_{DD}$
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC TEST
Low Output Voltage	V_{OL}	—	—	0.025	V	DC TEST
Output Resistance, High	R_{OH}	—	2.1	2.8	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	1.5	2.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	6.0	—	A	V_{DD} = 18V
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	> 1.5	—	A	Duty cycle ≤ 2%, t ≤ 300 µsec
Switching Time (Note 1)						
Rise Time	t_R	—	25	35	nsec.	**Figure 4-1**, C_L = 2,500 pF
Fall Time	t_F	—	25	35	nsec.	**Figure 4-1**, C_L = 2,500 pF
Delay Time	t_{D1}	—	55	75	nsec.	**Figure 4-1**
Delay Time	t_{D2}	—	55	75	nsec.	**Figure 4-1**
Power Supply						
Power Supply Current	I_S	— —	0.45 55	1.5 150	mA µA	V_{IN} = 3V V_{IN} = 0V
Operating Input Voltage	V_{DD}	4.5	—	18	V	

Note 1: Switching times ensured by design.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

Electrical Specifications: Unless otherwise noted, over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Voltage Range	V_{IN}	- 5	—	V_{DD} + 0.3	V	
Input Current	I_{IN}	-10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC TEST
Low Output Voltage	V_{OL}	—	—	0.025	V	DC TEST
Output Resistance, High	R_{OH}	—	3	5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	2.3	5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	—	32	60	nsec.	**Figure 4-1**, C_L = 2,500 pF
Fall Time	t_F	—	34	60	nsec.	**Figure 4-1**, C_L = 2,500 pF
Delay Time	t_{D1}	—	50	100	nsec.	**Figure 4-1**
Delay Time	t_{D2}	—	65	100	nsec.	**Figure 4-1**
Power Supply						
Power Supply Current	I_S	— —	0.45 60	3 400	mA µA	V_{IN} = 3V V_{IN} = 0V
Operating Input Voltage	V_{DD}	4.5	—	18	V	

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range (C)	T_A	0	—	+70	ºC	
Specified Temperature Range (I)	T_A	-25	—	+85	ºC	
Specified Temperature Range (E)	T_A	-40	—	+85	ºC	
Specified Temperature Range (M)	T_A	-55	—	+125	ºC	
Specified Temperature Range (V)	T_A	-40	—	+125	ºC	
Maximum Junction Temperature	T_J	—	—	+150	ºC	
Storage Temperature Range	T_A	-65	—	+150	ºC	
Package Thermal Resistances						
Thermal Resistance, 8L-PDIP	θ_{JA}	—	125	—	ºC/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	155	—	ºC/W	
Thermal Resistance, 8L-CERDIP	θ_{JA}	—	150	—	ºC/W	
Thermal Resistance, 5L-TO-220	θ_{JA}	—	71	—	ºC/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25ºC with 4.5V ≤ V_{DD} ≤ 18V.

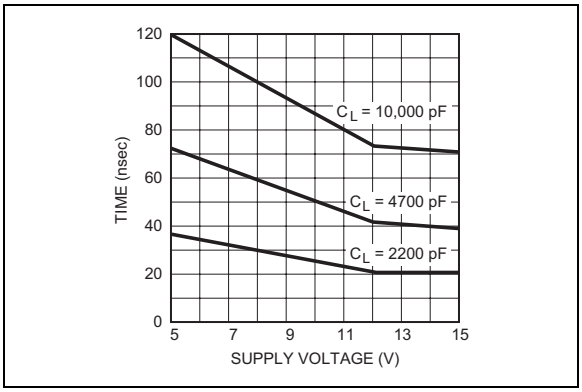


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

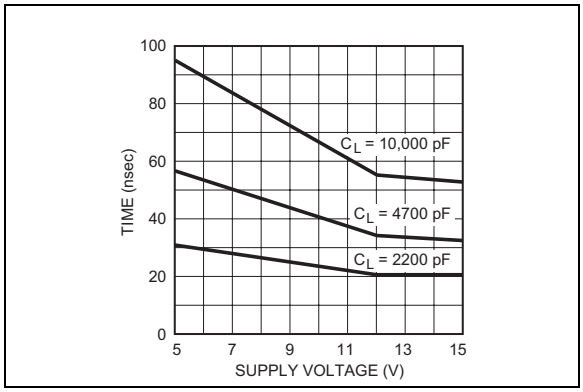


FIGURE 2-4: *Fall Time vs. Supply Voltage.*

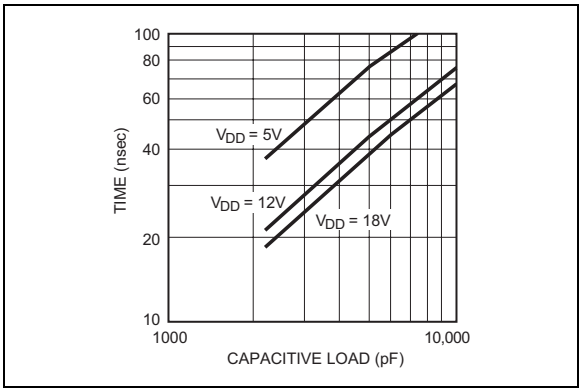


FIGURE 2-2: *Rise Time vs. Capacitive Load.*

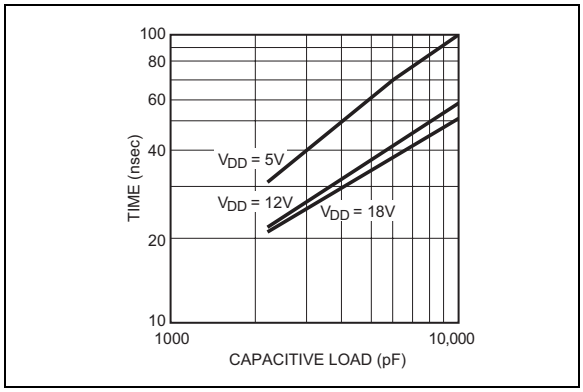


FIGURE 2-5: *Fall Time vs. Capacitive Load.*

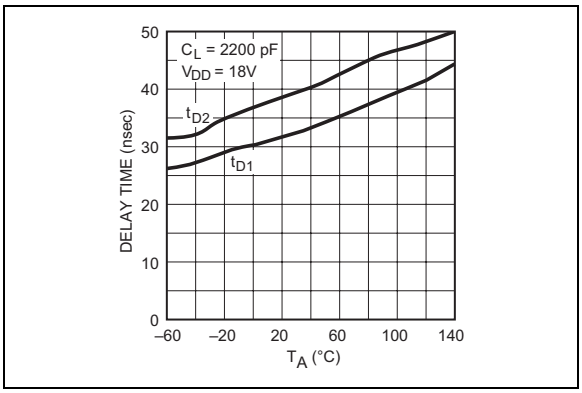


FIGURE 2-3: *Propagation Delay Time vs. Temperature.*

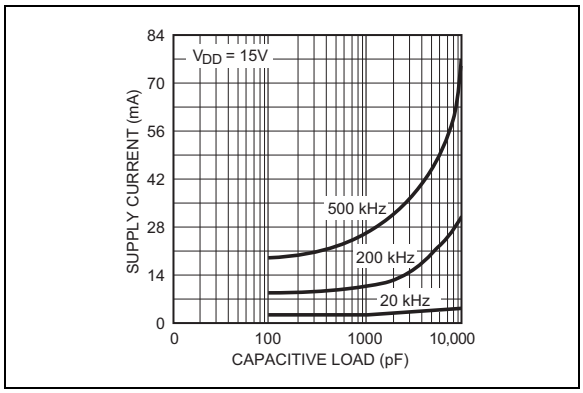


FIGURE 2-6: *Supply Current vs. Capacitive Load.*

Note: Unless otherwise indicated, T_A = +25ºC with 4.5V ≤ V_{DD} ≤ 18V.

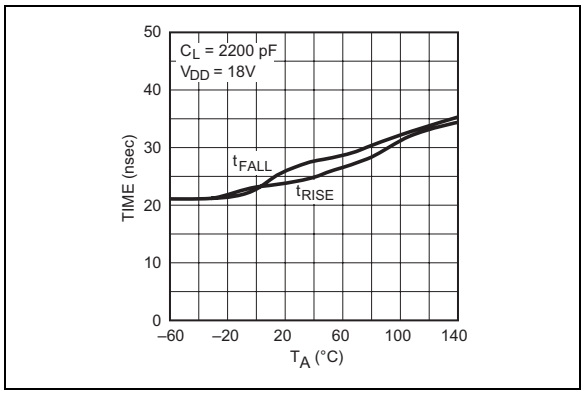


FIGURE 2-7: *Rise and Fall Times vs. Temperature.*

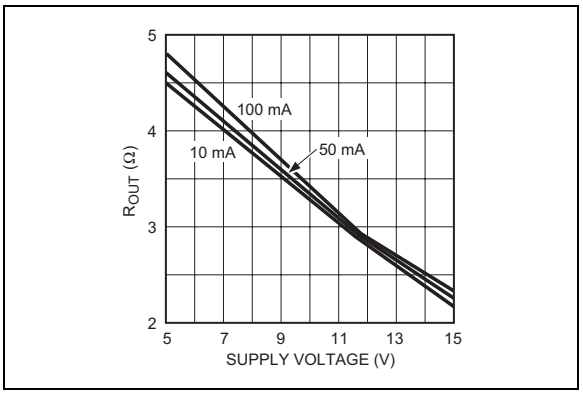


FIGURE 2-10: *High-State Output Resistance vs Supply Voltage.*

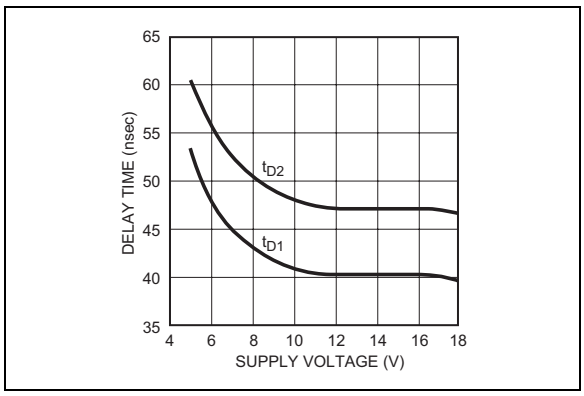


FIGURE 2-8: *Propagation Delay Time vs. Supply Voltage.*

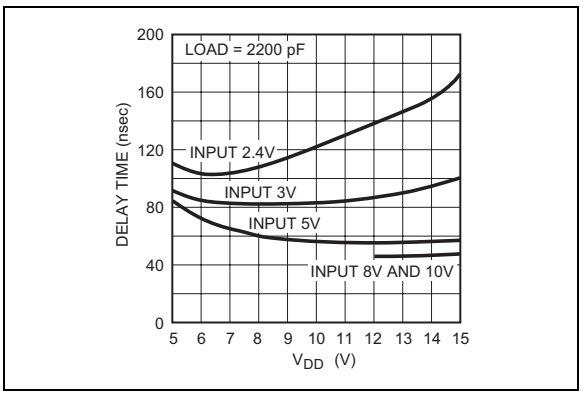


FIGURE 2-11: *Effect of Input Amplitude on Propagation Delay.*

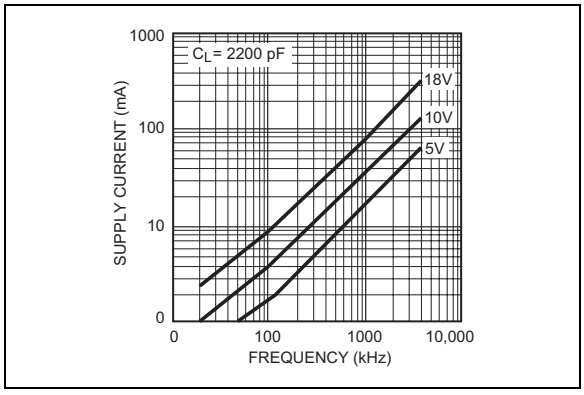


FIGURE 2-9: *Supply Current vs. Frequency.*

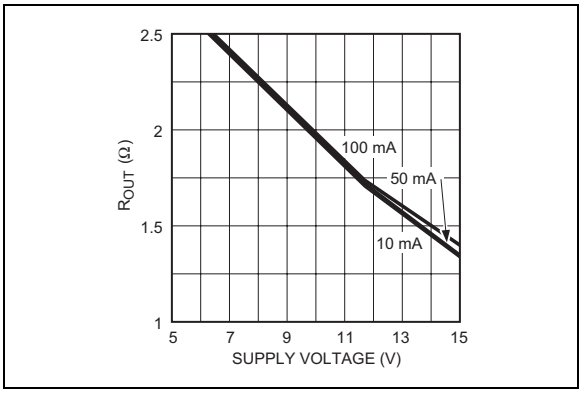


FIGURE 2-12: *Low-State Output Resistance vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25ºC with 4.5V ≤ V_{DD} ≤ 18V.

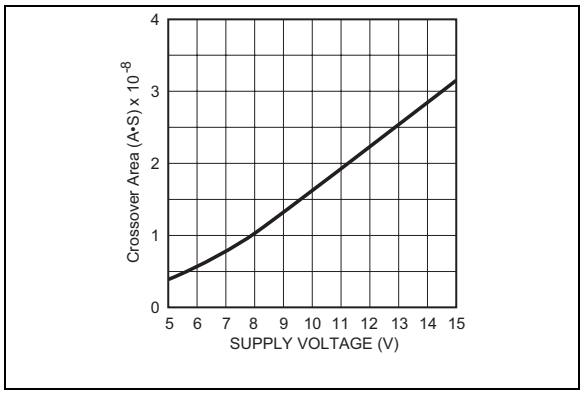


FIGURE 2-13: *Crossover Energy *.*

***** The values on this graph represent the loss seen by the driver during one complete cycle. For a single transition, divide the value by 2.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. (8-Pin PDIP, SOIC, CERDIP)	Pin No. (5-Pin TO-220)	Symbol	Description
1	—	V_{DD}	Supply input, 4.5V to 18V
2	1	INPUT	Control input, TTL/CMOS-compatible input
3	—	NC	No Connection
4	2	GND	Ground
5	4	GND	Ground
6	5	OUTPUT	CMOS push-pull output
7	—	OUTPUT	CMOS push-pull output
8	3	V_{DD}	Supply input, 4.5V to 18V

3.1 Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 18V with respect to the ground pins. The V_{DD} input should be bypassed to ground with a local ceramic capacitor. The value of the capacitor should be chosen based on the capacitive load that is being driven. A minimum value of 1.0 µF is suggested.

3.2 Control Input

The MOSFET driver input is a high-impedance, TTL/CMOS-compatible input. The input circuitry of the TC4420/TC4429 MOSFET driver also has a “speed-up” capacitor. This helps to decrease the propagation delay times of the driver. Because of this, input signals with slow rising or falling edges should not be used as this can result in double-pulsing of the MOSFET driver output.

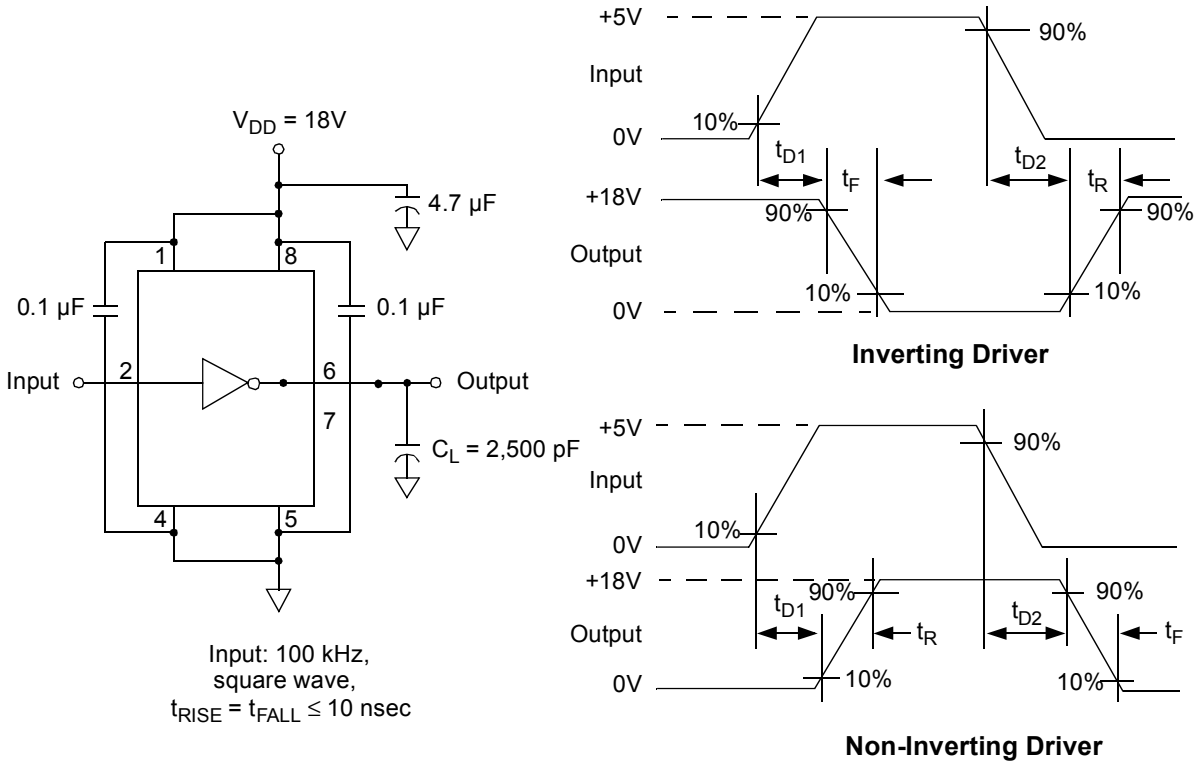
3.3 CMOS Push-Pull Output

The MOSFET driver output is a low-impedance, CMOS, push-pull style output, capable of driving a capacitive load with 6.0A peak currents. The MOSFET driver output is capable of withstanding 1.5A peak reverse currents of either polarity.

3.4 Ground

The ground pins are the return path for the bias current and for the high peak currents that discharge the load capacitor. The ground pins should be tied into a ground plane or have very short traces to the bias supply source return.

4.0 APPLICATIONS INFORMATION



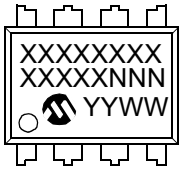
Note: Pinout shown is for the PDIP, SOIC and CERDIP packages.

FIGURE 4-1: *Switching Time Test Circuits.*

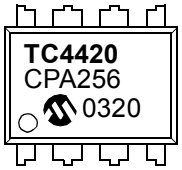
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

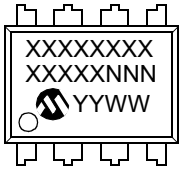
8-Lead PDIP (300 mil)



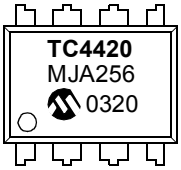
Example:



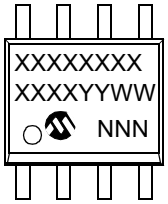
8-Lead CERDIP (300 mil)



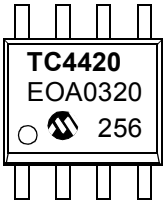
Example:



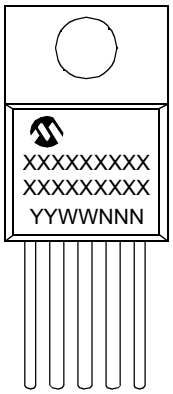
8-Lead SOIC (150 mil)



Example:



5-Lead TO-220



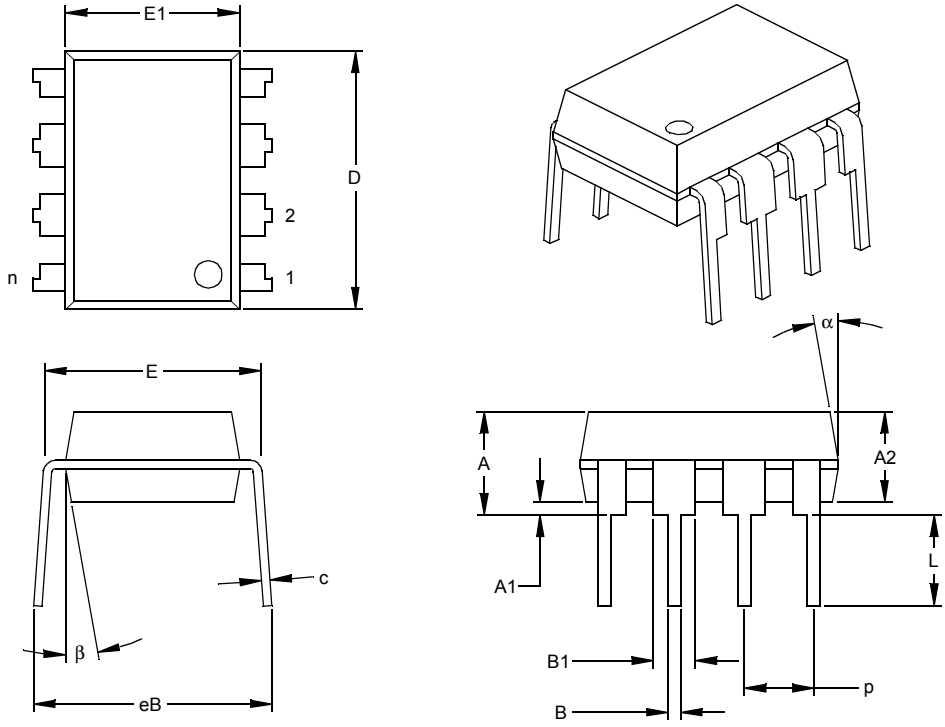
Example:

Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

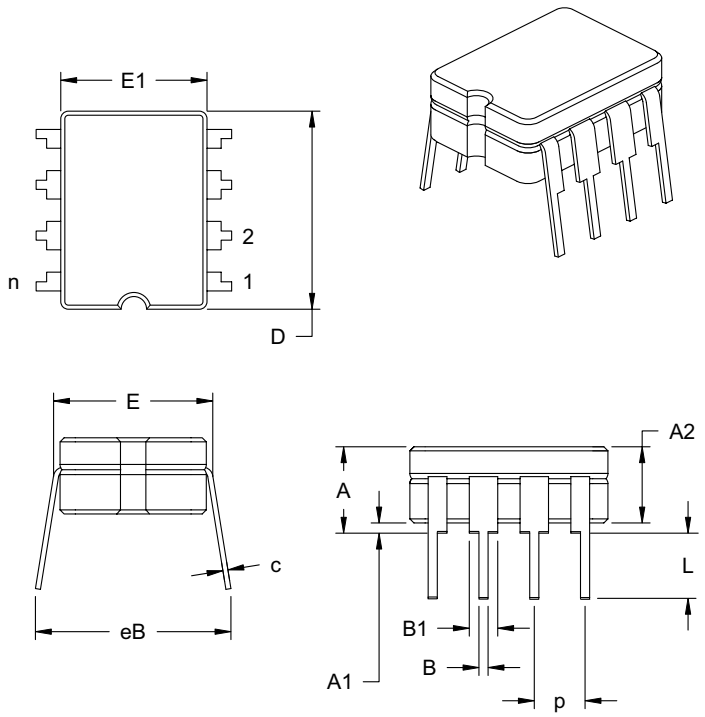


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Ceramic Dual In-line – 300 mil (CERDIP)



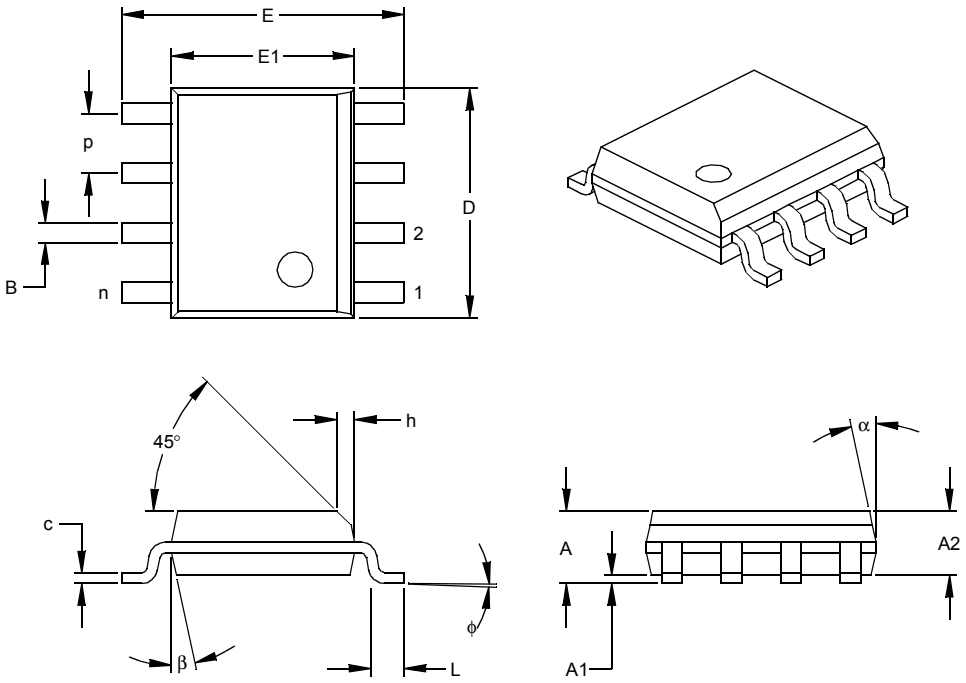
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.180	.200	4.06	4.57	5.08
Standoff §	A1	.020	.030	.040	0.51	0.77	1.02
Shoulder to Shoulder Width	E	.290	.305	.320	7.37	7.75	8.13
Ceramic Pkg. Width	E1	.230	.265	.300	5.84	6.73	7.62
Overall Length	D	.370	.385	.400	9.40	9.78	10.16
Tip to Seating Plane	L	.125	.163	.200	3.18	4.13	5.08
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.055	.065	1.14	1.40	1.65
Lower Lead Width	B	.016	.018	.020	0.41	0.46	0.51
Overall Row Spacing	eB	.320	.360	.400	8.13	9.15	10.16

*Controlling Parameter

JEDEC Equivalent: MS-030

Drawing No. C04-010

8-Lead Plastic Small Outline (OA) – Narrow, 150 mil (SOIC)

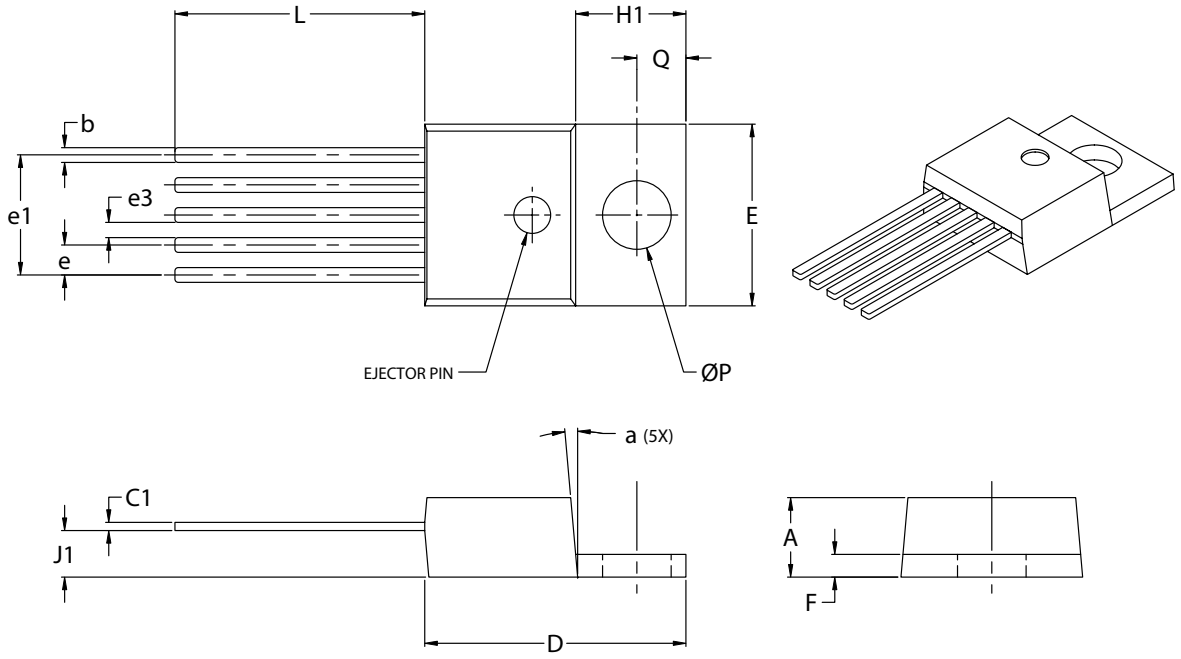


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

5-Lead TO-220



Units		INCHES*		MILLIMETERS	
Dimension Limits		MIN	MAX	MIN	MAX
Lead Pitch	e	.060	.072	1.52	1.83
Overall Lead Centers	e1	.263	.273	6.68	6.93
Space Between Leads	e3	.030	.040	0.76	1.02
Overall Height	A	.160	.190	4.06	4.83
Overall Width	E	.385	.415	9.78	10.54
Overall Length	D	.560	.590	14.22	14.99
Flag Length	H1	.234	.258	5.94	6.55
Flag Thickness	F	.045	.055	1.14	1.40
Through Hole Center	Q	.103	.113	2.62	2.87
Through Hole Diameter	P	.146	.156	3.71	3.96
Lead Length	L	.540	.560	13.72	14.22
Base to Bottom of Lead	J1	.090	.115	2.29	2.92
Lead Thickness	C1	.014	.022	0.36	0.56
Lead Width	b	.025	.040	0.64	1.02
Mold Draft Angle	a	3°	7°	3°	7°

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC equivalent: TO-220

Drawing No. C04-036

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	TC4420:	6A High-Speed MOSFET Driver, Non-Inverting
	TC4429:	6A High-Speed MOSFET Driver, Inverting
Temperature Range:	C =	0°C to +70°C
	I =	-25°C to +85°C (CERDIP Only)
	E =	-40°C to +85°C
	V =	-40°C to +125°C
	M =	-55°C to +125°C (CERDIP Only)
Package:	AT =	TO-220, 5-lead
	JA =	Ceramic Dual In-line (300 mil Body), 8-lead
	PA =	Plastic DIP (300 mil Body), 8-lead
	OA =	Plastic SOIC, (150 mil Body), 8-lead
	OA713 =	Plastic SOIC, (150 mil Body), 8-lead Tape and Reel

Examples:

a) TC4420CAT: 6A High-Speed MOSFET Driver, Non-inverting, TO-220 package, 0°C to +70°C.

b) TC4420IJA: 6A High-Speed MOSFET Driver, Non-inverting, CERDIP package, -25ºC to +85ºC.

c) TC4420EOA: 6A High-Speed MOSFET Driver, Non-inverting, SOIC package, -40ºC to +85ºC.

d) TC4420VAT: 6A High-Speed MOSFET Driver, Non-inverting, TO-220 package, -40ºC to +125ºC.

e) TC4420MJA: 6A High-Speed MOSFET Driver, Non-inverting, CERDIP package, -55ºC to +125ºC

a) TC4429CAT: A High-Speed MOSFET Driver, Inverting, TO-220 package, 0ºC to +70ºC

b) TC4429IJA: A High-Speed MOSFET Driver, Inverting, CERDIP package, -25ºC to +85ºC

c) TC4429EPA: A High-Speed MOSFET Driver, Inverting, PDIP package, -40ºC to +85ºC

d) TC4429VAT: A High-Speed MOSFET Driver, Inverting, TO-220 package, -40ºC to +125ºC

e) TC4429MJA: A High-Speed MOSFET Driver, Inverting, CERDIP package, -55ºC to +125ºC

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Atlanta
3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034
Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
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Fax: 978-692-3821

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Dallas
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Fax: 248-538-2260

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Kokomo, IN 46902
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Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888
Fax: 949-263-1338

Phoenix
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Chandler, AZ 85224-6199
Tel: 480-792-7966
Fax: 480-792-4338

San Jose
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San Jose, CA 95131
Tel: 408-436-7950
Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100
Fax: 86-10-85282104

China - Chengdu
Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200
Fax: 86-28-86766599

China - Fuzhou
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506
Fax: 86-591-7503521

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Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
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Fax: 852-2401-3431

China - Shanghai
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
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Fax: 86-21-6275-5060

China - Shenzhen
Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
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Fax: 86-755-8295-1393

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No. 2 Fengxiangnan Road, Ronggui Town
Shunde City, Guangdong 528303, China
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China - Qingdao
Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
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3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
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Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5932 or
82-2-558-5934

Singapore
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan
Kaohsiung Branch
30F - 1 No. 8
Min Chuan 2nd Road
Kaohsiung 806, Taiwan
Tel: 886-7-536-4818
Fax: 886-7-536-4803

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Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
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EUROPE

Austria
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A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45-4420-9895 Fax: 45-4420-9910

France
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany
Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy
Via Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands
P. A. De Biesbosch 14
NL-5152 SC Drunen, Netherlands
Tel: 31-416-690399
Fax: 31-416-690340

United Kingdom
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869
Fax: 44-118-921-5820

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