



FEATURES

- Ultra-low power consumption (1Mbps): 0.58mA/Channel
- High data rate: 200Mbps
- High common-mode transient immunity:
 - π 13xx3x: 75 kV/ μ s typical
 - π 13xx6x: 120 kV/ μ s typical
- High robustness to radiated and conducted noise
- Low propagation delay: 9 ns typical
- Isolation voltages:
 - π 13xx3x: AC 3000Vrms
 - π 13xx6x: AC 5000Vrms
- High ESD rating:
 - ESDA/JEDEC JS-001-2017
 - Human body model (HBM) \pm 8kV
- Safety and regulatory approvals:
 - UL certificate number: E494497
 - 3000Vrms/5000Vrms for 1 minute per UL 1577
 - CSA Component Acceptance Notice 5A
 - VDE certificate number: 40053041/40052896
 - DIN VDE V 0884-11:2017-01
 - $V_{IORM} = 565V$ peak/1200V peak
 - CQC certification per GB4943.1-2011
- 3 V to 5.5 V level translation
- Wide temperature range: $-40^{\circ}C$ to $125^{\circ}C$
- RoHS-compliant, NB SOIC-16, WB SOIC-16 and SSOP16 package

APPLICATIONS

- General-purpose multichannel isolation
- Industrial field bus isolation
- Isolation Industrial automation systems
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control

GENERAL DESCRIPTION

The π 1xxxx is a 2PaiSemi digital isolators product family that includes over hundreds of digital isolator products. By using matured standard semiconductor CMOS technology and 2PaiSemi *iDivider*[®] technology, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators.

Intelligent voltage divider technology (*iDivider*[®] technology) is a new generation digital isolator technology invented by 2PaiSemi. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The π 1xxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 5.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied.

FUNCTIONAL BLOCK DIAGRAMS

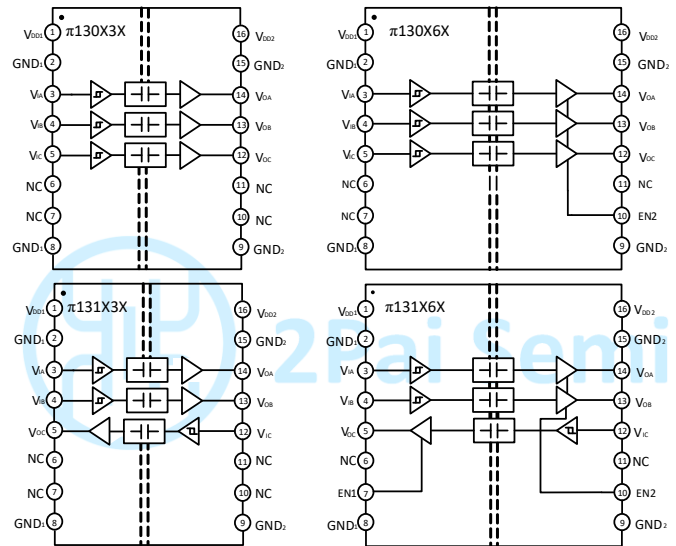


Figure 1. π 130xxx/ π 131xxx functional Block Diagram

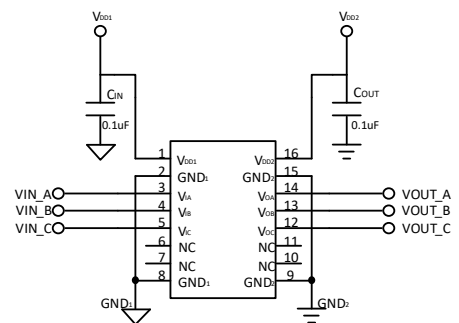


Figure 2. π 130x3x Typical Application Circuit

PIN CONFIGURATIONS AND FUNCTIONS

Table 1. π 130Exx Pin Function Descriptions

| Pin No. | Name | Description |
|---------|------------------|---|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 2 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 3 | V _{IA} | Logic Input A. |
| 4 | V _{IB} | Logic Input B. |
| 5 | V _{IC} | Logic Input C. |
| 6 | NC | No connect. |
| 7 | NC | No connect. |
| 8 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 9 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 10 | NC/EN2 | No connect for π 130E3X. |
| | | Output enable for π 130E6X. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low. |
| 11 | NC | No connect. |
| 12 | V _{OC} | Logic Output C. |
| 13 | V _{OB} | Logic Output B. |
| 14 | V _{OA} | Logic Output A. |
| 15 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 16 | V _{DD2} | Supply Voltage for Isolator Side 2. |

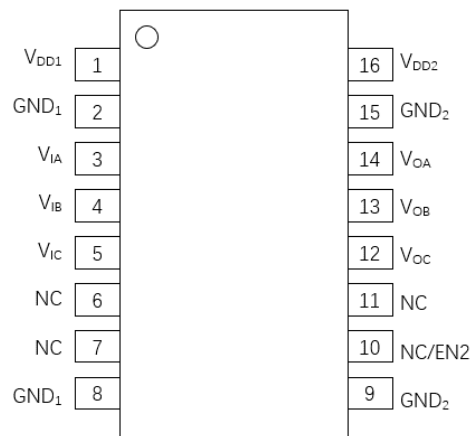


Figure 3. π 130Exx Pin Configuration

Table 2. π 131Exx Pin Function Descriptions

| Pin No. | Name | Description |
|---------|------------------|---|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 2 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 3 | V _{IA} | Logic Input A. |
| 4 | V _{IB} | Logic Input B. |
| 5 | V _{OC} | Logic Output C. |
| 6 | NC | No connect. |
| 7 | NC/EN1 | No connect for π 131E3X. |
| | | Output enable for π 131E6X. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low. |
| 8 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 9 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 10 | NC/EN2 | No connect for π 131E3X. |
| | | Output enable for π 131E6X. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low. |
| 11 | NC | No connect. |
| 12 | V _{IC} | Logic Input C. |
| 13 | V _{OB} | Logic Output B. |
| 14 | V _{OA} | Logic Output A. |
| 15 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 16 | V _{DD2} | Supply Voltage for Isolator Side 2. |

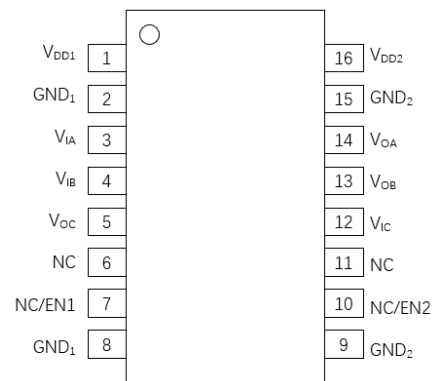


Figure 4. π 131Exx Pin Configuration

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings⁴

TA = 25°C, unless otherwise noted.

| Parameter | Rating |
|--|-----------------------------------|
| Supply Voltages (V _{DD1} -GND ₁ , V _{DD2} -GND ₂) | -0.5 V ~ +7.0 V |
| Input Voltages (V _{IA} , V _{IB}) ¹ | -0.5 V ~ V _{DDx} + 0.5 V |
| Output Voltages (V _{OA} , V _{OB}) ¹ | -0.5 V ~ V _{DDx} + 0.5 V |
| Average Output Current per Pin ² Side 1 Output Current (I _{O1}) | -10 mA ~ +10 mA |
| Average Output Current per Pin ² Side 2 Output Current (I _{O2}) | -10 mA ~ +10 mA |
| Common-Mode Transients Immunity ³ | -200 kV/μs ~ +200 kV/μs |
| Storage Temperature (T _{ST}) Range | -65°C ~ +150°C |
| Ambient Operating Temperature (T _A) Range | -40°C ~ +125°C |

Notes:

¹ V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.² See Figure 5 for the maximum rated current values for various temperatures.³ See Figure 13 for Common-mode transient immunity (CMTI) measurement.⁴ Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 4. Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------------|-------------------------------|-----------------------------------|-----|-----------------------------------|------|
| Supply Voltage | V _{DDx} ¹ | 3 | | 5.5 | V |
| High Level Input Signal Voltage | V _{IH} | 0.7*V _{DDx} ¹ | | V _{DDx} ¹ | V |
| Low Level Input Signal Voltage | V _{IL} | 0 | | 0.3*V _{DDx} ¹ | V |
| High Level Output Current | I _{OH} | -6 | | | mA |
| Low Level Output Current | I _{OL} | | | 6 | mA |
| Data Rate | | 0 | | 200 | Mbps |
| Junction Temperature | T _J | -40 | | 150 | °C |
| Ambient Operating Temperature | T _A | -40 | | 125 | °C |

Notes:

¹ V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Truth Tables

Table 5. π 130E3x/ π 131E3x Truth Table

| V _{ix} Input ¹ | V _{DDi} State ¹ | V _{DDO} State ¹ | Default Low V _{Ox} Output ¹ | Default High V _{Ox} Output ¹ | Test Conditions /Comments |
|------------------------------------|-------------------------------------|-------------------------------------|---|--|-----------------------------|
| Low | Powered ² | Powered ² | Low | Low | Normal operation |
| High | Powered ² | Powered ² | High | High | Normal operation |
| Open | Powered ² | Powered ² | Low | High | Default output |
| Don't Care ⁴ | Unpowered ³ | Powered ² | Low | High | Default output ⁵ |
| Don't Care ⁴ | Powered ² | Unpowered ³ | High Impedance | High Impedance | |

Notes:

¹ V_{ix}/V_{Ox} are the input/output signals of a given channel (A or B). V_{DDi}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.² Powered means V_{DDx} ≥ 2.95 V³ Unpowered means V_{DDx} < 2.30V⁴ Input signal (V_{ix}) must be in a low state to avoid powering the given V_{DDi}¹ through its ESD protection circuitry.⁵ If the V_{DDi} goes into unpowered status, the channel outputs the default logic signal after around 1μs. If the V_{DDi} goes into powered status, the channel outputs the input status logic signal after around 3μs.

Table 6. π 130E6x/ π 131E6x Truth Table

| V _{ix} Input ¹ | EN1/2 State | V _{DDI} State ¹ | V _{DDO} State ¹ | Default Low | Default High | Test Conditions /Comments |
|------------------------------------|-------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-----------------------------|
| | | | | V _{ox} Output ¹ | V _{ox} Output ¹ | |
| Low | High or NC | Powered ² | Powered ² | Low | Low | Normal operation |
| High | High or NC | Powered ² | Powered ² | High | High | Normal operation |
| Don't Care ⁴ | L | Powered ² | Powered ² | High Impedance | High Impedance | Disabled |
| Open | High or NC | Powered ² | Powered ² | Low | High | Default output ⁵ |
| Don't Care ⁴ | High or NC | Unpowered ³ | Powered ² | Low | High | Default output ⁵ |
| Don't Care ⁴ | L | Unpowered ³ | Powered ² | High Impedance | High Impedance | |
| Don't Care ⁴ | Don't Care ⁴ | Powered ² | Unpowered ³ | High Impedance | High Impedance | |

Notes:

¹V_{ix}/V_{ox} are the input/output signals of a given channel (A or B). V_{DDI}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.

²Powered means V_{DDx} ≥ 2.95 V

³Unpowered means V_{DDx} < 2.30V

⁴Input signal (V_{ix}) must be in a low state to avoid powering the given V_{DDI}¹ through its ESD protection circuitry.

⁵If the V_{DDI} goes into unpowered status, the channel outputs the default logic signal after around 1 μ s. If the V_{DDI} goes into powered status, the channel outputs the input status logic signal after around 3 μ s.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Table 7. π 13xE3x Switching Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} ± 10% or 5V_{DC} ± 10%, T_A = 25°C, unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-------------------------------------|-----|-----|------|---------------|--|
| Minimum Pulse Width | PW | | | 5 | ns | Within pulse width distortion (PWD) limit |
| Maximum Data Rate | | 200 | | | Mbps | Within pulse width distortion (PWD) limit |
| Propagation Delay Time ¹ | t _{pHL} , t _{pLH} | 5.5 | 8 | 12.5 | ns | @ 5V _{DC} supply |
| | | 6.5 | 9 | 13.5 | ns | @ 3.3V _{DC} supply |
| Pulse Width Distortion | PWD | | 0.3 | 3.0 | ns | The max different time between t _{pHL} and t _{pLH} @ 5V _{DC} supply. And The value is t _{pHL} - t _{pLH} |
| | | | 0.4 | 3.0 | ns | The max different time between t _{pHL} and t _{pLH} @ 3.3V _{DC} supply. And The value is t _{pHL} - t _{pLH} |
| Part to Part Propagation Delay Skew | t _{PSK} | | | 2 | ns | The max different propagation delay time between any two devices at the same temperature, load and voltage @ 5V _{DC} supply |
| | | | | 2 | ns | The max different propagation delay time between any two devices at the same temperature, load and voltage @ 3.3V _{DC} supply |
| Channel to Channel Propagation Delay Skew | t _{CSK} | | 0 | 1.8 | ns | The max amount propagation delay time differs between any two output channels in the single device @ 5V _{DC} supply. |
| | | | 0 | 2 | ns | The max amount propagation delay time differs between any two output channels in the single device @ 3.3V _{DC} supply |
| Output Signal Rise/Fall Time ⁴ | t _r /t _f | | 1.5 | | ns | See Figure 9. |
| Dynamic Input Supply Current per Channel | I _{DDI(D)} | | 9 | | μ A /Mbps | Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 5V _{DC} Supply |
| Dynamic Output Supply Current per Channel | I _{DDO(D)} | | 38 | | μ A /Mbps | Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 5V _{DC} Supply |
| Dynamic Input Supply Current per Channel | I _{DDI(D)} | | 5 | | μ A /Mbps | Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 3.3V _{DC} Supply |
| Dynamic Output Supply Current per Channel | I _{DDO(D)} | | 23 | | μ A /Mbps | Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 3.3V _{DC} Supply |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------|-----|---------|-----|-------------|---|
| Common-Mode Transient Immunity ³ | CMTI | | 75 | | kV/ μ s | $V_{IN} = V_{DDx}^2$ or 0V, $V_{CM} = 1000$ V |
| Jitter | | | 120 | | ps p-p | See the Jitter Measurement section |
| | | | 20 | | ps rms | |
| ESD (HBM - Human body model) | ESD | | ± 8 | | kV | |

Notes:

¹ t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See Figure 10.² V_{DDx} is the side voltage power supply V_{DD} , where $x = 1$ or 2.³ See Figure 13 for Common-mode transient immunity (CMTI) measurement.⁴ t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal, t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal.Table 8. $\pi 13x E6x$ Switching Specifications $V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$ or $5V_{DC} \pm 10\%$, $T_A = 25^\circ C$, unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------------------|-----|---------|------|------------------|--|
| Minimum Pulse Width | PW | | | 5 | ns | Within pulse width distortion (PWD) limit |
| Maximum Data Rate | | 200 | | | Mbps | Within pulse width distortion (PWD) limit |
| Propagation Delay Time ¹ | t_{pHL}, t_{pLH} | | 12 | 16 | ns | @ 5V _{DC} supply |
| | | | 14 | 18.5 | ns | @ 3.3V _{DC} supply |
| Pulse Width Distortion | PWD | | 0.3 | 3.0 | ns | The max different time between t_{pHL} and t_{pLH} @ 5V _{DC} supply. And The value is $ t_{pHL} - t_{pLH} $ |
| | | | 0.4 | 3.0 | ns | The max different time between t_{pHL} and t_{pLH} @ 3.3V _{DC} supply. And The value is $ t_{pHL} - t_{pLH} $ |
| Part to Part Propagation Delay Skew | t_{PSK} | | | 2 | ns | The max different propagation delay time between any two devices at the same temperature, load and voltage @ 5V _{DC} supply |
| | | | | 2 | ns | The max different propagation delay time between any two devices at the same temperature, load and voltage @ 3.3V _{DC} supply |
| Channel to Channel Propagation Delay Skew | t_{CSK} | | 0 | 1.8 | ns | The max amount propagation delay time differs between any two output channels in the single device @ 5V _{DC} supply. |
| | | | 0 | 2 | ns | The max amount propagation delay time differs between any two output channels in the single device @ 3.3V _{DC} supply |
| Output Signal Rise/Fall Time ⁴ | t_r/t_f | | 1.5 | | ns | See Figure 9. |
| Dynamic Input Supply Current per Channel | $I_{DDI(D)}$ | | 10 | | μA /Mbps | Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 5V _{DC} Supply |
| Dynamic Output Supply Current per Channel | $I_{DDO(D)}$ | | 45 | | μA /Mbps | Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 5V _{DC} Supply |
| Dynamic Input Supply Current per Channel | $I_{DDI(D)}$ | | 9 | | μA /Mbps | Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 3.3V _{DC} Supply |
| Dynamic Output Supply Current per Channel | $I_{DDO(D)}$ | | 28 | | μA /Mbps | Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 3.3V _{DC} Supply |
| Common-Mode Transient Immunity ³ | CMTI | | 120 | | kV/ μ s | $V_{IN} = V_{DDx}^2$ or 0V, $V_{CM} = 1000$ V |
| Jitter | | | 180 | | ps p-p | See the Jitter Measurement section |
| | | | 30 | | ps rms | |
| ESD (HBM - Human body model) | ESD | | ± 8 | | kV | |

Notes:

¹t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See Figure 10.

²V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

³See Figure 13 for Common-mode transient immunity (CMTI) measurement.

⁴t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal, t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal.

Table 9.DC Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted.

| | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------------------------------|------------------------------------|------------------------------------|-----------------------------------|------|--|
| Rising Input Signal Voltage Threshold | V _{IT+} | | 0.6*V _{DDx} ¹ | 0.7*V _{DDx} ¹ | V | |
| Falling Input Signal Voltage Threshold | V _{IT-} | 0.3* V _{DDx} ¹ | 0.4* V _{DDx} ¹ | | V | |
| High Level Output Voltage | V _{OH} ¹ | V _{DDx} - 0.1 | V _{DDx} | | V | -20 μA output current |
| | | V _{DDx} - 0.2 | V _{DDx} - 0.1 | | V | -2 mA output current |
| Low Level Output Voltage | V _{OL} | | 0 | 0.1 | V | 20 μA output current |
| | | | 0.1 | 0.2 | V | 2 mA output current |
| Input Current per Signal Channel | I _{IN} | -10 | 0.5 | 10 | μA | 0 V ≤ Signal voltage ≤ V _{DDx} ¹ |
| V _{DDx} ¹ Undervoltage Rising Threshold | V _{DDxUV+} | 2.45 | 2.75 | 2.95 | V | |
| V _{DDx} ¹ Undervoltage Falling Threshold | V _{DDxUV-} | 2.30 | 2.60 | 2.75 | V | |
| V _{DDx} ¹ Hysteresis | V _{DDxUVH} | | 0.15 | | V | |

Notes:

¹V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Table 10.Quiescent Supply Current

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 0 pF, unless otherwise noted.

| Part | Symbol | Min | Typ | Max | Unit | Test Conditions | |
|---------|----------------------|------|------|------|------|--------------------|----------------------------------|
| | | | | | | Supply voltage | Input signal |
| π130E3x | I _{DD1} (Q) | 0.13 | 0.16 | 0.20 | mA | 5V _{DC} | V _I =0V for π13xEx0 |
| | I _{DD2} (Q) | 1.25 | 1.56 | 2.03 | mA | | V _I =5V for π13xEx1 |
| | I _{DD1} (Q) | 0.31 | 0.39 | 0.50 | mA | 3.3V _{DC} | V _I =5V for π13xEx0 |
| | I _{DD2} (Q) | 1.18 | 1.48 | 1.92 | mA | | V _I =0V for π13xEx1 |
| | I _{DD1} (Q) | 0.12 | 0.15 | 0.20 | mA | 3.3V _{DC} | V _I =0V for π13xEx0 |
| | I _{DD2} (Q) | 1.24 | 1.54 | 2.01 | mA | | V _I =3.3V for π13xEx1 |
| π131E3x | I _{DD1} (Q) | 0.48 | 0.60 | 0.78 | mA | 5V _{DC} | V _I =0V for π13xEx0 |
| | I _{DD2} (Q) | 0.89 | 1.11 | 1.44 | mA | | V _I =5V for π13xEx1 |
| | I _{DD1} (Q) | 0.59 | 0.74 | 0.96 | mA | 3.3V _{DC} | V _I =5V for π13xEx0 |
| | I _{DD2} (Q) | 0.88 | 1.10 | 1.43 | mA | | V _I =0V for π13xEx1 |
| | I _{DD1} (Q) | 0.47 | 0.59 | 0.77 | mA | 3.3V _{DC} | V _I =0V for π13xEx0 |
| | I _{DD2} (Q) | 0.88 | 1.10 | 1.43 | mA | | V _I =3.3V for π13xEx1 |
| π130E6x | I _{DD1} (Q) | 0.10 | 0.12 | 0.20 | mA | 5V _{DC} | V _I =0V for π13xEx0 |
| | I _{DD2} (Q) | 1.25 | 1.65 | 2.23 | mA | | V _I =5V for π13xEx1 |
| | I _{DD1} (Q) | 0.31 | 0.44 | 0.61 | mA | 3.3V _{DC} | V _I =5V for π13xEx0 |
| | I _{DD2} (Q) | 1.18 | 1.52 | 2.06 | mA | | V _I =0V for π13xEx1 |
| | I _{DD1} (Q) | 0.09 | 0.11 | 0.20 | mA | 3.3V _{DC} | V _I =0V for π13xEx0 |
| | I _{DD2} (Q) | 1.24 | 1.60 | 2.17 | mA | | V _I =3.3V for π13xEx1 |
| π131E6x | I _{DD1} (Q) | 0.23 | 0.28 | 0.38 | mA | 5V _{DC} | V _I =3.3V for π13xEx0 |
| | I _{DD2} (Q) | 1.13 | 1.47 | 1.98 | mA | | V _I =0V for π13xEx1 |

| | | | | | | | |
|--|----------------------|------|------|------|----|--------------------|--------------------------|
| | I _{DD2} (Q) | 0.89 | 1.09 | 1.42 | mA | | VI=5V for π 13xEx1 |
| | I _{DD1} (Q) | 0.59 | 0.80 | 1.04 | mA | | VI=5V for π 13xEx0 |
| | I _{DD2} (Q) | 0.88 | 1.06 | 1.38 | mA | 3.3V _{DC} | VI=0V for π 13xEx1 |
| | I _{DD1} (Q) | 0.47 | 0.59 | 0.77 | mA | | VI=0V for π 13xEx0 |
| | I _{DD2} (Q) | 0.88 | 1.08 | 1.41 | mA | | VI=3.3V for π 13xEx1 |
| | I _{DD1} (Q) | 0.52 | 0.68 | 0.89 | mA | | VI=3.3V for π 13xEx0 |
| | I _{DD2} (Q) | 0.83 | 1.00 | 1.30 | mA | | VI=0V for π 13xEx1 |

Table 11.Total Supply Current vs. Data Throughput (CL = 0 pF)

 $V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$ or $5V_{DC} \pm 10\%$, $T_A = 25^\circ C$, $C_L = 0$ pF, unless otherwise noted.

| Part | Symbol | 150 Kbps | | | 10 Mbps | | | 100 Mbps | | | Unit | Supply voltage |
|--------------|------------------|----------|------|------|---------|------|------|----------|-------|-------|------|--------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| π 130E3x | I _{DD1} | | 0.26 | 0.39 | | 0.44 | 0.66 | | 2.87 | 4.31 | mA | 5V _{DC} |
| | I _{DD2} | | 1.52 | 2.28 | | 2.82 | 4.22 | | 13.08 | 19.61 | | |
| | I _{DD1} | | 0.21 | 0.32 | | 0.34 | 0.51 | | 1.69 | 2.54 | mA | 3.3V _{DC} |
| | I _{DD2} | | 1.49 | 2.23 | | 2.29 | 3.43 | | 8.50 | 12.75 | | |
| π 131E3x | I _{DD1} | | 0.66 | 0.99 | | 1.17 | 1.76 | | 6.21 | 9.32 | mA | 5V _{DC} |
| | I _{DD2} | | 1.11 | 1.67 | | 2.03 | 3.04 | | 9.68 | 14.51 | | |
| | I _{DD1} | | 0.62 | 0.93 | | 0.93 | 1.40 | | 3.90 | 5.85 | mA | 3.3V _{DC} |
| | I _{DD2} | | 1.08 | 1.62 | | 1.63 | 2.44 | | 6.22 | 9.33 | | |
| π 130E6x | I _{DD1} | | 0.29 | 0.40 | | 0.76 | 1.15 | | 6.55 | 9.82 | mA | 5V _{DC} |
| | I _{DD2} | | 1.60 | 2.40 | | 2.89 | 4.32 | | 14.62 | 21.93 | | |
| | I _{DD1} | | 0.20 | 0.30 | | 0.47 | 0.71 | | 3.83 | 5.74 | mA | 3.3V _{DC} |
| | I _{DD2} | | 1.55 | 2.32 | | 2.36 | 3.53 | | 9.92 | 14.88 | | |
| π 131E6x | I _{DD1} | | 0.72 | 1.08 | | 1.54 | 2.31 | | 9.63 | 14.45 | mA | 5V _{DC} |
| | I _{DD2} | | 1.62 | 2.44 | | 2.66 | 3.99 | | 11.94 | 17.90 | | |
| | I _{DD1} | | 0.64 | 0.96 | | 1.18 | 1.78 | | 5.97 | 8.96 | mA | 3.3V _{DC} |
| | I _{DD2} | | 1.54 | 2.31 | | 2.22 | 3.32 | | 8.04 | 12.06 | | |

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 12. Insulation Specifications

| Parameter | Symbol | Value | | Unit | Test Conditions/Comments |
|--|---------|--------------|--------------|---------|--|
| | | π 13xE3x | π 13xE6x | | |
| Rated Dielectric Insulation Voltage | | 3000 | 5000 | V rms | 1-minute duration |
| Minimum External Air Gap (Clearance) | L (CLR) | ≥ 4 | ≥ 8 | mm | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L (CRP) | ≥ 4 | ≥ 8 | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | ≥ 11 | ≥ 21 | μ m | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | >400 | V | DIN EN 60112 (VDE 0303-11):2010-05 |
| Material Group | | II | II | | IEC 60112:2003 + A1:2009 |

PACKAGE CHARACTERISTICS

Table 13. Package Characteristics

| Parameter | Symbol | Typical Value | | Unit | Test Conditions/Comments |
|-----------|--------|---------------|--------------|------|--------------------------|
| | | π 13xE3x | π 13xE6x | | |

| | | | | | |
|--|-----------------|------------------|------------------|-----------------------------|---|
| Resistance (Input to Output) ¹ | R _{IO} | 10 ¹¹ | 10 ¹¹ | Ω | |
| Capacitance (Input to Output) ¹ | C _{IO} | 1.5 | 1.5 | pF | @1MHz |
| Input Capacitance ² | C _I | 3 | 3 | pF | @1MHz |
| IC Junction to Ambient Thermal Resistance | θ_{JA} | 100 | 45 | $^{\circ}\text{C}/\text{W}$ | Thermocouple located at center of package underside |

Notes:

¹The device is considered a 2-terminal device; Short-circuit all terminals on the VDD1 side as one terminal, and short-circuit all terminals on the VDD2 side as the other terminal.

²Testing from the input signal pin to ground.

REGULATORY INFORMATION

See Table 14 for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 14.Regulatory

| Regulatory | $\pi 13x E3x$ | $\pi 13x E6x$ |
|------------|--|---|
| UL | Recognized under UL 1577 Component Recognition Program ¹ Single Protection, 3000 V rms Isolation Voltage File (E494497) | Recognized under UL 1577 Component Recognition Program ¹ Single Protection, 5000 V rms Isolation Voltage File (E494497) |
| VDE | DIN VDE V 0884-11:2017-01 ² Basic insulation, V _{IORM} = 565V peak, V _{IOSM} = 3615 V peak File (40053041) | DIN VDE V 0884-11:2017-01 ² Basic insulation, V _{IORM} = 1200 V peak, V _{IOSM} = 5000 V peak File (40052896) |
| CQC | Certified under CQC11-471543-2012 and GB4943.1-2011 Basic insulation at 500 V rms (707 V peak) working voltage Reinforced insulation at 250 V rms (353 V peak) NB SOIC-16 File (CQC20001260212) SSOP16 File (CQC20001260213) | Certified under CQC11-471543-2012 and GB4943.1-2011 Basic insulation at 845 V rms (1200 V peak) working voltage Reinforced insulation at 422 V rms (600 V peak) WB SOIC-16 File (CQC20001260258) |

Notes:

¹ In accordance with UL 1577, each $\pi 130E3X/\pi 131E3X$ is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec; each $\pi 130E6X/\pi 131E6X$ is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec

² In accordance with DIN VDE V 0884-11, each $\pi 130E3X/\pi 131E3X$ is proof tested by applying an insulation test voltage ≥ 848 V peak for 1 sec (partial discharge detection limit = 5 pC); each $\pi 130E6X/\pi 131E6X$ is proof tested by ≥ 1800 V peak for 1 sec.

DIN VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS

Table 15.VDE Insulation Characteristics

| Description | Test Conditions/Comments | Symbol | Characteristic | | Unit |
|--|---|--|---------------------------------|---------------------------------|--------|
| | | | $\pi 13x E3x$ | $\pi 13x E6x$ | |
| Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms | | | I to IV I to III I to III | I to IV I to III I to III | |
| Climatic Classification | | | 40/105/21 | 40/105/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | 2 | |
| Maximum repetitive peak isolation voltage | | V _{IORM} | 565 | 1200 | V peak |
| Input to Output Test Voltage, Method B1 | V _{IORM} \times 1.5 = V _{pd(m)} , 100% production test, t _{ini} = t _m = 1 sec, partial discharge < 5 pC | V _{pd(m)} | 848 | 1800 | V peak |
| Input to Output Test Voltage, Method A After Environmental Tests Subgroup 1 | V _{IORM} \times 1.2 = V _{pd(m)} , t _{ini} = 60 sec, t _m = 10 sec, partial discharge < 5 pC | V _{pd(m)} V _{pd(m)} | 678 | 1440 | V peak |

| Description | Test Conditions/Comments | Symbol | Characteristic | | Unit |
|--|--|------------|------------------|------------------|--------------|
| | | | π 13xE3x | π 13xE6x | |
| After Input and/or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC | | 678 | 1440 | V peak |
| Highest Allowable Overvoltage | | V_{IOTM} | 4200 | 7071 | V peak |
| Surge Isolation Voltage Basic | Basic insulation, 1.2/50 μ s combination wave, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification) ¹ | V_{IOSM} | 3615 | 5000 | V peak |
| Safety Limiting Values | Maximum value allowed in the event of a failure (see Figure 5) | | | | |
| Maximum safety Temperature | | T_S | 150 | 150 | $^{\circ}$ C |
| Maximum Power Dissipation at 25 $^{\circ}$ C | | P_S | 1.67 | 2.78 | W |
| Insulation Resistance at T_S | $V_{IO} = 500$ V | R_S | >10 ⁹ | >10 ⁹ | Ω |

Notes:

¹In accordance with DIN V VDE V 0884-11, π 1xxx3x is proof tested by applying a surge isolation voltage 4700 V, π 1xxx6x is proof tested by applying a surge isolation voltage 6500 V.

Typical Thermal Characteristic

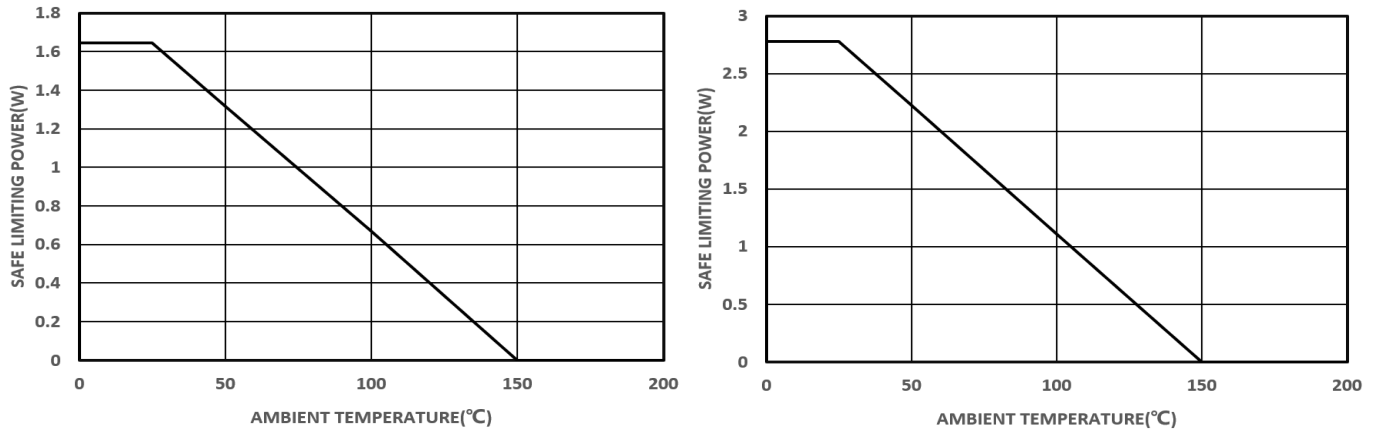


Figure 5. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE (left: π 13xE3x; right: π 13xE6x)

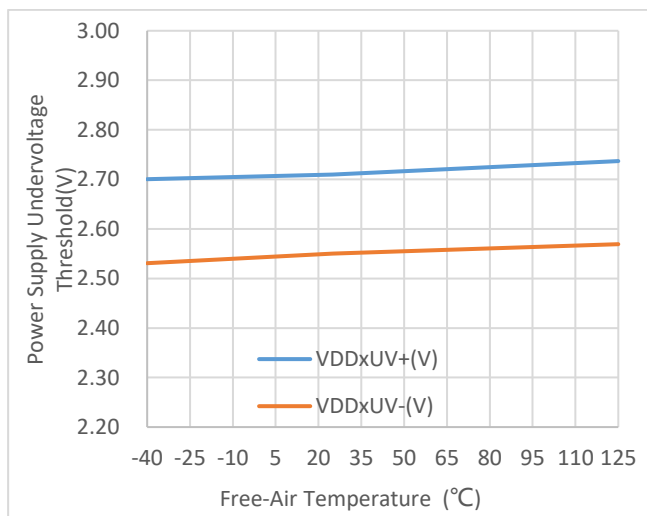


Figure 6. UVLO vs. Free-Air Temperature

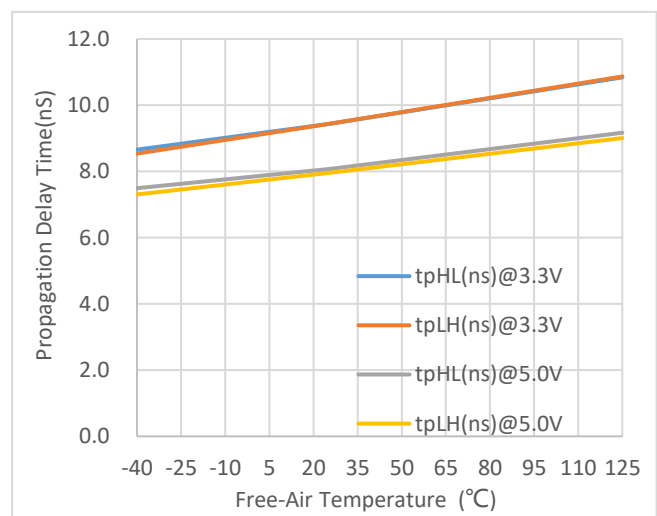


Figure 7. π 13xE3x Propagation Delay Time vs. Free-Air Temperature

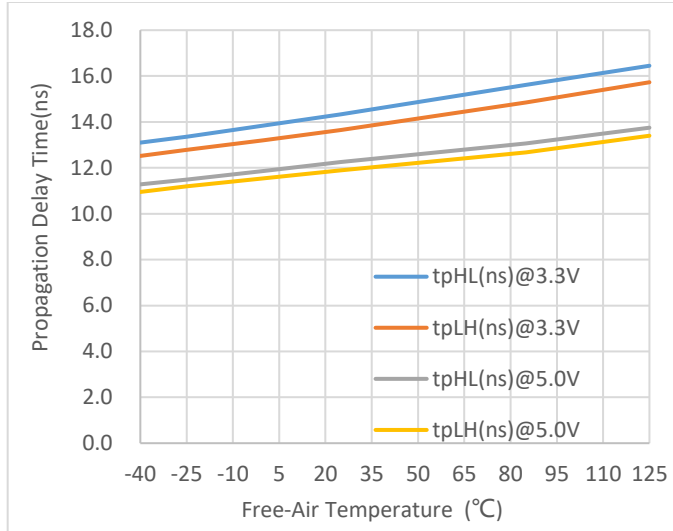


Figure 8. $\pi 13xM6x$ Propagation Delay Time vs. Free-Air Temperature

Timing test information

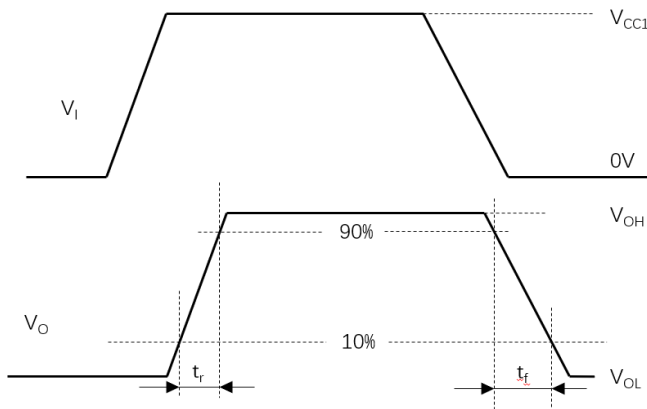


Figure 9. Transition time waveform measurement

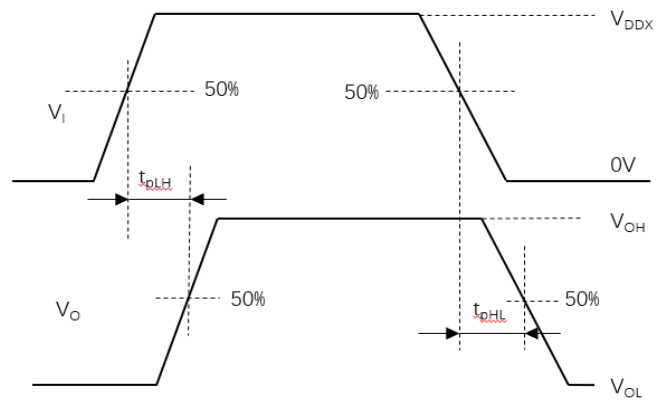


Figure 10. Propagation delay time waveform measurement

APPLICATIONS INFORMATION

OVERVIEW

The $\pi 1xxxx$ are 2PaiSemi digital isolators product family based on 2PaiSemi unique *iDivider*® technology. Intelligent voltage *Divider* technology (*iDivider*® technology) is a new generation digital isolator technology invented by 2PaiSemi. It uses the principle of capacitor voltage divider to transmit signal directly cross the isolator capacitor without signal modulation and demodulation. Compare to the traditional Opto-couple technology, icoupler technology, OOK technology, *iDivider*® is a more essential and concise isolation signal transmit technology which leads to greatly simplification on circuit design and therefore significantly improves device performance, such as lower power consumption, faster speed, enhanced anti-interference ability, lower noise.

By using matured standard semiconductor CMOS technology and the innovative *iDivider*® design, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators. The $\pi 1xxxx$ isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 5.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide).

The $\pi 130Exx/\pi 131Exx$ are the outstanding 200Mbps Triple-channel digital isolators with the enhanced ESD capability. the devices transmit data across an isolation barrier by layers of silicon dioxide isolation.

The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, offering voltage translation of 3.3 V, and 5 V logic. The $\pi 130Exx/\pi 131Exx$ have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

See the Ordering Guide for the model numbers that have the fail-safe output state of low or high.

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between V_{DD1} and GND_1 and between V_{DD2} and GND_2 . The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between 0.1 μF and 10 μF . The user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy, or in order to enhance the anti ESD ability of the system.

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and its return path.

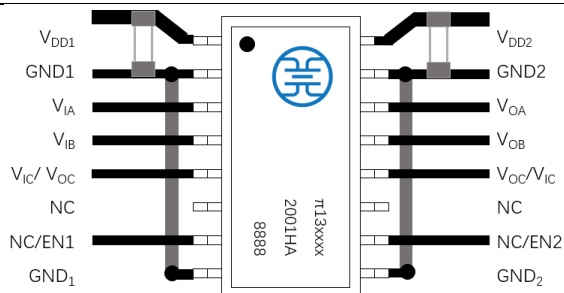


Figure 11. Recommended Printed Circuit Board Layout

JITTER MEASUREMENT

The eye diagram shown in the Figure 12 provides the jitter measurement result for the $\pi 130Exx/\pi 131Exx$. The Keysight 81160A pulse function arbitrary generator works as the data source for the $\pi 130Exx/\pi 131Exx$, which generates 100Mbps pseudo random bit sequence (PRBS). The Keysight DSOS104A digital storage oscilloscope captures the $\pi 130Exx/\pi 131Exx$ output waveform and recovers the eye diagram with the SDA tools and eye diagram analysis tools. The result shows a typical measurement jitter data.

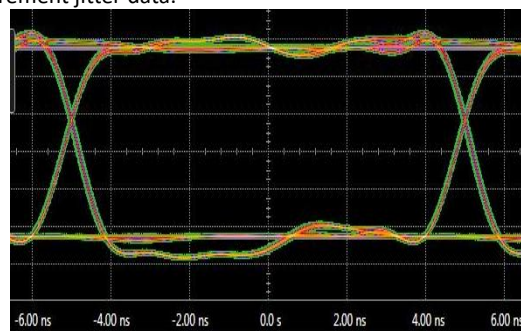


Figure 12. $\pi 130Exx/\pi 131Exx$ Eye Diagram

CMTI MEASUREMENT

To measure the Common-Mode Transient Immunity (CMTI) of $\pi 1xxxx$ isolator under specified common-mode pulse magnitude (VCM) and specified slew rate of the common-mode pulse (dVCM/dt) and other specified test or ambient conditions, The common-mode pulse generator (G1) will be capable of providing fast rise and fall pulses of specified magnitude and duration of the common-mode pulse (VCM), such that the maximum common-mode slew rates (dVCM/dt) can be applied to $\pi 1xxxx$ isolator coupler under measurement. The common-mode pulse is applied between one side ground GND_1 and the other side ground GND_2 of $\pi 1xxxx$ isolator, and shall be capable of providing positive transients as well as negative transients.

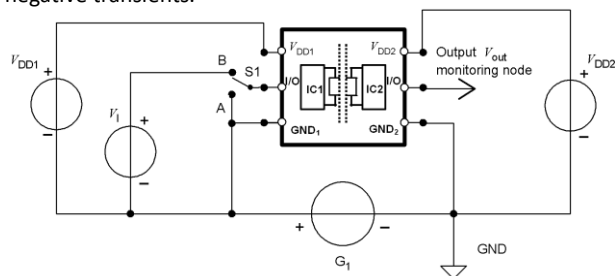


Figure 13. Common-mode transient immunity (CMTI) measurement

OUTLINE DIMENSIONS

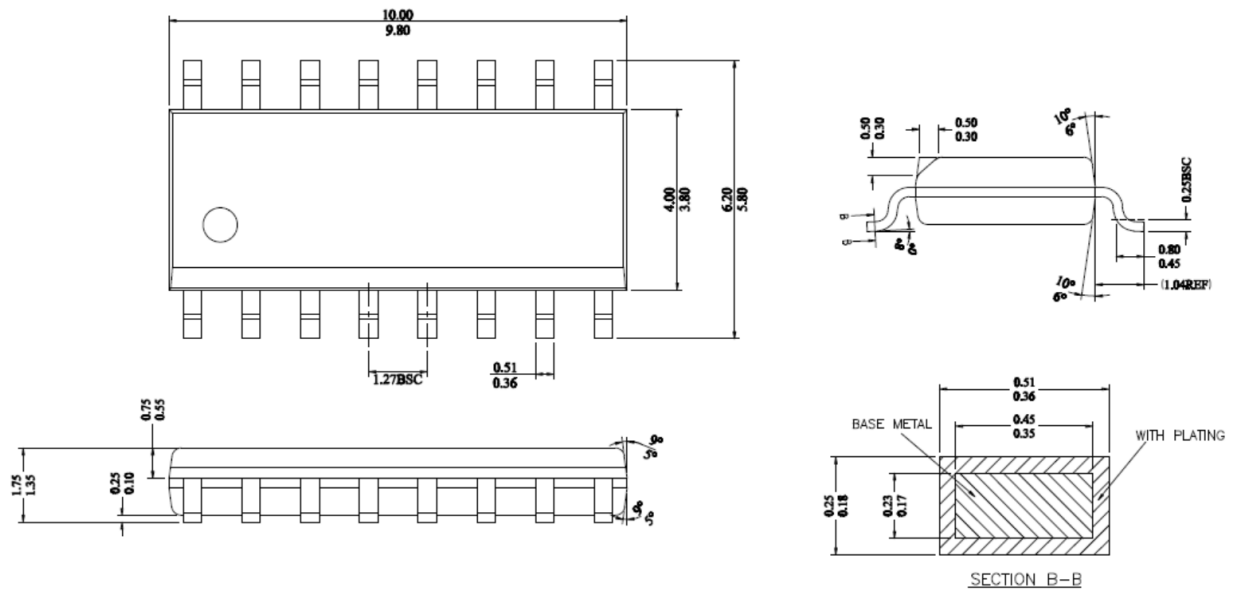


Figure 14. 16-Lead Narrow Body SOIC [NB SOIC-16] Outline Package—dimension unit(mm)

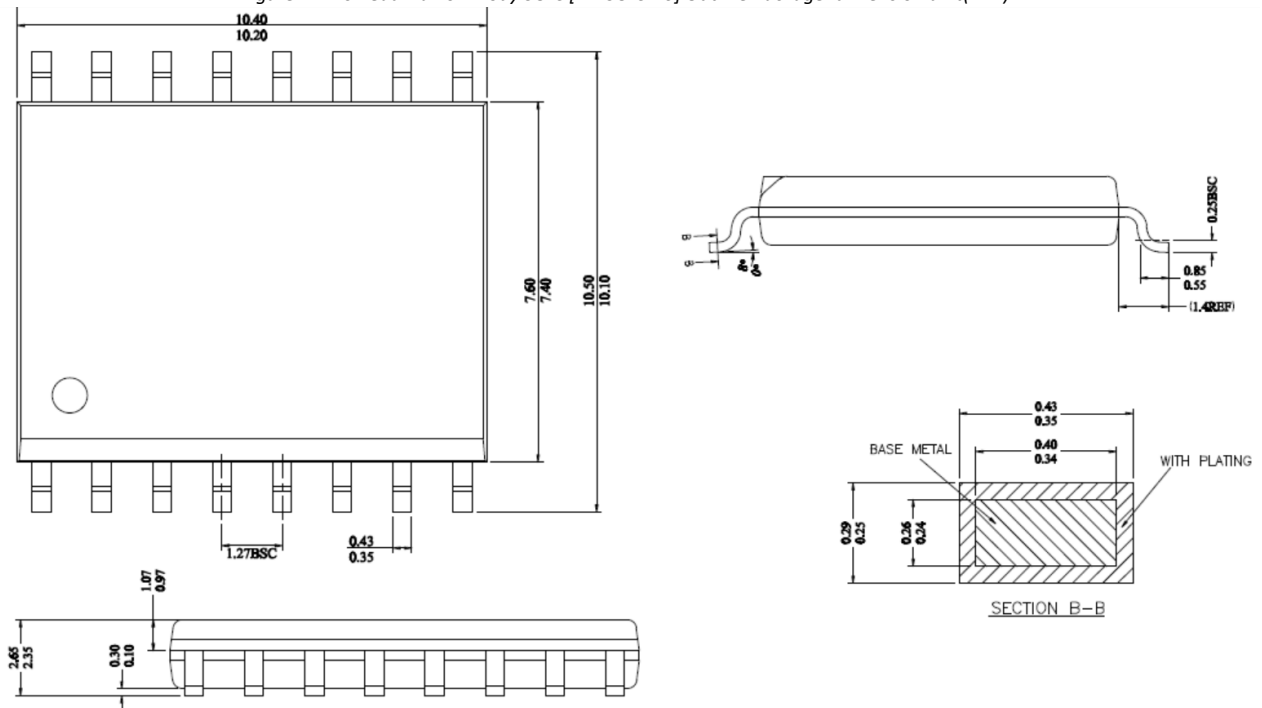
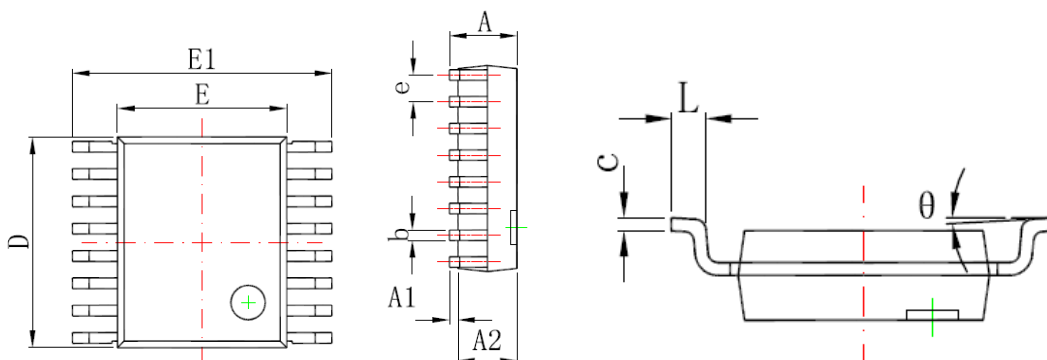


Figure 15. 16-Lead Wide Body SOIC [WB SOIC-16] Outline Package—dimension unit(mm)



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|----------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| c | 0.170 | 0.250 | 0.007 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 0.635(BSC) | | 0.025(BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

Figure 16.16-Lead SSOP [SSOP16] Outline Package

Land Patterns

16-Lead Narrow Body SOIC [NB SOIC-16]

The figure below illustrates the recommended land pattern details for the π 1xxxx in a 16-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

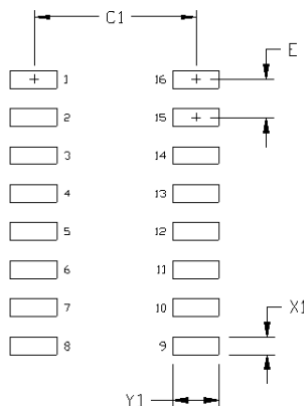


Figure 17.16-Lead Narrow Body SOIC [NB SOIC-16] Land Pattern

Table 16.16-Lead Narrow Body SOIC [NB SOIC-16] Land Pattern Dimensions

| Dimension | Feature | Parameter | Unit |
|-----------|--------------------|-----------|------|
| C1 | Pad column spacing | 5.40 | mm |
| E | Pad row pitch | 1.27 | mm |
| X1 | Pad width | 0.60 | mm |
| Y1 | Pad length | 1.55 | mm |

Note:

- 1.This land pattern design is based on IPC -7351
- 2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

16-Lead Wide Body SOIC [WB SOIC-16]

The figure below illustrates the recommended land pattern details for the π 1xxxx in a 16-pin wide-body SOIC package. The table lists the values for the dimensions shown in the illustration.

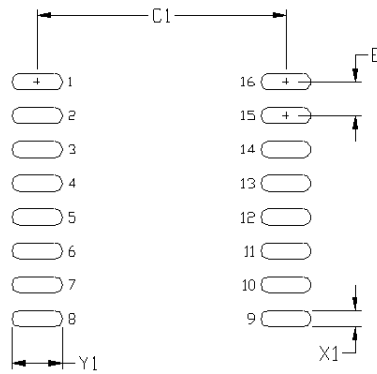


Figure 18. 16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern

Table 17. 16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern Dimensions

| Dimension | Feature | Parameter | Unit |
|-----------|--------------------|-----------|------|
| C1 | Pad column spacing | 9.40 | mm |
| E | Pad row pitch | 1.27 | mm |
| X1 | Pad width | 0.60 | mm |
| Y1 | Pad length | 1.90 | mm |

Note:

- 1.This land pattern design is based on IPC -7351
- 2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

16-Lead SSOP

The figure below illustrates the recommended land pattern details for the π 1xxxx in a 16-Lead SSOP package. The table lists the values for the dimensions shown in the illustration.

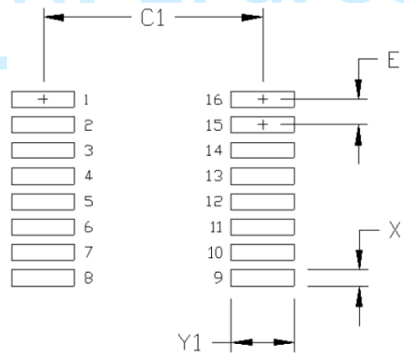


Figure 19. 16-Lead SSOP Land Pattern

Table 18. 16-Lead SSOP Land Pattern Dimensions

| Dimension | Feature | Parameter | Unit |
|-----------|--------------------|-----------|------|
| C1 | Pad column spacing | 5.40 | mm |
| E | Pad row pitch | 0.635 | mm |
| X1 | Pad width | 0.40 | mm |
| Y1 | Pad length | 1.55 | mm |

Note:

- 1.This land pattern design is based on IPC -7351
- 2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

Top Marking

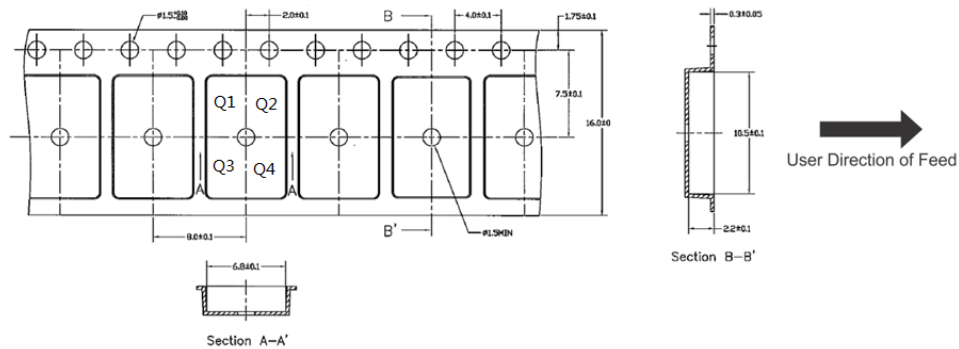


| | |
|--------|---|
| Line 1 | π XXXXXX=Product name |
| Line 2 | YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house |
| Line 3 | XXXX, no special meaning |

Figure 20. Top marking

REEL INFORMATION

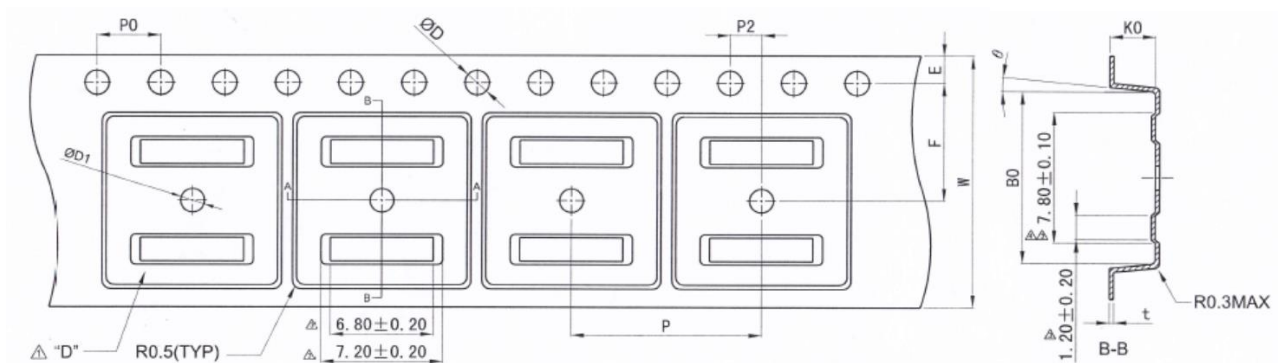
16-Lead Narrow Body SOIC [NB SOIC-16]



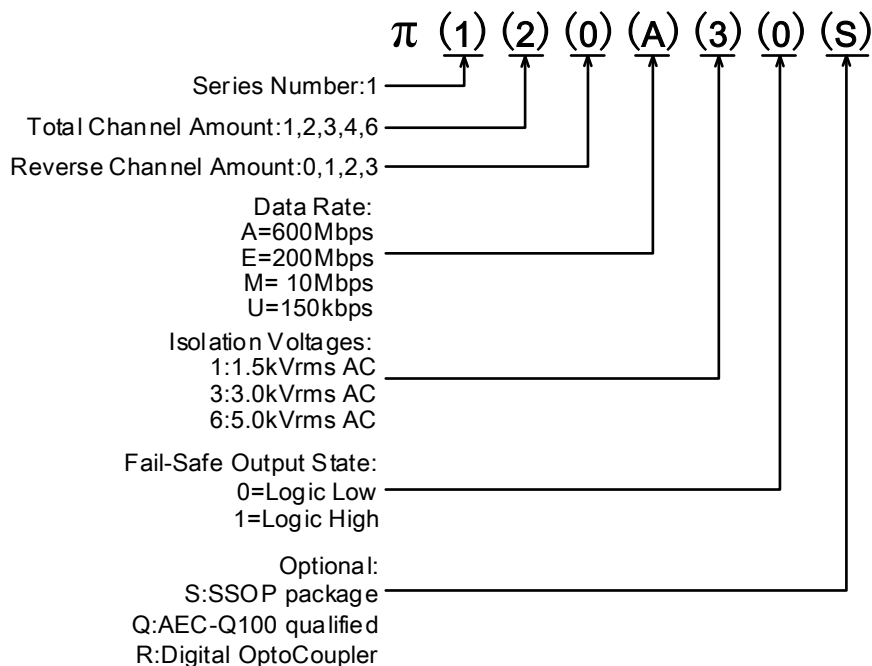
Note: The Pin 1 of the chip is in the quadrant Q1

Figure 21. 16-Lead Narrow Body SOIC [NB SOIC-16] Reel Information—dimension unit(mm)

16-Lead Wide Body SOIC [WB SOIC-16]



PART NUMBER NAMED RULE



Notes:
 Pai1xxxx is equals to π1xxxx in the customer BOM

Figure 24. Part Number Named Rule

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REVISION HISTORY

| Revision | Date | Page | Change Record |
|----------|------------|-------------|---|
| 1.0 | 2018/09/17 | All | Initial version |
| 1.1 | 2018/11/28 | P11 | Changed the recommended bypass capacitor value. |
| 1.2 | 2019/09/08 | Page1 | Changed the contact address. Add <i>iDivider</i> technology description in General Description. Changed propagation delay time, CMTI and HBM ESD. Added WB SOIC-16 Lead information. |
| 1.3 | 2019/12/20 | Page1,11,14 | Changed description of π 1xxx6x. |
| 1.4 | 2020/02/16 | Page1 | Changed propagation delay time. |
| 1.5 | 2020/02/25 | Page5 | Changed Pulse Width Distortion. |
| 1.6 | 2020/03/16 | Page6 | Changed VDDx Undervoltage Threshold and Regulatory Information. Added information of Land Patterns and Top Marking |
| 1.7 | 2020/04/16 | Page12 | Optimize description and format to make it consistent with the Chinese version. |
| 1.8 | 2021/05/17 | Page 1,5~10 | Changed Regulatory Information. Added propagation delay time and supply current of π 1xxE6x. |

