NOVOSENSE
纳芯微电子

NSi66x1A

Single-Channel Isolated Smart Gate Driver

Datasheet (EN) 1.0

Product Overview

The NSi66x1A is a single-channel reinforced isolated smart gate driver to drive IGBTs and SiC MOSFETs inf many applications. It can source and sink 10A peak current. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

The NSi66x1A includes crucial protection features such as miller clamp, DESAT ,UVLO and soft turn off. UVLO and short circuit fault are reported through separate pins. ASC feature is designed to force output on in emergency situation, which supports system fault management.

NSi66x1A is suitable for high reliability, power density and efficiency switching power system.

Key Features

- 5.7kV$_{RMS}$ withstand isolation voltage
- SiC MOSFETs and IGBTs up to 2121V$_{pk}$
- Driver side supply voltage: up to 32V with UVLO
- 10A peak source and sink output current
- High CMTI: ±150kV/us
- 200ns fast response time of DESAT
- Monitor status of device on FLT and RDY
- 80ns typical propagation delay
- 400mA soft turn off current
- 30ns maximum pulse width distortion
- Internal miller clamp
- Active short circuit protection
- Operation ambient temperature: -40°C ~125°C
- RoHS & REACH Compliant
- Lead-free component, suitable for lead-free soldering profile: 260°C, MSL2

Safety Regulatory Approvals

- UL recognition: 5700V$_{RMS}$
- DIN VDE V 0884-11:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2011

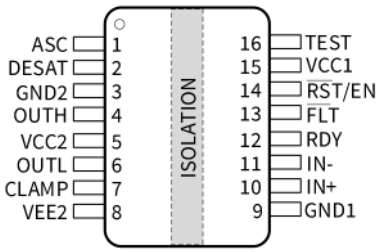
Applications

- Traction Inverter for EVs
- On-board Charger and DC/DC Converter for HEV/EVs
- Industrial Motor Drives and Solar Inverters
- UPS and Power Supplies

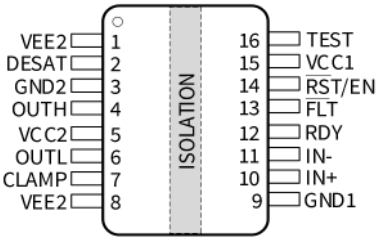
Device Information

Part Number	*Package*	*Body Size*
NSi6611ASC-DSWR	SOW16	10.3mm×7.5mm
NSi6651ASC-DSWR	SOW16	10.3mm×7.5mm
NSi6651ALC-DSWR	SOW16	10.3mm×7.5mm

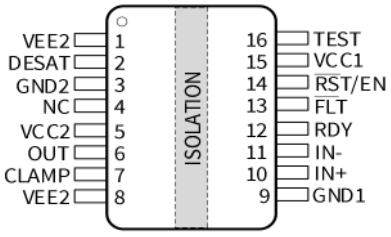
Functional Block Diagram



NSi6611ASC-DSWR



NSi6651ASC-DSWR

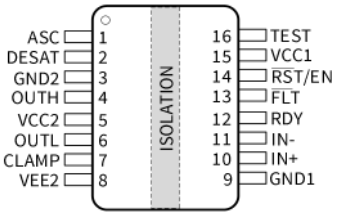


NSi6651ALC-DSWR

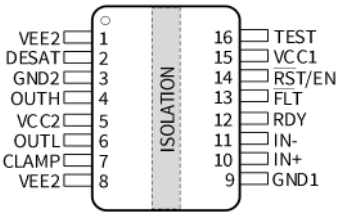
INDEX

1. Pin Configuration and Functions

NSi6611ASC Top View



NSi6651ASC Top View



NSi6651ALC Top View

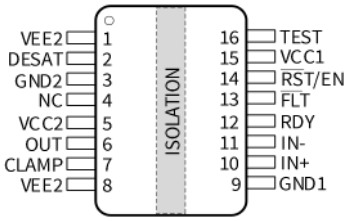


Table 1.1 NSi66x1A Pin Configuration and Description

SYMBOL	*PIN NO.*			*FUNCTION*
	NSi6611ASC	*NSi6651ASC*	*NSi6651ALC*	
ASC	1	/	/	Active Short Circuit pin. If ASC is set to high, the OUTH pin will be forced to output high under the emergency
DESAT	2	2	2	Fast overcurrent and short circuit protection
GND2	3	3	3	Driver side ground pin
OUTH	4	4	/	Driver source output pin
V_{CC2}	5	5	5	Driver side positive supply pin
OUTL	6	6	/	Driver sink output pin
CLAMP	7	7	7	Internal active miller clamp to prevent false turn-on
V_{EE2}	8	1,8	1,8	Driver side negative supply pin
GND1	9,16	9,16	9,16	Input-side ground pin
IN+	10	10	10	Non-inverting gate driver control input
IN-	11	11	11	Inverting gate driver control input
RDY	12	12	12	Power good signal. Active low to report under voltage lock
$\overline{FLT}$	13	13	13	Fault output pin. Active low to report overcurrent or short circuit
$\overline{RST}$	14	14	14	Enable the device if this pin is set to high, or reset the fault signal under DESAT condition if this pin is set to low
V_{CC1}	15	15	15	Input-side power supply
NC	/	/	4	No Connection
OUT	/	/	6	Driver output pin
Test	16	16	16	Test mode pin. It is recommended to connect to GND1

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Max*	*Unit*
Driver Side Supply Voltage	V_{CC2}-V_{EE2}	-0.3	35	V
Driver Side Supply Voltage	V_{CC2}-GND2	-0.3	35	V
Driver Side Supply Voltage	V_{EE2}-GND2	-17.5	0.3	V
Output Signal Voltage - DC	V_{OUTH}, V_{OUTL}, V_{CLAMP}	V_{EE2}-0.3	V_{CC2}	V
Operating Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C
Electrostatic discharge	V_{ESD_HBM}		±3000	V
	V_{ESD_CDM}		±1500	V
Input Side Supply Voltage	V_{CC1}	-0.3	6	V
Input Signal Voltage - DC	V_{IN+}, V_{IN-}, V_{RST}	GND1-0.3	V_{CC1}+0.3	V
RDY, FLT (Input Side)	V_{RDY}, V_{FLT}	GND1-0.3	V_{CC1}	V
FLT and RDY input current	I_{FLT}, I_{RDY}		20	mA
DESAT (Driver Side)	V_{DESAT}	GND2-0.3	V_{CC2}+0.3	V
ASC (Driver Side)	V_{ASC}	GND2-0.3	GND2+6	V

3. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Max*	*Unit*
Ambient Temperature	T_A	-40	125	°C
Input Side Supply Voltage	V_{CC1}-GND1	3	5.5	V
Driver Side Supply Voltage	V_{CC2}-GND2	13	32	V
Driver Side Supply Voltage	V_{CC2}-V_{EE2}	-	32	V
ASC (Driver Side)	V_{ASC}	GND2	GND2+5	V
IN+,IN-,$\overline{RST}$/EN (Respect to GND1)	High level input voltage	0.7×V_{CC1}	V_{CC1}	V
	Low level input voltage	0	0.3×V_{CC1}	

4. Thermal Information

Parameters	*Symbol*	*SOW16*	*Unit*
Junction–to-ambient thermal resistance	$R_{\theta JA}$	97.0	°C/W
Junction–to-top characterization parameter	Ψ_{JT}	35.8	°C/W
Junction–to-board characterization parameter	Ψ_{JB}	39.0	°C/W
Junction–to-case(top) thermal resistance	$R_{JC(top)}$	23.3	°C/W

1) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) in an environment described in JESD51-2a.
2) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) by transient dual interface test method described in JESD51-14.
3) Obtained by Simulating in an environment described in JESD51-2a.

5. Specifications

5.1. DC Electrical Characteristics

All min and max specifications are at T_J=-40°C to 125°C . Typical values are tested at V_{CC1}=3.3V or 5V, V_{CC2} =15 or 30V, V_{EE2}=GND2.

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Condition*
Input Side Supply						
Input side Supply Quiescent Current	I_{CC1}	0.6	1.6	3.6	mA	V_{CC1}=5V,OUT=High
V_{CC1} UVLO Rising Threshold	V_{CC1_ON}	2.5	2.7	2.9	V	
V_{CC1} UVLO Falling Threshold	V_{CC1_OFF}	2.3	2.5	2.7	V	
V_{CC1} UVLO Hysteresis	V_{CC1_HYS}		0.2		V	
V_{CC1} UVLO deglitch time	t_{VCC1_FIL}		10		us	
V_{CC1} UVLO on delay to output high	t_{VCC1H_OUT}		33		us	IN+=V_{CC1} IN-=GND1
V_{CC1} UVLO on delay to output low	t_{VCC1L_OUT}		10		us	
V_{CC1} UVLO on delay to RDY high	t_{VCC1H_RDY}		38		us	$\overline{RST}$/EN=V_{CC1}
V_{CC1} UVLO on delay to RDY low	t_{VCC1L_RDY}		10		us	
Driver Side Supply						
Driver side Supply Quiescent Current	I_{CC2}	2.5	3.3	4.3	mA	V_{CC2}=15V, V_{EE2}=GND2, OUT=High
V_{CC2} UVLO Rising Threshold	V_{CC2_ON}	10.5	11.2	12.8	V	
V_{CC2} UVLO Falling Threshold	V_{CC2_OFF}	9.8	10.4	11.8	V	
V_{CC2} UVLO Hysteresis	V_{CC2_HYS}		0.8		V	
V_{CC2} UVLO deglitch time	t_{VCC2_FIL}		5		us	
V_{CC2} UVLO on delay to output high	t_{VCC2H_OUT}		11		us	IN+=V_{CC1} IN-=GND1
V_{CC2} UVLO on delay to output low	t_{VCC2L_OUT}		10		us	
V_{CC2} UVLO on delay to RDY high	t_{VCC2H_RDY}		11		us	$\overline{RST}$/EN=V_{CC1}, DESAT=GND2
V_{CC2} UVLO on delay to RDY low	t_{VCC2L_RDY}		14		us	
RDY Reporting						
V_{CC2} UVLO RDY low minimum holding time	t_{RDY_HLD}			1	ms	
Open drain low output voltage	V_{RDY_L}			0.3	V	I_{SINK_RDY}=5mA
Input Pin Characteristic						
Logic High Input Threshold (IN+, IN-, RST)	V_{INH}		2.9	3.5	V	V_{CC1}=5V
Logic Low Input Threshold (IN+, IN-, RST)	V_{INL}	1.5	2.1		V	V_{CC1}=5V
Input Hysteresis Voltage (IN+, IN-, RST)	V_{hys_IN}		0.8		V	V_{CC1}=5V
IN+ Input Current	I_{IN+_H}		90		uA	V_{IN+}=5V

DC Electrical Characteristics(continued)

All min and max specifications are at T_J=-40°C to 125°C . Typical values are tested at V_{CC1}=3.3V or 5V, V_{CC2} =15 or 30V, V_{EE2}=GND2.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
IN- Input Current	I_{IN-_L}		-90		uA	V_{IN-}=GND1
ASC Pin Characteristic (only for NSi6611ASC)						
Logic High Input Threshold (ASC)	V_{ASCH}	2.7	2.9	3.2	V	
Logic Low Input Threshold (ASC)	V_{ASCL}	1.3	1.5	1.7	V	
ASC to output rising edge delay	t_{ASC_r}	390	560	1100	ns	
ASC to output falling edge delay	t_{ASC_f}	150	360	480	ns	
Enable Pin Characteristic						
RST deglitch filter time for Enable/Shutdown	t_{min_RST}	28	40	60	ns	
Output Pin Characteristic						
High Level Output Voltage	V_{OH}		V_{CC2}-0.6		V	I_{OUT}=-200mA, V_{IN+}=High, V_{IN-}=Low
Low Level Output Voltage	V_{OL}		0.1		V	I_{OUT}=200mA, V_{IN+}=Low, V_{IN-}=Low
Output pull-up resistance	R_{OH}		2.2		Ω	I_{OUT}=-0.1A, V_{IN+}=High, V_{IN-}=Low
Output pull-down resistance	R_{OL}		0.3		Ω	I_{OUT}=0.1A, V_{IN+}=Low, V_{IN-}=High
Low Level Clamp Voltage	V_{CLAMP}		V_{EE2}+0.8		V	I_{CLAMP}=1A, V_{IN+}=Low, V_{IN-}=Low
High Level Peak Output Current	I_{OUTH}		11		A	V_{CC2}=15V, pulse width<10us
Low Level Peak Output Current	I_{OUTL}		12		A	
			8		A	V_{OUT}=V_{EE2}+2.5V
Clamp Threshold Voltage	$V_{CLAMP-TH}$	1.5	2	2.5	V	V_{CLAMP} falling, V_{IN+}=Low, V_{IN-}=Low
Calmp Delay	t_{DCLMP}		60		ns	
OUT Short Circuit Clamping Voltage	V_{CLP_OUT}		V_{CC2}+1.1	V_{CC2}+2	V	V_{IN+}=High, V_{IN-}=Low, I_{OUTL}=0.5A, pulse width<10us
CLAMP Short Circuit Clamping Voltage	V_{CLP_CLAMP}		V_{CC2}+1.8	V_{CC2}+2.5	V	V_{IN+}=High, V_{IN-}=Low, I_{OUTH}=0.5A, pulse width<10us
			V_{CC2}+0.8		V	V_{IN+}=High, V_{IN-}=Low, I_{CLAMP}=20mA
OUT Active Pull-Down Voltage	V_{SD_OUT}	1.5	2.3	3.1	V	V_{CC2}=OPEN, I_{OUTL}=0.1×I_{OUTL}(typ)

DC Electrical Characteristics(continued)

All min and max specifications are at T_J=-40°C to 125°C . Typical values are tested at V_{CC1}=3.3V or 5V, V_{CC2} =15 or 30V, V_{EE2}=GND2.

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Condition*
Desaturation						
Blanking Capacitor Discharge Current	I_{DCHG}	12	14		mA	V_{DESAT}=6V
Blanking Capacitor Charge Current	I_{CHG}	430	500	600	uA	V_{DESAT}=2V
Detection Threshold	V_{DESAT_TH}	8.5	9.26	9.8	V	
Leading edge blank time	t_{DESAT_LEB}		200		ns	
DESAT deglitch filter time	t_{DESAT_FIL}	150	200	265	ns	
DESAT sense to OUT(L) 90% delay	t_{DESAT_OFF}	150	250	300	ns	
DESAT sense to FLT low delay	t_{DESAT_FLT}	400	650	750	ns	
FLT mute time	t_{FLT_MUTE}	0.55		1	ms	
RST deglitch filter time for Reseting FLT	t_{RST_FIL}	400	600	800	ns	
Soft turn off						
Soft turn off current	I_{STO}	250	400	570	mA	
FLT Reporting						
Open drain low output voltage	V_{FLT_L}			0.3	V	I_{SINK_FLT}=5mA

5.2. Switching Electrical Characteristics

Typical values are at V_{CC1}=5V, V_{CC2} =15V, V_{EE2}=GND2. All min and max specifications are at T_J=-40°C to 125°C， C_L=0.1nF

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Condition*
Minimum Pulse Width	$t_{PWmin\_IN+, IN-}$	20	40	70	ns	
Output Rise Time	t_R		56		ns	C_{LOAD}=10nF
Output Fall Time	t_F		53		ns	
Propagation Delay	$t_{pLH\_IN+, IN-}$	70	80	110	ns	C_{LOAD}=0.1nF
	$t_{pHL\_IN+, IN-}$	70	80	110	ns	
Pulse Width Distortion $\lvert t_{PHL}-t_{PLH}\rvert$	t_{PWD}			30	ns	
Common Mode Transient Immunity	CMTI	150			kV/us	

5.3. Typical Characteristics

V_{CC1}= 5V, V_{CC2} =15, V_{EE2}=GND2 for NSi66x1A. Output has no load unless otherwise noted.

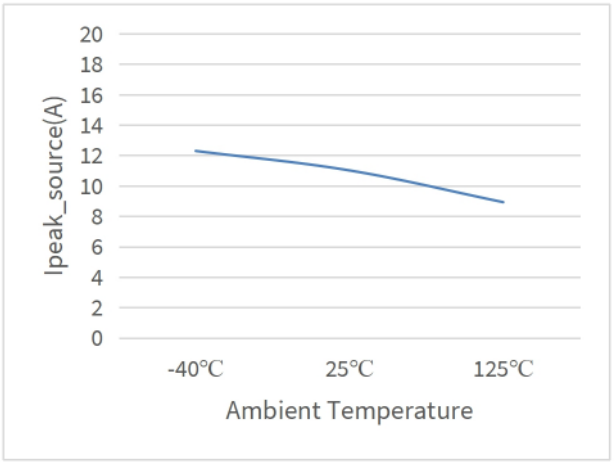


Figure 5.1 I_{peak_source} vs Temperature

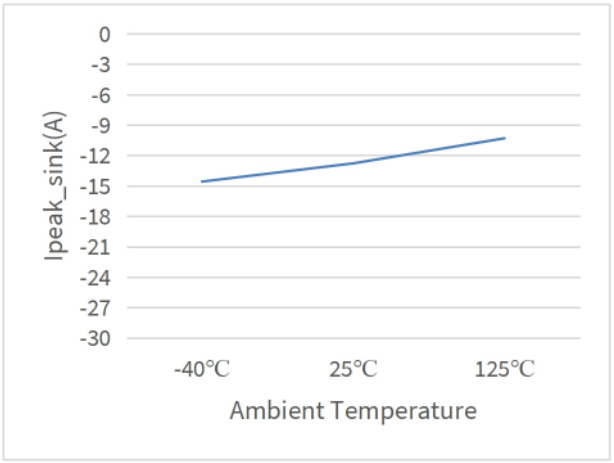


Figure 5.2 I_{peak_sink} vs Temperature

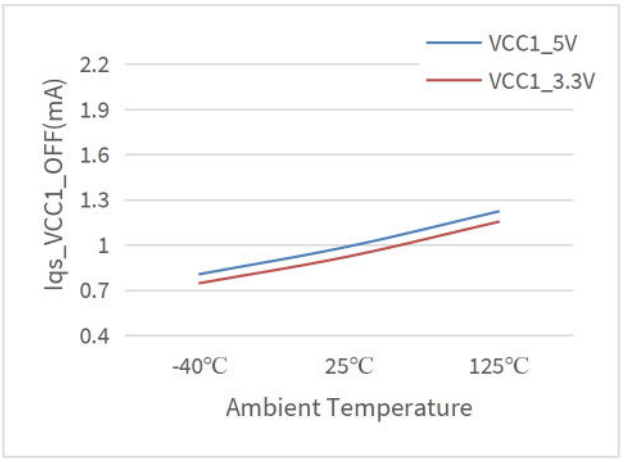


Figure 5.3 $I_{qs\_VCC1\_OFF}$ vs Temperature

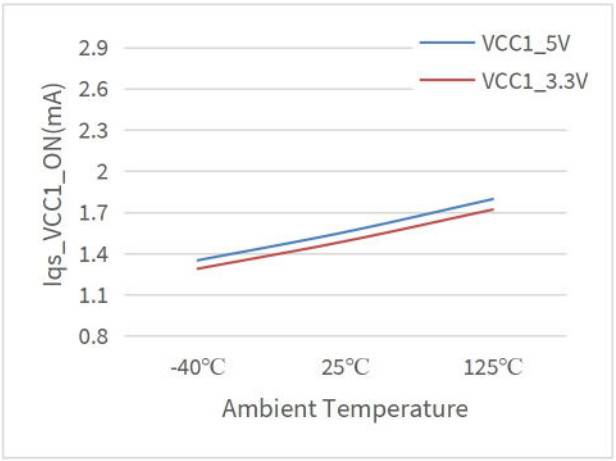


Figure 5.4 $I_{qs\_VCC1\_ON}$ vs Temperature

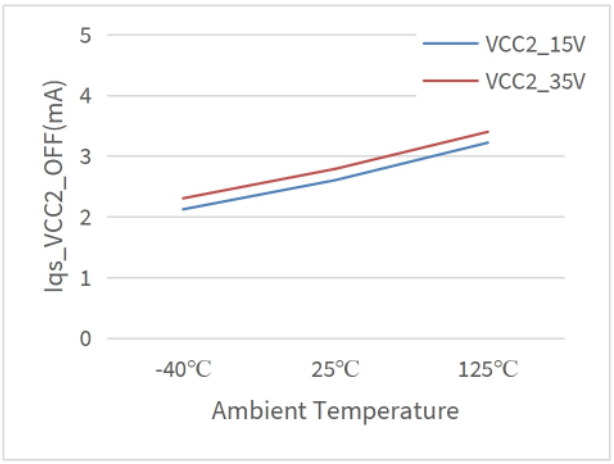


Figure 5.5 $I_{qs\_VCC2\_OFF}$ vs Temperature

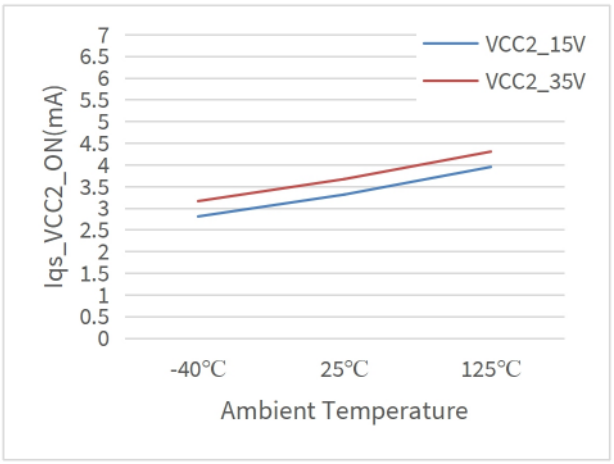


Figure 5.6 $I_{qs\_VCC2\_ON}$ vs Temperature

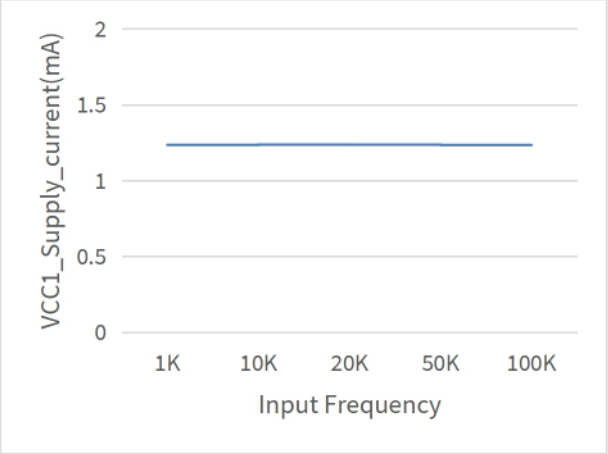


Figure 5.7 V_{CC1} Supply current vs Input Frequency

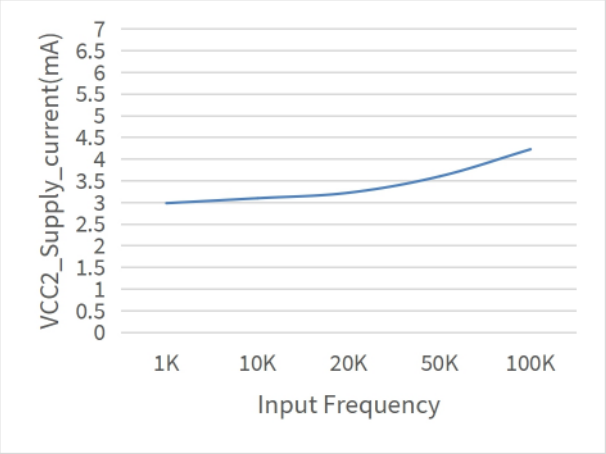


Figure 5.8 V_{CC2} Supply current vs Input Frequency

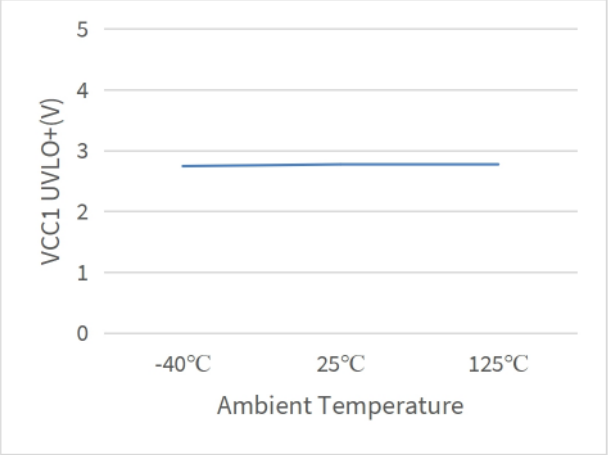


Figure 5.9 V_{CC1} UVLO+ vs Temperature

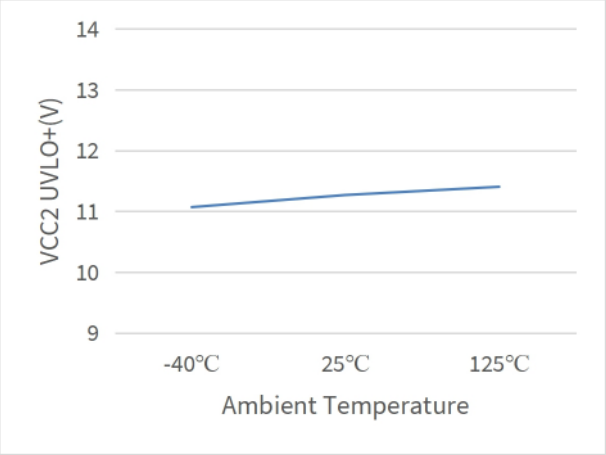


Figure 5.10 V_{CC2} UVLO+ vs Temperature

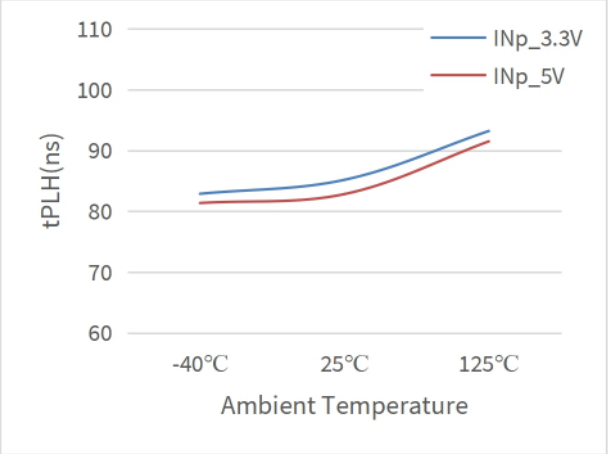


Figure 5.11 t_{PLH} vs Temperature

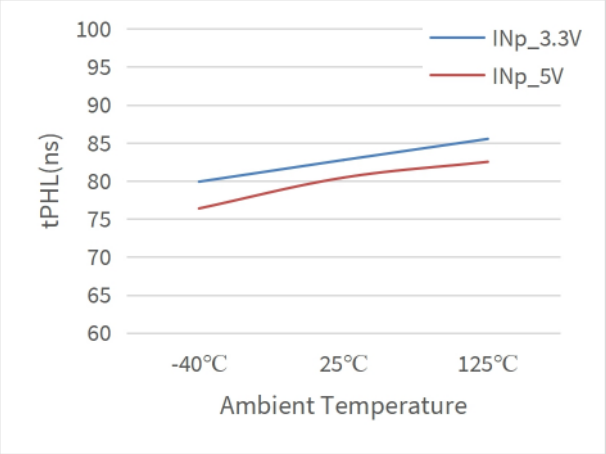


Figure 5.12 t_{PHL} vs Temperature

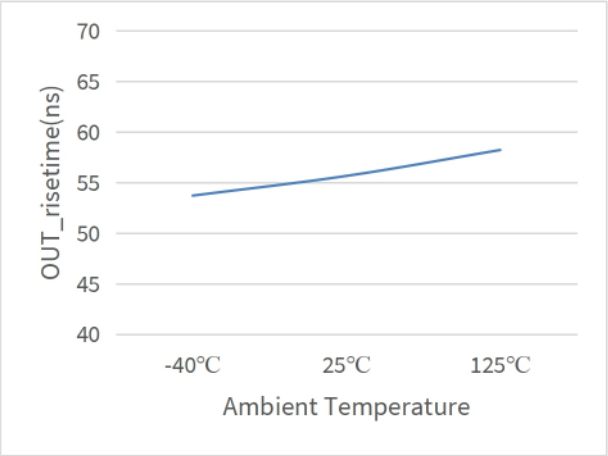


Figure 5.13 OUT_risetime vs Temperature

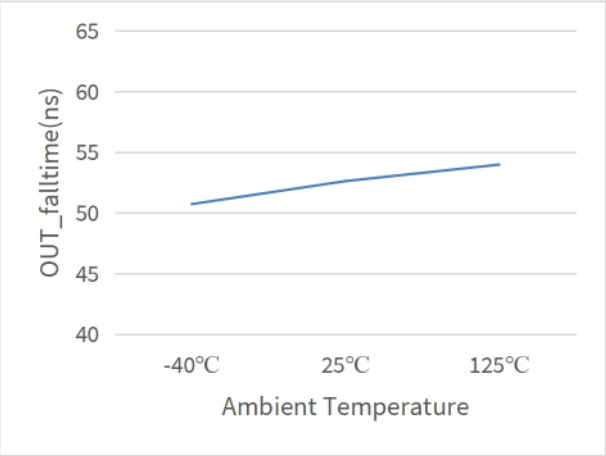


Figure 5.14 OUT_falltime vs Temperature

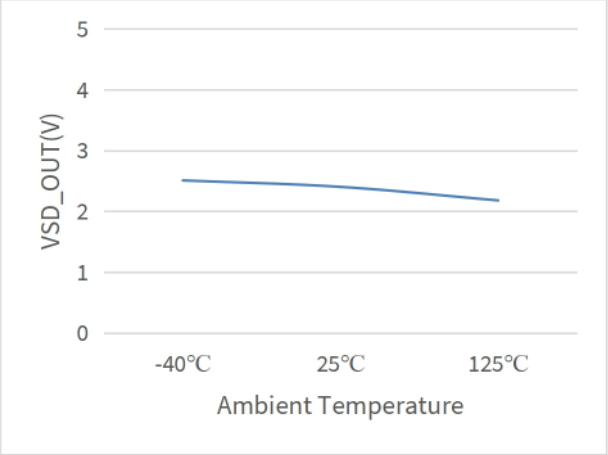


Figure 5.15 V_{SD_OUT} vs Temperature

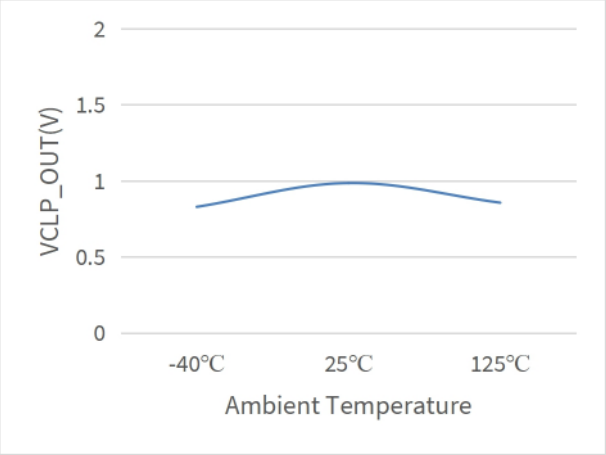


Figure 5.16 V_{CLP_OUT} vs Temperature

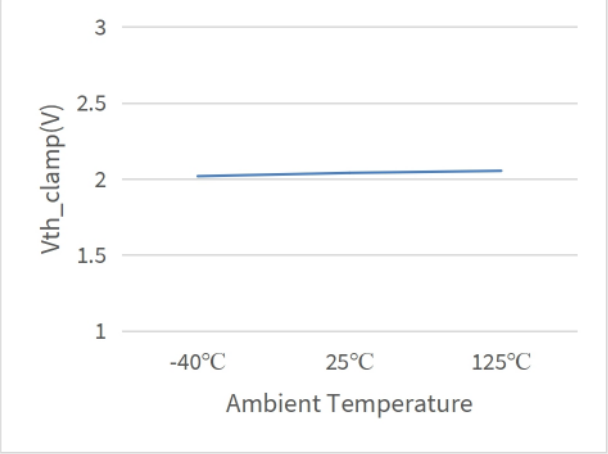


Figure 5.17 V_{th_clamp} vs Temperature

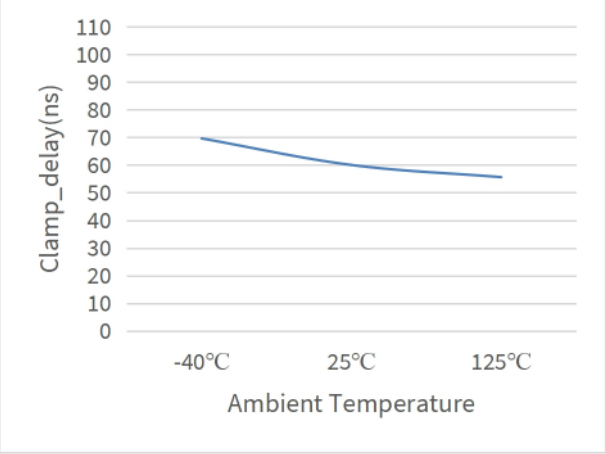


Figure 5.18 Clamp_delay vs Temperature

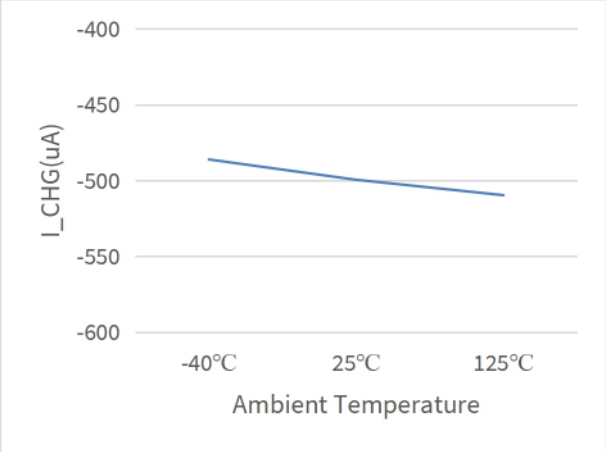


Figure 5.19 I_CHG vs Temperature

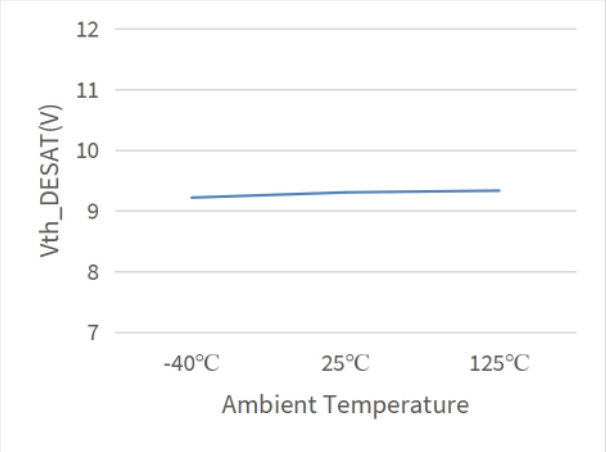


Figure 5.20 DESAT Threshold Voltage vs Temperature

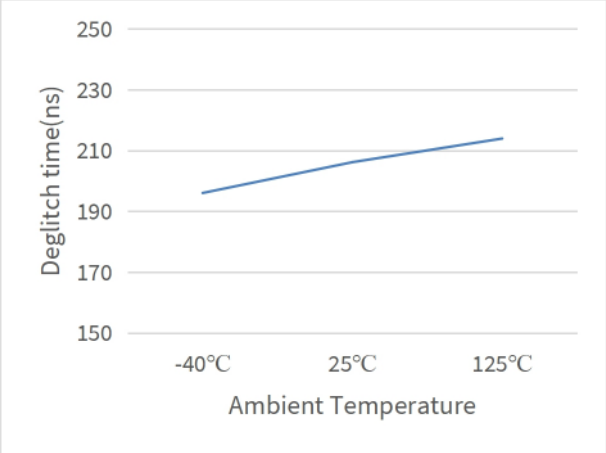


Figure 5.21 Deglitch time vs Temperature

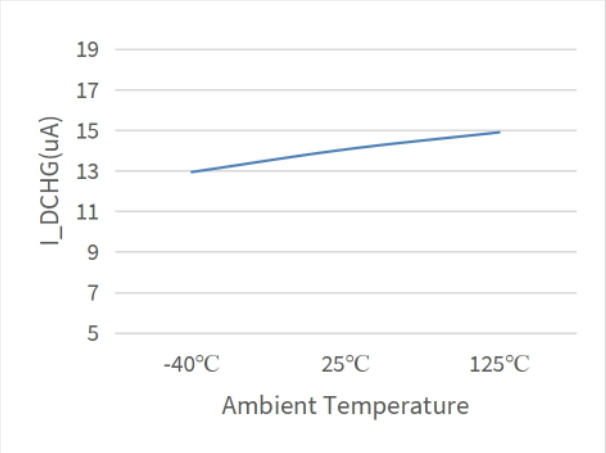


Figure 5.22 I_DCHG vs Temperature

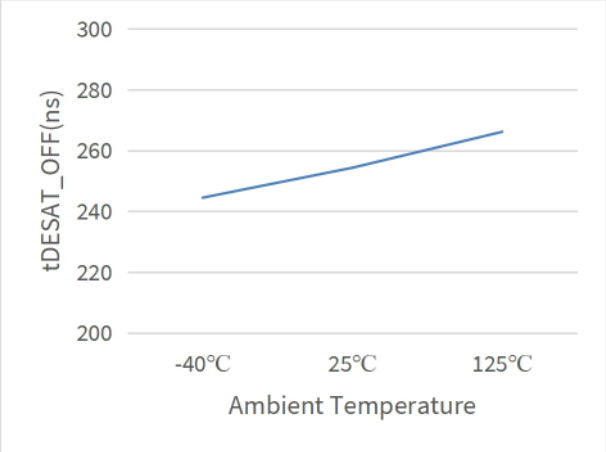


Figure 5.23 t_{DESAT_OFF} vs Temperature

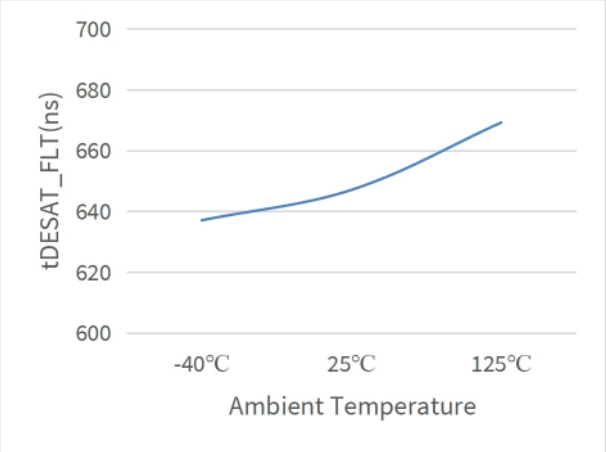


Figure 5.24 t_{DESAT_FLT} vs Temperature

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameter	*Symbol*	*SOW16*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	CLR	8.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8.0	mm	Shortest terminal-to-terminal distance across the package surface
Distance Through Insulation	DTI	20	um	Minimum internal gap
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		

6.2. DIN VDE V 0884-11 (VDE V 0884-11): 2017-01 Insulation Characteristics for SOW16 Package

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 600V_{RMS}			I to III	
For Rated Mains Voltage ≤ 1000V_{RMS}			I to II	
Climatic Category			40/125/21	
Pollution Degree			2	
Maximum Working Isolation Voltage		V_{IOWM}	1500	V_{RMS}
			2121	V_{DC}
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	2121	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{pd(m)}$=V_{IORM}×1.875, 100% production test, t_{ini}=t_m=1s, partial discharge<5pC	$V_{pd(m)}$	3977	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{pd(m)}$=V_{IORM}×1.6, t_{ini}=60s, t_m=10s, partial discharge <5pC	$V_{pd(m)}$	3394	V_{PEAK}
After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{pd(m)}$=V_{IORM}×1.2, t_{ini}=60s, t_m=10s, partial discharge <5pC	$V_{pd(m)}$	2545	V_{PEAK}
Maximum Transient Isolation Voltage	t = 60 s	V_{IOTM}	8000	V_{PEAK}
Maximum Withstanding Isolation Voltage	V_{TEST}= V_{ISO}, t = 60 s (qualification); V_{TEST}= 1.2 ×V_{ISO}, t = 1 s (100%production)	V_{ISO}	5700	V_{RMS}
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, V_{TEST}=V_{IOSM}×1.6	V_{IOSM}	6250	V_{PEAK}
Isolation Resistance	V_{IO}=500V at T_A=T_S=150°C	R_{IO}	>10^9	Ω
	V_{IO}=500V at 100°C≤T_A≤125°C		>10^{11}	Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1	pF

6.3. Safety Limiting Values for SOW16 Package

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
Maximum Safety Temperature		T_S	150		°C
Maximum Safety Power Dissipation	$R_{\theta JA}$=97°C/W, T_J=150°C, V_{CC2}=20V, V_{EE2}=-5V T_A=25°C	P_S	Total	1288	mW
Maximum Safety Current	$R_{\theta JA}$=97°C/W, V_{CC2}=15V, V_{EE2}=-5V T_J=150°C, T_A=25°C	I_S	Driver side	64.4	mA
	$R_{\theta JA}$=97°C/W, V_{CC2}=20V, V_{EE2}=-5V T_J=150°C, T_A=25°C		Driver side	51.5	

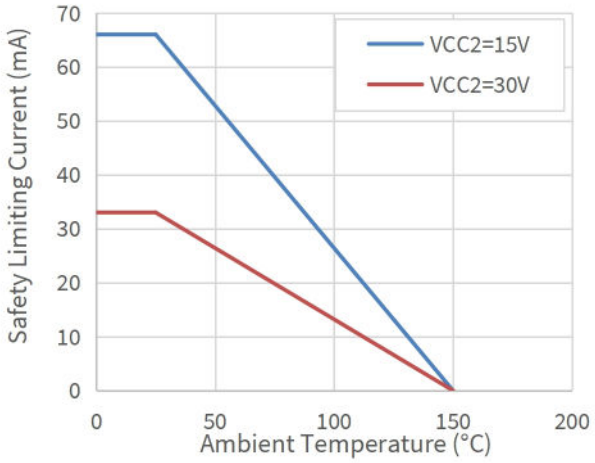


Figure 6.1 Thermal Derating Curve for Limiting Current per DIN VDE V 0884-11 for SOW16(300 mil) Package

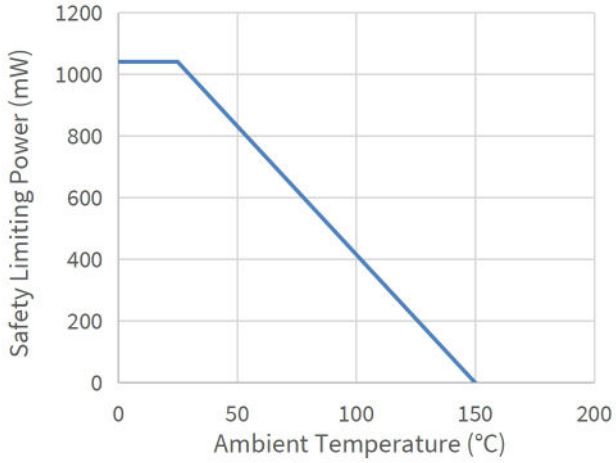


Figure 6.2 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-11 for SOW16 Package

6.4. Regulatory Information for SOW16 Package

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, $5700V_{RMS}$ Isolation Voltage	Single Protection, $5700V_{RMS}$ Isolation voltage	Reinforced Insulation $V_{IORM}=2121V_{PEAK}$, $V_{IOTM}=8000V_{PEAK}$, $V_{IOSM}=6250V_{PEAK}$	Reinforced Insulation
File (pending)	File (pending)	File (pending)	File (pending)

7. Function Description

7.1. Overview

The NSi66x1A is a high reliable power transistor gate driver. It can source and sink 10A peak current, which is suitable to drive MOSFET, IGBT, or SiC MOSFET. The NSi66x1A is available in SOW16 package, which can support 5700V_{RMS} isolation per UL1577. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

Besides, the NSi66x1A includes crucial protection features such as miller clamp, DESAT short circuit detection and soft turn off. UVLO and short circuit fault are reported through separate pins. ASC feature is designed to force output ON in emergency situation, which supports system fault management.

The isolation barrier inside NSi66x1A is based on a capacitive isolation. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI. The digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side.

The functional block diagram of NSi66x1A is shown in Figure 7.1. Two Input pins with non-inverting and inverting logic support interlock and shoot through protection. Low resistance of high side and low side MOSFET in the output stage ensures high driving capability. Split outputs can control the rise and fall time individually. Active pull-down and short circuit clamping features are implemented to protect power transistor.

In summary, the NSi66x1A is suitable to replace source and sink reinforced gate driver in high reliability, power density and efficiency switching power system.

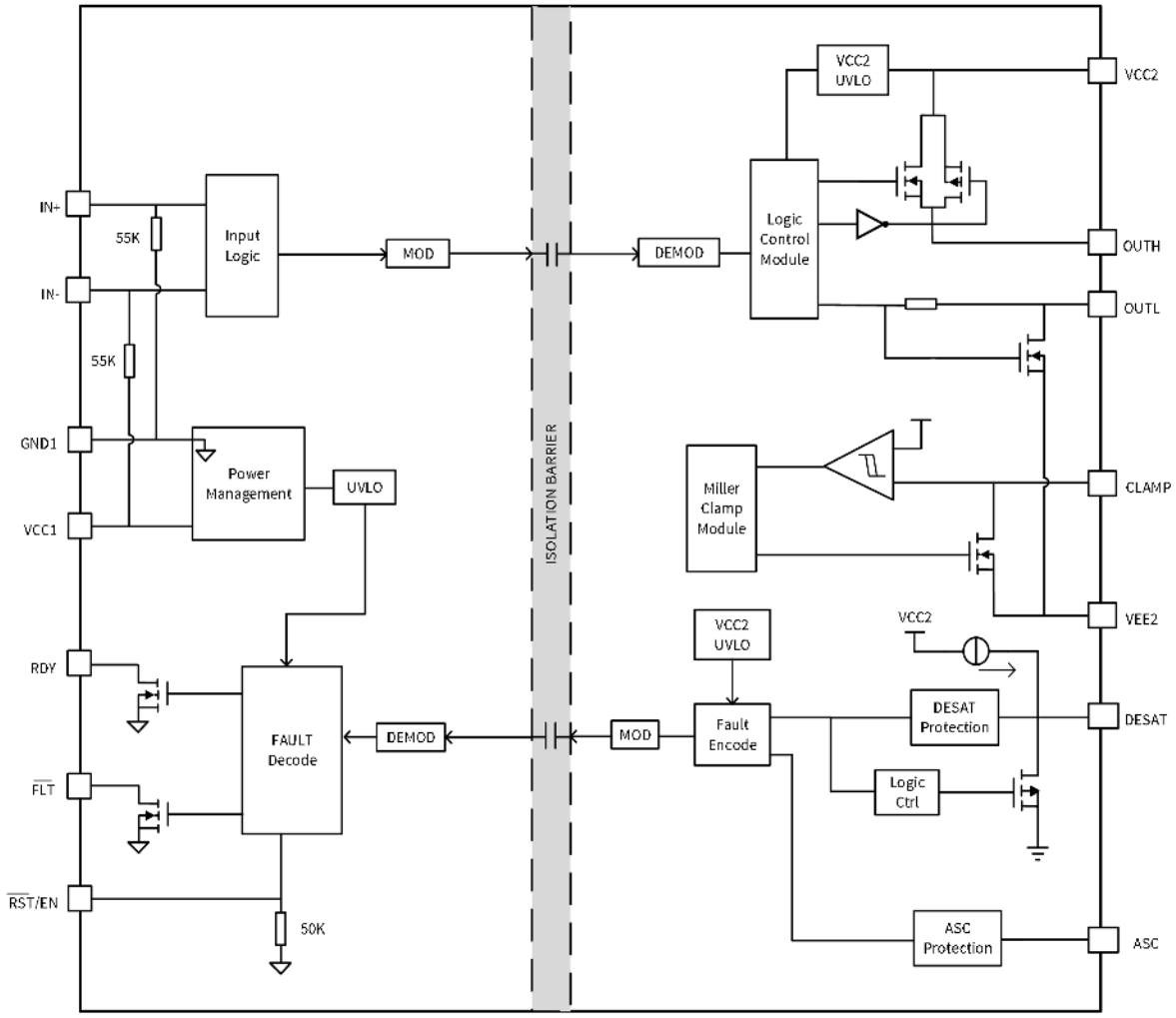


Figure 7.1 NSi66x1A Function Block Diagram

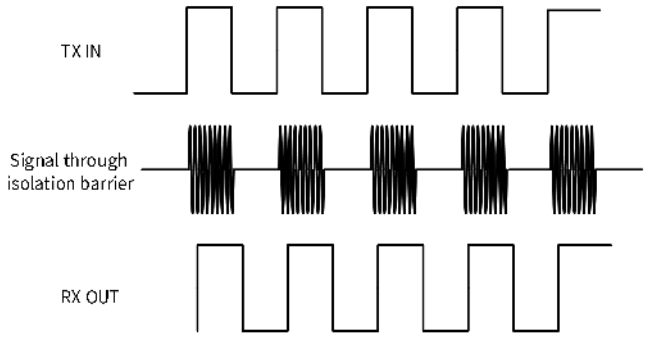


Figure 7.2 OOK Modulation

7.2. Power Supply

Power supply V_{CC1} is able to support from 3.3V to 5.5V. Power supply V_{CC2} is able to support from 13V to 32V. To be mentioned, NSi66x1A also supports bipolar power supply mode on the driver side. In the case of fast switching speed, the negative power supply is crucial to prevent false turn on from parasitic Miller capacitor.

7.3. Output Stage

The NSi66x1A has P-channel and N-channel MOSFET in parallel to pull up the OUTH pin when turning on external power transistor. During DC measurement, only the P-channel MOSFET is conducting. The measurement result R_{OH} represents the on-resistance of P-channel MOSFET. The voltage and current of external power transistor drain to source or collector to emitter change during turn on. At that time, the NSi66x1A N-channel MOSFET turns on to pull up OUTH more quickly. It results external power transistor faster turn on time, lower turn on power loss, also leads to lower temperature increase of NSi66x1A. The equivalent pull-up resistance of NSi66x1A is the parallel combination ROH || RNMOS. The result is quite small, indicating the strong driving capability of NSi66x1A.The pull-down structure of NSi66x1A is simply composed of an N-channel MOSFET with on-resistance of R_{OL}. The result is quite small, indicating the strong driving capability of NSi66x1A.

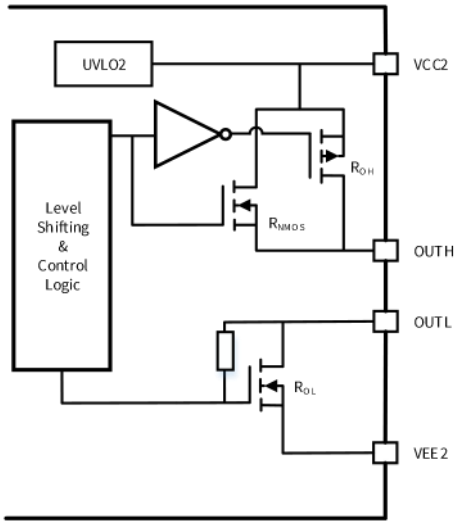


Figure 7.3 NSi66x1A output stage

7.4. V_{CC2} and Under Voltage Lock Out(UVLO)

To ensure correct switching NSi66x1A is equipped with an under voltage lockout for input and output power supply independently. V_{CC1} voltage should not fall below the UVLO threshold for normal operation, or the gate-driver output can become clamped low. Output supply UVLO is referred to GND2 pin. If V_{CC2}-GND2 falls below the UVLO threshold, OUTL of the gate-driver will be clamped low.

Local bypass capacitors should be placed between the V_{CC2} and GND2 pins, as well as the V_{CC1} and GND1 pins. 220-nF to 10- μ F is recommended for device biasing. Additional 100nF capacitor in parallel with the device biasing capacitor is recommended for high frequency filtering. The capacitors should be positioned as close to the device as possible for better noise filtering. Low-ESR,

ceramic surface-mount capacitors are recommended. The RDY pin will report a power good signal if the device is out of UVLO condition.

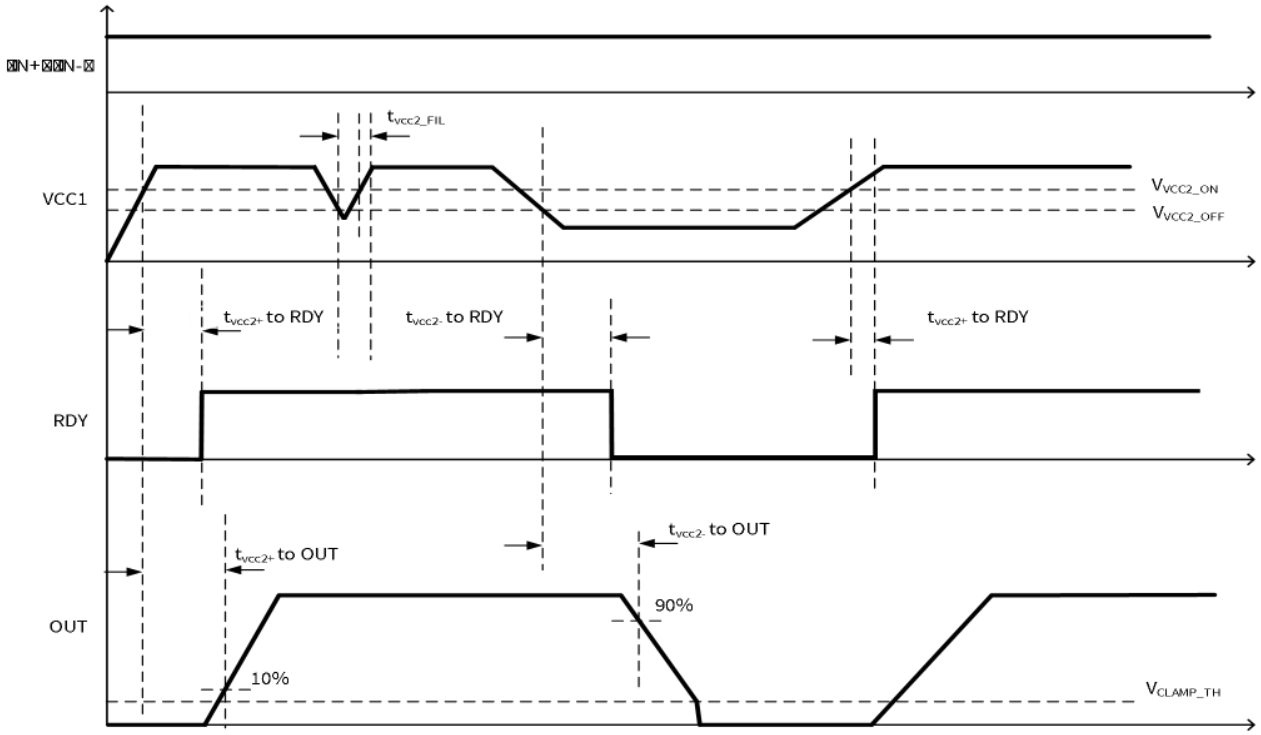


Figure 7.4 RDY vs V_{CC1} timing Diagram

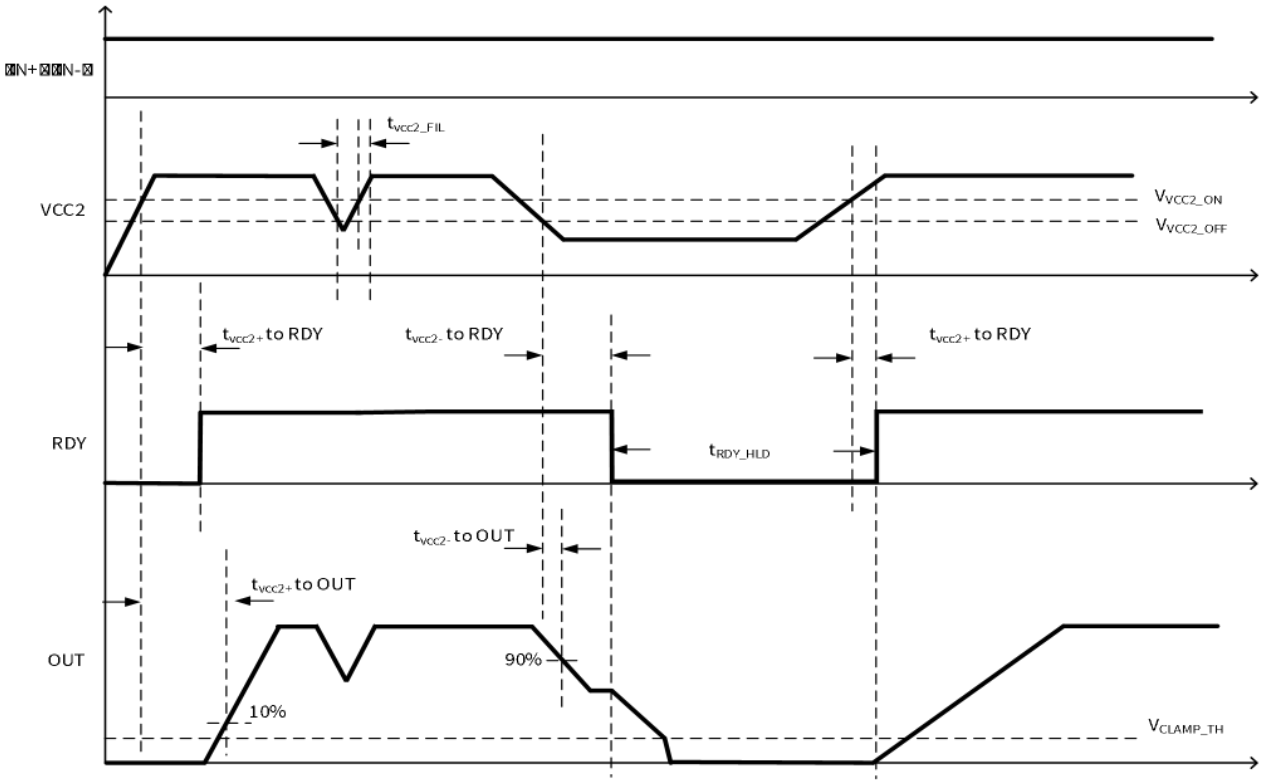


Figure 7.5 RDY vs V_{CC2} timing Diagram

7.5. Active Pull-Down

The Active Pull-Down feature ensures a safe IGBT or MOSFET off-state if V_{CC2} is not connected to the power supply. When V_{CC2} is floating, the driver output is held low and clamping OUT to approximately 1.8V higher than V_{EE2}.

7.6. Short circuit Clamping

During short circuit the gate voltage of IGBT or MOSFET tends to rise because of the feedback via the miller capacitance. The diode between OUTH/CLAMP and VCC2 pins inside the driver limits this voltage to approximately 0.7V higher than the supply voltage. A maximum current of 500mA may be fed back to the supply through this path for 10 μ s. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

7.7. Internal Active Miller Clamp

Active miller clamp is used to prevent false turn on. After the external power transistor is turned off, the other one of the phase leg is turned on. The voltage of the drain-source or collector-emitter rises instantly. The dv/dt will cause a high current on miller parasitic capacitor. The voltage-drop on the gate resistor possibly turn on the external power transistor unintentionally, which will cause a catastrophic damage. To deal with that, NSi66x1A is equipped with a miller clamp pin. The clamp pin detects the gate voltage of IGBT or MOSFET. When the gate voltage is decreasing and reaches the V_{CLAMP_TH}, the clamp pin will be pulled down by the internal MOSFET, providing a low impedance path to avoid the false turn on. To be mentioned, the V_{CLAMP_TH} is 2V higher than V_{EE2}. In the situation of fast switching speed, the negative power supply is necessary to avoid false turn on.

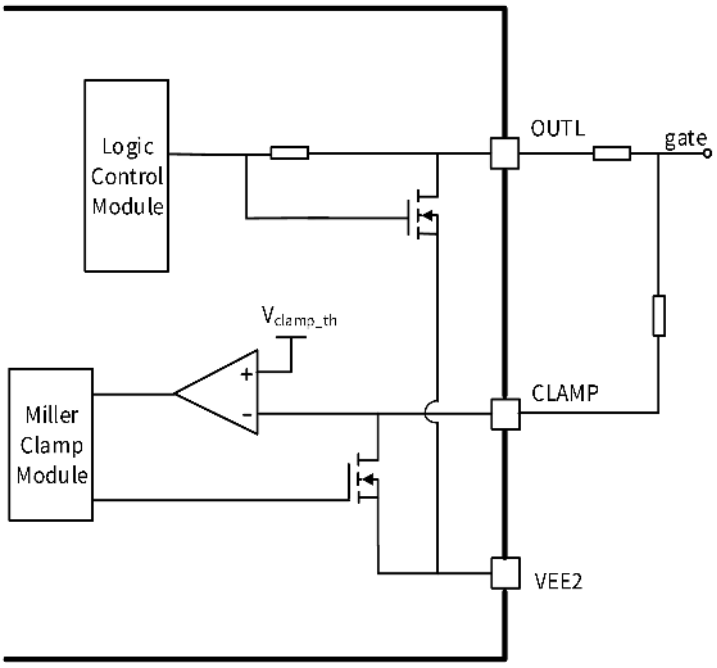


Figure 7.6 Active Miller Clamp

7.8. Desaturation (DESAT) Protection

Desaturation protection is used to prevent the power transistor from short circuit. The DESAT pin has a typical 9V threshold, which means the output will be driven low if DESAT pin reaches 9V. By default, the DESAT pin is pulled down by internal MOSFET. The internal 500 μ A current source is designed to work only when the output is high level. There is a 200ns leading edge blanking time to filter the overshoot when the external power transistor is turned on. The current source begin to charge after the internal leading edge blanking time.

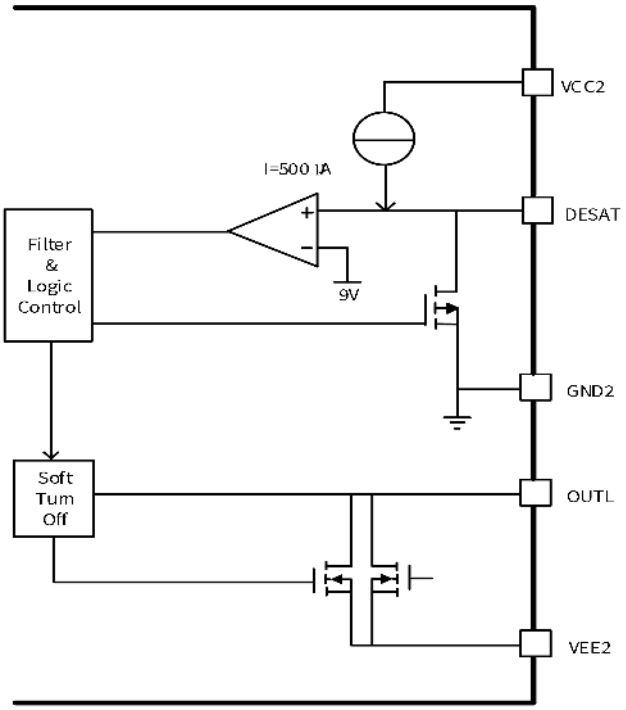


Figure 7.7 DESAT Protection

7.9. Soft Turn-off

The soft turn-off is designed to prevent the overshoot breakdown when DESAT protection is triggered. When the short circuit fault occurs, the external power transistor transits from the active zone to ohmic zone very quickly. The high di/dt may result in the overshoot voltage on the parasitic inductance of the emitter. Therefore ,the device should be turned off in a soft manner. But the turn off speed should not be too slow. There is a balance between the overshoot and large energy dissipation. 400mA soft turn off current is a compromising choice.

7.10. Fault($\overline{\text{FLT}}$ and $\overline{\text{RST}}$/EN)

The $\overline{\text{FLT}}$ pin of NSi66x1A is used to report a warning signal if the fault is detected on DESAT. If the fault occurs, the $\overline{\text{FLT}}$ pin will be pulled down and held in low state for a mute time . During the mute time, NSi66x1A ignores any reset signal. After that, the $\overline{\text{FLT}}$ pin will be reset to high impedance status if the reset signal is checked. The $\overline{\text{RST}}$/EN pin is pulled down to GND1 by an internal resistor,which means the device is disabled by default. Therefore , the $\overline{\text{RST}}$/EN pin must be pulled up externally to enable the device. Timing diagram of fault report is shown below.

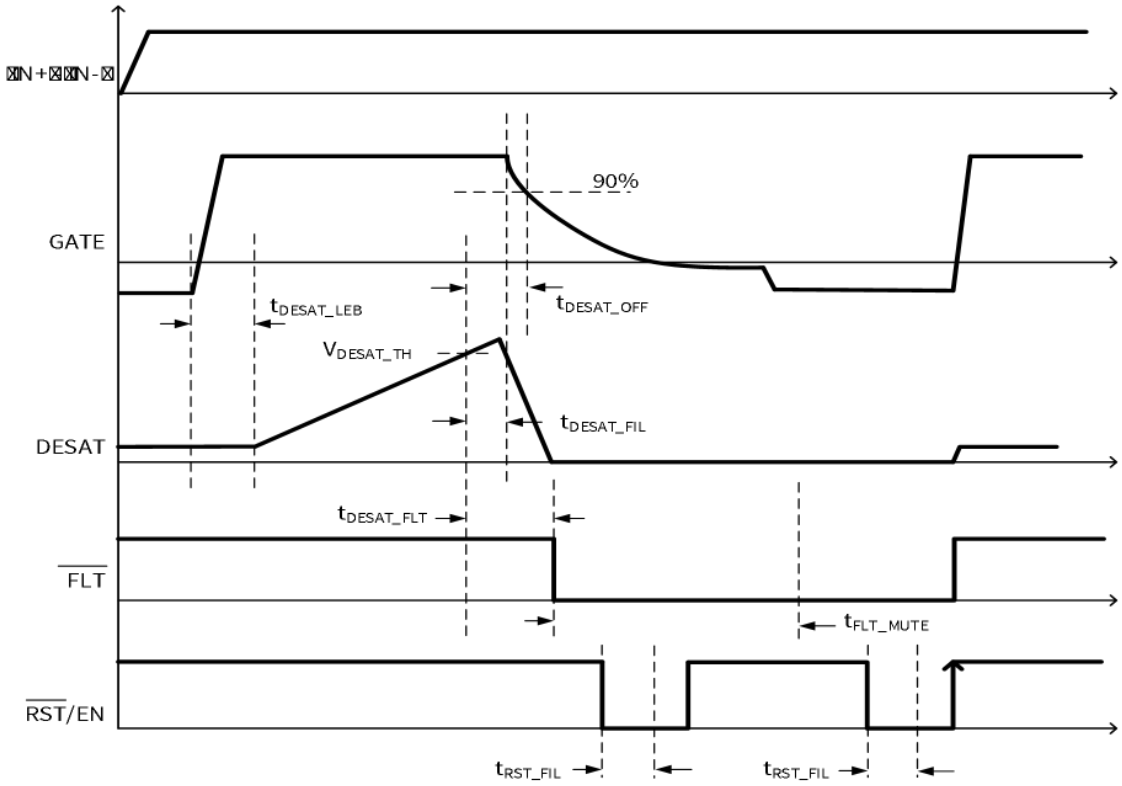


Figure 7.8 DESAT protection Timing Diagram

7.11. ASC Protection(only for NSi6611ASC)

If the active short circuit (ASC) pin is set to be high, the output will be high no matter how input-side configuration. To be mentioned, the priority of ASC protection is higher than the V_{CC1} UVLO but lower than the V_{CC2} UVLO and DESAT protection. To be mentioned, If V_{CC1} is open, DESAT protection will not be allowed. So the ASC is usable without DESAT protection.

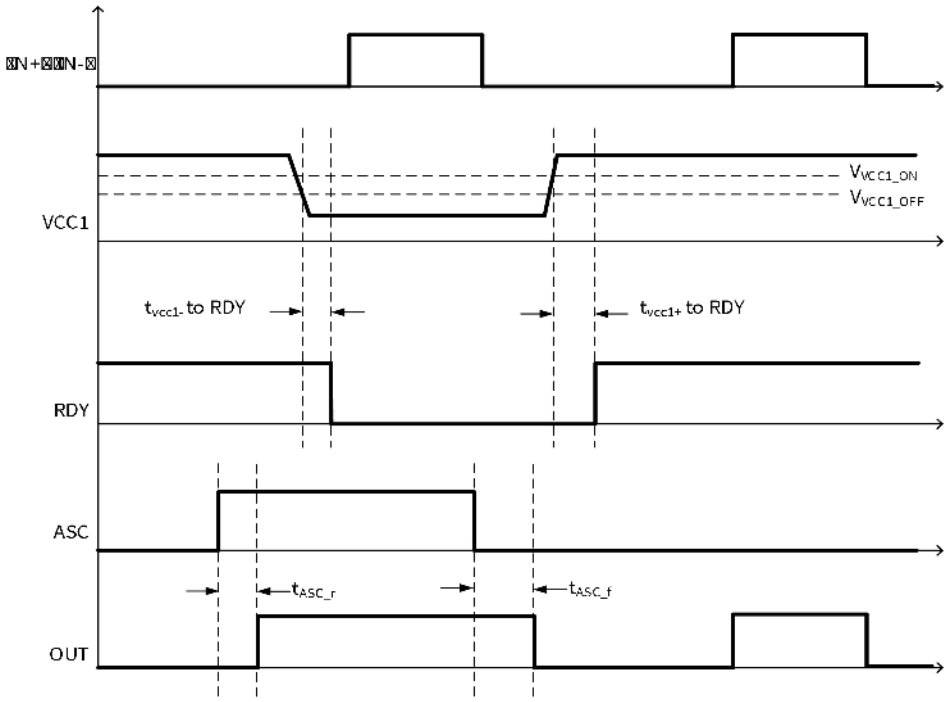


Figure 7.9 ASC protection with V_{CC1} UVLO Timing Diagram

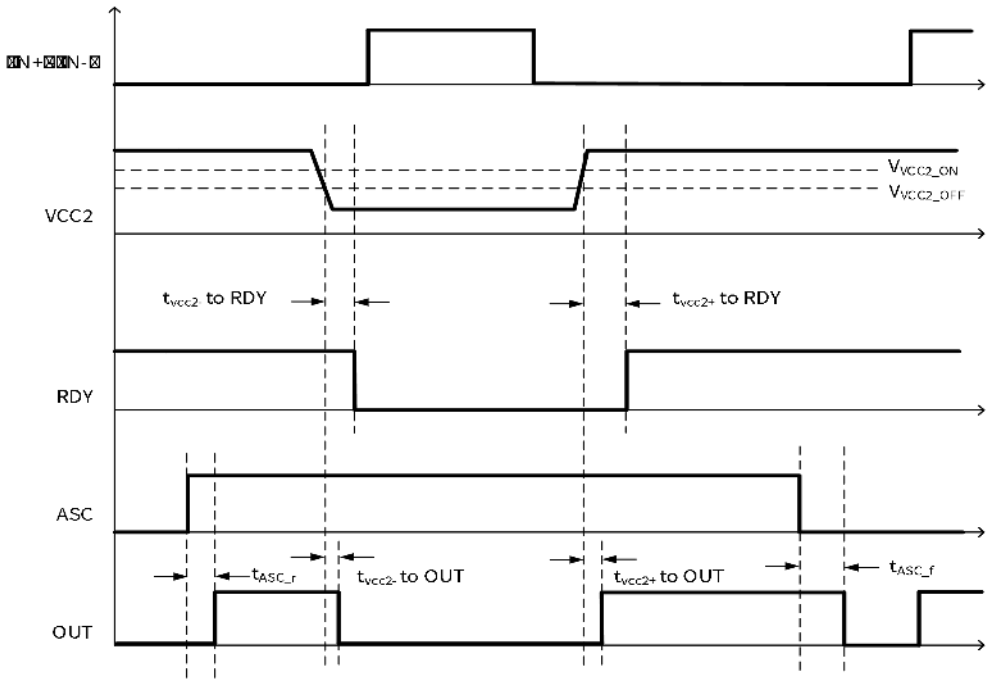


Figure 7.10 ASC protection with V_{CC2} UVLO Timing Diagram

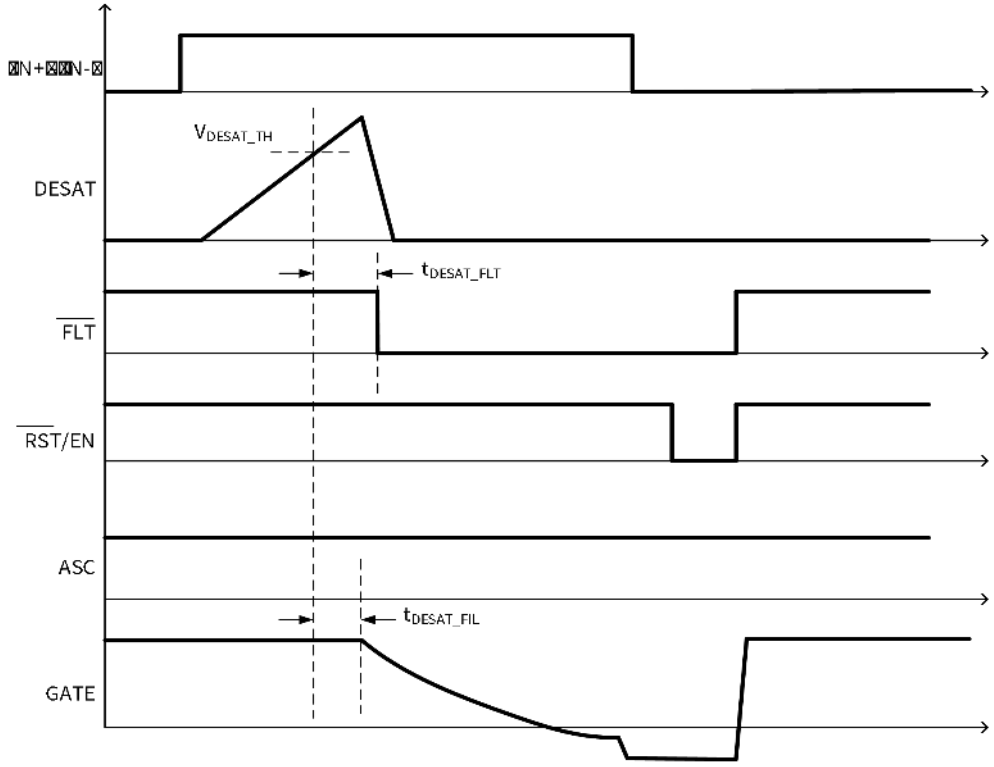


Figure 7.11 ASC protection with DESAT protection Timing Diagram

7.12. Device Functional Modes

Table lists the common functional modes of the device.

Input								Output			
V_{CC1}	V_{CC2}	V_{EE2}	IN+	IN-	EN/RST	DESAT	ASC	RDY	FLT	OUTH/OUTL	CLAMP
PU	PD/OPEN	X	X	X	X	X	X	LOW	HIZ	LOW	LOW
PD	PU	X	X	X	X	X	LOW	LOW	HIZ	LOW	LOW
OPEN	X	X	X	X	X	X	LOW	HIZ	HIZ	LOW	LOW
PU	PU	X	X	X	HIGH	LOW	HIGH	HIZ	HIZ	HIGH	HIZ
PU	PU	X	X	X	LOW	X	HIGH	HIZ	HIZ	HIGH	HIZ
PD/OPEN	PU	X	X	X	X	X	HIGH	X	HIZ	HIGH	HIZ
PU	PU	X	X	X	LOW	X	LOW	HIZ	HIZ	LOW	LOW
PU	PU	X	LOW	X	HIGH	X	LOW	HIZ	HIZ	LOW	LOW
PU	PU	X	HIGH	LOW	HIGH	FLOATING	X	HIZ	LOW	LOW	LOW
PU	PU	X	HIGH	LOW	HIGH	LOW	LOW	HIZ	HIZ	HIGH	HIZ
PU	PU	X	HIGH	HIGH	HIGH	X	LOW	HIZ	HIZ	LOW	LOW

Open: VCC <POR; PU: VCC>VCC UVLO; PD: POR < VCC <VCC UVLO; X: Irrelevant; HIZ: High impedance

POR is around 1.8V.

8. Application Note

8.1. Typical Application Circuit

Bypassing capacitors for V_{CC1} and V_{CC2} supplies are needed to achieve reliable performance. To filter noise, 0.1μF/50V ceramic capacitor is recommended to place as close as possible to NSi66x1A, both at V_{CC1} and V_{CC2} side. For V_{CC2} supply, additional 10μF/50V ceramic capacitor is recommended, to support high peak currents when turning on external power transistor. If the V_{CC1} or V_{CC2} power supply is located long distance from the IC, bigger capacitance is essential.

The input filter composed by R_{in} and C_{in} can be used if input PWM has ring due to long traces or bad PCB layout. However, it will introduce longer propagation delay.

A 5kΩ resistor can be used as pull-up resistor for $\overline{FLT}$,RDY and $\overline{RST}$/EN pins.

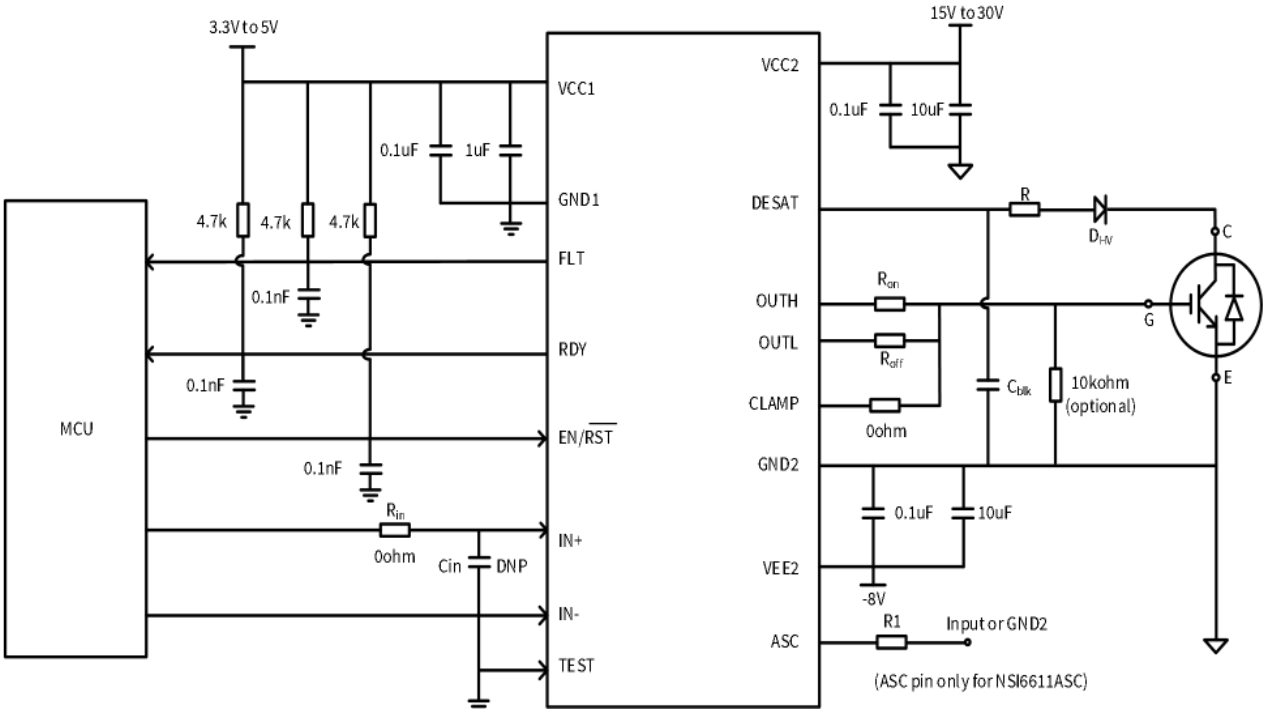


Figure8.1 Typical Application Schematic

8.2. Design for IN+,IN- and $\overline{RST}$/EN

In the application with NSi66x1A, the noise from parasitic inductance and coupled capacitance can not be ignored any more. To filter the noise, NSi66x1A is designed with a 40ns deglitch filter. Besides, the external low pass filter can also be placed near the input pins. Low pass filter will increase the noise immunity and delay time, so it should be based on the requirements.

8.3. Design for EN/$\overline{RST}$,RDY and $\overline{FLT}$

EN/$\overline{RST}$ pin is used to enable the device and reset the fault signal. It is pulled down by default. $\overline{FLT}$ and RDY pin are open-drain output, which means they can not work without externally pull-up resistor. In this application, a 5kΩ pull-up resistor is recommended for RDY, $\overline{FLT}$ and EN/$\overline{RST}$ pin. A 0.1nF can be placed near the device if it is necessary.

8.4. Design for Automatic Reset Control

$\overline{RST}$/EN pin has two functions. It is used to enable the device and reset the fault signal after DESAT is detected. The $\overline{RST}$/EN pin is pulled down to GND by a internal resistor ,so the $\overline{RST}$/EN pin must be pulled up externally to enable the device.

After DESAT is detected ,the FLT pin will be pulled down until the rising edge of the $\overline{RST}$/EN pin is coming. To be mentioned, there

is a FLT mute time, which means the reset signal must be held for at least t_{FLT_MUTE}.

NSi66x1A can be designed for automatic reset mode. $\overline{RST}$/EN pin can be connected with IN+ directly when the PWM is applied to the IN+. Besides, $\overline{RST}$/EN pin can be connected with IN- through a NOT logic if the PWM is applied to the IN-. Whichever mode is used, the PWM off time should be longer than the t_{FLT_MUTE}.

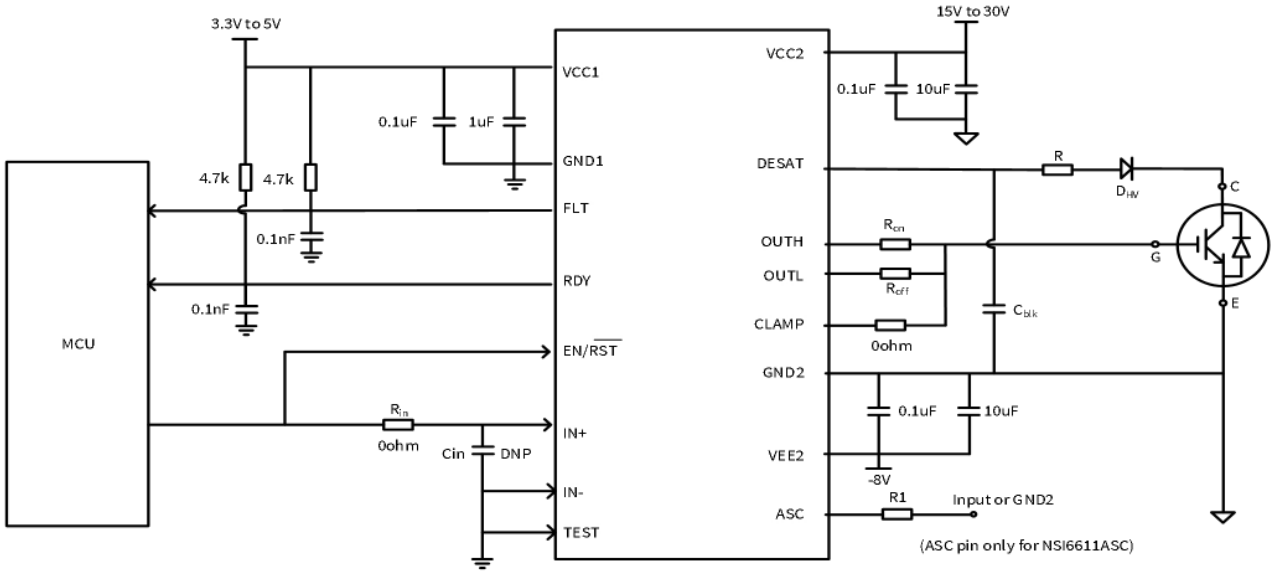


Figure8.2 Automatic Reset Control (IN+)

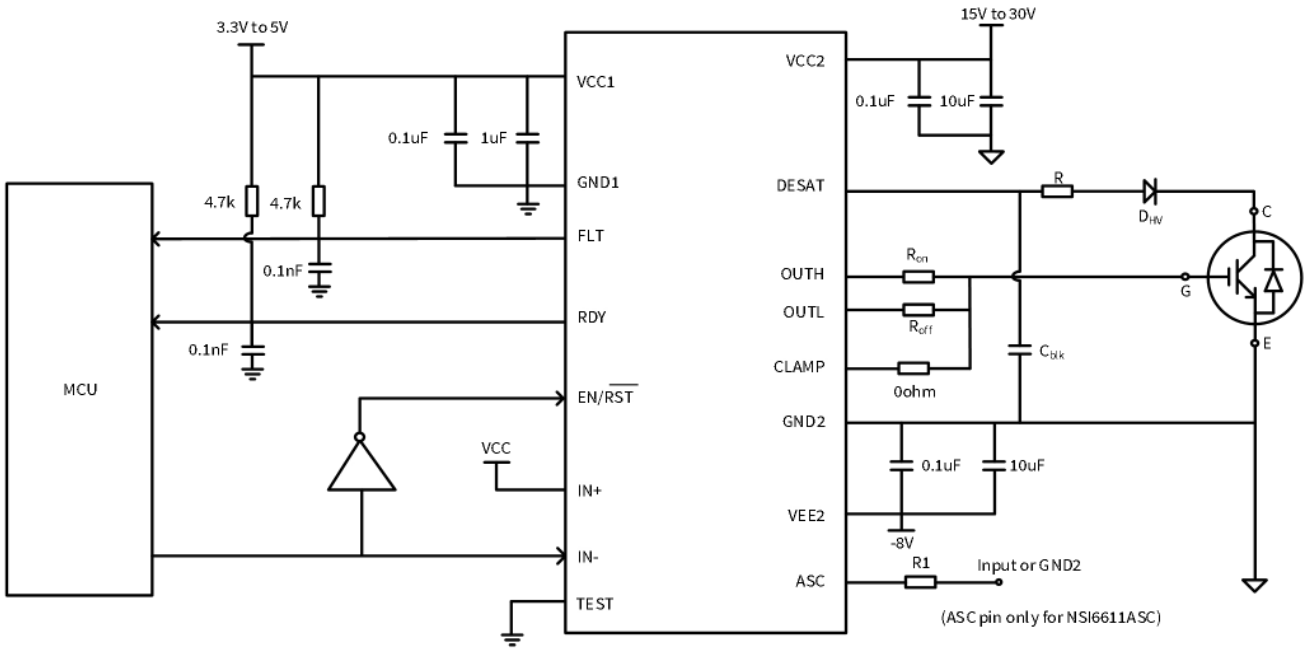


Figure8.3 Automatic Reset Control (IN-)

8.5. PWM Interlock Protection

For applications to drive power transistors in half bridge configuration, two NSi66x1A can be used. NSi66x1A support Interlock protection. If the controller has some mistakes, leading to negative dead time, the output PWM of NSi66x1A is adjusted to avoid power transistor shoot through.

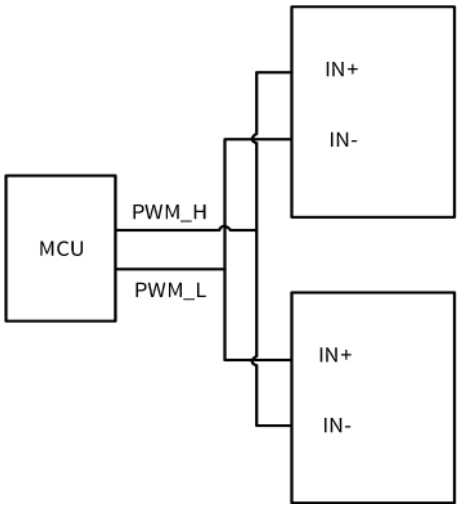


Figure 8.4 Interlock Protection

8.6. Design for R_{on} and R_{off}

NSi66x1A is featured with split output, so the turn on and turn off switching speed can be independently controlled. The turn on and turn off resistance determine the peak source and sink current,which can be estimated by the formula:

$$I_{source} = min(\frac{VCC2 - VEE}{R_{ON} + R_{OH} + R_{Gint}}, 10A)$$

$$I_{sink} = min(\frac{VCC2 - VEE}{R_{OFF} + R_{OL} + R_{Gint}}, 10A)$$

Where

R_{Gint} is the internal resistance of the SiC or IGBT .

8.7. Design for DESAT Protection

DESAT is used to protect the power semiconductor from overcurrent. When the voltage of DESAT is over the V_{DESAT_TH}, the block of soft turn off will be activated and the fault pin will be pulled down. For typical application, the crucial components required to build the DESAT circuit are the DESAT diode, DESAT resistor and the blank capacitor.

The DESAT diode function is to conduct forward current. In order to avoid the false detection caused by the reverse recovery spikes, a very fast reverse recovery time diode with small reverse parasitic capacitance is recommended. The DESAT detection threshold voltage of 9V can be reduced by the DESAT diode, which can be calculated as:

$$V_{DESAT}' = 9 - V_F$$

The anti-parallel diode of IGBT have a large transient forward voltage of the diode,which may result in a large negative voltage spike on the DESAT pin, then it may draw a large current from driver. DESAT resistor is used to limit the current. A 100 Ω resistor is recommended to be added in series with the DESAT diode.

The DESAT fault detection should remain a short blanking time so that the collector voltage can fall below the V_{DESAT_TH}. This blanking time can make sure that there is no nuisance tripping during the IGBT turn-on. It is based on the blank capacitor, which can be estimated as:

$$t_{BLK} = \frac{C_{BLK} \times V_{DESAT\_TH}}{I_{CHG}}$$

8.8. Design for External Current Buffer

Totem structure can be used as an external current buffer to increase the IGBT gate drive current, such as the NPN/PNP buffer shown as below. When the external buffer is used, the external components for soft turn off should be designed in addition. The capacitor is used to adjust the timing and the resistor ensure the sink current lower than the I_{OUTL}. Both resistor and capacitor can be estimated by the Equation below.

$$C_{STO} = \frac{I_{STO} \times t_{STO}}{VCC2\text{-}VEE2}$$

$$R_{STO} = \frac{VCC2\text{-}VEE2}{I_{OUTL}}$$

I_{STO} is the internal soft turn off current

T_{sto} is the expected timing

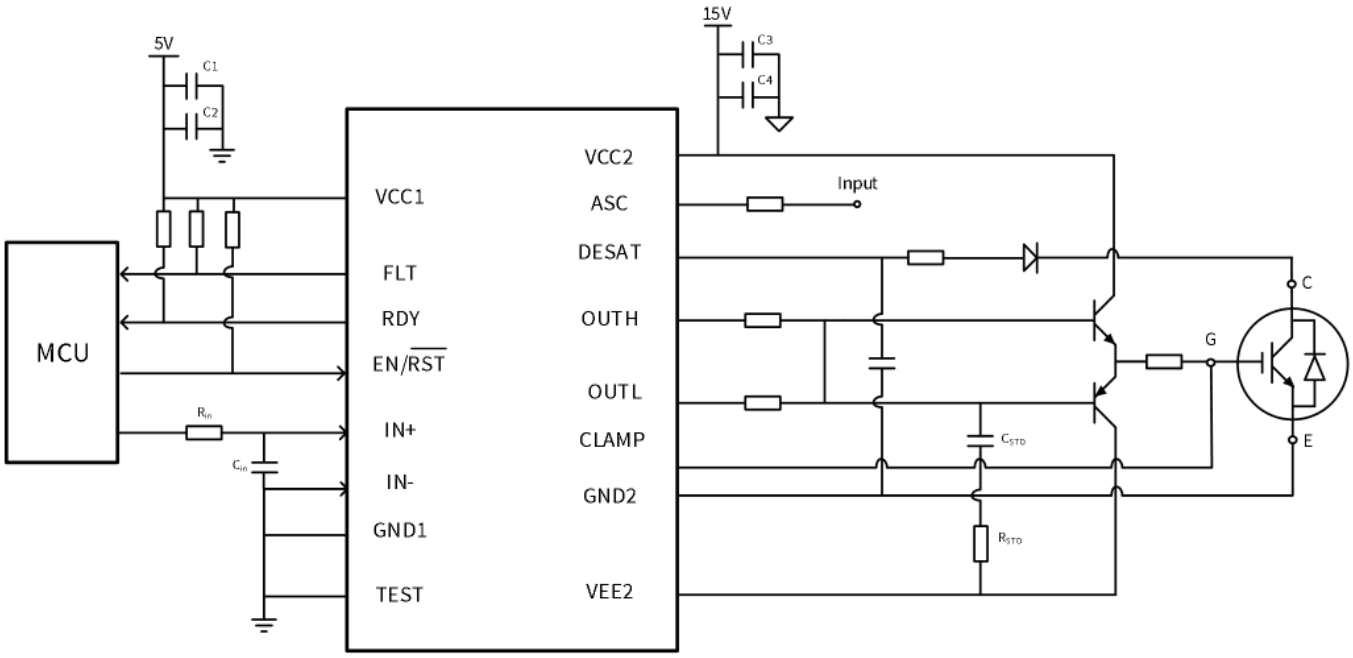


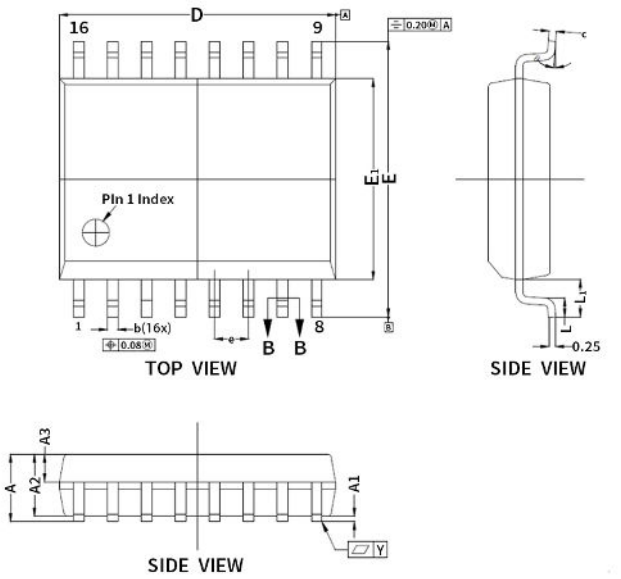
Figure 8.5 External current buffer circuit

8.9. PCB Layout

Careful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSi66x1A, between V_{CC1} to GND1, V_{CC2} to GND2 and V_{EE2} to GND2.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSi66x1A close to power transistor.
- Place large amount of copper connecting to V_{EE2} pin and V_{CC2} pin for thermal dissipation, with priority on V_{EE2} pin. If the system has multi-layers of V_{EE2} or V_{CC2}, use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

9. Package Information



* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0^0	---	8^0

Figure 9.1 SOW16 Package Shape and Dimension

Dimensions shown in millimeters

10. Ordering Information

Part Number	*ASC Feature*	*OUT Pin*	*MSL*	*Category*	*SPQ*	*Package Type*	*Package Drawing*
NSi6651ASC-DSWR	No	OUTH, OUTL	2	Industrial	1000	SOP16(300mil)	SOW16
NSi6651ALC-DSWR	No	OUT	2	Industrial	1000	SOP16(300mil)	SOW16
NSi6611ASC-DSWR	Yes	OUTH, OUTL	2	Industrial	1000	SOP16(300mil)	SOW16

11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolated Driver Selection Guide*
NSi66x1A	Click here	Click here	Click here	Click here

12. Tape and Reel Information

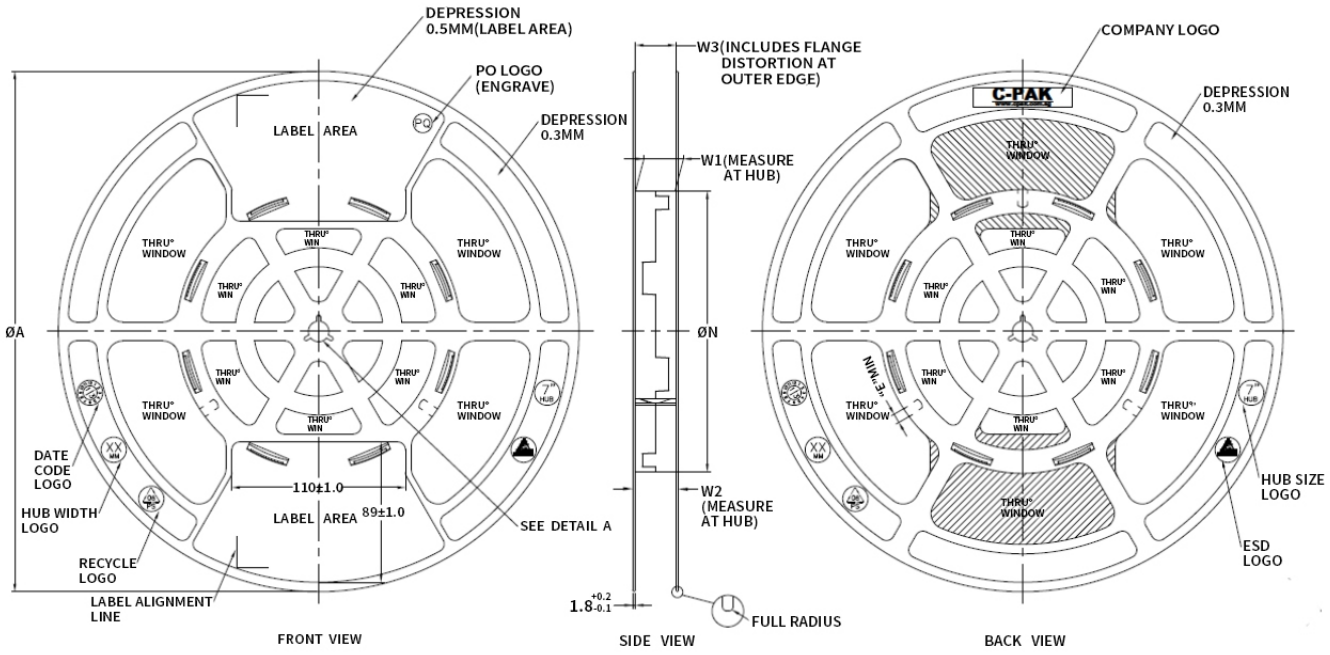


Figure 12.1 Reel Information

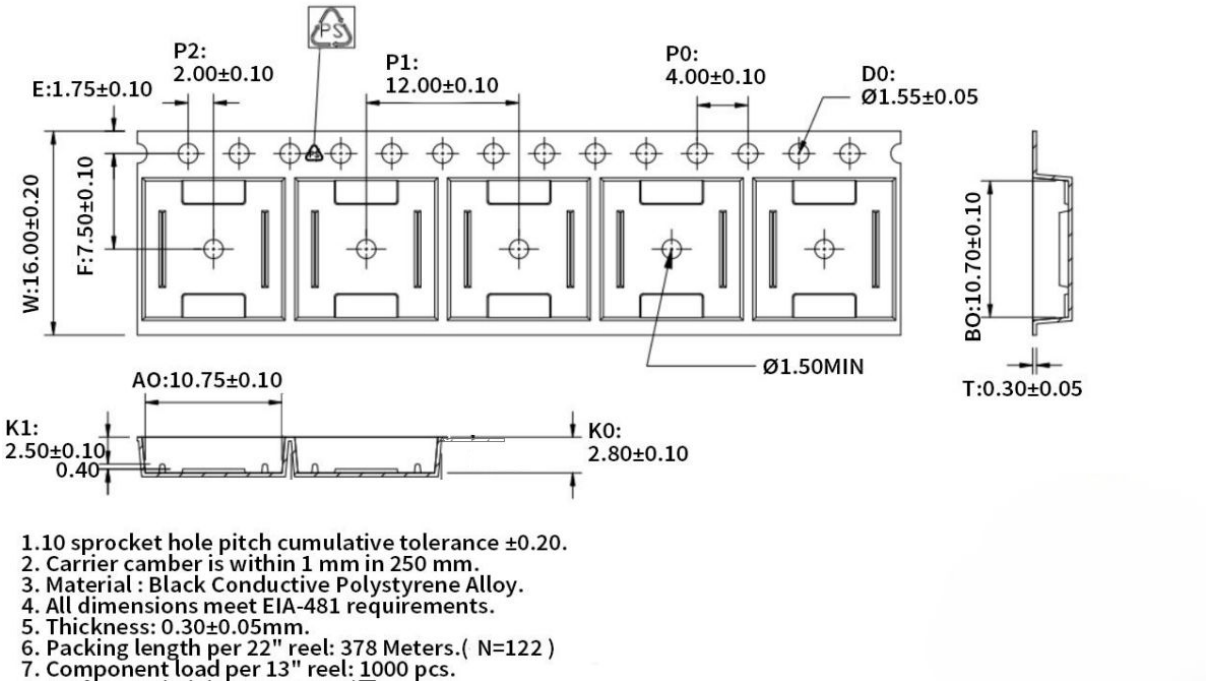


Figure 12.2 SOW16 Tape Information

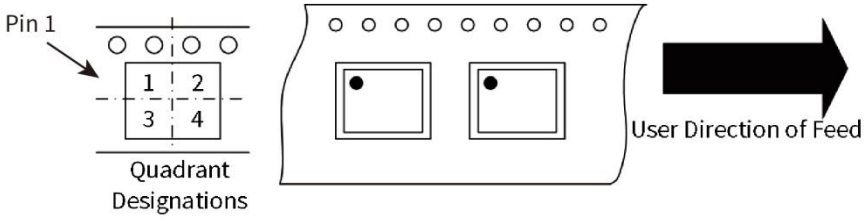


Figure 12.3 Quadrant Designation for Pin1 Orientation in Tape

13. Reversion History

Revision	Description	Date
1.0	Initial version	2022/7/29

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party's intellectual property rights.

You are solely responsible for your use of Novosense' s products and applications, and for the safety thereof. You shall comply with all laws, regulations and requirements related to Novosense' s products and applications, although information or support related to any application may still be provided by Novosense.

The resources are intended only for skilled developers designing with Novosense's products. Novosense reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided. Novosense authorizes you to use these resources exclusively for the development of relevant applications designed to integrate Novosense's products. Using these resources for any other purpose, or any unauthorized reproduction or display of these resources is strictly prohibited. Novosense shall not be liable for any claims, damages, costs, losses or liabilities arising out of the use of these resources.

For further information on applications, products and technologies, please contact Novosense (www.novosns.com).

Suzhou Novosense Microelectronics Co., Ltd