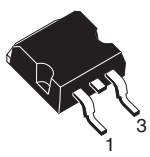
STP100NF04
STB100NF04

N-channel 40V - 0.0043Ω - 120A - TO-220 - D²PAK
STripFET™ II Power MOSFET

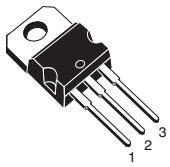
General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STP100NF04	40V	< 0.0046Ω	120A	300W
STB100NF04	40V	< 0.0046Ω	120A	300W

- Standard threshold drive
- 100% avalanche tested



D²PAK

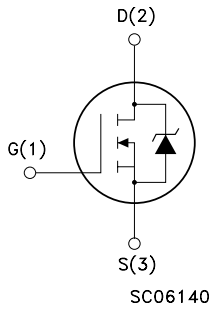


TO-220

Description

This Power MOSFET is the latest development of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STB100NF04	B100NF04	D²PAK	Tape & Reel
STP100NF04	P100NF04	TO-220	Tube

Contents:

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS}=0)	40	V
V_{GS}	Gate-source Voltage	±20	V
I_D(1)	Drain-current (continuous) at Tc=25°C	120	A
I_D (1)	Drain-current (continuous) at Tc=100°C	120	A
I_{DM}(2)	Drain-current (pulsed)	480	A
P_{TOT}	Total dissipation at Tc=25°C	300	W
	Derating factor	2	W/°C
dv/dt(3)	Peak Diode Recovery voltage slope	6	V/ns
E_{AS}(4)	Single Pulse Avalanche Energy	1.2	J
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 175	°C

1. Current limited by package
2. Pulse width limited by safe operating area.
3. I_{SD} ≤120A, di/dt ≤300A/µs, V_{DD} ≤ $V_{(BR)DSS}$, Tj ≤ Tjmax
4. Starting Tj=25°C, I_D=60A, V_{DD}=30V

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal Resistance Junction-case Max	0.5	°C/W
Rthj-pcb	Thermal Resistance Junction-pcb Max	(see *Figure 13*)	°C/W
Rthj-amb	Thermal Resistance Junction-ambient (Free Air) Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D=250µA, V_{GS}=0	40			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS}=0)	V_{DS}=Max Rating V_{DS}=Max Rating Tc=125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS}=0)	V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250µA	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS}=10V, I_D=50A		0.0043	0.0046	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
gfs	Forward Transconductance	V_{DS}=15V, I_D=50A		150		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS}=25V, f=1MHz,V_{GS}=0		5100 1300 160		pF pF pF
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=32V, I_D=120A V_{GS}=10V		110 35 70	150	nC nC nC
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise time Turn-off delay Time Fall Time	V_{DD}=20V, I_D=60A R_G=4.7Ω, V_{GS}=10V (see *Figure 21*)		35 220 80 50		ns ns ns ns

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain Current Source-drain Current (pulsed)				120 480	A A
V_{SD} (2)	Forward on Voltage	I_{SD}=120A, V_{GS}=0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse recovery Current	I_{SD}=120A, V_{DD}=20V, di/dt=100A/µs, Tj=150°C		75 185 5		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Power Derating vs. Tc

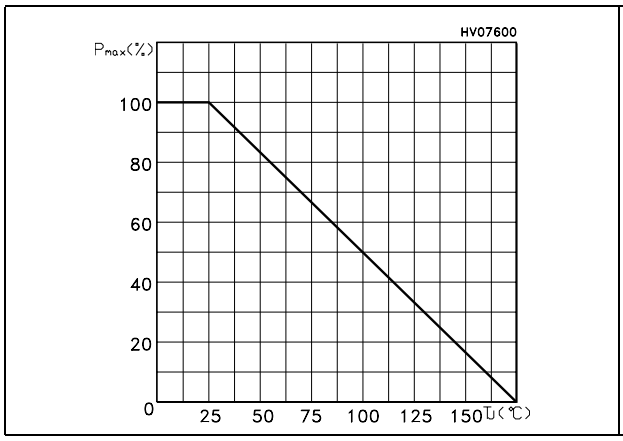


Figure 2. Max Id Current vs. Tc

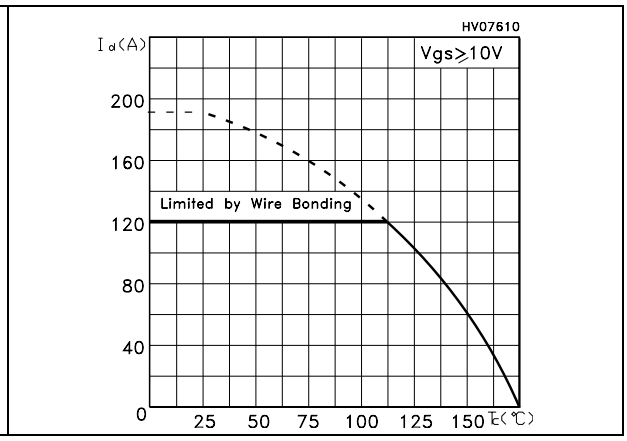


Figure 3. Output Characteristics

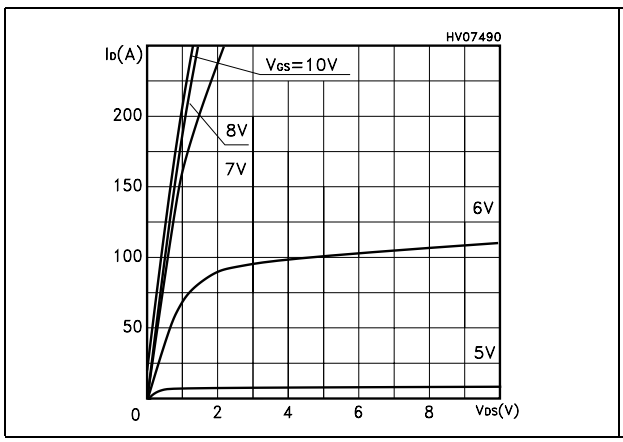


Figure 4. Transfer Characteristics

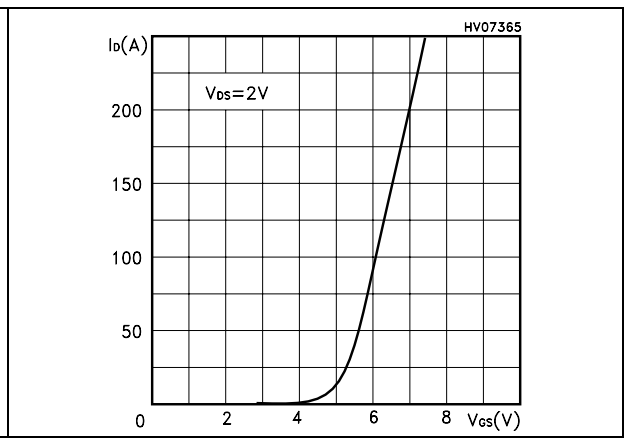


Figure 5. Transconductance

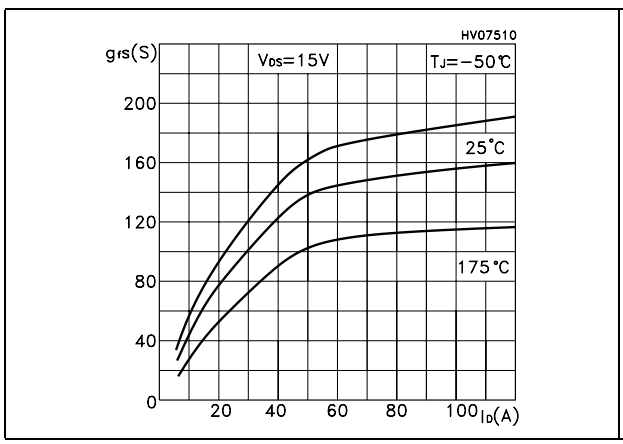


Figure 6. Static Drain-source on Resistance

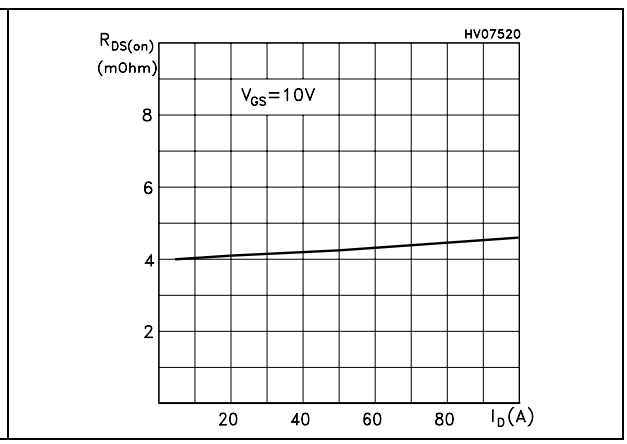


Figure 7. Gate Charge vs. Gate-source Voltage

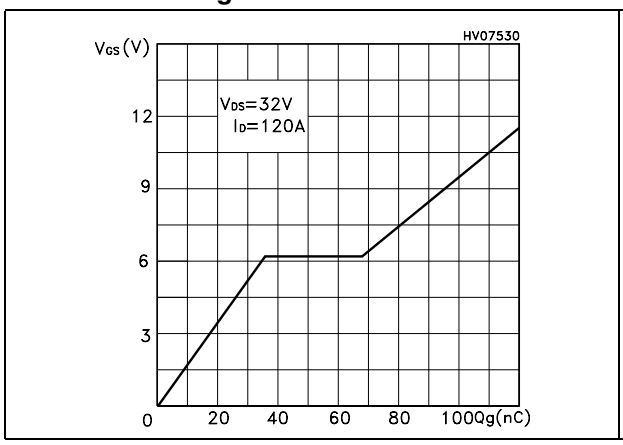


Figure 8. Capacitance Variations

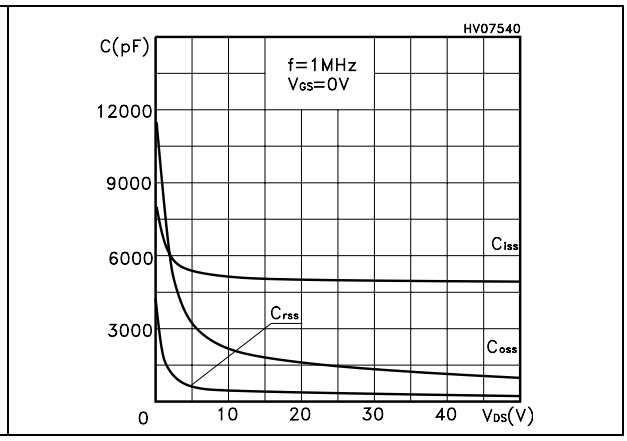


Figure 9. Normalized Gate Threshold Voltage vs. Temperature

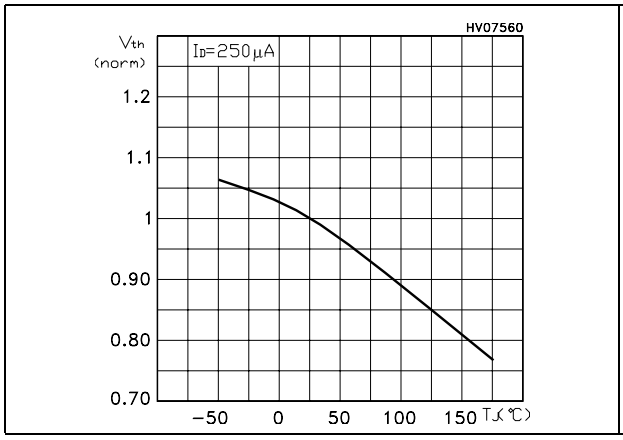


Figure 10. Normalized on Resistance vs. Temperature

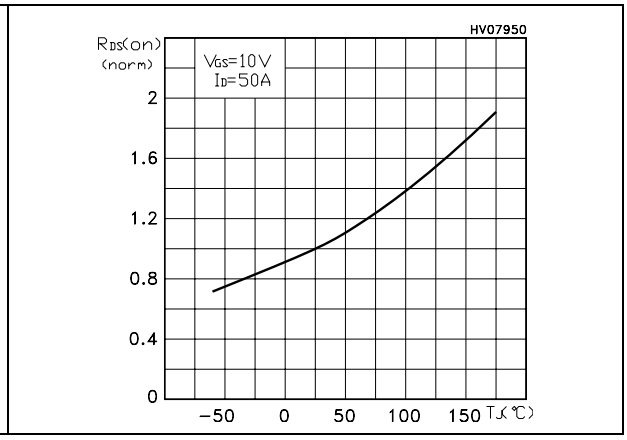


Figure 11. Source-Drain Diode Forward Characteristics

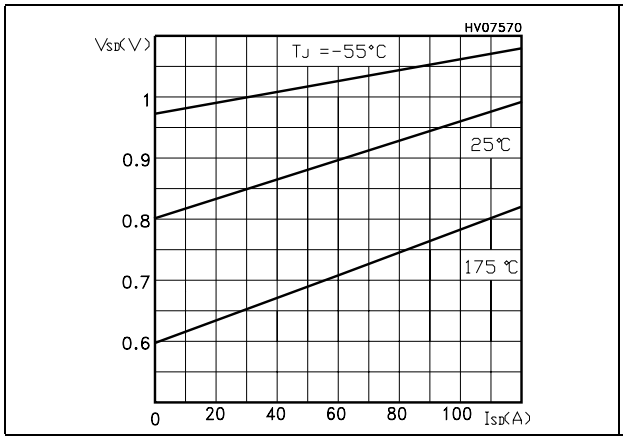


Figure 12. Normalized BVdss vs. Temperature

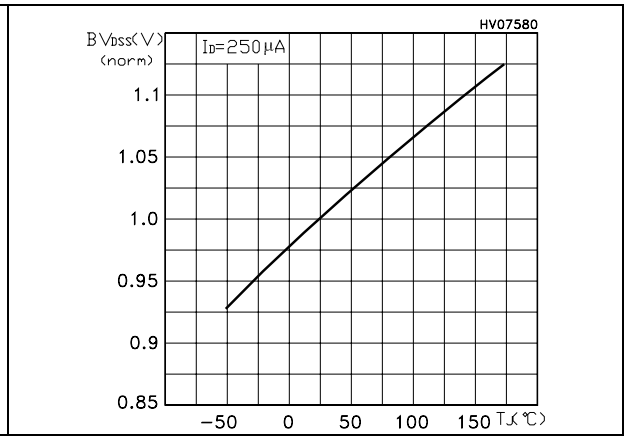


Figure 13. Thermal Resistance Rthj-pcb vs. PCB Copper Area

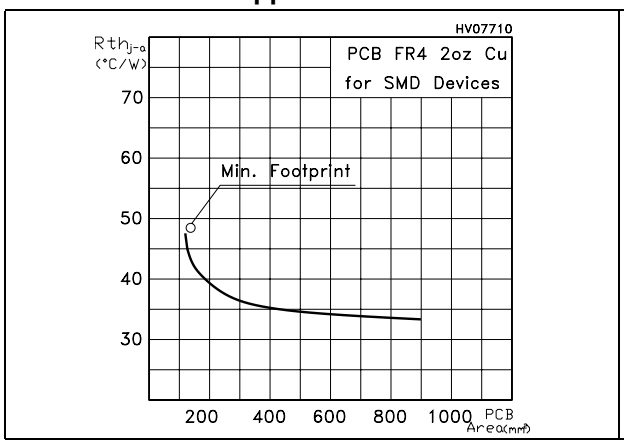


Figure 14. Thermal Impedance

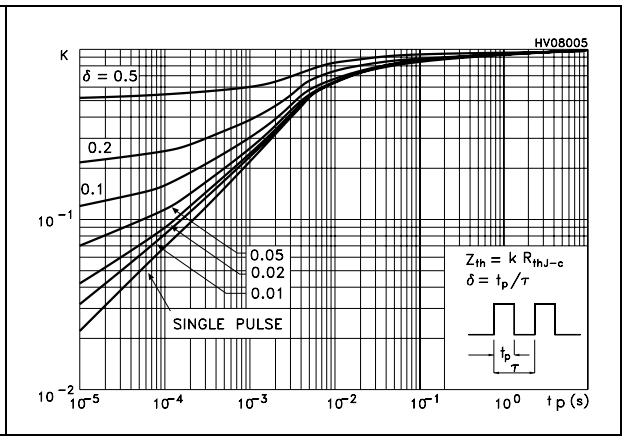


Figure 15. Max Power Dissipation vs. PCB Copper Area

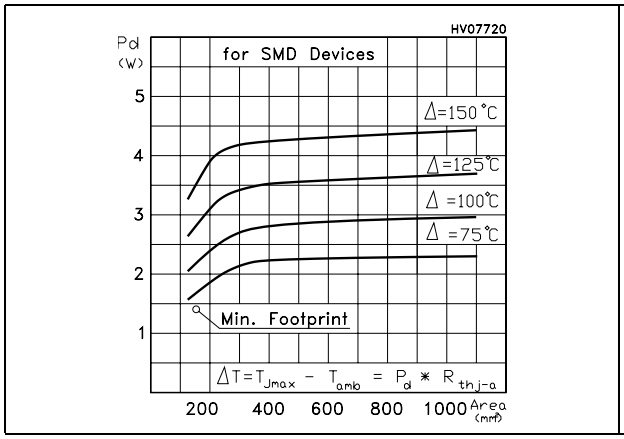


Figure 16. Safe Operating Area

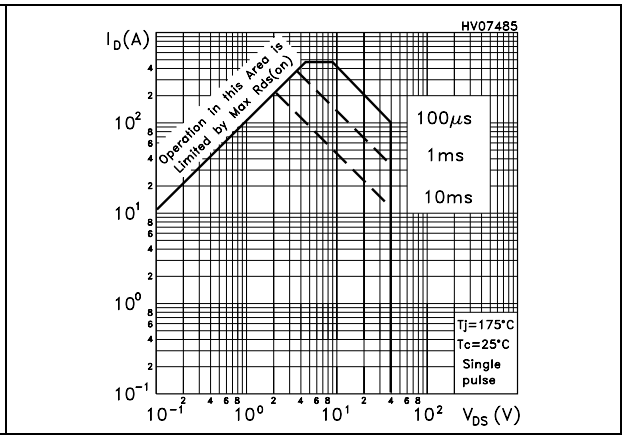
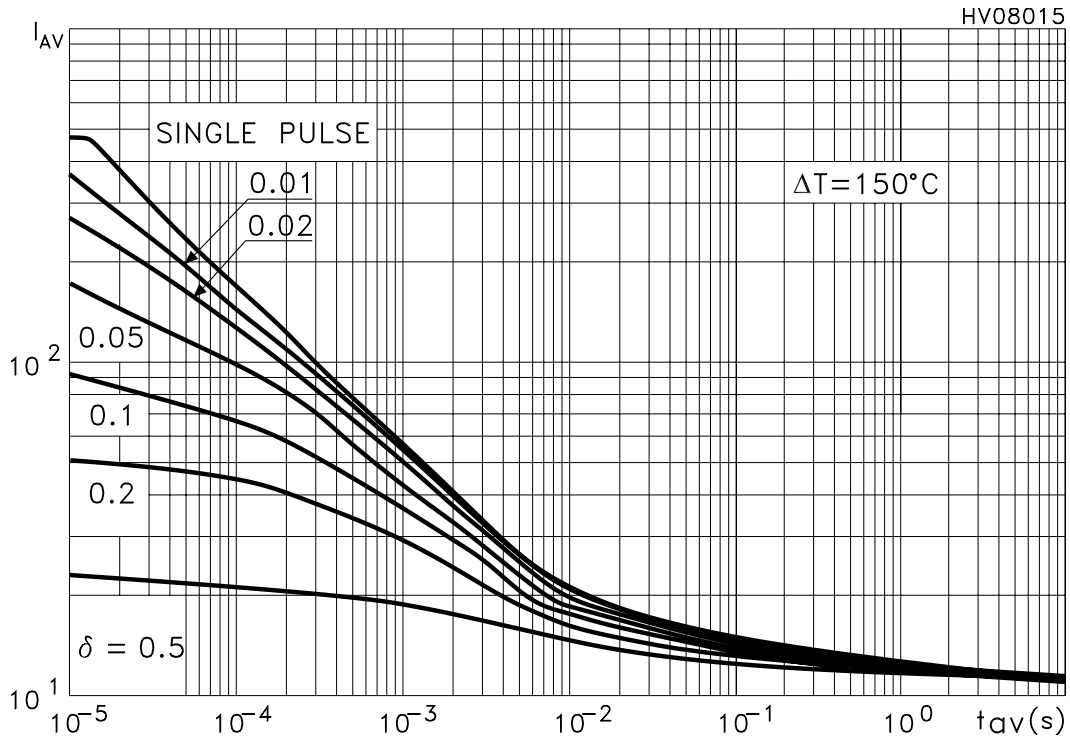


Figure 17. Allowable Iav vs. Time in Avalanche



The previous curve give the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$P_{D(AVE)} = 0.5*(1.3*BV_{DSS}*I_{AV})$

$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$

Where:

I_{AV} is the Allowable Current in Avalanche

$P_{D(AVE)}$ is the Average Power Dissipation in Avalanche (Single Pulse)

t_{AV} is the Time in Avalanche

To de rate above 25°C, at fixed I_{AV}, the following equation must be applied:

$I_{AV}=2*(T_{jmax} - T_{CASE}) / (1.3*BV_{DSS} * Z_{th})$

Where:

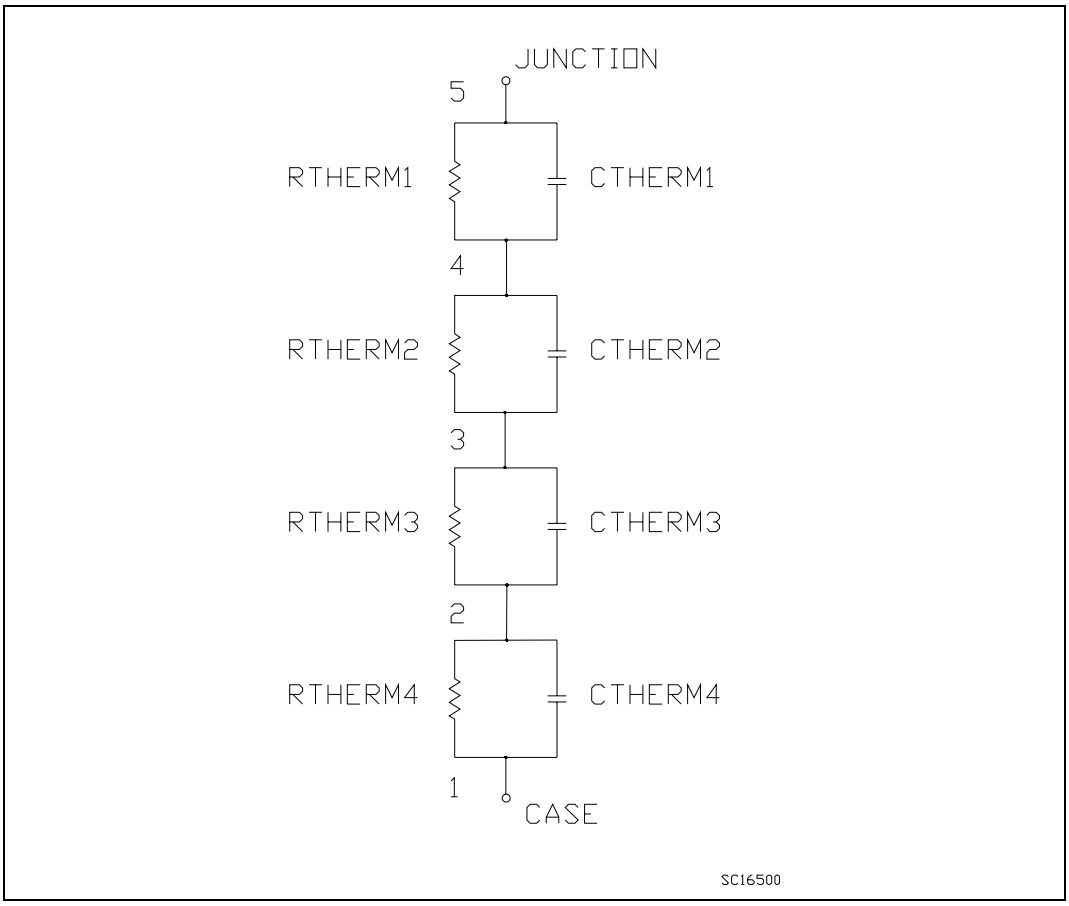
$Z_{th}= K*R_{th}$ is the value coming from Normalized Thermal Response at fixed pulse width equal to T_{AV}

2.2 Spice thermal model

Table 6. Spice parameter

Parameter	Node	Value
CTHERM1	5 - 4	0.011
CTHERM1	4 - 3	0.0012
CTHERM3	3 - 2	0.05
CTHERM4	2 - 1	0.1
RTHERM1	5 - 4	0.09
RTHERM2	4 - 3	0.02
RTHERM3	3 - 2	0.11
RTHERM4	2 - 1	0.17

Figure 18. Spice model schematic



3 Test circuit

Figure 19. Unclamped inductive load test circuit

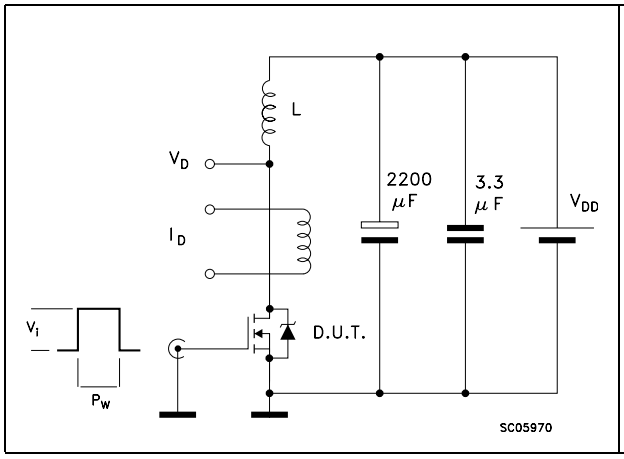


Figure 20. Unclamped inductive waveform

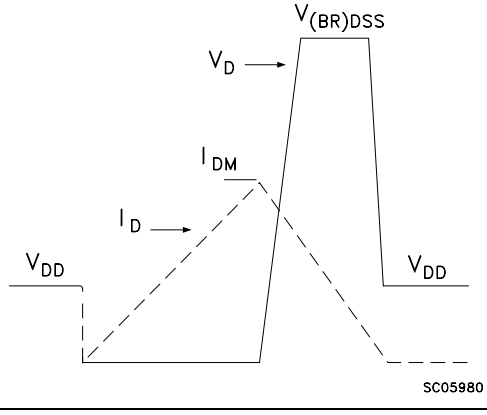


Figure 21. Switching times test circuit for resistive load

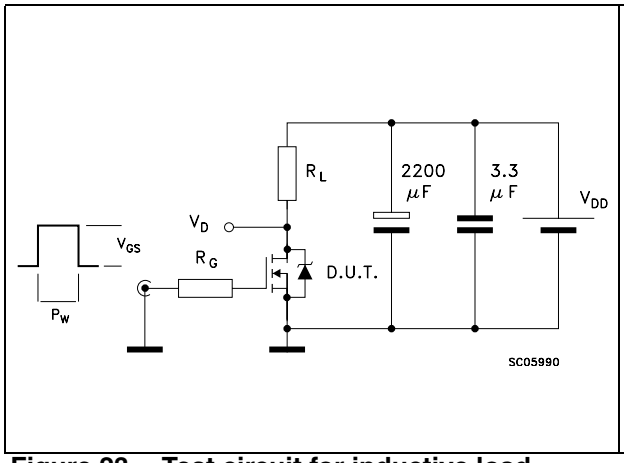


Figure 22. Gate charge test circuit

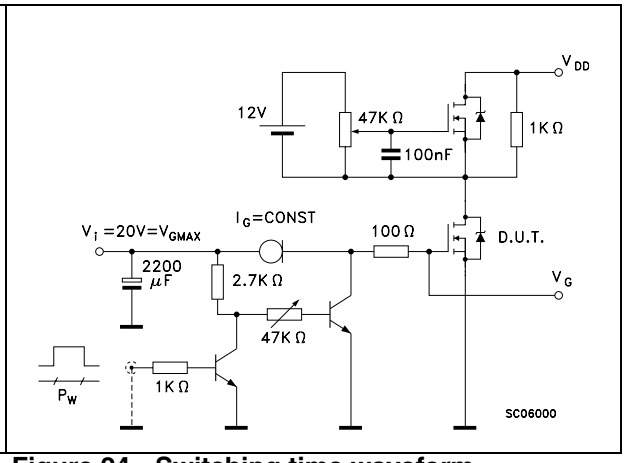


Figure 23. Test circuit for inductive load switching

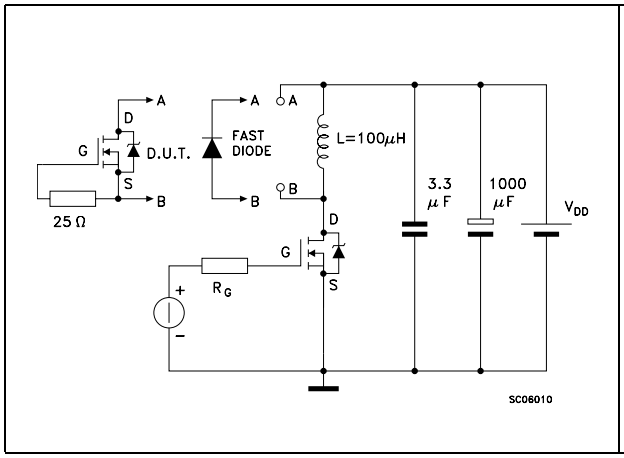
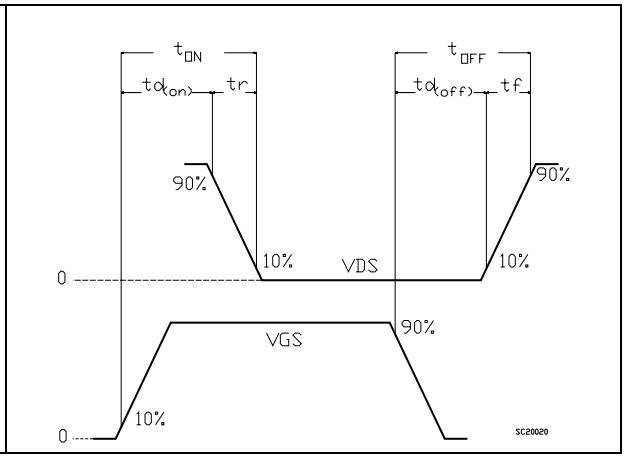


Figure 24. Switching time waveform

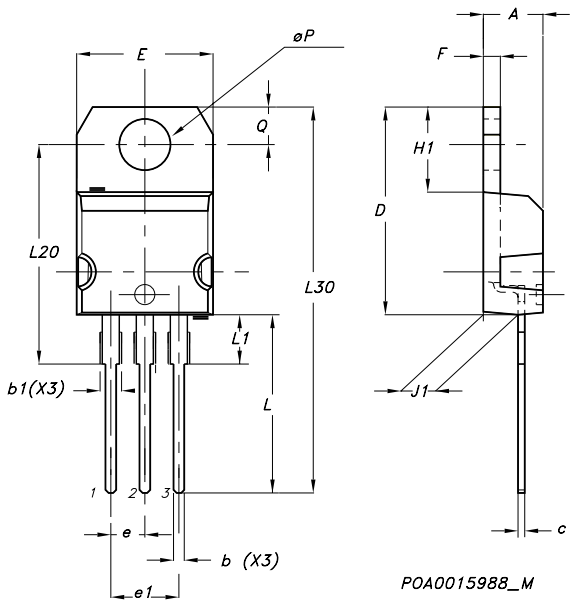


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

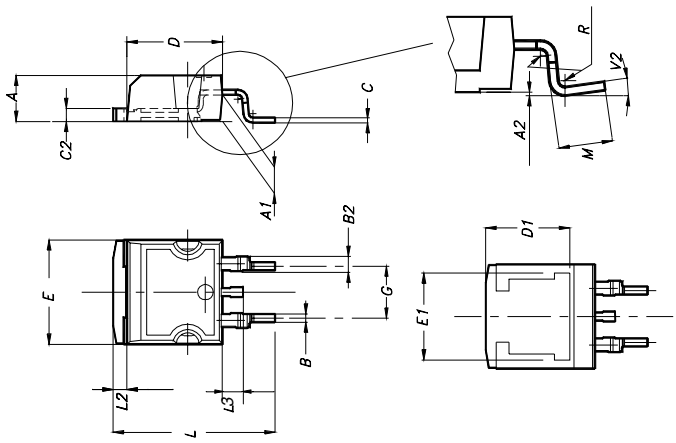
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



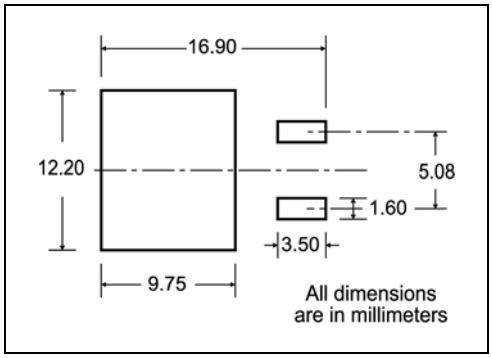
D^2PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0º		4º			

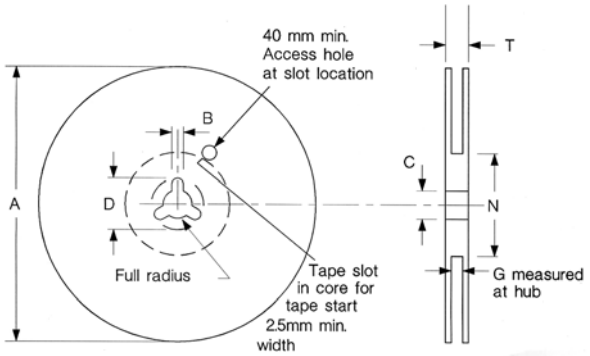


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



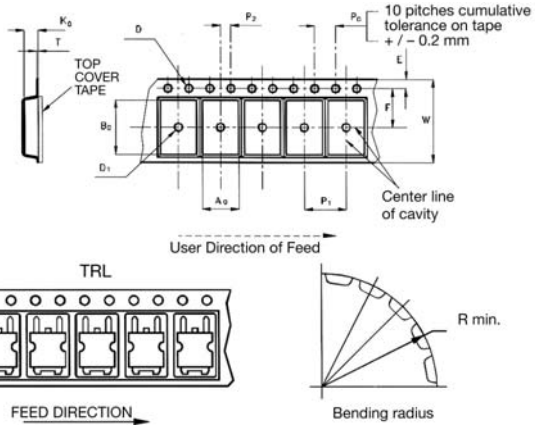
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956



* on sales type

6 Revision history

Table 7. Revision history

Date	Revision	Changes
23-Mar-2005	2	New template
01-Mar-2006	3	Removed I²PAK and inserted D²PAK.
04-Sep-2006	4	New template, no content change
20-Feb-2007	5	Typo mistake on page 1

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