ACT85610

Integrated High Voltage Power Loss Protection with PMIC

BENEFITS and FEATURES

- **HIGH PERFORMANCE POWER LOSS PROTECTION**
  - Wide 2.7 to 14V Operating Input Range
  - 20V Max Input Withstanding Voltage
  - Programmable 5.5V to 31V Boost Storage Voltage
  - 8A Synchronous Buck With 100% Duty Cycle Mode
  - Inrush Current Control
  - Programmable 10A Input Current Limit
  - Adjustable Start-Up Slew Rate
  - Configurable Power Failure Levels
  - Programmable up to 2.25MHz Buck Operating Frequency for Small Inductor Size
  - Undetectable Transition from Input Supply to Capacitor Bank Power
  - Compatible with Many Types of Storage Caps: Super Caps, Electrolytic, Tantalum, POSCAP etc.
  - Storage Capacitor Health Monitoring
  - Early Storage Capacitor Failure Detection
  - Storage Capacitance Measurement
  - eFuse, Boost, and Buck UV/OV/OC Protection

- **High Efficiency PMIC with Integrated FETs**
  - 4 High Voltage DC-DC Buck Converters
  - Integrated Synchronous Power Stage
  - Up to 96% Efficiency
  - Optimized Single Stage Conversion from Vin = 12V to Vout = 0.6V
  - Excellent Dynamic Response
  - Proprietary COT Control Algorithm
  - Small Inductor Sizes
  - Fast Transient Response
  - 1 High Voltage Nonsynchronous Boost Regulator
  - 1 LDO with Programmable Output Voltage
  - 500 kHz – 2.0MHz Configurable Frequency Range
  - Near Constant Frequency
  - Sensorless Over Current Protection (OCP)
  - Output UV and OV Detection
  - Optimized for Ceramic Output Capacitors

- **SYSTEM CONTROL AND INTERFACE**
  - Dedicated Power Loss Indicator Pin (PLI)
  - 6 Programmable General Purpose I/Os
  - I^2C Serial Interface with Password Protection
  - ADC Monitoring of Critical Signals
  - Independent On & Off Sequencing Control
  - Reset/Power Good Output
  - Configurable Rails On/Off though I2C/GPIO
  - Input Power, UV, and OV Monitoring
  - Configurable Interrupts to Inform Host of Faults/Status Change
  - Thermal Alert and Protection

- **SYSTEM MANAGEMENT**
  - Versatile GPIO Functions
  - Watchdog Supervision
  - Interrupt Function Available
  - I^2C Safety bits to Enhance Immunity against Spurious I^2C Transactions.
  - Thermal Enhanced FCQFN Package

APPLICATIONS

- Solid State Drives
- Industrial Applications
- Backup Power
- Hot Plug Devices

GENERAL DESCRIPTION

The ACT85610 is a highly integrated, highly configurable multiple output power management IC (PMIC) with built-in power loss protection (PLP). There are four high efficiency Bucks that can supply 3 x 4A and 1 x 2A output current. The output voltage can go as low as 0.6V. In addition, there is a 12V boost converter plus a Buck converter to provide the IC's bias power and to power the internal gate drivers for maximum efficiency.

The power loss protection provides backup storage power in the event of an input power failure. A built-in Boost converter provides high voltage energy storage to minimize storage capacitor size requirements. The built-in Buck converter regulates the storage voltage to a fixed output voltage during Supplement mode. The ACT85610 contains internal, back-to-back eFuse FETs to provide bi-directional input to output isolation. The IC also provides hot swap and inrush current control.

The ACT85610 features a programmable storage capacitor voltage to optimize the storage capacitor sizing and system run time. The internal ADC and health monitoring provide an extra layer of protection and improve system reliability and early capacitor failure notification. It checks the storage capacitor health and notifies the user when the energy in the storage caps is not sufficient for backup power. The built-in ADC also measures the input voltage, output voltage, storage voltage, eFuse current, and die temperature. The built-in synchronous Buck converter maximizes energy transfer from the storage caps to the system.

The high voltage step-down regulators use a proprietary control architecture that is based on a constant on-time (COT) topology. It is designed for high efficiency, has programmable switching frequency options, is suitable for high conversion ratios to support output voltages as low as 0.6V, and can operate at very low duty cycles as required in low output voltage applications.

The proprietary control architecture allows the regulators to work at near constant frequency at a given operating point, which is determined by the input and output voltage. As load is varied, the regulator operates at a near constant frequency while operating in continuous conduction mode. The frequency is selectable to accommodate a variety of inductor values and sizes. When load current is reduced, frequency is automatically scaled back to maintain high efficiency in discontinuous mode (DCM) operation. This functionality enables the converter to achieve high efficiencies even at very light loads.

The buck converter output inductors can be optimized for different applications. Proper inductor selection can optimize transient response or efficiency targets. Based on these criteria, a suitable switching frequency can also be selected to optimize these parameters. Careful analysis of operating points - input and output voltage ratio and load profiles, such as typical operating currents where efficiency is most important, peak switching currents, inductor current ripple and the desired dynamic response should all be considered while selecting inductors and switching frequency. All switching converters are internally compensated for stable operation using Qorvo proprietary circuitry. This allows the PMIC to work across a wide range of inductor values and switching frequencies while allowing the end user to balance requirements such as efficiency, dynamic load transient response, inductor form factors and current ratings, peak inductor current ripple and output voltage ripple.

The ACT85610 also contains a Boost regulator. It operates from a wide input voltage range of 2.5V to 14V and provides a programmable output voltage range of 10.8V to 13.2V.

The fixed output Buck regulator, Buck VCC, provides the ACT85610 bias power to the IC's internal circuitry and gate drivers. Bias power is applied to the VCC pin. The regulator provides up to 100mA of output current which can be used to power external circuitry or LDOs. When the system level input voltage, VBUS, is 3.3V or 5V, Buck VCC is not needed and the VCC pin can be directly tied to VBUS.

The ACT86510's integrated LDO can support 300mA output current to power external circuitry.

ACT85610 provides an I^2C bus interface to allow MCU control and monitoring. Its integrated voltage supervi-

sors monitor the input voltage, output voltage, and storage voltage. It contains six configurable GPIOs that can be programmed to implement a variety of system functions. They can be programmed to generate interrupts - as an interrupt request pin (nIRQ pin), to control and sequence external regulators, to enable or disable internal regulators, as input lines to control entry or exit from low power state, and other such system related functions. The GPIOs can also be used to perform dynamic voltage scaling or DVS for the buck regulators or control the external DC-DC regulator voltages. This function allows the user to scale the regulators' outputs between different output voltages to optimize system level power consumption during low power modes.

The ACT85610 includes an I²C a safety feature to eliminate accidentally changing register values. The I²C block requires a register passcode before I²C transactions are accepted to change register values.

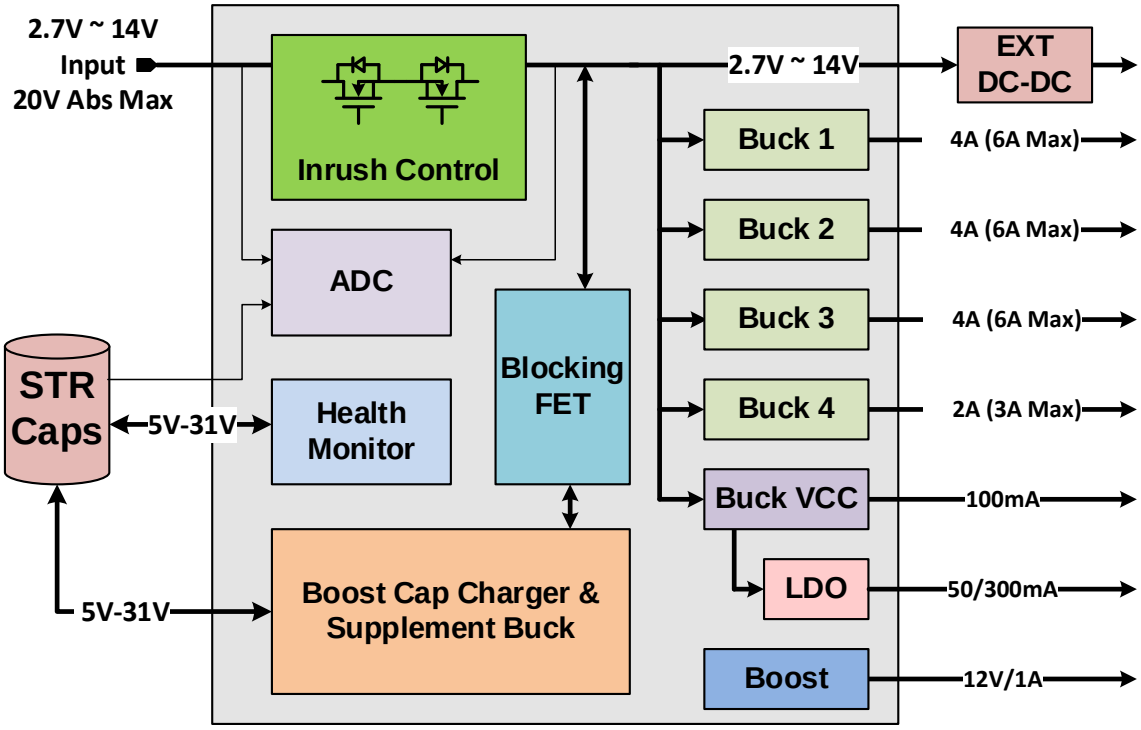


Figure 1: ACT85610 Blocks

FUNCTIONAL BLOCK DIAGRAM

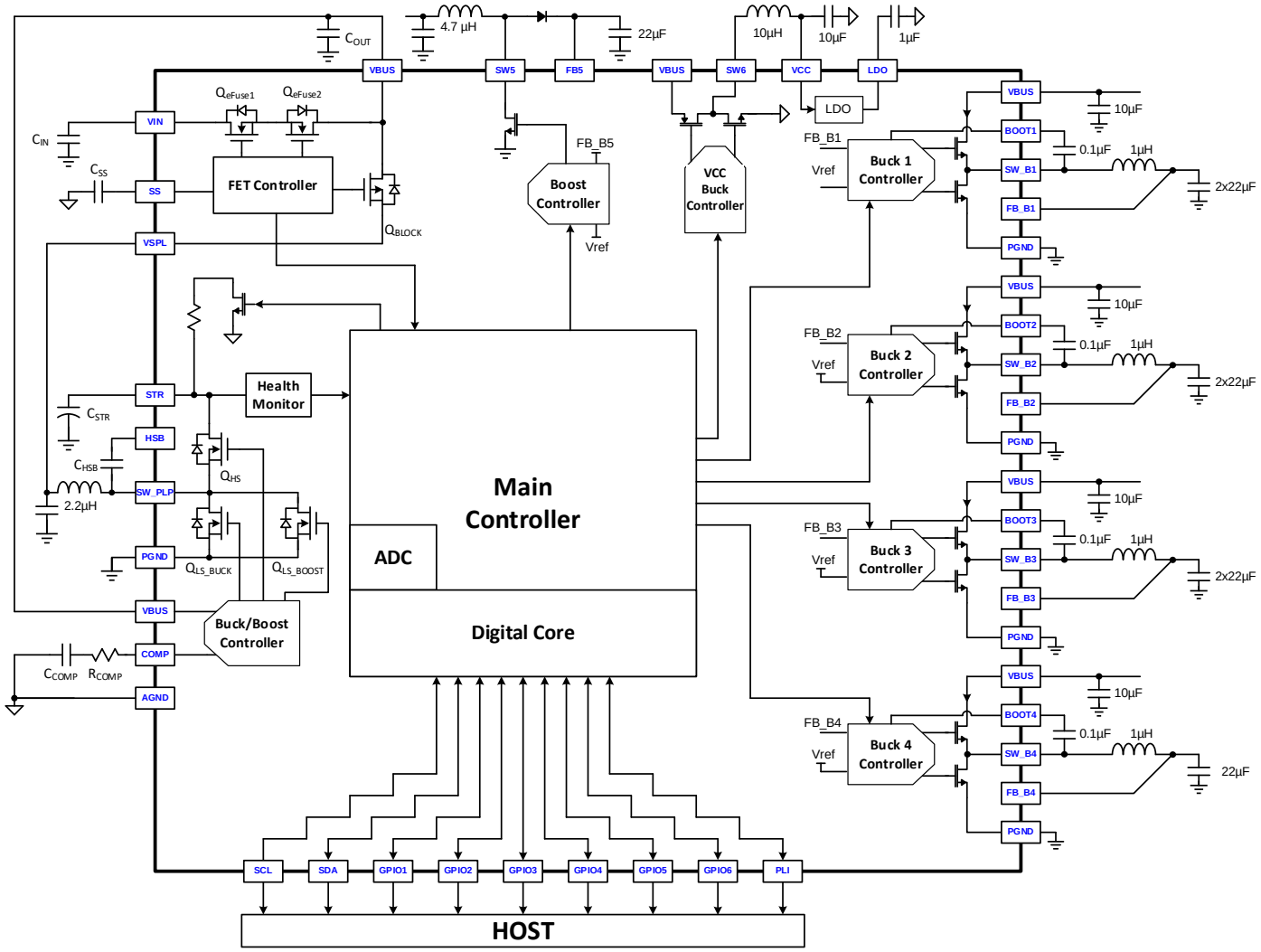
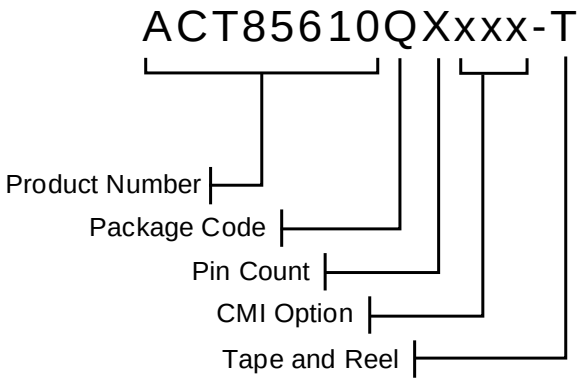


Figure 2: ACT85610 Functional Block Diagram

ORDERING INFORMATION

PART NUMBER	V_{IN}	V_{STR}	$V_{Sup-plement}$	V_{OUT1}	V_{OUT2}	V_{OUT3}	V_{OUT4}	V_{Vcc}	LDO
ACT85610QX101-T	12V	28V	4.3V	0.8V	1.2V	2.5V	1.8V	5.0V	2.5V
ACT85610QX108-T	12V	28V	7.5V	3.3V	3.3V	1.2V	0.8V	5.0V	3.3V
ACT85610QX110-T	12V	28V	5V	0.84V	1.2V	2.5V	1.8V	5.0V	3.3V



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: Package Code designator. “Q” represents QFN.

Note 3: Pin Count designator. “X”

Note 4: “xxx” represents the CMI (Code Matrix Index) option The CMI identifies the IC’s default register settings.

PIN CONFIGURATION

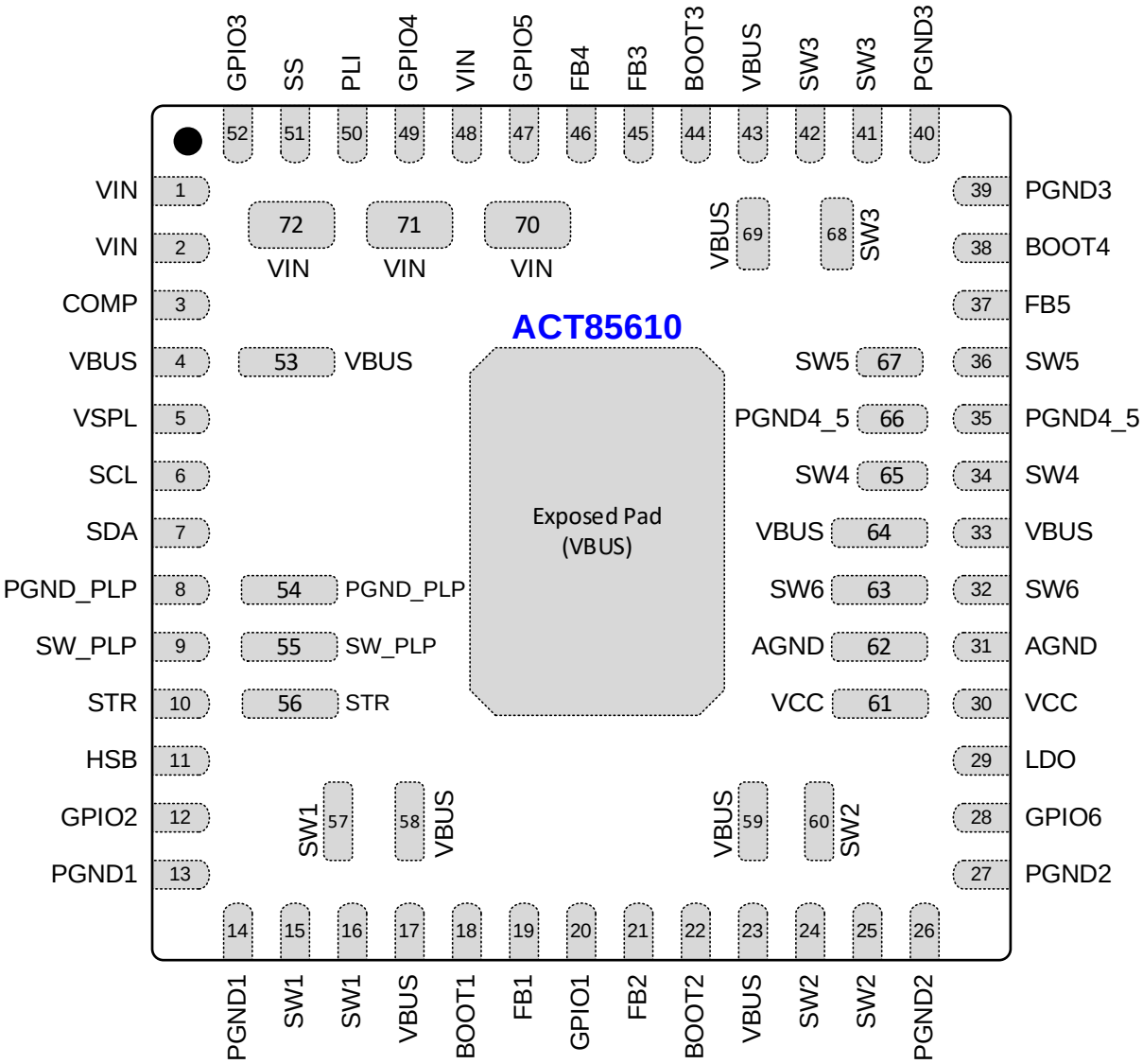


Figure 3: Pin Configuration – Top View – QFN6x6-52

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1, 2, 48, 70, 71, 72	VIN	Power Supply Input. Input to the eFuse. Connect a 0.1µF capacitor between VIN and PGND as close to the IC as possible.
3	COMP	Compensation input pin for the supplement Buck converter.
4, 17, 23, 33, 43, 53, 58, 59, 64, 69	VBUS	Output for by-pass mode, in-rush, and eFuse functionality. VBUS is also the input voltage bus for the downstream regulators.
5	VSPL	Supplement Buck circuit output and Boost circuit input pin. It is isolated from VBUS with the internal blocking FET. Place the inductor between VSPL and SW_PLP.
6	SCL	I^2C Clock Input. Needs an external pull up resistor.
7	SDA	I^2C Data Input and Output. Needs an external pull up resistor.
8, 54	PGND_PLP	PLP Power Ground. Connect to large ground plane on PCB
9, 55	SW_PLP	Power loss protection Buck switching node. This is the boost converter switch node and the buck converter switch node. Place the inductor between VSPL and SW_PLP.
10, 56	STR	Storage Capacitor Input. Connect the storage capacitors to STR. STR requires a minimum capacitor of 100µF to PGND.
11	HSB	High Side Bias, Boot strap pin. This provides power to the internal high-side MOSFET gate driver circuitry. Connect a 22nF-220nF capacitor from HSB pin to SW_PLP pin.
12	GPIO2	GPIO2 Pin
13, 14	PGND1	Buck1 Power Ground. Connect to large ground plane on PCB
15, 16, 57	SW1	Switch pin for HV Buck1 regulator
18	BOOT1	Boot strap voltage for HV Buck1 regulator. Connect a 22nF-220nF capacitor between BOOT1 and SW_B1.
19	FB1	Output and feedback pin for HV Buck1 regulator
20	GPIO1	GPIO1 Pin
21	FB2	Output and feedback pin for HV Buck2 regulator
22	BOOT2	Boot strap voltage for HV Buck2 regulator. Connect a 22nF-220nF capacitor between BOOT2 and SW_B2.
24, 25, 60	SW2	Switch pin for HV Buck2 regulator
26, 27	PGND2	Buck2 Power Ground. Connect to large ground plane on PCB
28	GPIO6	GPIO6 Pin
29	LDO	LDO output pin. Place 1uF or large ceramic between this pin and AGND.

30, 61	VCC	Output and feedback pin for VCC Buck regulator
31, 62	AGND	Analog Ground. Kelvin connect AGND to the PGND plane.
32, 63	SW6	Switch pin for VCC Buck regulator
34, 65	SW4	Switch pin for HV Buck4 regulator
35, 66	PGND4_5	Buck4 and Boost Power Ground. Connect to large ground plane on PCB
36, 67	SW5	Switch pin for Boost regulator
37	FB5	Output and feedback pin for Boost regulator
38	BOOT4	Boot strap voltage for HV Buck4 regulator. Connect a 22nF-220nF capacitor between BOOT4 and SW_B4.
39, 40	PGND3	Buck3 Power Ground. Connect to large ground plane on PCB
41, 42, 68	SW3	Switch pin for HV Buck3 regulator
44	BOOT3	Boot strap voltage for HV Buck3 regulator. Connect a 22nF-220nF capacitor between BOOT3 and SW_B3.
45	FB3	Output and feedback pin for HV Buck3 regulator
46	FB4	Output and feedback pin for HV Buck4 regulator
47	GPIO5	GPIO5 Pin
49	GPIO4	GPIO4 Pin
50	PLI	Power Loss Indicator Open-Drain Output for VIN. PLI goes high when the eFuse is turned on and goes low when the IC enters supplement mode. PLI is referenced to AGND.
51	SS	Soft Start Input. Place a capacitor from SS to VSS to control the eFuse startup voltage slew rate.
52	GPIO3	GPIO3 Pin
Exposed Pad	VBUS	Tie to top layer VBUS plane. All VBUS pins should be directly connected to the exposed pad on the top layer.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE	UNIT
All Pins to GND unless stated otherwise below	-0.3 to 6	V
VIN to PGND	-0.3 to 20	V
VBUS to PGND	-0.3 to 14.8	V
VSPL to AGND	-0.3 to VBUS+0.3	V
HSB to SW_PLP	-0.3 to 6	V
SW_PLP to PGND_PLP	-1 to STR+ 0.3	V
STR to PGND	-0.3 to 33	V
PGND1, PGND2, PGND3,PGND4_5, PGND_PLP to AGND	-0.3 to + 0.3	V
SW1,2,3,4 to PGND	-1 to VBUS + 1	V
BOOTx to SWx (BOOT1 to SW1, BOOT2 to SW2 etc.)	-0.3 to SWx + 6	V
SW5 to PGND	-0.3 to 18	V
FB5 to AGND	-0.3 to 15.5	V
FB1,2,3,4 to AGND	-0.3 to 6	V
VCC to PGND	-0.3 to min (6, VBUS+0.3)	V
SW6 to PGND	-1 to VBUS + 1	V
SCL, SDA, GPIOx, PLI, SS to AGND	-0.3 to 6.0	V
LDO to AGND	-0.3 to min (6, VCC+0.3)	V
AGND, PGND	-0.3 to + 0.3	V
ESD Rating (human body model), all pins	2	kV
Storage Temperature	-40 to 150	°C
Operating Junction Temperature (T_J)	-40 to 150	°C
Junction to Ambient Thermal Resistance (θ_{JA})	35	°C/W
Lead Temperature (Soldering, 10 sec)	300	°C
MSL Rating	MSL3	

Note 1: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Note 2: All other pins meet +/- 2kV HBM ESD

Note 3: Measured on Qorvo Evaluation Kit

DIGITAL I/O ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIOx Input Low	VIO = 1.8V			0.35	V
GPIOx Input High	VIO = 1.8V	1.25			V
GPIOx Open Drain Leakage Current	Output = 5V			1	µA
GPIOx Open Drain Output Low	IOL = 1mA			0.35	V
GPIOx Input Deglitch Time (falling)			20		µs
GPIOx Input Deglitch Time (rising)			10		µs

ELECTRICAL CHARACTERISTICS: PLP SYSTEM CHARACTERISTICS

(VIN = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply					
Input Supply Voltage Range	VIN (Note 1)	2.7		14	V
Input Supply Over Voltage Lock Out (VIN_OVLO)			14.4		V
Input Under Voltage Lock Out (VIN_UVLO)	VIN Rising	2.5	2.6	2.7	V
	VIN_UVLO hysteresis	20	50	80	mV
Input Operation Current	eFuse Enabled and Soft start completed Buck/Storage Regulator Disabled ADC Disabled Storage Health Check Disabled All PMIC BUCKs turned on, no load PMIC_Boost turned on, no load VIN=12V		3.3		mA
	eFuse Enabled and Soft start completed Buck/Storage Regulator Disabled ADC Enabled Storage Health Check Disabled All PMIC BUCKs turned on, no load PMIC_Boost turned on, no load VIN=12V		4.1		mA
Input Current (Shutdown)	VIN=12V, GPIO5 set as FORCE_OFF pin to turn off IC.		0.59		mA
Thermal					
Thermal Warning Rising	Sets nIRQ		125		°C
Thermal Warning Hysteresis			34		°C
Thermal Shutdown 1 Rising – Disables buck and boost			145		°C
Thermal Shutdown 1 Hysteresis			28		°C
Thermal Shutdown 2 Rising – Disables eFuse			155		°C
Thermal Shutdown 2 Hysteresis			28		°C
STR Thresholds					
Input Under Voltage Lock Out (STR_UVLO)	STR Falling	2.7	2.8	3.1	V
Input Under Voltage Lock Out (STR_UVLO)	STR Rising		3.1		V

VIN UV & OV Thresholds					
Under Voltage Falling Threshold Programmable Range	UV REF after POR release (-40°C ~ 125°C), percentage of VIN_SEL	80		95	%
Under Voltage Threshold Accuracy		-5	0	5	%
UV Hysteresis			2		%
Overvoltage Reference Rising Threshold Programmable Range	OV REF after POR release, percentage of VIN_SEL	106		120	%
Over Voltage Threshold Accuracy		-5.5	1%	5.5	%
OV Hysteresis			2		%

Note 1: PLP System will only turn on when VIN>VIN_UVLO rising threshold, but it will stay on until VIN drops below the VIN UV falling threshold.

ELECTRICAL CHARACTERISTICS: PLP REGULATOR

(VSTR = 28V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage Range	V_{STR}	3		31	V
Programmable Output Voltage Range		2.5		13.2	V
Standby Supply Current	V_{BUS} = 103%, Regulator Enabled, No Load, not switching	300	550	800	µA
Output Voltage Accuracy	V_{BUS} = 12V, I_{BUS} = 2A	-2	V_{NOM}	2	%
Line Regulation	V_{STR} = 31V to 16V, V_{BUS} = 12V, PWM Regulation		0.02		%/V
Load Regulation	V_{STR} = 28V, I_{OUT} = 500mA to 4A, V_{BUS} = 12V PWM Regulation		0.125		%/A
Power Good Threshold	V_{BUS} Rising		95		$\%V_{NOM}$
Power Good Hysteresis	V_{BUS} Falling		2		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{BUS} Rising	105	110	115	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{BUS} Falling		3		$\%V_{NOM}$
Programmable Switching Frequency Range	Not user selectable. Set by factory with CMI		562 1125 1500 2250		kHz
Current Limit, Cycle-by-Cycle	BK_CLIM = 000 BK_CLIM = 001 BK_CLIM = 010 BK_CLIM = 011 BK_CLIM = 100 BK_CLIM = 101 BK_CLIM = 110 BK_CLIM = 111		3 4 5 6 7 8 9 10		A
Current Limit, Cycle-by-Cycle Tolerance	At default BK_CLIM	-15		+15	%
	At other settings	-20		+20	%
Current Limit, Shutdown	Above BK_CLIM	+ 30	+55	+ 80	%
High Side On-Resistance	I_{SW} = -3A, V_{STR} = 12V		60		mΩ
Low Side On-Resistance	I_{SW} = 3A, V_{STR} = 12V		35		mΩ
SW Leakage Current	V_{STR} = 31V, V_{SW} = 0 or 31V			42	µA

ELECTRICAL CHARACTERISTICS: PLP EFUSE

(VIN = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Normal Mode					
Operating Voltage Range	VIN (Note 1)	2.7		14	V
eFuse On-Resistance (2 FETs Combined)	I_{SW} = -2A, VIN= 3.3V, 5V, and 12V, T_J = 25°C		17		mΩ
	I_{SW} = -2A, VIN= 3.3V, 5V, and 12V, T_J = 100°C		23		mΩ
Programmable eFuse Over Current Limit Range (ISET)	Set by ISET[3:0] (0x2D[3:0])	1.5		12	A
ISET Accuracy		-10		+10	%
Programmable eFuse Current Warning Threshold	VIN = 12V, Triggers nIRQ Pin, percentage vs ISET	75	90	99	%
	VIN = 3.3V, Triggers nIRQ Pin, percentage vs ISET	75	90	99	%
eFuse Overcurrent Detection Deglitch			10		µs
Current Limit Restart Time	Retry time when hit Over current limit when starting up		100		ms
eFuse Soft start slew	VBUS slew with CSS = 10nF	5.70	6.60	7.26	mV/us

Note 1: eFUSE starts when VIN goes above the VIN_UVLO rising threshold. The eFUSE stays on until VIN drops below the VIN UV falling threshold.

ELECTRICAL CHARACTERISTICS: PLP BLOCKING FET

(VIN = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Normal Mode					
Blocking FET On-Resistance	I_{SW} = -2A, V_{BUS}= 12V, T_J = 25°C		30		mΩ
	I_{SW} = -2A, V_{BUS}= 12V, T_J = 100°C		41		mΩ
Programmable Blocking FET Startup Soft Start Current	bfet_ISS = 00 bfet_ISS = 01 bfet_ISS = 10 bfet_ISS = 11 (not allowed)		150 210 305 n/a		mA
Current limit threshold	Full turn on state		2		A

ELECTRICAL CHARACTERISTICS: PLP STORAGE BOOST REGULATOR

(VIN = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Storage Boost Converter					
Operating Input Voltage Range	V_{BUS}	2.7		14	V
Programmable Output Voltage Range		5.5V or VIN		31	V
Peak switching Current	BST _CLIM = 00 BST _CLIM = 01 BST _CLIM = 10 BST _CLIM = 11		250 500 950 1500		mA
Standby Supply Current	V_{STR} = 103%, Regulator Enabled, not switching		125	215	µA
Output Voltage Accuracy	V_{STR} = 28V, I_{OUT} = 15mA (continuous PWM mode)	-3%	V_{NOM}	3%	V
Power Good Threshold (STR_UV)	V_{STR} Rising		95		$\%V_{NOM}$
Power Good Hysteresis	V_{STR} Falling		5		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{STR} Rising		110		$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{STR} Falling		3		$\%V_{NOM}$
Minimum On-Time			50		ns
Low Side FET On-Resistance	I_{SW} = 325mA		200		mΩ

ELECTRICAL CHARACTERISTICS: PLP HEALTH MONITOR

(VIN = 12V, TA = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Health Monitor					
Operating Voltage Range		4.2		31	V
Sink Current Source		9	10	11	mA
Programmable Health Monitor Current Sink Timer Range		2		2304	ms
Programmable Storage Capacitor power good Threshold	Configurable 0.5% steps	90.5		98	%
STR Capacitor Measurement Range		47		8000	µF
STR Capacitor Measurement Accuracy		-15		15	%
ADC Monitoring					
Supply Current	Enabled		2		mA
Total Error	5V scale and 12-bit range			1	LSB
Conversion Time	Total time for all channels			100	ms
Conversion Time	Total time for single channel			10	ms
Full Scale Input Range		0		2.5	V
Input Resistance			10		kΩ
Input Capacitance			5		pF

ELECTRICAL CHARACTERISTICS: PMIC SYSTEM CONTROL

(VBUS = 12.0V, VCC = 5.0V, TA = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{BUS}	2.7		14	V
Input UV Threshold, falling.		2.5	2.6	2.7	V
Input UV Threshold, hysteresis			110		mV
Input UV detection deglitch time.		75	100	125	µs
Power Up Delay after initial VIN	Time from VBUS > UVLO threshold to time when regulator starts turning on.		1200		µs
VBUSMON Threshold Rising. VBUS rising threshold triggers the power on sequence.	VBUSMON [2:0] = 000		3.0		V
	VBUSMON [2:0] = 001		3.2		V
	VBUSMON [2:0] = 010		3.4		V
	VBUSMON [2:0] = 011		3.6		V
	VBUSMON [2:0] = 100		3.8		V
	VBUSMON [2:0] = 101		4.0		V
	VBUSMON [2:0] = 110		8.0		V
	VBUSMON [2:0] = 111		9.0		V
VBUSMON Threshold Fallling. VBUS falling triggers nIRQ	VBUSMON [2:0] = 000.		2.8		V
	VBUSMON [2:0] = 001		3.0		V
	VBUSMON [2:0] = 010		3.2		V
	VBUSMON [2:0] = 011		3.4		V
	VBUSMON [2:0] = 100		3.6		V
	VBUSMON [2:0] = 101		3.8		V
	VBUSMON [2:0] = 110		7.0		V
	VBUSMON [2:0] = 111		8.0		V
Transition time from Low Power State to Active State	Time from I^2C command to clear LPM EN register bit (exit low power state) to time when the first regulator starts turning on.		510		µs
Oscillator Frequency		2.10	2.25	2.42	MHz

Regulator Programmable Startup Delay Timings between turn on events.	ONDLY=000 ONDLY=001 ONDLY=010 ONDLY=011 ONDLY=100 ONDLY=101 ONDLY=110 ONDLY=111	0 0.25 0.5 1 2 4 8 16		ms
Regulator Programmable Turn Off Delay	Configurable in 1ms steps	0	15	ms
nRESET, Programmable Delay Timing	Configurable to 20, 40, 60, and 100ms	20	100	ms
Retry time after entering PMIC Fault state	Time when all regulators are forced off before trying ON sequence again	100		ms
Watch dog timer	Monitors I^2C inactivity and time out function	8		s
Hard reset wait timer	Hard reset turns off the regulators, waits in the reset state for a “hard-reset time delay” and restarts the on sequence.	0.5		s

ELECTRICAL CHARACTERISTICS: PMIC BUCK1,2,3 STEP-DOWN DC/DC REGULATOR

(VBUS = 12.0V, VCC = 5.0V TA = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage		2.7		14	V
FB1,2,3, Output Voltage Range	Configurable in 20mV steps	0.6		5.26	V
	Configurable in 5mV steps	0.6		1.875	V
Continuous Output Current	DC current output, 0.47µH, Switching frequency = 1.0MHz, FB1,2,3, = 1.2V	4.0			A
Standby Supply Current	FB1,2,3 >= 103%, Regulator Enabled, FB1,2,3 = 1.8V, No Load		400		µA
DC Output Voltage Accuracy	0.6V > FB1,2,3 > 1.25V, IOUT = 3A (Continuous Conduction or CCM mode)	-12.5	VNOM	12.5	mV
	FB1,2,3 >= 1.25V, IOUT = 3A (Continuous Conduction or CCM mode)	-1	VNOM	1	%
Line Regulation	FB1,2,3 = 1.8V, VBUS = 5.0V to 13.2V, (Continuous Conduction or CCM mode)		0.5		%
Load Regulation	FB1,2,3 = 1.8V,0.1AA to 4.0A (Continuous Conduction or CCM mode)		0.6		%
Power Good Threshold / POK	FB1,2,3 Rising, POK [] = 1	86	90	94	%VNOM
	FB1,2,3 Rising, POK [] = 0	83	87	91	%VNOM
Power Good Hysteresis / POK	FB1,2,3 Falling, relative to regulation point		3		%VNOM
Overvoltage Fault Threshold	FB1,2,3 Rising, relative to regulation point	107	114	118	%VNOM
Overvoltage Fault Hysteresis	FB1,2,3 Falling, relative to regulation point		3		%VNOM
Emulated Switching Frequency, CCM - Continuous Conduction Mode.	Freq = 0000, VIN = 12.0V, VFB1,2 = 1.0V		0.4		MHz
	Freq = 0001, VIN = 12.0V, VFB1,2 = 1.0V		0.5		MHz
	Freq = 0010, VIN = 12.0V, VFB1,2 = 1.0V		0.6		MHz
	Freq = 0011, VIN = 12.0V, VFB1,2 = 1.2V		0.7		MHz
	Freq = 0100, VIN = 12.0V, VFB1,2 = 1.2V		0.8		MHz
	Freq = 0101, VIN = 12.0V, VFB1,2 = 1.2V		0.9		MHz
	Freq = 0110, VIN = 12.0V, VFB1,2 = 1.8V		1.0		MHz
	Freq = 0111, VIN = 12.0V, VFB1,2 = 1.8V		1.1		MHz
	Freq = 1000, VIN = 12.0V, VFB1,2 = 1.8V		1.2		MHz
	Freq = 1001, VIN = 12.0V, VFB1,2 = 2.5V		1.3		MHz
	Freq = 1010, VIN = 12.0V, VFB1,2 = 2.5V		1.4		MHz
	Freq = 1011, VIN = 12.0V, VFB1,2 = 2.5V		1.5		MHz
	Freq = 1100, VIN = 12.0V, VFB1,2 = 3.3V		1.6		MHz

	Freq = 1101, VIN = 12.0V, VFB1,2 = 3.3V		1.7		MHz
	Freq = 1110, VIN = 12.0V, VFB1,2 = 3.3V		1.8		MHz
	Freq = 1111, VIN = 12.0V, VFB1,2 = 3.3V		1.9		MHz
Emulated switching frequency accuracy	At the default switching frequency setting	-20		20	%
TMIN, Minimum on Time			50		ns
Softstart Period TSS	5% to 95% VNOM	540	1000	1500	µs
Tstart, Time from EN to PG	Time from enable to PGOOD		1350		µs
Peak Current Limit, Cycle-by-Cycle	ILIM set = 00		6		A
	ILIM set = 01		7		A
	ILIM set = 10		8		A
	ILIM set = 11		9		A
Peak Current Limit, Cycle-by-Cycle Accuracy	At default ILIM setting	-15		15	%
Valley Current Limit, Cycle-by-Cycle	ILIM set = 00		5		A
	ILIM set = 01		6.1		A
	ILIM set = 10		6.8		A
	ILIM set = 11		7.5		A
Valley Current Limit, Cycle-by-Cycle Accuracy	At default ILIM setting	-33		33	%
LS FET reverse conduction current limit			3.6		A
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	115	125	135	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	69	78	91	%
HS On-Resistance	ISW = 1A, VCC5 = 5.0V		33		mΩ
LS NMOS On-Resistance	ISW = 1A, VCC5 = 5.0V		16		mΩ
SW Leakage Current	VIN = 12.0V, VSW = 0 or 12.0V			1	µA
Dynamic Voltage Scaling Rate	Buck output voltage range set to 5mV steps		0.022		mV/us
	Buck output voltage range set to 20mV steps		0.088		mV/us
Output Pull Down Resistance	Pull Down resistor is enabled when the regulator is turned off. PD_OPTION[]=0		6		Ohms
	PD_OPTION[]=1		20		Ohms

ELECTRICAL CHARACTERISTICS: PMIC BUCK4 STEP-DOWN DC/DC REGULATOR

(VBUS = 12.0V, VCC = 5.0V, TA = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage		2.7		14	V
FB4, Output Voltage Range	Configurable in 20mV steps	0.6		5.26	V
	Configurable in 5mV steps	0.6		1.875	V
Continuous Output Current	DC current output, 0.47µH, Switching frequency = 1.0MHz, FB4 = 1.2V.	2.0			A
Standby Supply Current	FB4 >= 103%, Regulator Enabled, FB4 = 1.8V, No Load		428		µA
DC Output Voltage Accuracy	0.6V > FB4 > 1.25V, IOUT = 1A (Continuous Conduction or CCM mode)	-12.5	VNOM	12.5	mV
	FB4 >= 1.25V, IOUT = 1A (Continuous Conduction or CCM mode)	-1	VNOM	1	%
Line Regulation	FB4 = 1.8V, VBUS = 5.0V to 13.2V, (Continuous Conduction or CCM mode)		0.5		%
Load Regulation	FB4 = 1.8V, 0.1A to 2.0A (Continuous Conduction or CCM mode)		0.6		%
Power Good Threshold / POK	FB4 Rising, POK [] = 1	86	90	94	%VNOM
	FB4 Rising, POK [] = 0	83	87	91	%VNOM
Power Good Hysteresis / POK	FB4 Falling, relative to regulation point		3		%VNOM
Overvoltage Fault Threshold	FB4 Rising, relative to regulation point	108	114	118	%VNOM
Overvoltage Fault Hysteresis	FB4 Falling, relative to regulation point		3		%VNOM
Emulated Switching Frequency, CCM - Continuous Conduction Mode.	Freq = 0000, VIN = 12.0V, VFB3,4 = 1.0V		0.4		MHz
	Freq = 0001, VIN = 12.0V, VFB3,4 = 1.0V		0.5		MHz
	Freq = 0010, VIN = 12.0V, VFB3,4 = 1.0V		0.6		MHz
	Freq = 0011, VIN = 12.0V, VFB3,4 = 1.2V		0.7		MHz
	Freq = 0100, VIN = 12.0V, VFB3,4 = 1.2V		0.8		MHz
	Freq = 0101, VIN = 12.0V, VFB3,4 = 1.2V		0.9		MHz
	Freq = 0110, VIN = 12.0V, VFB3,4 = 1.8V		1.0		MHz
	Freq = 0111, VIN = 12.0V, VFB3,4 = 1.8V		1.1		MHz
	Freq = 1000, VIN = 12.0V, VFB3,4 = 1.8V		1.2		MHz
	Freq = 1001, VIN = 12.0V, VFB3,4 = 2.5V		1.3		MHz
	Freq = 1010, VIN = 12.0V, VFB3,4 = 2.5V		1.4		MHz
	Freq = 1011, VIN = 12.0V, VFB3,4 = 2.5V		1.5		MHz
	Freq = 1100, VIN = 12.0V, VFB3,4 = 3.3V		1.6		MHz

	Freq = 1101, VIN = 12.0V, VFB3,4 = 3.3V		1.7		MHz
	Freq = 1110, VIN = 12.0V, VFB3,4 = 3.3V		1.8		MHz
	Freq = 1111, VIN = 12.0V, VFB3,4 = 3.3V		1.9		MHz
Emulated switching frequency accuracy	At the default switching frequency setting	-20		20	%
TMIN, Minimum on Time			50		ns
Softstart Period TSS	5% to 95% VNOM	540	1000	1500	µs
Tstart, Time from EN to PG	Time from enable to PGOOD		1350		µs
Peak Current Limit, Cycle-by-Cycle	ILIM set = 00		2		A
	ILIM set = 01		3		A
	ILIM set = 10		4		A
	ILIM set = 11		5		A
Peak Current Limit, Cycle-by-Cycle Accuracy	At default ILIM setting	-15		15	%
Valley Current Limit, Cycle-by-Cycle	ILIM set = 00		2.0		A
	ILIM set = 01		2.5		A
	ILIM set = 10		3.1		A
	ILIM set = 11		3.8		A
Valley Current Limit, Cycle-by-Cycle Accuracy	At default ILIM setting	-33		33	%
LS FET reverse conduction current limit			2.9		A
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	110	125	135	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	69	80	91	%
HS On-Resistance, Buck 1	ISW = 1A, VCC5 = 5.0V		60		mΩ
LS NMOS On-Resistance, Buck 1	ISW = 1A, VCC5 = 5.0V		30		mΩ
HS On-Resistance, Buck 2	ISW = 1A, VCC5 = 5.0V		60		mΩ
LS NMOS On-Resistance, Buck 2	ISW = 1A, VCC5 = 5.0V		30		mΩ
SW Leakage Current	VIN = 12.0V, VSW = 0 or 12.0V			1	µA
Dynamic Voltage Scaling Rate	Buck output voltage range set to 5mV steps		0.022		mV/us
	Buck output voltage range set to 20mV steps		0.088		mV/us
Output Pull Down Resistance	Pull Down resistor is enabled when the regulator is turned off. PD_OPTION[]=0		6		Ohms
	PD_OPTION[]=1		20		Ohms

ELECTRICAL CHARACTERISTICS: PMIC BOOST STEP-UP DC/DC REGULATOR

(VBUS = 12V, VCC = 5.0V, TA = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Boost Operating Input Voltage	Can be external supply not connected to ACT85610	2.5		13.2	V
Output Voltage Range	Configurable in 50mV steps	MAX (VIN, 10.8)	12	13.2	V
Output Step Size			50		mV
Output Voltage Accuracy	VINB = 5.0V, VOUT = 12.0V, IOUT = 0.5A	-2		2	%
	VINB = 5.0V, VOUT = 12.0V, IOUT = 0.1A	-2		2	%
Continuous Output Current	VINB = 12.0V, 4.7µH, VOUT = 12.0V, ILIM set = 11.			2	A
	VINB = 5.0V, 4.7µH, Switching frequency = 1MHz, VOUT = 12.0V, ILIM set = 11.			1	A
	VINB = 3.3V, 4.7µH, Switching frequency = 1MHz, VOUT = 12.0V, ILIM set = 11.			0.6	A
Iq, Supply Current.	Regulator is switching, no load		120		µA
SW5 leakage from VINB and VOUT (input or output)	SW5 = 0V / 12V, VINB =12V			1	µA
Line Regulation (DC)	VOUT = 12V, VINB = 3V-11V, Iout = 200mA.		0.5		%
Load Regulation	VOUT = 12.0V, VINB = 5.0V, 0.1A to 0.5A.		0.2		%
Power Good Threshold	VOUT Rising, relative to regulation point	82	86	90	%VNOM
Power Good Hysteresis	VOUT Falling, relative to regulation point		3		%VNOM
Overvoltage Fault Threshold	VOUT Rising, relative to regulation point	109	112	116	%VNOM
Overvoltage Fault Hysteresis	VOUT Falling, relative to regulation point		3		%VNOM
Switching Frequency, CCM - Continuous Conduction Mode.	Frequency VINB = 5.0V, VOUT = 12.0V	-7 %	1125	+7 %	kHz
Softstart Period TSS	5% to 95% VNOM, VOUT = 12.0V		10		ms
Tstart, Time from EN to PG	Time from enable to PGOOD		11		ms
Current Limit, Cycle-by-Cycle	ILIM set = 00, Boost Mode		1.2		A
	ILIM set = 01, Boost Mode		1.7		A
	ILIM set = 10, Boost Mode		2.1		A
	ILIM set = 11, Boost Mode		2.5		A
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	115	125	140	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	69	80	90	%
LS1 NMOS On-Resistance	ISW = 0.2A, VCC = 5.0V,		0.1	0.15	Ω

ELECTRICAL CHARACTERISTICS: VCC REGULATOR

(VBUS = 12.0V, VCC = 5.0V, TA = 25°C, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage Range	VCC Regulator input voltage	2.7		14	V
Output Current	For external circuit and LDO input			100	mA
Output Voltage – mini-Buck			4.9 5.0 5.1 5.2		V
Output Voltage – mini-Buck Accuracy	With 100mA Current	-5		5	%
Output Voltage – mini-LDO	mBK_5V_LDO = 0 mBK_5V_LDO = 1		4.5 5		V
Output Voltage – mini- LDO Accuracy	With 10mA Current	-6		6	%
HS PMOS on Resistance	VBUS = 12.0V		520		mΩ
LS NMOS on Resistance	VBUS = 12.0V		470		mΩ
Recommended Component Values					
Input Capacitor, C_{VBUS}	25V, SMT, 0603		1		µF
Output Capacitor, C_{OUTVCC}	10V, SMT, 0402		0.22		µF
Output Capacitor, C_{OUTVCC}	10V, SMT, 0603		10		µF
Inductor	10uH, I_{SAT} > 500mA		10		µH

ELECTRICAL CHARACTERISTICS: LDO

(VIN_LDO = 5V, TA = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.6		5.5	V
Output Voltage Range – VSET	Configurable in 50mV steps	0.6		3.75	V
Output Voltage Accuracy	V_{IN_LDO} - V_{LDO_OUT} > 0.4V	-2	V_{SET}	2	%
Line Regulation	V_{IN_LDO} - V_{LDO_OUT} > 0.4V V_{IN_LDO} = 2.8V to 5.5V I_{LDO_OUT} = 1mA		0.026		% / V
Load Regulation	I_{LDO_OUT} = 1mA to 100mA, LDO_ILIM=1X		-1	0.5	% / A
Power Supply Rejection Ratio	f = 1kHz, I_{LDO_OUT} = 20mA, V_{LDO_OUT} = 1.8V		34		dB
	f = 10kHz, I_{LDO_OUT} = 20mA, V_{LDO_OUT} = 1.8V		37		
	f = 2.25MHz, I_{LDO_OUT} = 20mA, V_{LDO_OUT} = 1.8V		7.1		
Supply Current per Output	Regulator Disabled		0		µA
Supply Current per Output	Regulator Enabled, No load		25		µA
Softstart Period	V_{LDO_OUT} = 1.8V Setting (10% to 90%) LDO SS_RAMP=00 LDO SS_RAMP=01 LDO SS_RAMP=10 LDO SS_RAMP=11		 110 110 165 215		µs
	V_{LDO_OUT} = 2.5V Setting (10% to 90%) LDO SS_RAMP=00 LDO SS_RAMP=01 LDO SS_RAMP=10 LDO SS_RAMP=11		 145 145 175 215		
	V_{LDO_OUT} = 3.3V Setting (10% to 90%) LDO SS_RAMP=00 LDO SS_RAMP=01 LDO SS_RAMP=10 LDO SS_RAMP=11		 200 200 210 235		
Power Good Threshold	V_{LDO_OUT} Rising	89	93	97	$\%V_{NOM}$
Power Good Hysteresis	V_{LDO_OUT} Falling		3		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{LDO_OUT} Rising	104	110	115	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{LDO_OUT} Falling		3		$\%V_{NOM}$
Discharge Resistance			1600		Ω
Dropout Voltage	I_{LDO_OUT} = 30mA		20	90	mV
Dropout Voltage	I_{LDO_OUT} = 50mA, LDO_ILIM=01		33	150	mV
Dropout Voltage	I_{LDO_OUT} = 100mA, LDO_ILIM=1x		68	310	mV

Dropout Voltage	I_{LDO_OUT} = 150mA V_{IN_LDO23} > 2.8 LDO_ILIM=11	103	500	mV
Output Current Limit	LDO_ILIM=00 LDO_ILIM=01 LDO_ILIM=10 LDO_ILIM=11	80 145 225 390		mA

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{IO_IN} = 1.8V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low				0.35	V
SCL, SDA Input High	V_{IO_IN} = 1.8V	1.2			V
SDA Leakage Current	SDA = 5V			1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Frequency, f_{SCL}		0		1000	kHz
SCL Low Period, t_{LOW}		0.5			µs
SCL High Period, t_{HIGH}		0.26			µs
SDA Data Setup Time, t_{SU}		50			ns
SDA Data Hold Time, t_{HD}	(Note1)	0			ns
Start Setup Time, t_{ST}	For Start Condition	260			ns
Stop Setup Time, t_{SP}	For Stop Condition	260			ns
Capacitance on SCL or SDA Pin				10	pF
SDA Rise Time SDA, Tr	Device requirement			120	ns
SDA Fall Time SDA, Tf	Device requirement			120	ns
Pulse Width of spikes must be suppressed on SCL and SDA		0		50	ns

Note1: Comply to I²C timings for 1MHz operation - “Fast Mode Plus”.

Note2: No internal timeout for I²C operations, however, I²C communication state machine will be reset when entering UV/POR state.

Note3: This is an I²C system specification only. Rise and fall time of SCL & SDA not controlled by the device.

Note4: The ACT85610 has two I²C addresses. Address 0x26h is for the PLP and address 0x25h is for the PMIC.

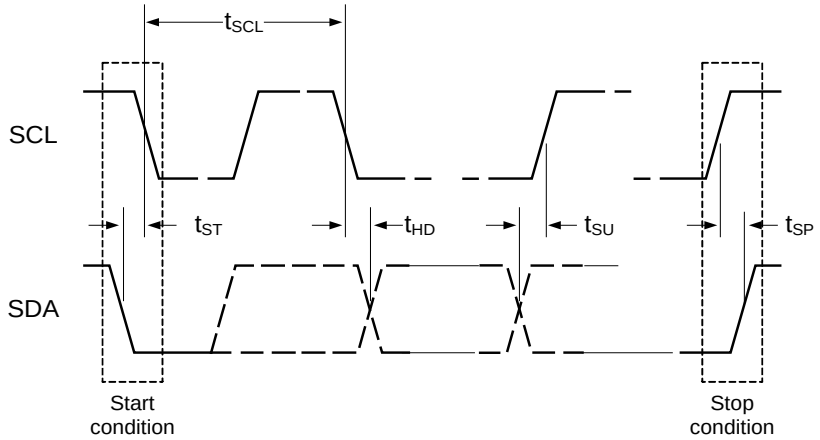


Figure 4: I²C Data Transfer

FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

ACT85610 provides protection, control, and supplemental storage for power failure prevention systems. This functionality goes by many names: Power Loss Protection (PLP), Power Loss Imminent (PLI) and Power Failure Protection (PFP). It provides a system with additional run time after a power failure so the system can save critical data before shutting down. Typical applications include solid state disk drives (SSD) and servers. In normal operation when input power is good, the IC connects the input to the output through the eFuse. This powers the system load from the system input power. If an input voltage fault occurs, the IC disconnects the input from the output and enters supplement mode. Supplement mode is an operating state where output power comes from the high voltage storage capacitor power. The internal buck converter efficiently converts the storage voltage down to the regulated output voltage. All startup, storage capacitor charging, and switching between normal and supplement mode operation is autonomous and does not require user intervention.

During start up, the ACT85610 limits the VBUS output voltage dV/dt to minimize system level inrush currents. After soft start is complete, the IC charges the storage capacitors with the internal boost converter. The IC automatically recharges the storage capacitors as needed. The IC contains extensive protection circuitry to protect against input voltage overvoltage and under voltage, output voltage overload and short circuit, degraded storage capacitors, and thermal overload.

When the ACT85610 detects that the input voltage drops below the programmed threshold, it turns the eFuse off and supplement mode is activated. This discharges the storage cap to provide back up power to VBUS. The integrated buck converter works in synchronous mode and can provides up to 8A current.

The ACT85610 is also a highly integrated high voltage PMIC. It contains four buck regulators and one boost regulator. The four buck regulators are high voltage or “HV” buck regulators and can operate over a wide input voltage range of 2.7V to 14V.

The boost regulator can accept input voltages between 2.5V to 14V. The output voltage is configurable between 10.8V to 13.2V. The typical output voltage is in the 12.0V range for many SSD applications.

The ACT85610 also has a combined mini buck and mini LDO to provide the power for internal blocks and gate driver. The IC operates with the highest efficiency when the input voltage is 5V or higher. This is because it is able to drive the internal gate drive circuitry with 5V to give the lowest on-resistance.

The IC communicates with the host processor via I^2C and GPIOs. The ACT85610 contains 6 GPIO pins. These GPIOs allow a variety of functions to be implemented. They can be used as inputs, open drain outputs, or as analog input/outputs. The analog GPIOs also allow an analog comparator function where the input to the GPIO pin is compared against an internal reference voltage and the result can be output as an internal signal or can also be routed back through a second GPIO output pin.

In addition, the dedicated Power Loss Indicator (PLI) pin automatically and immediately goes low to indicate a power loss condition. This gives the system advanced warning to complete all active tasks and shutdown. See the Pin Function section for additional PLI pin functionality.

The GPIO configurability and flexibility allow the user to optimize the IC functionality for their requirements. GPIO programmability includes nRESET, Power Good (PG), interrupt pin (nIRQ), “power okay” (POK) outps from individual regulators, digital inputs to control power sequencing of internal regulators, digital inputs/outputs to control external regulators, digital inputs to enter or exit low power mode, digital inputs to monitor power good signals from external regulators, Dynamic Voltage Scaling (DVS) inputs to control the buck regulator voltage, and an ADC input.

The output turn on sequence is fully configurable. The same is true for the power OFF sequence. The dependency of each regulator output on other regulator outputs and the ON/OFF delays for each regulator can all be configured for each of the Buck regulators and the

Boost regulator independently. The output voltages for each regulator are programmable via I²C and the default value during power up can be changed by programming different settings during factory test – referred to as a CMI or Coding Matrix Index. By changing the CMI program during factory testing, the default values during power up that control the power-on/off sequence, output voltage and current settings of regulators, fault detection settings, interrupt generation, GPIO functions and low power mode settings can all be factory programmed to specifically suit different applications. The PMIC can use its GPIOs to control external regulators which allows it to behave like a single, but larger power management system. It provides system level power control without the need for external logic and extra microcontrollers.

The default configuration values are also modifiable via I²C commands and can therefore be altered by firmware at any time. During power up, the user has I²C control and can change default power sequencing for outputs that are not automatically turned on at startup.

In low power state, some or all regulator outputs can be turned OFF, or their volage can be lowered do save power. The user has full control over which power supplies respond either stay on, turn off, or change voltage in the low power state. The low power state should be viewed as configurable state that the user is allowed to configure. This state can be defined or altered each time before entering it or left unchanged from the default programmed state. The default behavior for low power state is independently configurable for each output. Low power mode can also be configured differently before entering the state each time, which allows the user to control and change the low power configuration based on system level conditions.

GPIO power sequencing (turning an output on with a GPIO input) has four turn-on delay options: 0ms, 2.5ms, 5ms, and 10ms delay setting options. This time delay is added to the rising edge GPIO input signal before triggering a regulator to turn on. Each GPIO delay time can be independently programmed.

STATE MACHINE DESCRIPTION

ACT85610 has several main states of operation: VIN UV/POR, eFuse Softstart, eFuse Fully On, PMIC Sequence Start, Power On, Low Power Mode, PMIC Fault, Health Check and Supplement. There are also two fault shutdown states, Thermal Shutdown and PMIC Fault

VIN UV/POR — this state is the first time power up, or when the input voltage is below the VIN_UV threshold. VIN_UV is set by register bits.

eFuse Softstart — this state is the eFuse inrush prevention turn on state. It monitors VIN and VBUS and uses the SS capacitor to control the current into VIN.

eFuse Fully On — this state is when the PLP system is operating normally after powering up. The eFuse is fully turned on and shorts VIN to VBUS. If the boost converter is programmed to turn on in this state, it turns on and charges the storage capacitors.

Health Check — this state is part of eFuse Fully On state. The IC uses its integrated health checking circuitry to check the storage capacitor capacity.

Supplement — this state occurs when a fault condition is detected. The ACT85610 usually enters supplement mode when there is an input power failure, and the input voltage has dropped below the VIN_UV threshold. The following conditions move the IC into this state:

1. VIN voltage below VIN_UV threshold
2. VIN voltage above the VIN_OV threshold which is set in register bits
3. Input voltage above the VIN_MAX threshold
4. eFuse current above the OC threshold
5. VIN – VBUS > 560mV
6. VBUS – VIN > 130mV

Supplement Disable — this state is when junction temperature is over 135°C, or there is an overvoltage on the storage capacitors. In this state, supplement mode is disabled and the IC will NOT provide power to VBUS if input power fails. The eFuse still stays on in this state.

PMIC Sequence Start — this state is when the eFuse is fully turned on, there is no fault condition in the PLP circuitry, and the PMIC portion of the IC starts to power up with the programmed sequence.

Power On — this state is when system is fully powered, all rails are on.

Low Power Mode — this state is when PMIC outputs turned off or changed voltage, which can be configured by GPIO or register bits.

PMIC Fault — this state is when PMIC outputs have OC/OV/UV conditions.

The eFuse, Boost converter, Buck converter, and ADC operation mode at each state are shown in the table below.

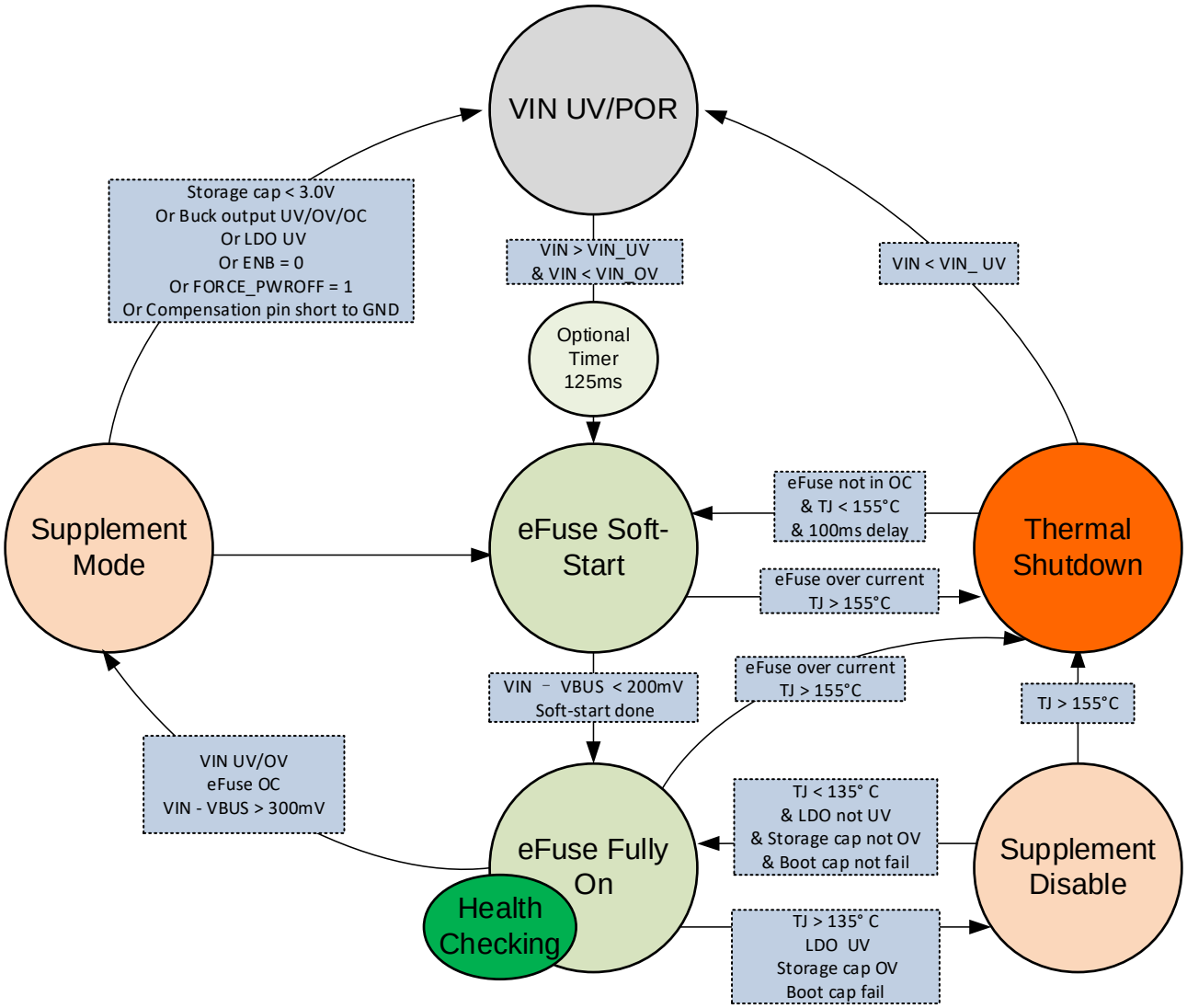
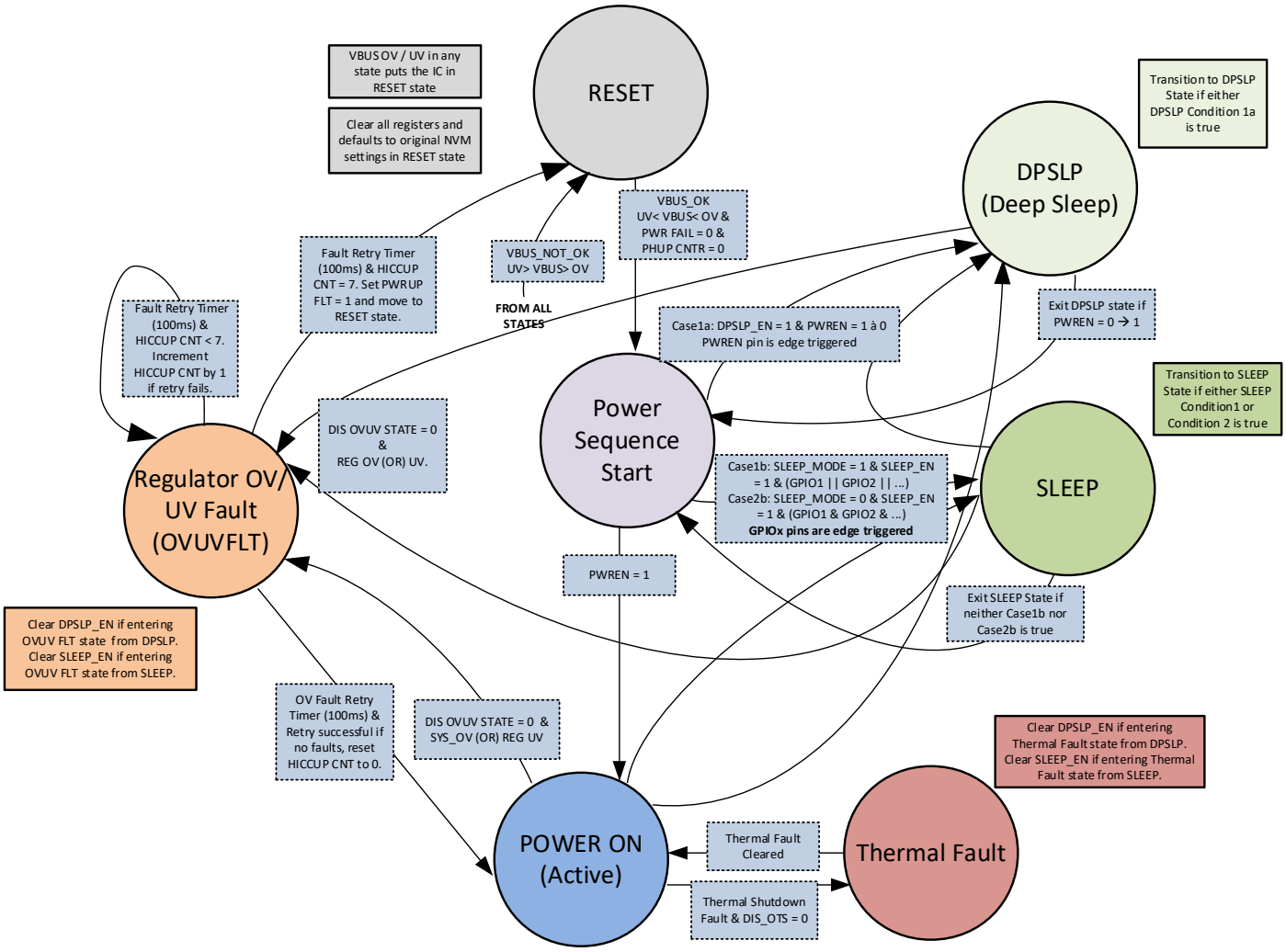


Figure 5: eFuse State Machine Diagram



LEGEND

DPSLP_MODE: Factory NVM Register bit to choose AND/OR Function for DPSLP conditions.

SLEEP_MODE: Factory NVM Register bit to choose AND/OR Function for SLEEP conditions.

DPSLP_EN: Basic NVM Register bit that has to be factory programmed or set to 1 by I^2C to allow entry into DPSLP state.

SLEEP_EN: Basic NVM Register bit that has to be factory programmed or set to 1 by I^2C to allow entry into DPSLP state.

GPIO1,2,3...: One or more GPIO pins that are configured as control inputs for DPSLP or SLEEP states (single GPIO can control one of SLEEP or DPSLP states)

Figure 6: PMIC State Machine Diagram

Table 1: Operation States

Operation Conditions	eFuse	Blocking FET	PLP Boost	PLP Buck	PMIC	PLI	PG_STR	IC Action
Normal Operation	On	On	Enabled	Off	On	High	High	Boost Charges STR Cap as needed
Input OC Vin - Vbus< 560mV (t < 10us)	On	On	Enabled	Off	On	High	High	eFuse in LDO Mode
Input OC Vin - Vbus > 560mV	On → Off	On	Off	On	On	Low	High → Low	Enter Supplement Mode
VBUS Short	On → Off	On	Off	On → Off	Off	Low	High → Low	Enter Supplement Mode
Input Over Voltage	On → Off	On	Off	On	On	Low	High → Low	Enter Supplement Mode
Input Under Voltage	On → Off	On	Off	On	On	Low	High → Low	Enter Supplement Mode
Health Checking	On	On	Standby or turn of for recharge	Off	On	High	High	If failed, PS_STR and nIRQ go low
Low Power Mode	On	On	Enabled	Off	As configured	High	High	PMIC outputs are as programmed
120°C < Tj < 145 °C	On	On	Enabled	Off	On	High	High	Sends out thermal alert
145 °C < Tj < 155 °C	On	On	Off	Off	On	High	Depends on Vstr	PG_STG depends on Vstr
Tj > 155 °C	Off	Off	Off	Off	Off	Low	Low	IC is disabled

EFUSE

DESCRIPTION

The ACT85610 performs as an eFuse for input transient voltage protection up to 20V. The internal eFuse FETs provide inrush current control, protection for high input voltage transients, defend against input and output short circuits, and block reverse current during power loss. This function is useful for hot-plugging environments when large transients occur due to the insertion and remove of large loads.

Input UV/OV

The ACT85610 senses the voltage at the VIN pin for the undervoltage, overvoltage, enable, and supplement mode thresholds.

The ACT85610 has a hard coded UVLO voltage at 2.6V and OVLO at 14.4V. If the input voltage drops below 2.6V, the IC shuts down. When VIN is above 2.6V, I^2C is active, but the outputs won't turn on until the voltage goes above the secondary programable threshold discussed below. If the input voltage rises above 14.4V, the IC turns off the eFuse and enters supplement mode.

The ACT85610 has a second programmable VIN_UV and VIN_OV threshold to determine when to turn on and when to enter supplement mode. .

The programmable secondary UV and OV voltages are each set by a main register and a secondary register.

The VIN_UV threshold is set by the VIN_UV_SEL register and the VIN_UV_2nd_PER register. The VIN_UV_2nd_PER scales the VIN_UV_SEL threshold between 80% and 95% of the nominal value. For example, with a 12V system, set the VIN_UV threshold to 10.8V by setting VIN_UV_SEL = 12V and setting VIN_UV_2nd_PER = 90%. 12V*0.90=10.8V. Note that

VIN_UV_SEL is not user adjustable. The VIN_UV threshold should be set above the supplement buck's undervoltage threshold.

The VIN_OV threshold is set by the VIN_OV_SEL register and the VIN_OV_2nd_PER register. The VIN_OV_2nd_PER scales the VIN_OV_SEL threshold between 106% and 120% of the nominal value. For example, with a 12V system, set the VIN_OV threshold to 14.16V by setting VIN_OV_SEL = 12V and setting VIN_OV_2nd_PER = 118%. 12V*1.18=14.16V. VIN_OV can also be disabled. Note that VIN_OV_SEL is not user adjustable.

Table 2: Input Voltage Selection

VIN_UV_SEL [1:0] VIN_OV_SEL [1:0]	Input Voltage
00	3.3V
01	5V
10	7.5V
11	12V

Table 3: Under Voltage Reference Settings

VIN_UV_2ND_PER [2:0]	VIN_UV Threshold (V)	
	VIN_UV_2ND_PER [3] = 0	VIN_UV_2ND_PER [3] = 1
000	80%	88%
001	81%	89%
010	82%	90%
011	83%	91%
100	84%	92%
101	85%	93%
110	86%	94%
111	87%	95%

Table 4: Over Voltage Reference Settings

VIN_OV_2ND_PER [2:0]	VIN_OV Threshold (V)	
	VIN_OV_2ND_PER [3] = 0	VIN_OV_2ND_PER [3] = 1
000	Disabled	113%
001	106%	114%
010	107%	115%
011	108%	116%
100	109%	117%
101	110%	118%
110	111%	119%
111	112%	120%

eFuse Current Limit Setting

ACT85610 eFuse uses two separate settings to limit the inrush current. The first is an internal current limit circuit. Current limit is set by the ISET[3:0] register bits.

Table 5: eFuse Current Limit Settings

ISET [2:0]	ISET [3] = 0	ISET [3] = 1
000	1.5A	9A
001	2A	10A
010	3A	11A
011	4A	12A
100	5A	12A
101	6A	12A
110	7A	12A
111	8A	12A

When the eFuse current is over the ISET threshold, it works in linear mode. This limits the current and results in the VBUS voltage dropping. After 10us, the eFuse turns off to avoid overheating. The eFuse also turns off if the VIN to VBUS voltage difference exceeds 560mV. The IC enters supplement mode when the eFuse turns

off. Note that during startup, if the eFuse current exceeds 90% of the ISET value, the IC turns the eFuse off and restarts the softstart process.

The IC also has a secondary overcurrent protection threshold to protect against short circuit events. If the eFuse current reaches this secondary level set by the EFUSE_OC SETTING [1:0] bits in register 0x2Ch [3:2], the eFuse current immediately turns off and enter supplement mode.

Table 6: eFuse Over Current Protection Threshold

EFUSE_OC SETTING [1:0]	OC Threshold
00	6.5A
01	10.5A
10	14.5A
11	18.5A

Softstart

The second overcurrent protection is set by a softstart capacitor connected to the SS pin. This capacitor set the softstart time to ramp the VBUS to its final voltage. The voltage on the SS pin controls the start-up of the eFuse output. The SS pin can be used to program the softstart time or it can be connected to an different voltage source to force the VBUS startup time to track another supply during startup. The SS pin has an internal pull-up current source of 5μA (typical) that charges the external softstart capacitor to provide a linear ramping voltage at the SS pin. The following equation calculates the required softstart capacitance

$$C_{SS}(nF) = \frac{65 \times T_{SS}(ms)}{V_{BUS}(V)} \qquad \text{Equation 1}$$

Where the T_{SS} is the softstart time, and the VBUS is the output voltage.

PLI Function

The PLI pin has three possible functions which are set by the internal I²C registers. The PLI_FUNC_SEL bits in register 0x26h set these functions.

nSPLMNT. Set register bits PLI_FUNC_SEL[1:0] in 0x26h to 00 to configure PLI for this function. With this setting, PLI goes low when the IC is in Supplement mode and goes open drain when the IC is not in Supplement mode. This setting lets the system uP know that power loss is imminent.

PG_STR function. Set PLI_FUNC_SEL = 01 to configure PLI for this function. With this setting, PLI starts low during softstart and then goes high when the storage capacitor voltage is in regulation. It goes low if the storage voltage drops below 95% of its programmed output voltage.

VIN_VALID&nSPLMNT function. Set PLI_FUNC_SEL = 11 to configure PLI for this function. With this setting, PLI is open drain when VIN>VIN_UV and VIN< VIN_OV and the IC is not in Supplement mode. PLI goes low when VIN<VIN_UV or VIN>VIN_OV or the IC is in Supplement mode.

Note that PLI_FUNC_SEL = 10 is not a valid setting and it cannot be programmed to this value.

SUPPLEMENT BUCK REGULATOR

Description

The supplement Buck regulator is a voltage mode, synchronous PWM step-down converter that achieves peak efficiencies of up to 95%. The Buck minimizes noise in sensitive applications and allows the use of small external components. The buck is available with a variety of standard and custom output voltages and may be software-controlled via the I²C interface for systems that require advanced power management functions.

In supplement mode operation, the Buck can be disabled by setting FORCE_PWROFF = 0. If the Buck is forced off when the IC enters supplement mode, the IC immediately moves to the POR state. If the EN_DISC_VBUS = 1, VBUS and STR are discharged with a 50mA current sink. See Table 13 for details of the interaction between the EN_DISC_VBUS_VSTR and DISCHARGE_ALL bits.

Buck Output Voltage Range

The Buck regulator output voltage can be programmed by the BK_VOUT_SET [6:0] in register 0xCBh [6:0] from 2.5V to 13.2V in 100mV steps.

Table 7: Supplement Buck Output Voltage

BK_VOUT_SET [4:0]	BK_VOUT_SET [6:5] =			
	00	01	10	11
00000	2.5	5.7	8.9	12.1
00001	2.6	5.8	9.0	12.2
00010	2.7	5.9	9.1	12.3
00011	2.8	6.0	9.2	12.4
00100	2.9	6.1	9.3	12.5
00101	3.0	6.2	9.4	12.6
00110	3.1	6.3	9.5	12.7
00111	3.2	6.4	9.6	12.8
01000	3.3	6.5	9.7	12.9
01001	3.4	6.6	9.8	13.0
01010	3.5	6.7	9.9	13.1
01011	3.6	6.8	10.0	13.2
01100	3.7	6.9	10.1	13.2
01101	3.8	7.0	10.2	13.2
01110	3.9	7.1	10.3	13.2
01111	4.0	7.2	10.4	13.2
10000	4.1	7.3	10.5	13.2
10001	4.2	7.4	10.6	13.2
10010	4.3	7.5	10.7	13.2
10011	4.4	7.6	10.8	13.2
10100	4.5	7.7	10.9	13.2
10101	4.6	7.8	11.0	13.2
10110	4.7	7.9	11.1	13.2
10111	4.8	8.0	11.2	13.2
11000	4.9	8.1	11.3	13.2
11001	5.0	8.2	11.4	13.2
11010	5.1	8.3	11.5	13.2
11011	5.2	8.4	11.6	13.2
11100	5.3	8.5	11.7	13.2
11101	5.4	8.6	11.8	13.2
11110	5.5	8.7	11.9	13.2
11111	5.6	8.8	12.0	13.2

Protection

The Supplement Buck converter has several protection mechanisms to insure safe operation. It stops operation when input voltage from storage cap drops to STR_UVLO (2.8V); or the output voltage drops below the power good threshold; or the output voltage is above the over voltage threshold.

The UV threshold is set by the BUCK_VOUT_UVSET register, and can be set to 60% or 70% of the setpoint. When the buck output voltage goes below the threshold, the BUCK_nPG register bit goes high and the IC moves to the UV/POR state. BUCK_nPG can be masked by the BK_nPG_IRQ_Mask bit. If masked when the buck voltage drops below the threshold, the Buck converter runs in 100% duty cycle mode when the input voltage drops below the output voltage. The supplement buck undervoltage threshold should be set below the VIN_UV threshold.

Undervoltage lockout is achieved with the VBUSMON bits in register0x0Fh. VBUSMON can be programmed between 3.0V and 9V. The PMIC outputs will not turn on until the VBUS voltage rises above VBUSMON rising threshold. When VBUS falls below the VBUSMON falling threshold, nIRQ is asserted low, but the converters stay on.

The OV threshold is fixed at 110% of the setpoint.

The buck converter has cycle-by-cycle current limit that can be set between 3A and 10A. When the buck power FET current is over the 22.5% of ILIMSET, the converter immediately shuts down.

Table 8: Factory-set Buck Current Limit

BK_CLIM[2:0]	ILIMSET (A)
000	3
001	4
010	5
011	6
100	7
101	8
110	9
111	10

100% Duty Cycle Operation

The Buck regulator is capable of operating at up to 100% duty cycle. During 100% duty cycle operation, the high-side power MOSFET is held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage. This allows the system to use as much storage capacitor energy as possible.

Compensation

The Buck regulator utilizes external compensation placed on the COMP pin. The compensation of the design is required; simply follow a few simple guidelines described below when choosing external components.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A high quality ceramic capacitor must be connected between STR and PGND as close to the IC as possible.

Output Capacitor Selection

The Buck regulator is designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR. The Buck regulator is designed to operate with 44uF output capacitor over most of their output voltage ranges, although more capacitance may be desired depending on the duty cycle and load step requirements.

Two of the most common dielectrics are Y5V and X5R. Whereas Y5V dielectrics are inexpensive and can provide high capacitance in small packages, their capacitance varies greatly over their voltage and temperature ranges and are not recommended for DC/DC applications. X5R and X7R dielectrics are more suitable for output capacitor applications.

Inductor Selection

The Buck regulator utilizes voltage-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. These devices were optimized for operation with 1.5uH inductors at 1500kHz operation. Choose an inductor with a low DC-resistance and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%.

Operation Frequency

The Buck operation frequency can be factory-set to 562 kHz, 1.125 MHz, 1.5 MHz, or 2.25 MHz which allows the system to be optimized for different applications. The switching frequency is not user accessible.

Table 9: Recommended Supplement Buck Operation Frequency

STR voltage	Frequency max
<18V	2.25Mhz
18V-25V	1.5Mhz
25V-31V	1.125Mhz

STORAGE BOOST REGULATOR

General Description

The Storage regulator provides the ability to store charge on a bank of capacitors by boosting the voltage. It keeps the capacitors charged while the input supply is available. This regulator is an asynchronous boost regulator. When the IC switches from the eFuse Fully On to the Supplement Mode state, the boost turns off and is reconfigured into a buck regulator to transfer the storage voltage to the VBUS voltage. The boost output

voltage is set using internal registers and can be programmed between 5.5V and 31V.

Operating Mode

By default, the storage boost regulator operates in peak current mode, non-fixed frequency mode.

The peak switch current is programmed by a factory register, which is not customer accessible.

Table 10: Factory-set Boost Peak Current Settings

BST_ILIM [1:0]	(mA)
00	250
01	500
10	950
11	1500

Storage Capacitor Voltage

The storage capacitor voltage can is set by BST_VSET [7:0] in register 0xCAh between 5.5V and 31V with 100mV steps. Note that the storage voltage must always be set higher than the input voltage.

Table 11: Storage Cap Voltage Settings

BST_VSET [4:0]	BST_VSET [7:5]							
	000	001	010	011	100	101	110	111
00000	5.5	8.7	11.9	15.1	18.3	21.5	24.7	27.9
00001	5.6	8.8	12.0	15.2	18.4	21.6	24.8	28.0
00010	5.7	8.9	12.1	15.3	18.5	21.7	24.9	28.1
00011	5.8	9.0	12.2	15.4	18.6	21.8	25.0	28.2
00100	5.9	9.1	12.3	15.5	18.7	21.9	25.1	28.3
00101	6.0	9.2	12.4	15.6	18.8	22.0	25.2	28.4
00110	6.1	9.3	12.5	15.7	18.9	22.1	25.3	28.5
00111	6.2	9.4	12.6	15.8	19.0	22.2	25.4	28.6
01000	6.3	9.5	12.7	15.9	19.1	22.3	25.5	28.7
01001	6.4	9.6	12.8	16.0	19.2	22.4	25.6	28.8
01010	6.5	9.7	12.9	16.1	19.3	22.5	25.7	28.9
01011	6.6	9.8	13.0	16.2	19.4	22.6	25.8	29.0
01100	6.7	9.9	13.1	16.3	19.5	22.7	25.9	29.1
01101	6.8	10.0	13.2	16.4	19.6	22.8	26.0	29.2
01110	6.9	10.1	13.3	16.5	19.7	22.9	26.1	29.3
01111	7.0	10.2	13.4	16.6	19.8	23.0	26.2	29.4
10000	7.1	10.3	13.5	16.7	19.9	23.1	26.3	29.5
10001	7.2	10.4	13.6	16.8	20.0	23.2	26.4	29.6
10010	7.3	10.5	13.7	16.9	20.1	23.3	26.5	29.7
10011	7.4	10.6	13.8	17.0	20.2	23.4	26.6	29.8
10100	7.5	10.7	13.9	17.1	20.3	23.5	26.7	29.9
10101	7.6	10.8	14.0	17.2	20.4	23.6	26.8	30.0
10110	7.7	10.9	14.1	17.3	20.5	23.7	26.9	30.1
10111	7.8	11.0	14.2	17.4	20.6	23.8	27.0	30.2
11000	7.9	11.1	14.3	17.5	20.7	23.9	27.1	30.3
11001	8.0	11.2	14.4	17.6	20.8	24.0	27.2	30.4
11010	8.1	11.3	14.5	17.7	20.9	24.1	27.3	30.5
11011	8.2	11.4	14.6	17.8	21.0	24.2	27.4	30.6
11100	8.3	11.5	14.7	17.9	21.1	24.3	27.5	30.7
11101	8.4	11.6	14.8	18.0	21.2	24.4	27.6	30.8
11110	8.5	11.7	14.9	18.1	21.3	24.5	27.7	30.9
11111	8.6	11.8	15.0	18.2	21.4	24.6	27.8	31.0

Output Capacitor Selection

The storage regulator is designed to take advantage of the benefits of both super capacitors or bulk capacitors. The storage capacitors can be electrolytic, polymer, Tantalum, ceramic, super capacitors, or a combination of these.

Output Power Good Selection

The storage capacitor power good signal indicates if the capacitor voltage is over the programmed threshold. The threshold can be programmed by register HMON_THR [3:0]. The threshold is also used for storage capacitor health checking.

Table 12: Storage Capacitor PG Threshold

HMON_THR[2:0]	HMON_THR[3]	
	0	1
000	90.5%	94.5%
001	91.0%	95.0%
010	91.5%	95.5%
011	92.0%	96.0%
100	92.5%	96.5%
101	93.0%	97.0%
110	93.5%	97.5%
111	94.0%	98.0%

Storage Cap Discharge

In normal operation, the storage buck converter turns off before the storage capacitor is fully discharged. The ACT85610 allows the user to fully discharge the storage capacitor after the buck converter turns off. This feature is typically used during testing so the user can start the system with the storage voltage at 0V.

This circuit discharges VSTR and VBUS with a 50mA current sink to ground. Enable this function with the EN_DIS_CHG_VBUS_STR in register 0x2Ah bit 4. If this bit = 1 when the IC enters the VIN UV/POR state, the 50mA current sink will discharge VSTR and VBUS down to approximately 1.2V.

When ACT85610 enters power loss protection mode (Supplement state), the buck converter turns on to provide power to VBUS to power the system. A well designed system will have more than enough energy in the storage capacitor to allow the system to save its data and shutdown properly. This means that after the backup is complete, there will still be energy in the storage capacitors. With no load, the storage capacitors can stay charged for a long amount of time before the voltage drops to the UV threshold. The storage capacitor discharge function speeds up the process to pull the voltages down so the system can restart quicker. This discharge function can be activated through either an I²C command or a GPIO input.

The user can manually start the discharge process via I²C or with a GPIO. To start it with I²C, write a 1 into the DISCHARGE_ALL bit in register 0xEBh. Note that this bit's default value is 0.

To start the discharge process using a GPIO, first write a 1 into the EN_GPIO_DISCHARGE_ALL bit in register 0xEBh. Then pull the GPIO low to start the discharge process. The specific GPIO for this function is set by the ICs specific CMI. The resulting functionality is identical to using the I²C setting.

Note that neither the I²C or the GPIO option turns off the PMIC or VCC regulators. The just turn off the eFUSE They continue to run until their input voltage drops below UVLO. See Table 13 for the detailed interaction between DISCHARGE_ALL and EN_DISC_VBUS_VSTR.

Table 13 – Discharge Function Truth Table

I2C Bit settings			Behavior							
EN_DISC_VBUS_VSTR[]	DISCHARGE_ALL[]	FORCE_PWR_OFF[]	VBUS Output 50mA Discharge	STR Output 50mA Discharge	eFuse	STR Buck/Boost/BFET	VCC Regulator	PMIC Regulators	PLP State Machine Latches in POR	Condition to Exit POR State
0	1	0	No	No	Turns off	Off	n/a	n/a	No	VBUS < UVLO
0	0	1	No	No	Turns off	Off	n/a	n/a	Yes	VBUS & STR & VIN < UVLO
1	1	0	Yes	Yes	Turns off	Off	n/a	n/a	No	VBUS & STR < UVLO
1	0	1	Yes	Yes	Turns off	Off	n/a	n/a	Yes	VBUS & STR & VIN < UVLO

Below is a typical process for the discharge:

1. The IC enters supplement mode and the Buck starts supplying energy from the storage capacitors to VBUS.
2. System backup is complete. A typical application would be a solid-state drive (SSD). At this time, the storage capacitors can still have a significant amount of charge left in them.
3. Write a 1 into the DISCHARGE_ALL bit or pull the GPIO low with the EN_GPIO_DISCHARGE_ALL bit = 1.
4. The Supplement Buck converter turns off and then the IC disables Boost and turns off the eFuse Blocking FET.
5. VSTR and VBUS are then discharged by a 50mA current sink to ground.
6. When the VSTR & VBUS voltages drop below approximately 1.2V, the IC can no longer sink 50mA to ground. When the sink current drops below 10mA, the DISCHARGE_DONE bit changes to 1.
7. After the discharge stops, the DISCHARGE_ALL register is cleared and the IC moves into the VIN_UV/POR state.
8. Soft start starts again

Note that when the discharge process starts, the IC is latched into this state until the process completes. Even if the input voltage goes back above UVLO, the IC will continue the discharge process until the DISCHARGE_DONE bit is set to 1. After this time, the IC can restart. See Table 13 for details.

Blocking FET

The blocking FET is an internal MOSFET that provides isolation between the system output voltage (VBUS) and the storage capacitors. It provides system level fault tolerance that allows the system to continue operating normally in the event of a storage capacitor failure. During the blocking FET soft start, the blocking FET provides constant current to charge the storage capacitors. This current is programmable between 150mA and 500mA, and it is valid when the storage capacitor voltage is lower than the VBUS voltage. The blocking FET stays in soft start until the voltage across it (VBUS-VSPL) approaches 0V. After soft start is complete, the blocking FET turns on fully and the current limit is automatically set to 2A.

During startup, the constant current source linearly charges up the storage capacitors. If the storage capacitors are not charged up to VIN within 250ms, the IC assumes there is a fault condition and turns the blocking FET off for 250ms. It then retries to startup. This hiccup mode minimizes power dissipation and IC temperature with very large storage capacitance or with fault conditions. The BFET_HIC_OPTION register sets the number of times the BFET retries to startup into a fault condition. When BFET_HIC_OPTION[]=1 (0x34[0]) the BFET only tries to startup one time. If unsuccessful, the IC moves to Supplement Disable state. If BFET_HIC_OPTION = 0, the BFET continues to restart indefinitely. With extremely large storage capacitors such as supercapacitors, setting BFET_HIC_OPTION[]=0 results in the blocking FET turning on and off at a 250ms period until the storage capacitors are charged up to VIN. This is expected functionality and minimizes the power dissipation in the IC.

In normal operation, when the blocking FET is fully turned on, it applies VIN power to the boost converter, allowing the storage capacitors to charge up to their final value. When the IC enters supplement mode, the buck output power flows into the VSPL pin, through the blocking FET, and out of VBUS to the system.

The blocking FET limits a storage capacitor overload or short circuit condition to 2A. The blocking FET immediately turns off when its current reaches 2A. This causes the voltage at VSPL to drop and the IC generates a VSPL undervoltage fault and pulls nIRQ low. After 250ms, the blocking FET turns back on. If the fault has cleared, it enters softstart again. If the fault if still present, it immediately turns off again. Hiccup mode applies to both normal startup with very large storage capacitors and to short circuit conditions. Note that the IC enters the SUPPLEMENT-DISABLE state during both startup and short circuit conditions.

During this condition, the eFuse stays on and system continues to operate normally, even with a short circuit on VSPL or the storage capacitor.

The blocking FET can be manually turned on and off by the EN_BFET bit in register 0xEBh [0] with 0x34[1] = 1.

Note that disabling the blocking FET also disables the boost converter. This allows systems to startup faster by keeping the boost disabled until the system is up and running.

STORAGE CAP HEALTH MONITOR

GO/NO GO Test

The ACT85610 has an internal health monitor for the storage capacitors. It applies a constant 10mA for a selected time (HMON_TSET) followed by a 50mA current for 200us. It monitors the voltage on STR. If the voltage falls below a predetermined level (HMON_THR), a fault is indicated on PG_STR.

An MCU can control the health checking parameters and timing via I²C. It allows the user to adjust the duration of the current sink to account for different capacitor values and to also control when health checking is started. This can be used to avoid a health check routing during a critical system operation.

The boost converter is disabled during the health check. The HMON_THR is monitored only while the current source is on, and if the STR voltage falls below it, a fault is latched and both PG_STR and nIRQ are set low. After the health check is complete, the boost is turned on to replace the charge removed from the storage capacitor.

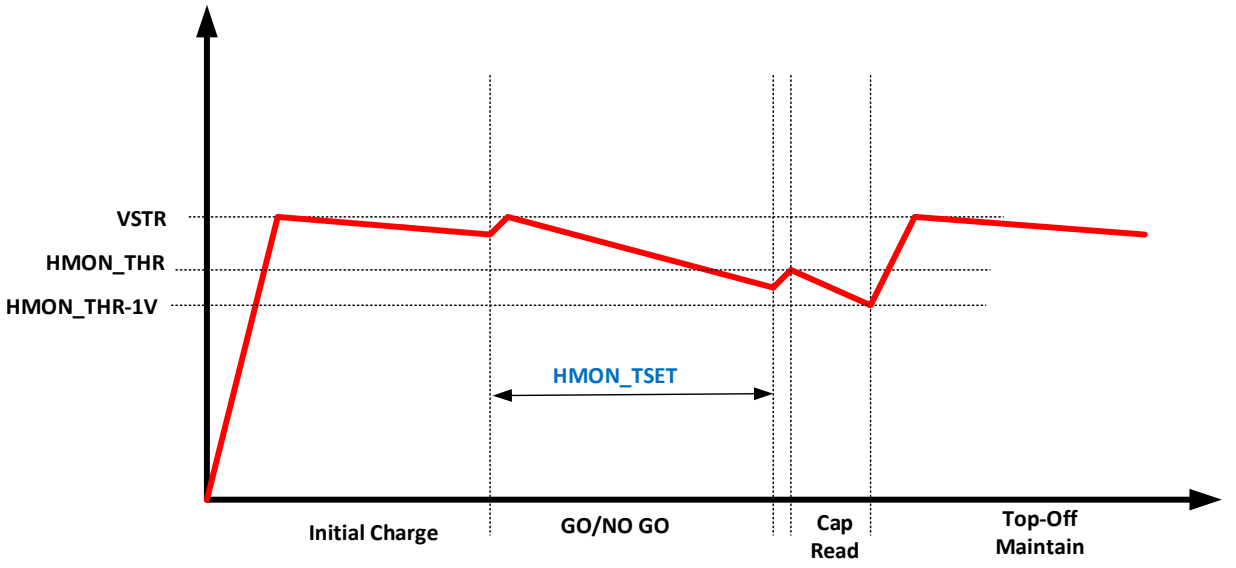
The health check routine can be manually started using I²C at any time using the steps below.

- Increase the storage capacitor voltage to at least 103% higher than the normal storage voltage setting using the 0xCAh BST_VSET register. This forces the boost converter to recharge the storage caps to the new voltage.
- Immediately send the command to start the health check routine by setting the FORCE_HLTHCHK bit in register 0xEAh to 1. Sending this command before the storage caps fully charge to the new setpoint ensures that the health check starts when the storage capacitor voltage is at its highest point.
- After the health check is complete, change the storage capacitor voltage back to the normal storage voltage.

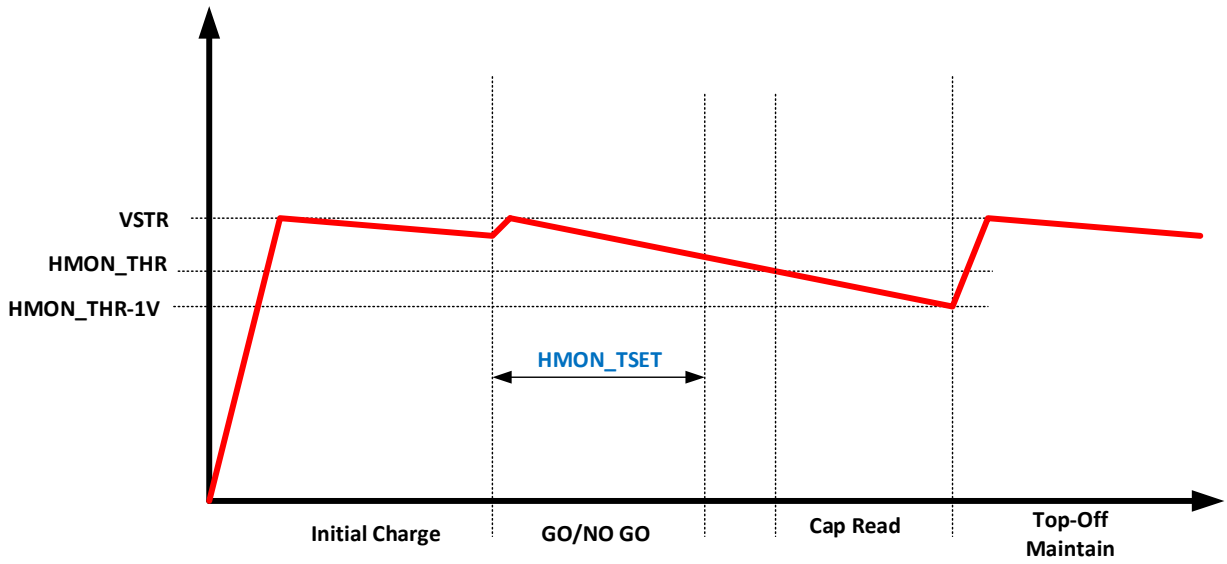
The health check discharge time is set by register HMON_TSET [3:0], as shown in Table 14. This also allows the use of the ADC to check the slope of the discharge and calculate the capacitance.

Table 14: Health Check Discharge Time

HMON_TSET[2:0]	HMON_TSET[3] (ms)	
	0	**1**
000	2	512
001	4	768
010	8	1024
011	16	1280
100	32	1536
101	64	1792
110	128	2048
111	256	2304



VSTR < BST_VSSET*HMON_THR after GO/NO GO test



VSTR > BST_VSSET*HMON_THR after GO/NO GO test

Figure 7: Storage Voltage at Different Stages

Storage Capacitance Read

ACT86510 also has a feature to calculate the storage capacitance. Each time the IC enters the health check state, after finishing the GO / NO GO health checking, the IC automatically measures the storage capacitance. If the capacitor voltage after the GO /NO GO checking is lower than the voltage set by BST_VSET * HMON_THR, then the boost turns on to charge the storage capacitor voltage to the BST_VSET * HMON_THR voltage and then reads the capacitance. For example, if BST_VSET = 28V and HMON_THR = 95%, the IC makes sure the storage voltage is at or above 28V*0.95 = 26.6V before starting the capacitance check. If the GO / NO GO checking passes and the capacitor voltage is still higher than the BST_VSET * HMON_THR threshold, the IC continues to discharge the capacitor and immediately starts a capacitance read when the capacitor voltage drops to BST_VSET * HMON_THR without turning on the boost to recharge the storage capacitors.

ACT85610 uses the 10mA current sink to discharge the storage cap while monitoring the voltage on STR. It discharges the storage capacitors until the voltage drops to 1V below the starting point. Based on the discharge time, the ACT85610 calculates the capacitance and stores the value in CAP_VALUE [12:0] in register 0xE0h [7:3] and 0xE4h [7:0].

The maximum capacitance that can be read is 8.191mF. A larger capacitance values returns the value 0x1FFFh.

There's a 5s timer for the total time of GO / NO GO checking and capacitance read. If the timer expires before the capacitance measurement is complete, the measurement routine stops and the IC moves back to the eFUSE Fully On state.

HIGH VOLTAGE STEP-DOWN DC/DC REGULATORS

General Description

BUCK1,2,3,4 are high voltage regulators and use a proprietary topology based on a Constant ON Time (COT) architecture. They are synchronous step-down converters that use a hysteretic constant on time mode that allow them to achieve low quiescent current during standby operation. The regulators can achieve high peak efficiencies higher than 95%. Typical efficiency depends on input and output voltage conditions and on load current. The HV buck regulators are highly configurable with many configurable parameters including switching frequency. They allow the use of small external components while emulating a constant frequency PWM mode regulator during continuous current mode operation under high load current situations. All regulators are available with a variety of standard and custom output voltages and may be software-controlled via the I^2C interface for systems that require advanced power management functions.

100% Duty Cycle Operation

The HV buck regulators are capable of operating at NEARLY 100% duty cycle but NOT fully 100% mode due to the minimum off-time needed for the Constant on Time hysteretic mode architecture. The maximum duty cycle limit is about 95% but is a function of the switching frequency and operating conditions such as input and output voltage and the load current. A minimum off-time is needed for controlling and bounding the frequency of operation for the switching regulators. During high duty cycle operation, the high-side power MOSFETs are held on continuously for the majority of the time as the constant on-time scales according to the ratio of Vout/Vin. This prolongs the high-side on time for high duty cycle cases and keeps the high-side on for nearly 100% of the time and provides a direct connection from the input to the output (through the inductor) to ensure the lowest possible dropout. However, the HS switch needs to turn off for at least the minimum off-time every switching cycle which limits the overall duty cycle to less than 100%.

Operating Mode

By default, the BUCK regulators operate in a pseudo fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary COT mode at light loads in order to improve efficiency at light loads.

Synchronous Rectification

Each BUCK regulator features an integrated synchronous rectifier (or LS FET), maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Softstart

The BUCK regulators include a fixed internal softstart ramp which limit the rate of change of the output voltage, minimizing input inrush current and ensuring that the output powers up in a monotonic manner that is independent of current load on the outputs. This circuitry is effective any time the regulator is enabled, as well as during re-try after responding to a short-circuit or other fault condition and helps control the inrush current during power up.

Dynamic Voltage Scaling

Dynamic Voltage Scaling (DVS) is supported through the I^2C interface. Change register bit EN_DVS_BY_I2C to a 1 to enter DVS mode. Two voltage settings are available for configuration in each Buck regulator. When DVS is enabled, the regulator transitions from VSET0 to the VSET1 setting and returns back to VSET0 during normal operation (DVS is off). During DVS, the regulator may be forced into a “forced PWM” mode. This is to ensure that the output reaches the new set point as quickly as possible when the output capacitor needs to be discharged. This helps to quickly slew the output voltage to its new setting when the new output voltage setting is lower than the previous setting. Without the feature, the transition to the lower voltage would be limited by how quickly the load current can discharge the output capacitor. When the output voltage register setting is changed via the I^2C, the digital logic in the regulator will step the output setting through each step between the initial and final settings. When the register values in the VSET [] register bits (See Register Map for BUCK regulators) is changed, the control logic steps the code between the previous and current settings. During this transition, the

regulators' OV and UV thresholds are ignored to avoid triggering any false OV or UV faults.

Output Pull Down Resistor

Each output has two options of discharge resistance to discharge the output voltage when the Bucks are off. The user can choose 6Ω or 20Ω pulldown resistance, or they can disable the pulldown resistance.

Enable / Disable Control

During normal operation, each BUCK regulator may be enabled or disabled via the I²C interface by writing to the regulator's ON [ ] bit.

POK [ ] and Output Fault Interrupt

Each regulator features a Power-OK (POK) status bit that can be read by the system microprocessor via the I²C interface. If an output voltage is lower than the power-OK threshold, typically ~10.0% below the programmed regulation voltage, that regulator's POK [ ] bit will be 0.

If a DC/DC's nFLTMSK [ ] bit is set to 1, the ACT85610 will interrupt the processor if the DC/DC's output voltage falls below the Power-OK (POK) threshold. In this case, the nIRQ pin (interrupt request pin) will assert low and remain asserted until either the regulator is turned off or back in regulation, and the POK [ ] bit has been read via I²C. The POK interrupt is latched low, and is only cleared when the condition that caused the interrupt is no longer present and the POK bit is read via I²C.

Compensation

The buck regulators utilize a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guidelines described below when choosing external components such as the inductor and output capacitor. While selecting these external components, the peak inductor current ripple, input and output voltage conditions, efficiency requirements and expected load conditions must be considered.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A 10μF ceramic capacitor is required for each regulator's input pins.

Output Capacitor Selection

The buck regulators were designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR capacitors. The buck regulators are designed to operate with 44μF (2x22μF) output capacitors over most of their output voltage ranges. More capacitance may be desired depending on the load current requirements of the regulator as well as the duty cycle, ripple, and the desired load step response. In addition, low power mode behavior and discharge time of the output capacitors, when experiencing bursts of load current intermittently, are also important criteria that can determine the value of output capacitors selected. Voltage de-rating that is more common and significant in small package sizes such 0402 should be carefully considered when choosing output capacitors. This is especially true with higher output voltages in which case there is a larger voltage bias on the output capacitors.

Two of the most common dielectrics are Y5V and X5R. Y5V dielectrics are inexpensive and can provide high capacitance in small packages, but their capacitance varies greatly over their voltage and temperature ranges, so they are not recommended for DC/DC applications. X5R and X7R dielectrics are more suitable for output capacitor applications.

Inductor Selection

All BUCK regulators utilize a Constant on Time and a hysteretic mode hybrid topology and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. The regulators in ACT85610 are optimized for operation with inductors in the 0.47μH to 2.2μH range. It is best to choose inductors with a low DC-resistance or DCR for higher efficiency and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum inductor peak current by at least 30%. Additionally, the inductor peak-to-peak current ripple must

be carefully considered along with the selected switching frequency before selecting appropriate inductor values with adequate current rating.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Ground shielding the output or feedback traces to the PMIC is recommended. Care must be taken by kelvin (star) connecting the feedback points for precise voltage regulation. In general, the output capacitors should be placed closest to the point of load and the feedback trace connected directly to the capacitors. High frequency bypass caps can be added to improve ripple and dynamic response to fast transients. Placing the inductor close to the PMIC is a good practice and minimizing currents in the ground plane that can cause ground current loops is important.

Step-down DC/DCs exhibit discontinuous input current, so the input capacitors must be placed as close as possible. Avoid using vias in the input capacitor PCB routing. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple vias. The output node for each regulator should be connected to its corresponding feedback/output pin (on the PMIC) through the shortest possible route, while keeping sufficient distance from switching nodes to prevent noise injection. Shielding the feedback traces with ground traces can help as stated earlier. Finally, the exposed pad should be directly connected to the backside ground plane using multiple via to achieve low electrical and thermal resistance.

BUCK Output Voltage Range

The Buck 1/2/3/4 output voltage can be programmed in 20mV steps from 0.6V to 5.26V or in 5mV steps from 0.6V to 1.875V.

Table 13: HV Buck Regulator Output Voltage Settings for BUCKS 1/2/3/4 with 20mV steps

BUCK_VSET [4:0]	BUCK_VSET [7:5]							
	000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
0 0000	0.60	1.24	1.88	2.52	3.16	3.80	4.44	5.08
0 0001	0.62	1.26	1.90	2.54	3.18	3.82	4.46	5.10
0 0010	0.64	1.28	1.92	2.56	3.20	3.84	4.48	5.12
0 0011	0.66	1.3	1.94	2.58	3.22	3.86	4.50	5.14
0 0100	0.68	1.32	1.96	2.60	3.24	3.88	4.52	5.16
0 0101	0.70	1.34	1.98	2.62	3.26	3.90	4.54	5.18
0 0110	0.72	1.36	2.00	2.64	3.28	3.92	4.56	5.20
0 0111	0.74	1.38	2.02	2.66	3.30	3.94	4.58	5.22
0 1000	0.76	1.4	2.04	2.68	3.32	3.96	4.60	5.24
0 1001	0.78	1.42	2.06	2.70	3.34	3.98	4.62	5.26
0 1010	0.80	1.44	2.08	2.72	3.36	4.00	4.64	5.26
0 1011	0.82	1.46	2.10	2.74	3.38	4.02	4.66	5.26
0 1100	0.84	1.48	2.12	2.76	3.40	4.04	4.68	5.26
0 1101	0.86	1.5	2.14	2.78	3.42	4.06	4.70	5.26
0 1110	0.88	1.52	2.16	2.80	3.44	4.08	4.72	5.26
0 1111	0.90	1.54	2.18	2.82	3.46	4.10	4.74	5.26

1 0000	0.92	1.56	2.20	2.84	3.48	4.12	4.76	5.26
1 0001	0.94	1.58	2.22	2.86	3.50	4.14	4.78	5.26
1 0010	0.96	1.6	2.24	2.88	3.52	4.16	4.80	5.26
1 0011	0.98	1.62	2.26	2.90	3.54	4.18	4.82	5.26
1 0100	1.00	1.64	2.28	2.92	3.56	4.20	4.84	5.26
1 0101	1.02	1.66	2.30	2.94	3.58	4.22	4.86	5.26
1 0110	1.04	1.68	2.32	2.96	3.60	4.24	4.88	5.26
1 0111	1.06	1.7	2.34	2.98	3.62	4.26	4.90	5.26
1 1000	1.08	1.72	2.36	3.00	3.64	4.28	4.92	5.26
1 1001	1.10	1.74	2.38	3.02	3.66	4.30	4.94	5.26
1 1010	1.12	1.76	2.40	3.04	3.68	4.32	4.96	5.26
1 1011	1.14	1.78	2.42	3.06	3.70	4.34	4.98	5.26
1 1100	1.16	1.80	2.44	3.08	3.72	4.36	5.00	5.26
1 1101	1.18	1.82	2.46	3.10	3.74	4.38	5.02	5.26
1 1110	1.20	1.84	2.48	3.12	3.76	4.40	5.04	5.26
1 1111	1.22	1.86	2.50	3.14	3.78	4.42	5.06	5.26

Table 16: HV Buck Regulator Output Voltage Settings for BUCKS 1/2/3/4 with 5mV steps

BUCK_VSET [4:0]	BUCK_VSET [7:5]							
	000	001	010	011	100	101	110	111
0 0000	0.600	0.760	0.920	1.080	1.240	1.400	1.560	1.720
0 0001	0.605	0.765	0.925	1.085	1.245	1.405	1.565	1.725
0 0010	0.610	0.770	0.930	1.090	1.250	1.410	1.570	1.730
0 0011	0.615	0.775	0.935	1.095	1.255	1.415	1.575	1.735
0 0100	0.620	0.780	0.940	1.100	1.260	1.420	1.580	1.740
0 0101	0.625	0.785	0.945	1.105	1.265	1.425	1.585	1.745
0 0110	0.630	0.790	0.950	1.110	1.270	1.430	1.590	1.750
0 0111	0.635	0.795	0.955	1.115	1.275	1.435	1.595	1.755
0 1000	0.640	0.800	0.960	1.120	1.280	1.440	1.600	1.760
0 1001	0.645	0.805	0.965	1.125	1.285	1.445	1.605	1.765
0 1010	0.650	0.810	0.970	1.130	1.290	1.450	1.610	1.770
0 1011	0.655	0.815	0.975	1.135	1.295	1.455	1.615	1.775
0 1100	0.660	0.820	0.980	1.140	1.30	1.460	1.620	1.780
0 1101	0.665	0.825	0.985	1.145	1.305	1.465	1.625	1.785
0 1110	0.670	0.830	0.990	1.150	1.310	1.470	1.630	1.790
0 1111	0.675	0.835	0.995	1.155	1.315	1.475	1.635	1.795
1 0000	0.680	0.840	1.000	1.160	1.320	1.480	1.640	1.800
1 0001	0.685	0.845	1.005	1.165	1.325	1.485	1.645	1.805
1 0010	0.690	0.850	1.010	1.170	1.330	1.490	1.650	1.810
1 0011	0.695	0.855	1.015	1.175	1.335	1.495	1.655	1.815
1 0100	0.700	0.860	1.020	1.180	1.340	1.500	1.660	1.820
1 0101	0.705	0.865	1.025	1.185	1.345	1.505	1.665	1.825
1 0110	0.710	0.870	1.030	1.1900	1.350	1.510	1.670	1.830
1 0111	0.715	0.875	1.035	1.195	1.355	1.515	1.675	1.835
1 1000	0.720	0.880	1.040	1.200	1.360	1.520	1.680	1.840
1 1001	0.725	0.885	1.045	1.205	1.365	1.525	1.685	1.845
1 1010	0.730	0.890	1.050	1.210	1.370	1.530	1.690	1.850
1 1011	0.735	0.895	1.055	1.215	1.375	1.535	1.695	1.855
1 1100	0.740	0.900	1.060	1.220	1.380	1.540	1.700	1.860
1 1101	0.745	0.905	1.065	1.225	1.385	1.545	1.705	1.865
1 1110	0.750	0.910	1.070	1.230	1.390	1.550	1.710	1.870
1 1111	0.755	0.915	1.075	1.235	1.395	1.555	1.715	1.875

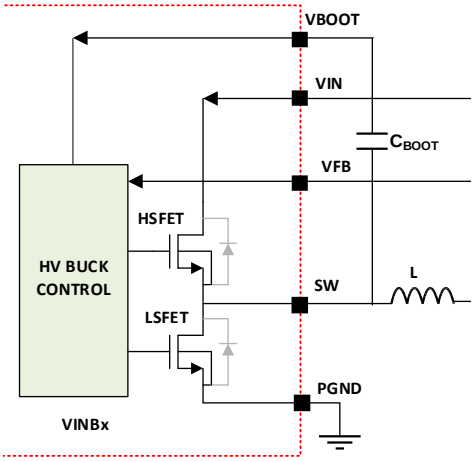


Figure 8: Buck Regulator Output Voltages

BOOST REGULATOR

General Description

The Boost regulator provides the ability to drive a high output voltage up to 13.2V and up to a maximum load current of 1.2A. The output voltage can be set between 10.8V to 13.2V in 50mV steps. The regulator is designed to use inductor values of 4.7µH or 6.8µH and has a switching frequency of 1125 kHz. By selecting a suitable value of inductor and an appropriate output capacitor, the regulator provides options to allow optimization of the regulator efficiency, output ripple and dynamic transient response under switched load conditions.

Note that the boost is a standard non-synchronous boost converter with a discrete diode. To ensure clean PWM switching without pulse skipping, the output voltage should be programmed higher than the input voltage. If the input voltage is programmed higher than the output voltage, the input voltage is passed straight through to the output and pulse skipping may occur. This will not damage the IC. Also note that the input voltage is passed straight through to the output when the boost is disabled. There are two options to make the boost output voltage equal to 0V when disabled. The first is to keep the boost input voltage at 0V when it is disabled. This can include powering the input voltage to the boost from one of the other PMIC output voltages that is turned off when the boost is turned off. The second option is to add a discrete FET between the boost output and the load. The Boost regulator has cycle-by-cycle current limiting on the low side FET (LSFET) to prevent the over current conditions.

Table 17: Boost Regulator Output Voltage Settings

Boost VSET [3:0]	Boost VSET [6:4]			
	000	001	010	011
0000	10.80	11.60	12.40	13.20
0001	10.85	11.65	12.45	13.20
0010	10.90	11.70	12.50	13.20
0011	10.95	11.75	12.55	13.20
0100	11.00	11.80	12.60	13.20
0101	11.05	11.85	12.65	13.20
0110	11.10	11.90	12.70	13.20
0111	11.15	11.95	12.75	13.20
1000	11.20	12.00	12.80	13.20
1001	11.25	12.05	12.85	13.20
1010	11.30	12.10	12.90	13.20
1011	11.35	12.15	12.95	13.20
1100	11.40	12.20	13.00	13.20
1101	11.45	12.25	13.05	13.20
1110	11.50	12.30	13.10	13.20
1111	11.55	12.35	13.15	13.20

VCC Regulator

ACT85610 has a 5V Buck VCC regulator to power the internal blocks. It can also provide 100mA to power external circuits. The Buck VCC is actually two circuits in one. It operates as a miniBuck and a miniLDO. The output should be connected to the VCC pin to power the

IC's internal circuitry. The miniBuck output voltage can be programmed to 4.9V, 5.0V, 5.1V, or 5.2V. The miniLDO can be programmed to 4.5V or 5.0V

At startup when VBUS increases above 2V, the miniLDO turns on to pull VCC higher than VCC_UVLO (2.6V). When VBUS increases above 3.5V, the mini-Buck turns on in parallel with the miniLDO to help quickly get the output to the output voltage setpoint. When VCC increases above the LDO's output voltage setpoint, the LDO effectively turns off and no longer supplies any current. However, if VCC drops below the miniBuck voltage setpoint due to excessive load, the miniLDO turns back on to provide extra load current to prevent the output voltage from dropping any more. The miniLDO is always enabled, but the miniBuck can be enable or disabled. Disable the miniBuck by setting the Force_Off_mBK bit in register 0x34h to 1. When the miniBuck is disabled, VCC is automatically regulated to the miniLDO setpoint.

Note that the VCC regulator output (miniBuck and miniLDO) is also the input source for the LDO.

With a 3.3V or 5V input, the miniBuck and miniLDO can be bypassed by connecting VCC directly to VBUS. However, with high load currents, load transients, and insufficient bypass capacitance, the switching noise on VBUS can directly couple into the VCC pin and affect the IC's internal bias supply. This condition can be minimized by inserting a small (0.1Ohm) resistor between VCC and VBUS and adding additional capacitance to VCC. Disabling the miniBuck and connecting SW6 directly to VCC also reduces noise coupled into VCC. This connection uses the miniLDO to help filter noise.

The miniBuck output inductor should be 10µH with at least a 500mA current rating.

LDO

ACT85610 has a built in LDO. The LDO input is internally connected to the VCC pin. When the VBUS voltage is 3.3V and the VCC pin is connected to VBUS, the maximum LDO output current is 300mA. When the Buck VCC is in switching mode, the maximum output current is 50mA because of VCC buck current capability limitation.

The LDO output range is 0.6V to 3.75V with 50mV steps.

Table 14: LDO Output Voltage

Lockset[3:0]	LDOx_VSET[5:4]			
	00	01	10	11
0000	0.60	1.40	2.20	3.00
0001	0.65	1.45	2.25	3.05
0010	0.70	1.50	2.30	3.10
0011	0.75	1.55	2.35	3.15
0100	0.80	1.60	2.40	3.20
0101	0.85	1.65	2.45	3.25
0110	0.90	1.70	2.50	3.30
0111	0.95	1.75	2.55	3.35
1000	1.00	1.80	2.60	3.40
1001	1.05	1.85	2.65	3.45
1010	1.10	1.90	2.70	3.50
1011	1.15	1.95	2.75	3.55
1100	1.20	2.00	2.80	3.60
1101	1.25	2.05	2.85	3.65
1110	1.30	2.10	2.90	3.70
1111	1.35	2.15	2.95	3.75

ADC

General Description

The ACT85610 contains a built-in analog to digital converter, ADC, which can be used to monitor eight system level parameters. These include input voltage, VBUS voltage, storage capacitor voltage, eFuse current, Buck 1 output voltage, GPIO1&2 A2D inputs, and die temperature. It is a single 12-bit delta-sigma ADC that uses an analog input multiplexer to select one of eight channels for the A/D conversion. For better accuracy, the last 2 LSB are not used for calculation. The resulting digital results are stored in eight digital registers. An eight to one multiplexer connects one of the ADC output registers to the user accessible register map.

ADC Configuration

The ACT85610 ADC is configured through the I²C interface. It is enabled and disabled by the EN_ADC register bit. The ADC has two conversion modes, manual single-shot conversion and automatic polling conversion.

Single-Channel Conversion

Configure the IC for single-channel conversion mode by setting the following I²C bits in register 0xE8h

ADC_ONE_SHOT = 1.

ADC_CH_SCAN = 0

EN_ADCBUF = 1

In single channel mode, the user defines the input channel to be converted and then manually initiates the ADC conversion. I²C bits ADC_CH_CONV [2:0] in register 0xE8h select the input channel to be converted. ADC_CH_READ [2:0] selects the ADC channel to be read. These should be set to the same channel. The user initiates an ADC read by writing a 1 into EN_ADC in register 0xE8h. When ADC conversion is complete, the ADC_DATA_READY bit (register 0xE7h [7]) is set to 1, nIRQ is asserted low, and EN_ADC automatically changes back to 0. The uP can then read the status bits to find that the ADC conversion is complete. The ADC data are stored in ADC_DOUT [13:6] in register 0xE5h for 8 MSB and in ADC_DOUT [5:0] in register 0xE6h for 6 LSB. The last 2 LSB data are not used for value calculation for better accuracy. nIRQ stays asserted low and the ADC_READY_BIT stays equal to 1 until the ADC data is read. Reading the ADC data automatically deasserts nIRQ. To initiate another ADC conversion for the same channel, set EN_ADC=1. To initiate an ADC conversion for another channel, change ADC_CH_CONV and ADC_CH_READ to the appropriate channel and then set EN_ADC=1.

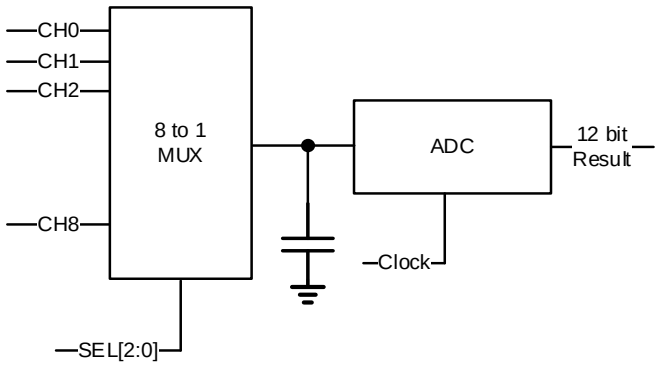


Figure 9: ADC Block Diagram

Multiple Channel Conversion

Configure the IC for multiple channel conversion by setting the following I²C bits in register 0xE8h

ADC_ONE_SHOT = 1

ADC_CH_SCAN = 1

EN_ADCBUF = 1

Start a conversion by changing EN_ADC to 1. This reads and stores the ADC results for all channels. After the conversion is complete, set ADC_CH_SCAN = 0. Define the channel to be read with the ADC_CH_CONV [2:0] bits in register 0xE8h and then read the ADC_DOUT values. Change ADC_CH_CONV to read additional channels.

ADC Value Calculation

Table 19 shows how to calculate the values of each channel with the 12-bit ADC data. Where for CH0 input current measurement, the V_Isense is the value that related with input current limit ISET [3:0]. Table 19 shows the setting. The DOUT_25 is the die temperature ADC value at 25C and stored at 0x23[3:0] as 4 MSB and 8 LSB at 0x24[7:0].

Table 15: ADC Channel Value Calculation

Channel	Channel Description	ADC_CH_CONV[2:0]	ADC_CH_READ[2:0]	Value
CH0	Input Current	000	000	IIN = (Dout_final -2048)*1.531*1e-3/V_Isense (A)
CH1	Input Voltage (bit 0x32[5]=0)	001	001	VIN = (Dout_final -2048)*0.0245 (V)
CH2	Storage Cap Voltage	010	010	VSTR = (Dout_final -2048)* 0.0245 (V)
CH3	Output Voltage	011	011	VOUT = (Dout_final -2048)* 0.0245 (V)
CH4	Die Temperature	100	100	Temp = (Dout_final - DOUT_25)/(DOUT_25-2048)*298 +25 (C)
CH5	Buck 1 Output	101	101	VBK1 = (Dout_final -2048)* 0.004593 (V)
CH6	A2D GPIO Input 1	110	110	VGPIO1 = (Dout_final -2048)* 0.00153125 (V)
CH7	A2D GPIO Input 2	111	111	VGPIO2 = (Dout_final -2048)* 0.00153125 (V)

ADC_offset = (-1)^Reg0x2E[7]*BIN (Reg0x2E[6:0])

Gain_Error = (-1)^Reg0x2F[5] * BIN (Reg0x2F[4:0])

Dout= 16 * BIN(Reg0xE5[7:0]) + BIN(Reg0xE6[5:2])

Dout_final = 2048 + (Dout - ADC_offset - 2048) * (1+Gain_Error/1000)

Table 20: V_Isense vs ISET

ISET[2:0]	V_Isense (V/A)	
	ISET[3] = 0	ISET[3] = 1
000	0.533	0.089
001	0.400	0.080
010	0.267	0.073
011	0.200	0.067
100	0.160	0.067
101	0.133	0.067
110	0.114	0.067
111	0.100	0.067

Input Power Monitoring

ACT85610 can monitoring the input power by measuring input voltage and current with the ADC. The resulting power calculation should be accurate to within 5% with an input current of 1.5A.

For input power measurement, the user must measure the input current and VIN separately, and then calculate input power by multiple them together in their microprocessor. Also note that the voltage and current are measured at different times, so the resulting power calculation is not a true instantaneous power.

To achieve the best accuracy when measuring input power, set the MES_POWER bit in register 0x32h [5] to 1.

When just measuring individual ADC inputs, but not input power, set MES_POWER = 0.

Anti-Aliasing Filter

To prevent aliasing interference when measuring the input power. An anti-aliasing filter is used for input voltage and input current measurements. The anti-aliasing filter is enabled by default, but can be disabled if desired.

GPIO Configuration

ACT85610 has 6 GPIOs that can be used as digital inputs, analog inputs, and open-drain outputs. These GPIOs allow a variety of functions to be implemented. These configurable options allow implementation of a variety of system functions and allow flexibility of functions tied to each pin. Some pin functions can be changed on-the-fly. Some examples of system functions that can be implemented are regulator enable (PWREN), system reset signal output (nRESET) , Power Good (PG) output, interrupt request or interrupt pin (nIRQ), digital output controlled by the “power okay” (POK) signal from individual regulators, digital input to control power sequencing of internal regulators, digital inputs/outputs to control external regulators (EXT_EN), input lines to monitor power good signals from external regulators (EXT_PG), to control Dynamic Voltage Scaling (DVS) in Buck regulators, enable signal for the storage cap Boost charger and blocking FET (ENB), open drain output for storage cap voltage power good (STR_PG) and VBUS (VB_PG), storage cap discharge enable, and the analog input for internal ADC (A2D), Buck output power good.

When configured as an input, each GPIO can be independently configured with 200kΩ pullup resistor to an internal 1.8V supply. Set I^2C register bit GPIOx_Pullup_Enable = 1 to enable the pullup resistor.

Regulators On/OFF Enable– PWREN

PWREN is a logic input that can be used to control the regulators power on/off and DVS. When PWREN pulled low, the configured rails can be turned off and some Buck rail will change the output voltage to different setting (DVS). It will be a convenience way to put the system in low power mode.

If PWREN pin pulls low, the configured rails will not turned on until the PWREN pin pulls high.

Alternately, an always-on mode is also possible with the ACT85610, where the PWREN input is not required to start the power-on sequence or to power up the system. After power up, PWREN can be used to put the IC in low power mode.

nIRQ

ACT85610 has the interrupt pin to inform the host any fault happens. In general anything with a status change the IRQ is inserted. The status changes can be masked by set the corresponding register bits. If the IRQ is set the fault must be read before it clears the IRQ. If the fault remains the IRQ will remain set.

The below status changes will set the IRQ:

- Input over-voltage, under-voltage
- Thermal warning, thermal shutdown
- eFuse VIN to VBUS over limits
- eFuse current warning and limit
- Storage capacitor over-voltage, under-voltage
- Supplemental mode active
- Buck operation faults
- Buck under-voltage shutdown
- VCC under-voltage
- ADC data is ready
- Any buck regulator exceeding peak current limit for 16 cycles after soft start or a UV/OV condition.
- Any regulator exceeding current limit for more than 20uS after soft start or a UV/OV condition.
- Watch Dog timer expiring.

If any of these status changes that is not desired to trigger the nIRQ, they can be masked in the register bit.

nRESET

The nRESET is an open drain 5V compatible output used to issue the main reset to the CPU/controller used in the system. The reset circuit monitors the input voltage and valid regulator outputs to trigger a reset if the input or a regulator output voltage is not valid. The STR_PG signal can also be an input trigger to nRESET. The nRESET delay time is controlled by the TRST_DLY [1:0] control bits. Programmable delay time from 20ms, 40ms, 60ms, and 100ms. The nRESET is essentially the same as a Power Good (PG) function but with a fixed delay after all the supply rails are up and in regulation.

The nRESET output signal is typically tied to all regulators whose outputs are necessary for the system controller and I/Os to function properly. Configurable register bits in each regulator determine if the regulator's POK signal is allowed to control the nRESET output signal or not. In general, the behavior of the nRESET output is such that the nRESET output is low if any one of the Power Okay (POK) signals from the controlling regulators is low. In other words, if any one of the controlling regulator outputs is not okay, the nRESET output will be low and will not assert high. The POK signal for any regulator can be low only when the regulator is enabled and the output is not regulating at normal levels. Any regulator that is disabled does not affect the nRESET signal even if its POK signal is configured to control the nRESET output. This is because, the POK signal from any regulator that is disabled is high and can only be low or "not okay" if the regulator is enabled but the output is not at the target regulation voltage. When a regulator is enabled, it has a softstart and it typically takes time as the output is ramped to the final regulation voltage. The POK signal is therefore typically low only from the time when a regulator is enabled (enable to the regulator goes high) to the time when the output ramps toward the final value and reaches 90% or higher of the final output voltage. The POK signal should go high if the output reaches a value greater than ~90% of the final value after it is enabled.

Hard Reset

GPIO5 can be configured as a Hard Reset input. When Hard Reset is asserted is asserted high, the ACT85610 is forced into the POR state and stays there until it is de-asserted. All registers are reset to their default values. When Hard Reset is de-asserted, IC starts the soft start process. The polarity can be set high or low by factory registers.

Force Supplement Mode

GPIO5 can be configured as an input to force the IC to enter supplement mode. This function is active high. The bits required to configure GPIO5 for this function are not user accessible, so this functionality must be configured at the factory.

OPERATION

Watch-Dog Supervision

The ACT85610 features a watchdog supervisory function. An internal watchdog timer of 8s is unmasked by setting either WDSREN [ ] or WDPCEN [ ] bit to one. WDSREN stands for Watch Dog Soft Reset Enable and WDPCEN stands for Watch Dog Power Cycle Enable. Once enabled, the watchdog timer is reset whenever there is I²C activity for the PMIC. In the case where the system software stops responding and that there is no I²C transactions for 8s, the watchdog timer expires. As a result, the PMIC either performs a soft-reset or power cycle, depending on whether WDSREN [ ] or WDPCEN [ ] bit is set. The watch dog timer can be enabled as necessary and is disabled by default.

Software-Initiated Power Cycle

ACT85610 supports software-initiated power cycle. Writing a 1 into the MR bit in register 0x04h turns off all buck regulators and clears all volatile register bits. The buck converters restart in 8ms. Note that the LDO and the Boost converter do not turn off.

Software Power Off

ACT85610 supports a software enable function. Writing a 1 into the POWER_OFF bit in register 0x04h moves the PMIC into the RESET state and turn off all regulators. This bit must be changed back to 0 to restart the outputs.

SDA & SCL

The input pins for the I²C are SDA and SCL. The SDA is an input and open drain output and requires a pull-up resistor. That pull-up resistor is typically tied to the MCU IO voltage. The IO voltage can range from 1.8V to 5.0V.

I2C Passcode

The ACT85610 implements a special register passcode that enables I²C write transactions. This prevents accidental register changes. Enable I²C write functionality by writing a value of 0xAAh to register 0x0Ah (Unlock Register Key). Changing this register to any other value locks the registers to prevent accidental changes to the I²C register values. The PMIC and the PLP portion of the IC use different I²C slave addresses. The passcode must be independently written for each I²C address.

Thermal Alert and Shutdown

The ACT85610 sets the THERMAL_ALERT register bit and asserts nIRQ when the die temperature is over 120°C. If the die temperature is over 145°C, the Boost and Buck converters are disabled and the THERMAL_PWRDWN register bit and nIRQ are asserted. If the die temperature is over 155°C, all circuits are disabled and the THERMAL_SHUTDWN register bit and nIRQ are asserted. The IC resumes normal operation when the die temperature drops by 15°C.

APPLICATION INFORMATION

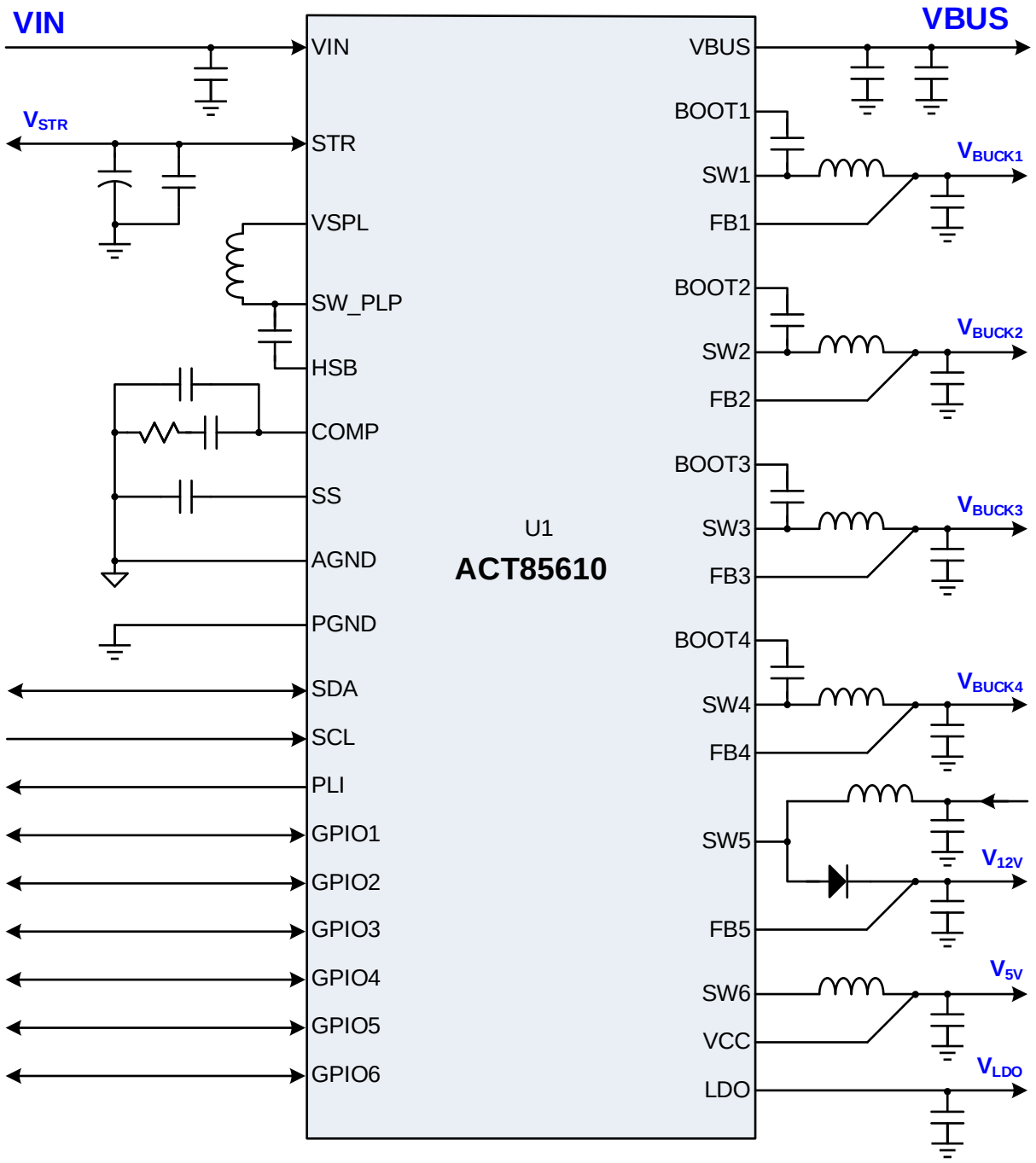


Figure10: Application Schematic (12V Input)

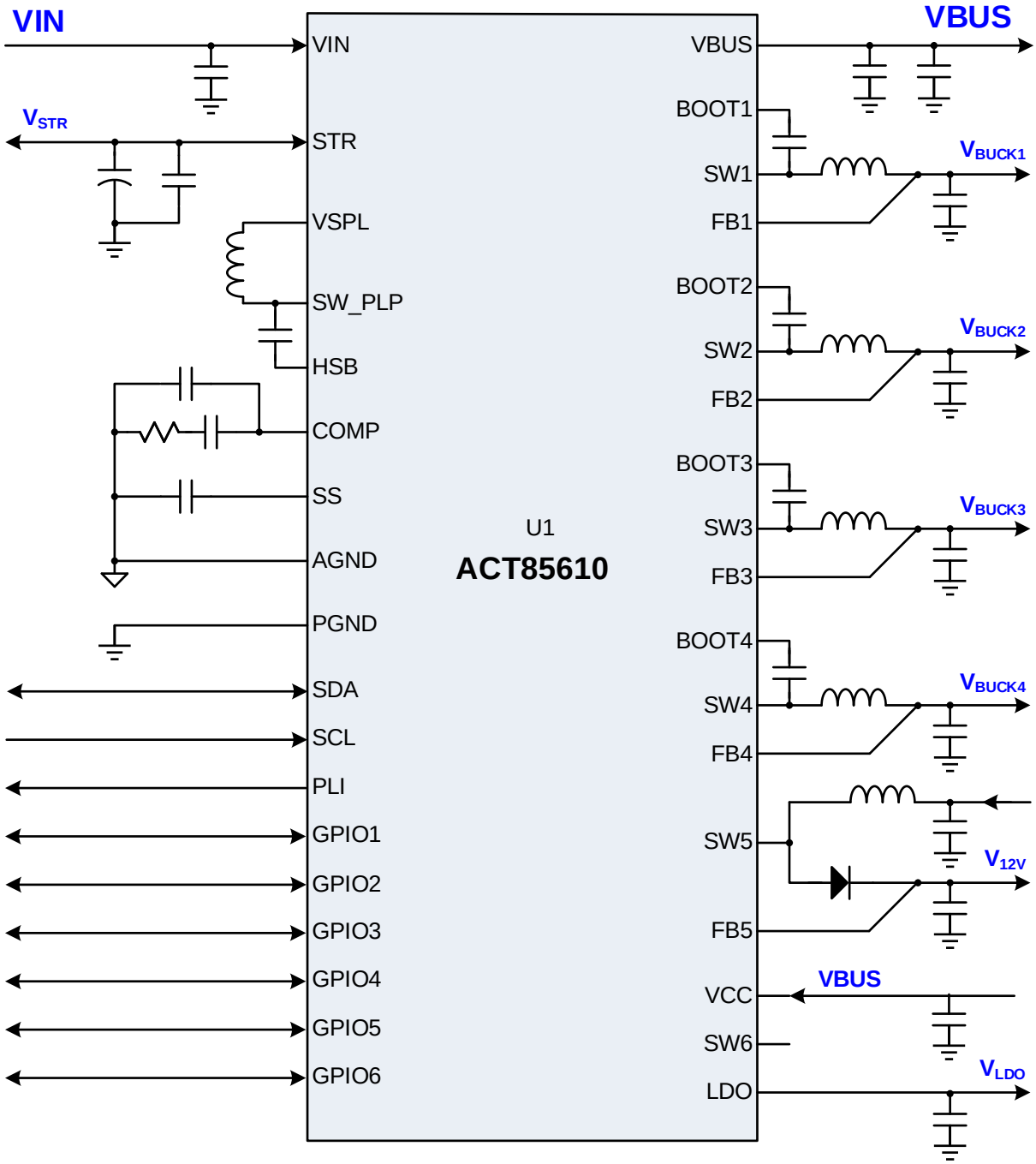


Figure 11: Application Schematic (3.3V and 5V Input)

LAYOUT RECOMMENDATIONS

Proper parts placement and PCB layout are critical to the operation of switching power supplies. Follow the following layout guidelines when designing the ACT85610 PCB. Refer to the Qorvo ACT85610 Evaluation Kit for layout examples

1. Place the buck input capacitors as close as possible to the IC. Connect the capacitors directly to the buck input pins and PGNDx power ground pins on the same PCB layer as the IC. Avoid using vias.
2. Place the ceramic capacitors on the STR pin as close as possible to the IC. Connect the capacitors directly to the STR pin and directly to pin 8 PGND pin.
3. Place the ceramic capacitors on the VSPL pin as close as possible to the IC. Connect the capacitors directly to the VSPL pin and directly to pin 8 PGND pin. The STR capacitor placement takes precedence over this capacitor placement.
4. Minimize the switch node trace length between each SWx pin and the inductor. Avoid routing sensitive analog signals near these high frequency, high dV/dt traces.
5. Place the LDO input capacitor close to its input pin. Connect its ground pin into the ground plane that connects the IC's PGND pins. The LDO input capacitor can be on the back sided of the PCB.
6. Place the ceramic bypass capacitors on VCC and VIN as close as possible to the IC. Connect the capacitors directly to the IC power and ground pins on the same PCB layer.
7. The buck input capacitor and output capacitor grounds should be connected as close together as possible, with short, direct, and wide traces.
8. Connect the compensation components and the SS capacitor to the AGND pin. The AGND trace should be routed separately from the power ground planes to effectively kelvin connect those components' ground connections to the IC's AGND pin. Connect the AGND pin to the main power plane near the IC.
9. Connect the PGND pins directly to the top layer ground plane. Connect the top layer ground plane to the internal ground planes and the PCB backside ground plane with thermal vias. Provide ground plane routing on multiple layers that allows the IC's heat to flow into the PCB and then spread radially from the IC. Avoid cutting the ground planes and adding vias that restrict the radial flow of heat of operating conditions and are relatively insensitive to layout considerations.
10. Kelvin connect the switching convert feedback pins to the output capacitor that is farthest from the inductor.
11. Note that the IC's exposed pad is internally connected to VBUS. The exposed pad can not be connected to the top layer ground plane. Add thermal vias to the back of the PCB to increase heat flow out of the IC.

This section provides the basic default configuration settings for each available ACT85610 CMI option. IC functionality in this section supersedes functionality in the main datasheet. Generating the desired functionality for a custom CMI sometimes requires reassigning internal resources, resulting in removal of base IC functionality. The following sections attempt to describe any removed functionality from the base IC functionality. The user is required to fully test all required functionality to ensure the CMI fully meets their requirements.

CMI 101: ACT85610QX101-T

CMI 101 is a general purpose CMI that allows customers to evaluate the ACT85610 functionality. It is designed for a 12V input.

The following tables describe the ACT85610QX101 IC settings.

Voltage and Currents

Rail	Active Mode Voltage VSET0 (V)	DVS Voltage VSET1 (V)	DVS Input Trigger	Sleep Mode Voltage (V)	DPSLP Mode Voltage (V)	Current Limit (A)	Fsw (kHz)
Buck1	0.8	0.75	I2C	VSET1	n/a	7	600
Buck2	1.2	1.2	n/a	OFF	n/a	7	800
Buck3	2.5	2.5	n/a	OFF	n/a	7	1000
Buck4	1.8	1.8	n/a	OFF	n/a	4	800
VCC Buck	5.0	n/a	n/a	OFF	n/a	n/a	1125
LDO	2.5	n/a	n/a	OFF	n/a	0.148	n/a
Boost	12	n/a	n/a	OFF	n/a	2.1	1125
EXT_EN	ON	n/a	n/a	OFF	n/a	n/a	n/a

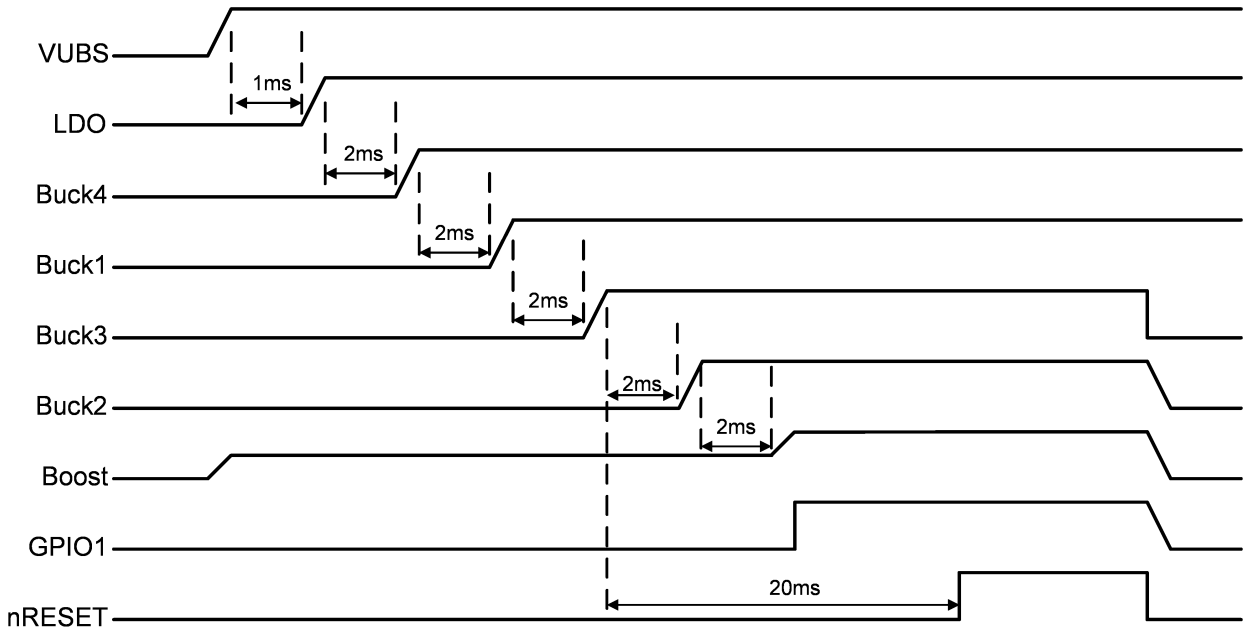
Startup and Sequencing

Rail	Sequence Order	Sequencing Input Trigger	StartUp Delay (ms)	Soft-Start (us)	Shutdown Delay (ms)
LDO	1	VBUS	1	215	1
Buck4	2	LDO	2	1000	2
Buck1	3	Buck4	1	1000	2
Buck3	4	Buck1	2	1000	2
Buck2	5	Buck3	2	1000	2
Boost	6	Buck2	2	10000	2
EXT_EN	7	Boost	0	n/a	2

Voltage Thresholds

Setting	Voltage Threshold
Input Voltage (V)	12
Storage Voltage (V)	28
Supplement Mode Output Voltage (V)	4.3
EN UV (V)	6.0
EN OV (V)	14.2

CMI 101 Startup



SLEEP Mode

SLEEP Mode is not used in CMI 101.

DPSLP Mode

DPSLP Mode is enabled. The DPSLP_MODE bit = 1 which programs a logical OR between a GPIO input and I2C to enter DPSLP Mode. No GPIO is configured as a DPSLP input, so only I2C can be used to enter DPSLP Mode.

DVS Mode

DVS mode can be implemented via I2C by writing a 1 into the EN_DVS_BY_I2C bit.

VIO Internal Pullup

The VIO internal pullup resistor functionality is disabled.

GPIO1 – EXT_EN

GPIO1 is configured as an open drain EXT_EN output. EXT_EN goes open drain with a 0ms delay from Boost going into regulation.

GPIO2 – PG_STR

GPIO2 is configured as an open drain PG_STR output. PG_STR goes open drain when the storage voltage is in regulation.

GPIO3 – Discharge

GPIO3 is configured as an input. When pulled high, it starts the discharge process. The EN_DISC_VBUS bit is set to 1, so pulling GPIO3 high discharges both VBUS and STR

GPIO4 – nIRQ

GPIO4 is configured as an open drain nIRQ output.

GPIO5 – Hard Reset

GPIO5 is configured as the Hard Reset input. Pulling GPIO5 high puts the IC into the POR state.

GPIO6 – nRESET

GPIO6 is configured as an open drain nRESET output. It has a 20ms delay from Boost.

I2C Address

The ACT85610 has two 7-bit I^2C addresses. The CMI 108 PMIC address is 0x25h and the PLP address is 0x26h. This results in 0x4Ah and 0x4Ch for a write address and 0x4Bh 0x4Dh for a read addresses.

CMI 108: ACT85610QX108-T

The ACT85610QX108 is a joint development between Qorvo and Innogrit and is specifically designed to power Innogrit's IG56356 Rainier SSD Processor. Innogrit uses the PMIC to power their IG5636 on their PCB0513/PCB0539 Gen4 PCIeU.2 and PCB1005 Gen 5 PCIe EDSFF reference designs supporting Tantalum or Electrolytic capacitors. The ACT85610QX108 provides built-in 12V VPP support which improves the power efficiency of the SSD. The reference designs are optimized for a 12V input voltage. More details about Innogrit's PCB0513/PCB0539 and PCB1005 can be found on the Innogrit website.

The following tables describe the ACT85610QX108 IC settings.

Voltage and Currents

Rail	Active Mode Voltage VSET0 (V)	DVS Voltage VSET1 (V)	DVS Input Trigger	Sleep Mode Voltage (V)	DPSLP Mode Voltage (V)	Current Limit (A)	Fsw (kHz)
Buck1	3.3	3.3	n/a	VSET0	VSET0	7	1000
Buck2	3.3	2.5	n/a	VSET0	OFF	7	1000
Buck3	1.2	1.2	n/a	VSET0	OFF	7	600
Buck4	0.8	0.8	n/a	VSET0	VSET0	4	600
VCC Buck	5	n/a	n/a	ON	ON	n/a	1125
LDO	3.3	n/a	n/a	ON	ON	0.39	n/a
Boost	12	n/a	n/a	ON	OFF	2.5	1125
EXT_EN	n/a	n/a	n/a	ON	OFF	n/a	n/a

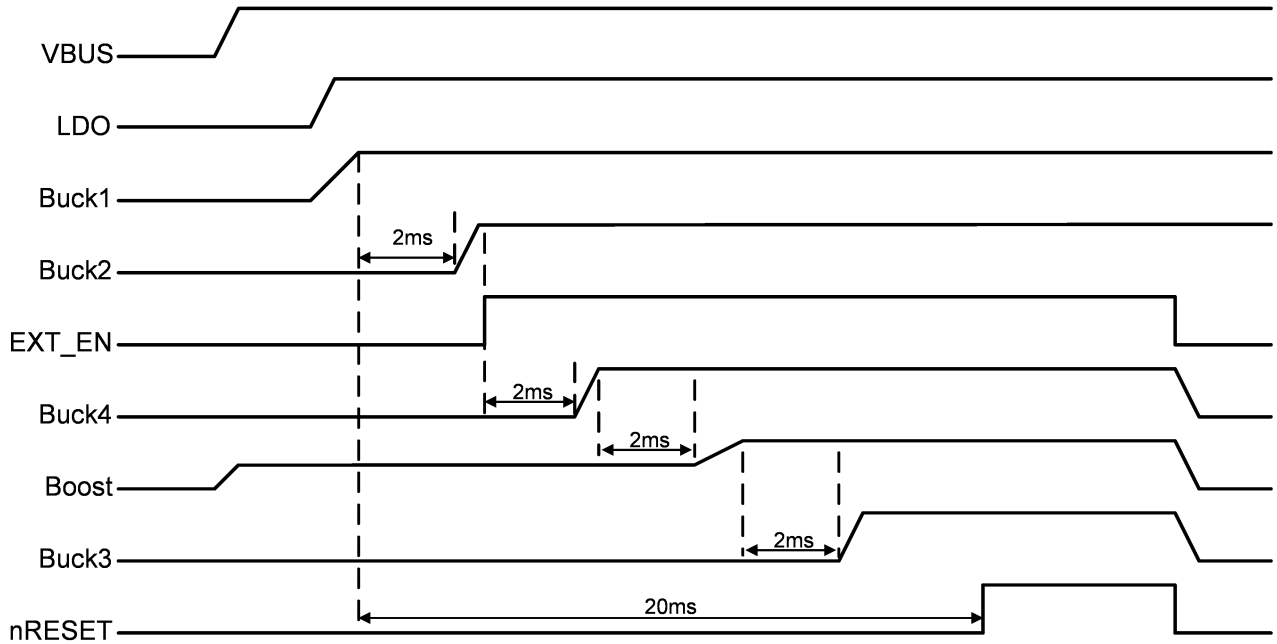
Startup and Sequencing

Rail	Sequence Order	Sequencing Input Trigger	StartUp Delay (ms)	Soft-Start (us)	Shutdown Delay (ms)
LDO	1	VBUS	0	215	0
Buck1	1	VBUS	0	1000	0
Buck2	2	Buck1	2	1000	2
EXT_EN	3	Buck2	0	n/a	0
Buck4	4	Buck2	2	1000	0
Boost	5	Buck4	2	10000	0
Buck3	6	Boost	2	1000	3

Voltage Thresholds

Setting	Voltage Threshold
Input Voltage (V)	12
Storage Voltage (V)	28
Supplement Mode Output Voltage (V)	7.5
EN UV (V)	9.6
EN OV (V)	14.4

CMI 108 Startup



SLEEP Mode

SLEEP Mode is not used in CMI 108.

DPSLP Mode

DPSLP Mode is enabled. The DPSLP_MODE bit = 1 which programs a logical OR between a GPIO input and I2C to enter DPSLP Mode. Note that GPIO4 is programmed as the active low PWREN digital input to control DPSLP Mode.

DVS Mode

GPIO3 is programmed as the DVS input. Note that only Buck2 has the DVS function.

When GPIO3 = H, Buck2 is set to its VSET1 voltage, 2.5V.

When GPIO3 = L, Buck2 is set to its VSET0 voltage, 3.3V.

VIO Internal Pullup

The VIO internal pullup resistor functionality is disabled.

GPIO1 – nIRQ

GPIO1 is configured as an open drain nIRQ output.

GPIO2 – VSTR POK

GPIO2 is configured as an open drain VSTR POK output. VSTR goes open drain when the storage voltage is in regulation.

GPIO3 – BUCK2 DVS

GPIO3 is configured as an input to select the Buck2 output voltage. When GPIO3 is L, VSET0 sets Buck2 to 3.3V. When GPIO3 is H, VSET1 sets Buck2 to 2.5V. Note that the user can manually change the VSETx voltages to different levels after startup.

GPIO4 – PWREN

GPIO4 is configured as an input. The first time GPIO4 is pulled high it enables the IC. After this, when GPIO4 is pulled low, the IC enters DPSLP mode. When GPIO4 is pulled H again, the IC goes back to Active Mode.

GPIO5 – EXT_EN

GPIO5 is configured as an open drain EXT_EN output. EXT_EN goes open drain with a 0ms delay from BUCK2 going into regulation.

GPIO6 – nRESET

GPIO6 is configured as an open drain nRESET output. It has a 20ms delay from BUCK1.

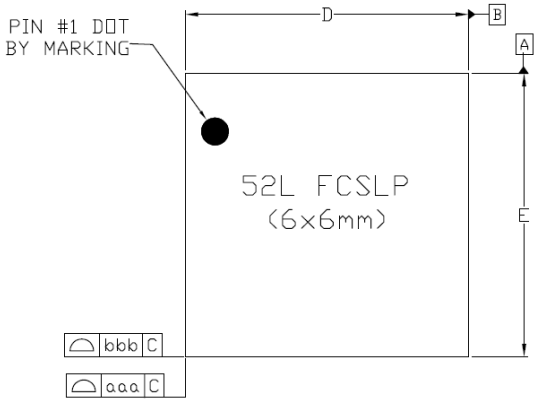
I2C Address

The ACT85610 has two 7-bit I^2C addresses. The CMI 108 PMIC address is 0x25h and the PLP address is 0x26h. This results in 0x4Ah and 0x4Ch for a write address and 0x4Bh 0x4Dh for a read address.

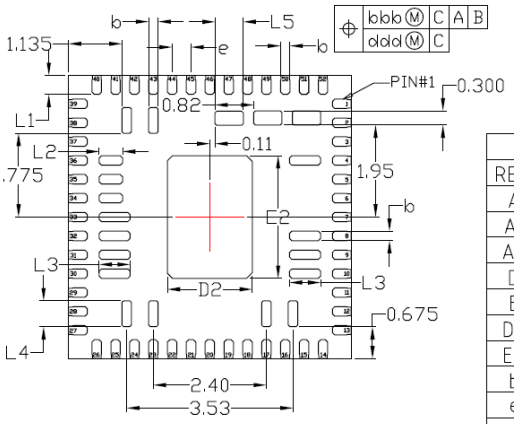
CMI 110: ACT85610QX110-T

The ACT85610QX110-T is a custom design for a custom processor. Contact Qorvo for more details about this IC.

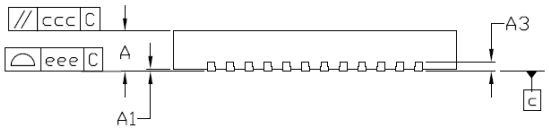
QFN-52 PACKAGE OUTLINE AND DIMENSIONS



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	---	---	0.050
A3	0.203 Ref.		
D	5.950	6.000	6.050
E	5.950	6.000	6.050
D2	1.750	1.800	1.850
E2	2.550	2.600	2.650
b	0.150	0.200	0.250
e	0.400 BSC		
L1	0.350	0.400	0.450
L2	0.450	0.500	0.550
L3	0.610	0.660	0.710
L4	0.500	0.550	0.600
L5	0.550	0.600	0.650
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Notes

1. All DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER JEDEC MO-220.

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- SVHC Free
- PFOS Free
- Antimony Free
- TBBP-A (C15H12Br402) Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

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