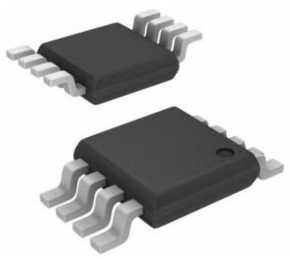
2-bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Application

PRODUCT DESCRIPTION



MSOP8

The MS4553M is a bidirectional voltage-level translator that can be used in a mixed-voltage digital signal system. It is powered by two separate architectures. The power supply range of terminal A is 1.65V to 5.5V, and that of terminal B is 2.3V to 5.5V. It can be used in logic signal conversion systems with power supply voltage of 1.8V, 2.5V, 3.3V and 5V. When OE terminal is low level, all IO terminals are in high impedance state, which significantly reduces the static power dissipation. When VCCA is powered up, OE terminal integrates pulldown current source. To ensure that the terminal maintains high impedance during power up or power down, OE terminal should be grounded by a pulldown resistor whose resistance value is determined by the ability to drive the current source.

The MS4553M has lead MSOP8 package. Operating temperature range is from -40°C to +100°C.

FEATURES

- No Need for Direction Control
- Data Rate: 20Mbps (Push-Pull Mode), 2Mbps (Open-Drain Mode)
- A Terminal Voltage Range: 1.65V to 5.5V,
  B Terminal Voltage Range: 2.3V to 5.5V ($V_{CCA} \leq V_{CCB}$)
- VCC Isolation: If VCCA or VCCB is low level to GND, terminals are in high impedance state
- No Power Up Sequencing Requirement
- Support Power Down Mode

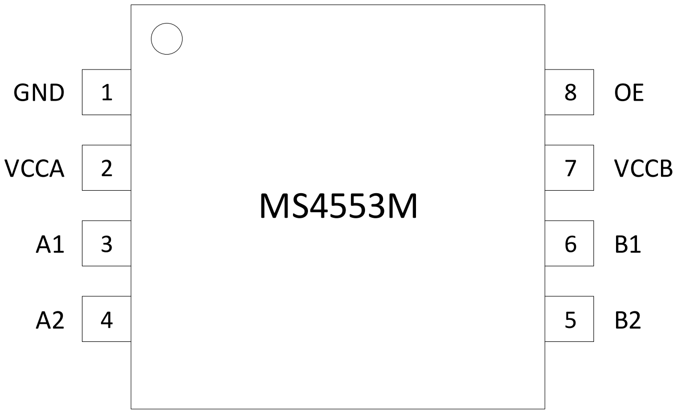
APPLICATIONS

- I^{2}C/SMBus (System Management Bus)
- UART (Universal Asynchronous Receiver/Transmitter)
- GPIO (General-Purpose Input/Output)

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS4553M	MSOP8	MS4553M

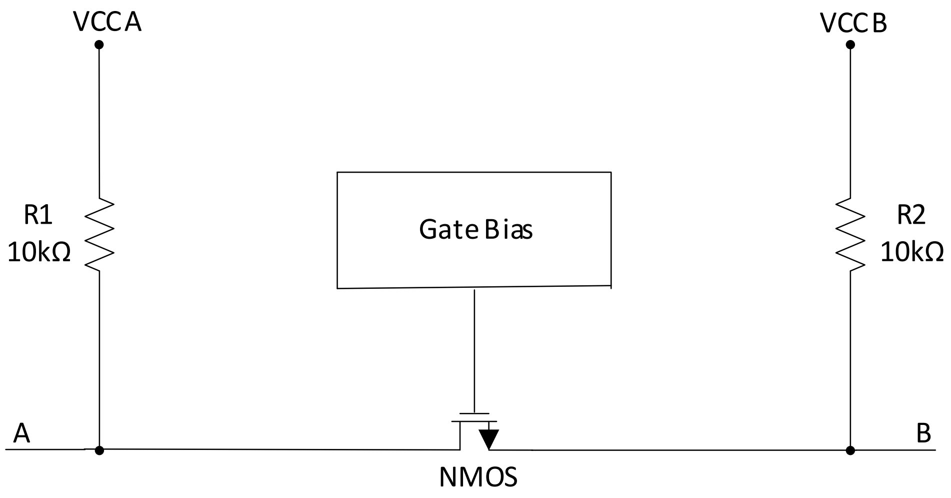
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	GND	-	Ground
2	VCCA	-	A Terminal Power Supply, 1.65V≤V_{CCA}≤5.5V, V_{CCA}≤V_{CCB}
3	A1	I/O	Input/Output A, Referenced VCCA
4	A2	I/O	Input/Output A, Referenced VCCA
5	B2	I/O	Input/Output B, Referenced VCCB
6	B1	I/O	Input/Output B, Referenced VCCB
7	VCCB	-	B Terminal Power Supply, 2.3V≤V_{CCB}≤5.5V
8	OE	I	Enable Output, pull OE low, all outputs are set to high impedance state

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Condition	Ratings	Unit
Power Supply (V_{CCA})		-0.3 ~ +6.0	V
Power Supply (V_{CCB})		-0.3 ~ +6.0	V
Input Voltage Range		-0.3 ~ +6.0	V
Voltage Applied to Output in High-Impedance or Power-down State		-0.3 ~ +6.0	V
Voltage Applied to Output in Normal State	A Terminal	-0.3 ~ V_{CCA}+0.3V	V
	B Terminal	-0.3 ~ V_{CCB}+0.3V	V
Input Clamp Current	V_I<0V	-50	mA
Output Clamp Current	V_O<0V	-50	mA
Output Continuous Current IO		±50	mA
Continuous Current through VCCA, VCCB and GND		±100	mA
Operating Temperature		-40 ~ +100	°C
Junction Temperature		150	°C
Storage Temperature		-65 ~ +150	°C
Soldering Temperature (10s)		260	°C

RECOMMENDED OPERATING CONDITIONS

V_{CCA}=1.65V-5.5V, V_{CCB}=2.3V-5.5V, typical values at T_A=25°C, unless otherwise noted.

<table>
<tr><th>Parameter</th><th>Symbol</th><th colspan="2">Condition</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td rowspan="2">Power Supply</td><td>V_{CCA}</td><td colspan="2"></td><td>1.65</td><td></td><td>5.5</td><td rowspan="2">V</td></tr>
<tr><td>V_{CCB}</td><td colspan="2"></td><td>2.3</td><td></td><td>5.5</td></tr>
<tr><td rowspan="4">High Level Input Voltage</td><td rowspan="4">V_{IH}</td><td rowspan="2">A Terminal</td><td>V_{CCA}=1.65V~1.95V
V_{CCB}=2.3V~5.5V</td><td>V_{CCI}-0.4</td><td></td><td>V_{CCI}</td><td rowspan="4">V</td></tr>
<tr><td>V_{CCA}=2.3V~5.5V,
V_{CCB}=2.3V~5.5V</td><td>V_{CCI}-0.4</td><td></td><td>V_{CCI}</td></tr>
<tr><td>B Terminal</td><td></td><td>V_{CCI}-0.4</td><td></td><td>V_{CCI}</td></tr>
<tr><td>OE Terminal</td><td></td><td>V_{CCA}×0.8</td><td></td><td>5.5</td></tr>
<tr><td rowspan="3">Low Level Input Voltage</td><td rowspan="3">V_{IL}</td><td>A Terminal</td><td></td><td>0</td><td></td><td>0.4</td><td rowspan="3">V</td></tr>
<tr><td>B Terminal</td><td></td><td>0</td><td></td><td>0.4</td></tr>
<tr><td>OE Terminal</td><td></td><td>0</td><td></td><td>V_{CCA}×0.2</td></tr>
<tr><td rowspan="3">Change for Input Signal Edge</td><td rowspan="3">(Δt/ΔV)</td><td colspan="2">A Terminal Push-Pull Driving</td><td></td><td></td><td>10</td><td rowspan="3">ns/V</td></tr>
<tr><td colspan="2">B Terminal Push-Pull Driving</td><td></td><td></td><td>10</td></tr>
<tr><td colspan="2">Control Input</td><td></td><td></td><td>10</td></tr>
</table>

Note:

1. V_{CCI} is relevant to input terminal.

2. V_{CCO} is relevant to output terminal.

3. V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} can't exceed 5.5V.

ELECTRICAL CHARACTERISTICS

V_{CCA}=1.65V-5.5V, V_{CCB}=2.3V-5.5V, typical values at T_A=25°C, unless otherwise noted.

Electrical Characteristics

Parameter	Symbol	Condition		Min	Typ	Max	Unit
A Terminal High Level Output Voltage	V_{OHA}	I_{OH}=-20μA, V_{IB}≥V_{CCB}-0.4V			V_{CCA}×0.8		V
A Terminal Low Level Output Voltage	V_{OLA}	I_{OL}=1mA, V_{IB}≤0.15V			0.2		V
B Terminal High Level Output Voltage	V_{OHB}	I_{OH}=-20μA, V_{IA}≥V_{CCA}-0.4V			V_{CCB}×0.8		V
B Terminal Low Level Output Voltage	V_{OLB}	I_{OL}=1mA, V_{IA}≤0.15V			0.2		V
OE Input Current	I_I	OE			0.1		μA
Power down Leakage Current	I_{OFF}	A Terminal	V_{CCA}=0V, V_{CCB}=0V~5.5V		0.1		μA
		B Terminal	V_{CCA}=0V~5.5V, V_{CCB}=0V		0.1		μA
Three-state Output Leakage Current	I_{OZ}	A or B Terminal	OE=0V		0.1		μA
Quiescent Current	I_{CCA}	V_I=V_O=OPEN, I_O=0	V_{CCA}=1.65V~V_{CCB}, V_{CCB}=2.3V~5.5V		0.1		μA
			V_{CCA}=5.5V, V_{CCB}=0V		0.1		μA
			V_{CCA}=0V, V_{CCB}=5.5V		0.1		μA
	I_{CCA} +I_{CCB}	V_I=V_O=OPEN, I_O=0	V_{CCA} = 1.65V~V_{CCB}, V_{CCB} = 2.3V~5.5V		5.5		μA
	I_{CCB}	V_I=V_O=OPEN, I_O=0	V_{CCA}=1.65V~V_{CCB}, V_{CCB}=2.3V~5.5V		5.5		μA
			V_{CCA}=5.5V, V_{CCB}=0V		0.1		μA
			V_{CCA}=0V, V_{CCB}=5.5V		0.1		μA
	I_{CCZA}	V_I=V_O=OPEN I_O=0, OE=GND	V_{CCA}=1.65V~V_{CCB}, V_{CCB}=2.3V~5.5V		0.1		μA
			V_{CCA}=5.5V, V_{CCB}=0V		0.1		μA
			V_{CCA}=0V, V_{CCB}=5.5V		0.1		μA

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Quiescent Current	I_{CCZB}	V_I=V_O=OPEN I_O=0, OE=GND	V_{CCA}=1.65V~V_{CCB}, V_{CCB}=2.3V~5.5V		0.1		μA
			V_{CCA}=5.5V, V_{CCB}=0V		0.1		
			V_{CCA}=0V, V_{CCB}=5.5V		0.1		
OE Input Capacitance	C_I	V_{CCA}=3.3V, V_{CCB}=3.3V			5		pF
A Terminal Input Capacitance	C_{IO}	V_{CCA}=3.3V, V_{CCB}=3.3V			6.5		pF
B Terminal Input Capacitance					6.5		

Timing Requirement

Parameter		V_{CCB}=2.5V	V_{CCB}=3.3V	V_{CCB}=5V	Unit
		Typ	Typ	Typ	
T_A = +25°C, V_{CCA} = 1.8V, unless otherwise noted					
Data Rate	Push-Pull Mode	18	18	16	Mbps
	Open-Drain Mode	2	2	2	
T_A = +25°C, V_{CCA} =2.5V, unless otherwise noted					
Data Rate	Push-Pull Mode	25	18	17	Mbps
	Open-Drain Mode	2	2	2	
T_A = +25°C, V_{CCA} = 3.3V, unless otherwise noted					
Data Rate	Push-Pull Mode		20	17	Mbps
	Open-Drain Mode		2	2	
T_A = +25°C, V_{CCA} = 5V, unless otherwise noted					
Data Rate	Push-Pull Mode			17	Mbps
	Open-Drain Mode			2	

Switching Characteristics

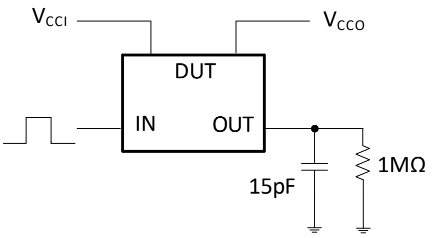
T_A = +25°C, V_{CCA} = 1.8V, unless otherwise noted.

Parameter	Symbol	Condition	V_{CCB} = 2.5V Typ	V_{CCB} = 3.3V Typ	V_{CCB} = 5V Typ	Unit
V_{CCA} = 1.8V						
A to B Delay	t_{PHL}	Push-Pull Mode	2.4	3.0	5.4	ns
		Open-Drain Mode	26.0	26.3	26.7	
	t_{PLH}	Push-Pull Mode	4.0	3.6	3.5	
		Open-Drain Mode	175	145	110	
B to A Delay	t_{PHL}	Push-Pull Mode	2.0	2.6	3.6	ns
		Open-Drain Mode	26.0	26.1	26.2	
	t_{PLH}	Push-Pull Mode	1.7	1.5	1.4	
		Open-Drain Mode	133	69	51	
OE Enable Time (t_{PZH} and t_{PZL})	t_{EN}		5.2	4.4	3.8	ns
OE Disable Time (t_{PHZ} and t_{PLZ})	t_{DIS}		614	616	626	ns
A Terminal Rise Time	t_{rA}	Push-Pull Mode	16	15	14	ns
		Open-Drain Mode	89	31	10	
B Terminal Rise Time	t_{rB}	Push-Pull Mode	12	11	9	ns
		Open-Drain Mode	128	98	58	
A Terminal Fall Time	t_{fA}	Push-Pull Mode	10	9	8	ns
		Open-Drain Mode	1.9	1.7	1.6	
B Terminal Fall Time	t_{fB}	Push-Pull Mode	9	14	18	ns
		Open-Drain Mode	2.2	2.3	2.9	
Channel to Channel Skew	$t_{sk(0)}$		0.5	0.5	0.5	ns
Data Rate		Push-Pull Mode	18	18	17	Mbps
		Open-Drain Mode	2	2	2	
V_{CCA} = 2.5V						
A to B Delay	t_{PHL}	Push-Pull Mode	2.7	3.3	4.8	ns
		Open-Drain Mode	26.2	26.4	26.7	
	t_{PLH}	Push-Pull Mode	2.6	2.4	2.3	
		Open-Drain Mode	169	144	110	
B to A Delay	t_{PHL}	Push-Pull Mode	2.4	2.3	2.4	ns
		Open-Drain Mode	26.3	26.4	26.5	
	t_{PLH}	Push-Pull Mode	2.0	1.9	1.8	
		Open-Drain Mode	165	118	55	

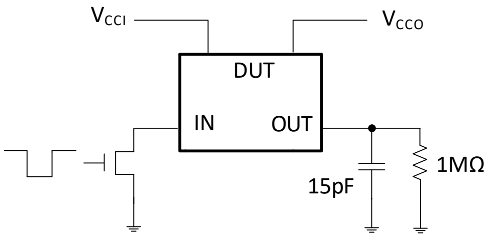
Parameter	Symbol	Condition	V_{CCB} = 2.5V Typ	V_{CCB} = 3.3V Typ	V_{CCB} = 5V Typ	Unit
V_{CCA} = 2.5V						
OE Enable Time (t_{PZH} and t_{PZL})	t_{EN}		14	13	12	ns
OE Disable Time (t_{PHZ} and t_{PLZ})	t_{DIS}		630	635	640	
A Terminal Rise Time	t_{rA}	Push-Pull Mode	13	13	12	ns
		Open-Drain Mode	120	70	10	
B Terminal Rise Time	t_{rB}	Push-Pull Mode	4.5	3.4	2.6	ns
		Open-Drain Mode	122	96	62	
A Terminal Fall Time	t_{fA}	Push-Pull Mode	8	7	6	ns
		Open-Drain Mode	2.0	1.9	1.7	
B Terminal Fall Time	t_{fB}	Push-Pull Mode	8	12	15	ns
		Open-Drain Mode	1.9	2.1	2.7	
Channel to Channel Skew	$t_{sk(0)}$		0.5	0.5	0.5	ns
V_{CCA} = 3.3V						
A to B Delay	t_{PHL}	Push-Pull Mode		3.5	4.9	ns
		Open-Drain Mode		26.3	26.7	
	t_{PLH}	Push-Pull Mode		2.2	2.0	
		Open-Drain Mode		133	104	
B to A Delay	t_{PHL}	Push-Pull Mode		3.0	3.2	ns
		Open-Drain Mode		26.6	26.8	
	t_{PLH}	Push-Pull Mode		1.8	1.7	
		Open-Drain Mode		132	83	
OE Enable Time (t_{PZH} and t_{PZL})	t_{EN}			12	11	ns
OE Disable Time (t_{PHZ} and t_{PLZ})	t_{DIS}			630	635	
A Terminal Rise Time	t_{rA}	Push-Pull Mode		12	11	ns
		Open-Drain Mode		87	36	
B Terminal Rise Time	t_{rB}	Push-Pull Mode		10	9	ns
		Open-Drain Mode		87	56	

Parameter	Symbol	Condition	V_{CCB} = 2.5V Typ	V_{CCB} = 3.3V Typ	V_{CCB} = 5V Typ	Unit
V_{CCA} = 3.3V						
A Terminal Fall Time	t_{fA}	Push-Pull Mode		12	11	ns
		Open-Drain Mode		2.3	2.0	
B Terminal Fall Time	t_{fB}	Push-Pull Mode		13	16	ns
		Open-Drain Mode		2.0	2.5	
Channel to Channel Skew	$t_{sk(0)}$			0.5	0.5	ns
V_{CCA} = 5.0V						
A to B Delay	t_{PHL}	Push-Pull Mode			5.4	ns
		Open-Drain Mode			26.7	
	t_{PLH}	Push-Pull Mode			1.9	
		Open-Drain Mode			120	
B to A Delay	t_{PHL}	Push-Pull Mode			5.6	ns
		Open-Drain Mode			27.3	
	t_{PLH}	Push-Pull Mode			1.7	
		Open-Drain Mode			126	
OE Enable Time (t_{PZH} and t_{PZL})	t_{EN}				10	ns
OE Disable Time (t_{PHZ} and t_{PLZ})	t_{DIS}				636	
A Terminal Rise Time	t_{rA}	Push-Pull Mode			8	ns
		Open-Drain Mode			79	
B Terminal Rise Time	t_{rB}	Push-Pull Mode			7	ns
		Open-Drain Mode			73	
A Terminal Fall Time	t_{fA}	Push-Pull Mode			8.7	ns
		Open-Drain Mode			2.7	
B Terminal Fall Time	t_{fB}	Push-Pull Mode			8.6	ns
		Open-Drain Mode			2.4	
Channel to Channel Skew	$t_{sk(0)}$				0.5	ns

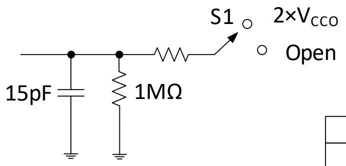
TEST CIRCUIT



Push-Pull Mode

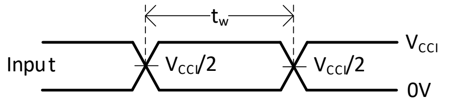


Open-Drain Mode

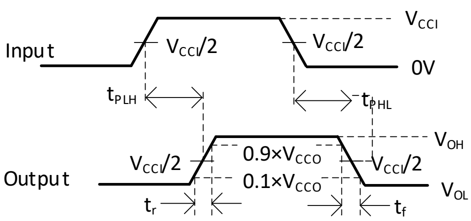


OE input enable and disable
timing measurement

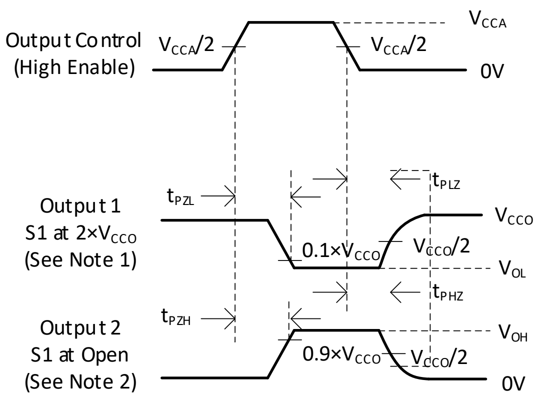
TEST	S1
t_{PZL}/t_{PLZ}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	Open



Pulse Time



Propagation Delay Time



Enable and Disable Time

Note:

1. C_L includes probe and jig capacitance.

2. Waveform 1 is used for outputs with internal conditions to make the output low unless the output control terminal to be disabled. Waveform 2 is used for outputs with internal conditions to make the output high unless the output control terminal to be disabled.

3. All input pulses are supplied by a generator with the following characteristics: PRR≤10MHz, Z_O=50Ω, dv/dt ≥1V/ns.

4. Output measurements once, each measurement needs to be converted once.

5. t_{PLZ}, t_{PHZ} and t_{DIS} are the same.

6. t_{PZL}, t_{PZH} and t_{EN} are the same.

7. t_{PLH}, t_{PHL} and t_{PD} are the same.

8. V_{CCI} is relevant to input terminal.

9. V_{CCO} is relevant to output terminal.

10. All parameters and waveforms are not applicable to all devices.

APPLICATION DESCRIPTION

The MS4553M could be applied to interface two different voltage nodes, in order to connect logic level in electronic system. The MS4553M is used in point-to-point topology to connect the device or system which mutually operate in different interface voltages. The main purpose is to connect open-drain driver and I/O terminals, such as I^2C and 1-Wire. And the data is bidirectional transmission without control signal. It's also used to data connection between push-pull driver and I/O terminals.

Input Driver Requirement

The fall time (t_{fA}, t_{fB}) depends on the output impedance of external driver, which could drive the data I/O of the MS4553M. In addition, t_{PHL} and data rate also are up to the output impedance of external driver. t_{fA}, t_{fB}, t_{PHL} and conversion rate are defined as the value where the output impedance of external driver is less than 50Ω.

Power up

During operation, ensure $V_{CCA} \leq V_{CCB}$. And each power sequencing couldn't destroy device. Therefore, elevating any power would be no problem.

Output Load Caution

It's recommended to apply PCB layout with short traces, in order to avoid overlarge capacitance load and ensure correct one trigger. PCB signal traces should be enough short to make sure that the reflex go-back delay is less than one trigger duration. Signal integrity can be improved by ensuring that there is low impedance at driver in any reflex. The period of one trigger approaches to 30ns. In addition, the maximum capacitance driving total lumped loads is also directly up to one trigger duration. For very large capacitive load, one trigger could be overtime before the signal is driven completely. Through balancing dynamic characteristic I_{CC}, load driving capacity and the maximum bit rate, set one trigger duration is the best condition. The PCB trace length and connector would increase the capacitance value seeing from the output of the MS4553M. Therefore, recommend to use lumped load capacitor to avoid system-stage influences, such as one trigger, bus competition, output signal shock and so on.

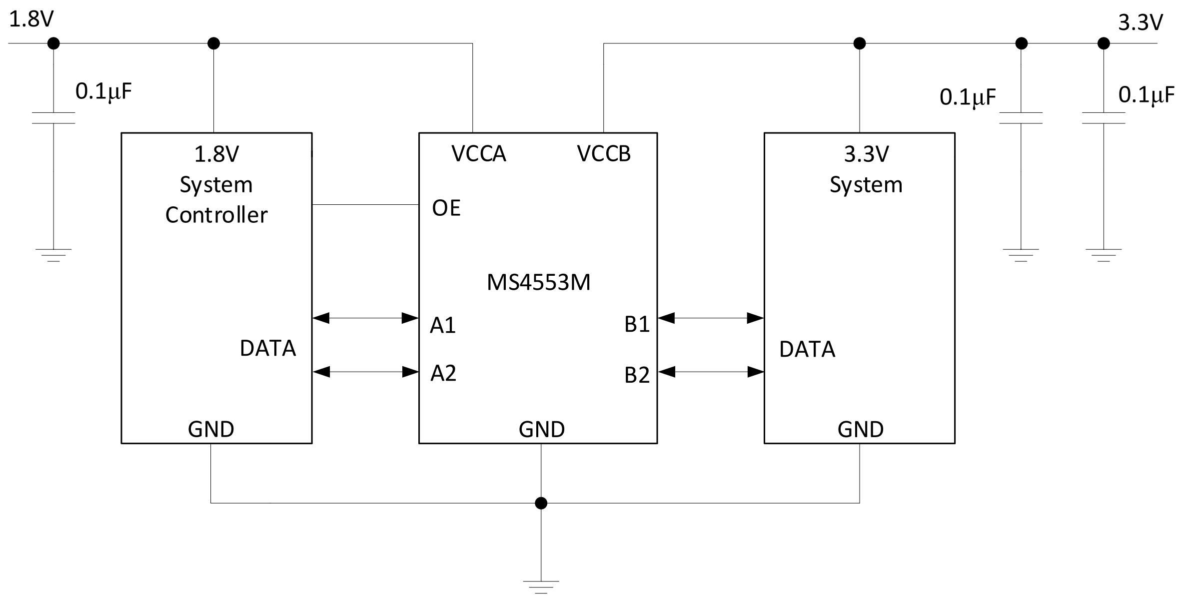
Enable and Disable

The MS4553M has one OE input terminal, which is used to disable device when OE is low level state, thus all I/Os are in high impedance state. Only VCCA is supplied, OE would have one internal pulldown current source. Disable time(t_{DIS}) represents that the delay time between OE becoming low and output in high impedance state. Enable time(t_{EN}) represents the time when user must allow that one trigger circuit just starts to operate after OE goes high.

I/O Pullup and Pulldown Resistors

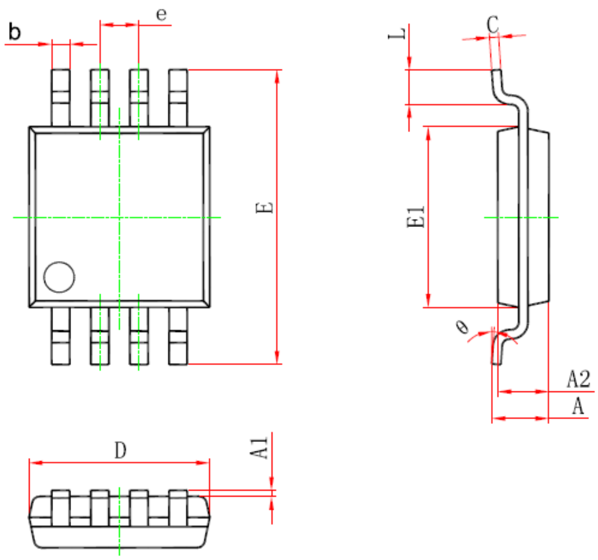
Each A terminal has an internal 10kΩ pullup resistor for VCCA. Each B terminal has an internal 10kΩ pullup resistor for VCCB. If a smaller pullup resistor is required, must connect an external resistor between I/O and VCCA/VCCB. While applying a smaller pullup resistor would affect V_{OL}. When OE goes low, internal pullup resistor would be disabled.

TYPICAL APPLICATION



PACKAGE OUTLINE DIMENSIONS

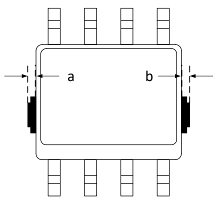
MSOP8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	-	1.100	-	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650BSC		0.026BSC	
E	4.750	5.050	0.187	0.199
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031
θ	0º	6º	0º	6º

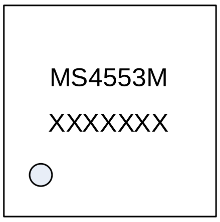
Note: In addition to the package size, a and b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.

The diagram is as follows: taking SOP8 package as an example.



MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: MS4553M

Product Code: XXXXXXX

1. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

2. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS4553M	MSOP8	3000	1	3000	8	24000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don’t release additional notice.
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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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