Product Folder

Sample & Buy

Technical Documents

Tools & Software

Support & Community

Reference Design

![Texas Instruments]

TS3A24159

SCDS238D –MARCH 2007–REVISED JULY 2015

TS3A24159 0.3-Ω 2-Channel SPDT Bidirectional Analog Switch Dual-Channel 2:1 Multiplexer and Demultiplexer

1 Features

- Specified Break-Before-Make Switching
- Low ON-State Resistance (0.3 Ω Max)
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 3.6-V Single-Supply Operation
- Control Inputs Are 1.8-V Logic Compatible
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
    - 2000-V Human-Body Model (A114-B, Class II)
    - 1000-V Charged-Device Model (C101)

2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
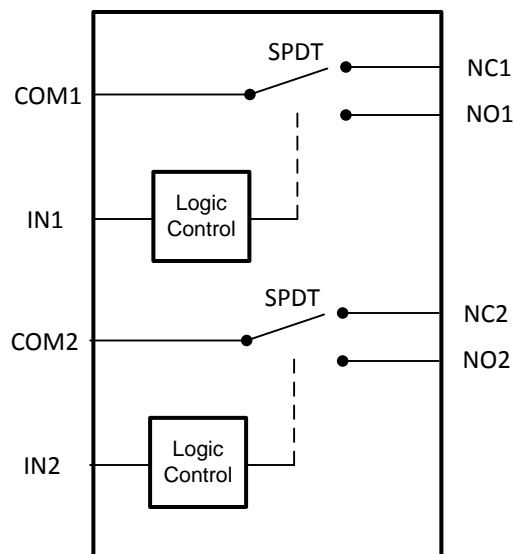- Wireless Terminals and Peripherals

3 Description

The TS3A24159 is a 2-channel single-pole double-throw (SPDT) bidirectional analog switch that is designed to operate from 1.65 V to 3.6 V. It offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance, low ON-state resistence, and consumes very low power. These are some of the features that make this device suitable for a variety of markets and many different applications.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3A24159	VSSOP (10)	3.00 mm × 3.00 mm
	VSON (10)	3.00 mm × 3.00 mm
	DSBGA (10)	1.86 mm × 1.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

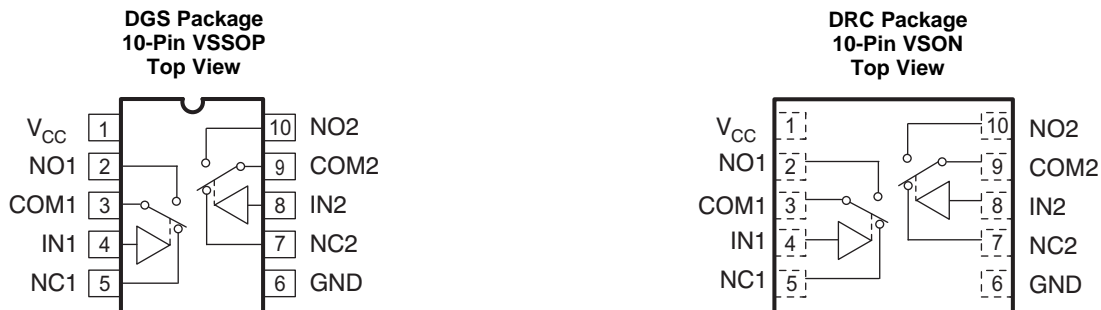**Functional Block Diagram**

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2008) to Revision D   **Page**

Product Folder Links: *TS3A24159*

5 Pin Configuration and Functions

**DGS Package
10-Pin VSSOP
Top View**

**DRC Package
10-Pin VSON
Top View**

Pin Functions - VSSOP and VSON

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{CC}	—	Power Supply
2	NO1	I/O	Normally Open Signal Path
3	COM1	I/O	Common Signal Path
4	IN1	I	Digital Control to Connect COM to NO or NC
5	NC1	I/O	Normally Closed Signal Path
6	GND	—	Ground
7	NC2	I/O	Normally Closed Signal Path
8	IN2	I	Digital Control to Connect COM to NO or NC
9	COM2	I/O	Common Signal Path
10	NO2	I/O	Normally Open Signal Path

**YZP Package
10-Pin DSBGA
Top-Through View**
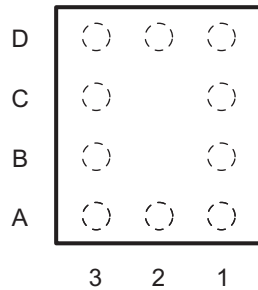
YZP Package Terminal Assignments

D	NO2	V_{CC}	NO1
C	COM2		COM1
B	IN2		IN1
A	NC2	GND	NC1
	3	**2**	**1**

Pin Functions - DSBGA

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	NC1	I/O	Normally Closed Signal Path
A2	GND	—	Ground
A3	NC2	I/O	Normally Closed Signal Path
B1	IN1	I	Digital Control to Connect COM to NO or NC
B3	IN2	I	Digital Control to Connect COM to NO or NC
C1	COM1	I/O	Common Signal Path
C3	COM2	I/O	Common Signal Path
D1	NO1	I/O	Normally Open Signal Path
D2	V_{CC}	—	Power Supply
D3	NO2	I/O	Normally Open Signal Path

Product Folder Links: *TS3A24159*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1] [2]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[3]		−0.5	3.6	V
V_{NC} V_{NO} V_{COM}	Signal voltage[3] [4] [5]		−0.5	V_{CC} + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	−50	50	mA
I_{NC} I_{NO} I_{COM}	ON-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_{CC}	−300	300	mA
	ON-state peak switch current[6]		−500	500	
V_{IN}	Digital input voltage		−0.5	3.6	V
I_{IK}	Digital input clamp current[3] [4]	V_I < 0	−50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		−100		mA
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions.* Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration <10% duty cycle

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	1.65	3.6	V
V_{NC} V_{NO} V_{COM}	Signal Voltage	0	V_{CC}	V
V_{IN}	Digital Input Voltage	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC[1]		TS3A24159			UNIT
		DGS (VSSOP)	DRC (VSON)	YZP (DSBGA)	
		10 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	154	49.4	90.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.9	71.2	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.6	23.8	8.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	2.2	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82.2	23.8	8.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	6.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 3-V Supply

V_{CC} = 2.7 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted) [1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_{CC}	V
Peak ON resistance	r_{peak}	$0 \leq (V_{NO}$ or $V_{NC}) \leq V_{CC}$, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V		0.2	0.3	Ω
				Full				0.35	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V		0.26	0.3	Ω
				Full				0.34	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V		0.01	0.05	Ω
				Full				0.05	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO}$ or $V_{NC}) \leq V_{CC}$, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V		0.13		Ω
		V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C			0.01	0.04	Ω
				Full				0.05	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = 3 V, or V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 11	25°C	3.6 V	–10		10	nA
				Full		–50		50	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 12	25°C	3.6 V	–10		10	nA
				Full		–100		100	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 3 V,	Switch ON, See Figure 12	25°C	3.6 V	–10		10	nA
				Full		–100		100	
DIGITAL CONTROL INPUTS (IN1, IN2)[2]									
Input logic high	V_{IH}			Full		1.4			V
Input logic low	V_{IL}			Full				0.5	V
Input leakage current	I_{IH}, I_{IL}	V_I = 3.6 V or 0		25°C	3.6 V	–40	5	40	nA
				Full		–50		50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 3-V Supply (continued)

V_{CC} = 2.7 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted) [1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 19	25°C	3 V		9		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 13	25°C	3 V		90		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON,	See Figure 13	25°C	3 V		224		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 13	25°C	3 V		250		pF
Digital input capacitance	C_I	V_{IN} = V_{CC} or GND,	See Figure 13	25°C	3 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	3 V		23		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See Figure 17	25°C	3 V		–72		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See Figure 18	25°C	3 V		–96		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 20	25°C	3 V		0.003%		
SUPPLY									
Positive supply current	I_{CC}	V_{IN} = V_{CC} or GND		25°C	3.6 V		15	100	nA
				Full			1		µA

6.6 Electrical Characteristics for 2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted) [1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V			0.35	Ω
				Full				0.45	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V				Ω
				Full				0.4	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.8 V, 0.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V		0.01	0.05	Ω
				Full			0.05	0.05	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V		0.05		Ω
		V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C			0.03	0.08	
				Full				0.1	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 2.2 V, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 11	25°C	2.7 V	–10		10	nA
				Full		–50		50	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = Open, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = Open,	Switch ON, See Figure 12	25°C	2.7 V	–10		10	nA
				Full		–100		100	

(1)   The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 2.5-V Supply (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted) [1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH (continued)									
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.5 V, or V_{NC} or V_{NO} = Open, V_{COM} = 2.2 V,	Switch ON, See Figure 12	25°C	2.7 V	–10		10	nA
				Full		–100		100	
DIGITAL CONTROL INPUTS (IN1, IN2) [2]									
Input logic high	V_{IH}			Full		1.25			V
Input logic low	V_{IL}			Full				0.5	V
Input leakage current	I_{IH}, I_{IL}	V_I = 2.7 V or 0		25°C	2.7 V	–40	5	40	nA
				Full		–50		50	
DYNAMIC									
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 19	25°C	2.5 V		8		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 13	25°C	2.5 V		90		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON,	See Figure 13	25°C	2.5 V		250		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 13	25°C	2.5 V		250		pF
Digital input capacitance	C_I	V_I = V_{CC} or GND,	See Figure 13	25°C	2.5 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	2.5 V		23		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See Figure 17	25°C	2.5 V		–72		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See Figure 18	25°C	2.5 V		–96		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 20	25°C	2.5 V		0.003%		
SUPPLY									
Positive supply current	I_{CC}	V_I = V_{CC} or GND		25°C	2.7 V		10	100	nA
				Full			700		

(2)   All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.7 Electrical Characteristics for 1.8-V Supply

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted) [1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO} or V_{NC}) ≤V_{CC}, I_{COM} = –2 mA,	Switch ON, See Figure 10	25°C	1.65 V		0.4	0.7	Ω
				Full				0.8	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 10	25°C	1.65 V		0.3	0.45	Ω
				Full				0.5	

(1)   The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Product Folder Links: *TS3A24159*

Electrical Characteristics for 1.8-V Supply (continued)

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted) [1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH (continued)									
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 10	25°C	1.65 V		0.02	0.04	Ω
				Full				0.05	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO}$ or $V_{NC}) \leq V_{CC}$, I_{COM} = –2 mA,	Switch ON, See Figure 10	25°C	1.65 V		0.13		Ω
		V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C			0.08	0.15	
				Full				0.2	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, See Figure 11	25°C	1.95	–10		10	nA
				Full		–50		50	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = Open, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 12	25°C	1.95 V	–10		10	nA
				Full		–100		100	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.3 V, or V_{NC} or V_{NO} = Open, V_{COM} = 1.65 V,	Switch ON, See Figure 12	25°C	1.95 V	–10		10	nA
				Full		–100		100	
DIGITAL CONTROL INPUTS (IN1, IN2)[2]									
Input logic high	V_{IH}			Full		1			V
Input logic low	V_{IL}			Full				0.4	V
Input leakage current	I_{IH}, I_{IL}	V_I = 1.95 V or 0		25°C	1.95 V	–40	5	40	nA
				Full		–50		50	
DYNAMIC									
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 19	25°C	1.8 V		5		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 13	25°C	1.8 V		90		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON,	See Figure 13	25°C	1.8 V		250		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 13	25°C	1.8 V		250		pF
Digital input capacitance	C_{IN}	V_I = V_{CC} or GND,	See Figure 13	25°C	1.8 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	1.8 V		23		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See Figure 17	25°C	1.8 V		–73		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See Figure 18	25°C	1.8 V		–97		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 20	25°C	1.8 V		0.005%		
SUPPLY									
Positive supply current	I_{CC}	V_I = V_{CC} or GND		25°C	1.95 V		100	50	nA
				Full				700	

(2)   All unused digital inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Product Folder Links: *TS3A24159*

6.8 Switching Characteristics for a 3-V Supply

V_{CC} = 2.7 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic									
Turnon time	t_{ON}	$V_{COM} = V_{CC}$, $R_L = 50\ \Omega$	C_L = 35 pF, See Figure 14	25°C	2.5 V		20	35	ns
				Full	2.3 V to 2.7 V			40	
Turnoff time	t_{OFF}	$V_{COM} = V_{CC}$, $R_L = 50\ \Omega$	C_L = 35 pF, See Figure 14	25°C	2.5 V		12	25	ns
				Full	2.3 V to 2.7 V			30	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_{CC}$, $R_L = 50\ \Omega$	C_L = 35 pF, See Figure 15	25°C	2.5 V	1	10	25	ns
				Full	2.3 V to 2.7 V	0.5		30	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

6.9 Switching Characteristics for a 2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic									
Turnon time	t_{ON}	$V_{COM} = V_{CC}$, $R_L = 50\ \Omega$	C_L = 35 pF, See Figure 14	25°C	1.8 V		23	45	ns
				Full	1.65 V to 1.96 V			50	
Turnoff time	t_{OFF}	$V_{COM} = V_{CC}$, $R_L = 50\ \Omega$	C_L = 35 pF, See Figure 14	25°C	1.8 V		17	27	ns
				Full	1.65 V to 1.96 V			30	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_{CC}$, $R_L = 50\ \Omega$	C_L = 35 pF, See Figure 15	25°C	1.8 V	2	14	30	ns
				Full	1.65 V to 1.96 V	1		35	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

6.10 Switching Characteristics for a 1.8-V Supply

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic									
Turnon time	t_{ON}	$V_{COM} = V_{CC}$, $R_L = 50\ \Omega$	C_L = 35 pF, See Figure 14	25°C	1.8 V		53	75	ns
				Full	1.65 V to 1.96 V			80	
Turnoff time	t_{OFF}	$V_{COM} = V_{CC}$, $R_L = 50\ \Omega$	C_L = 35 pF, See Figure 14	25°C	1.8 V		24	35	ns
				Full	1.65 V to 1.96 V			40	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_{CC}$, $R_L = 50\ \Omega$	C_L = 35 pF, See Figure 15	25°C	1.8 V	2	30	40	ns
				Full	1.65 V to 1.96 V	1		50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Product Folder Links: *TS3A24159*

6.11   Typical Characteristics
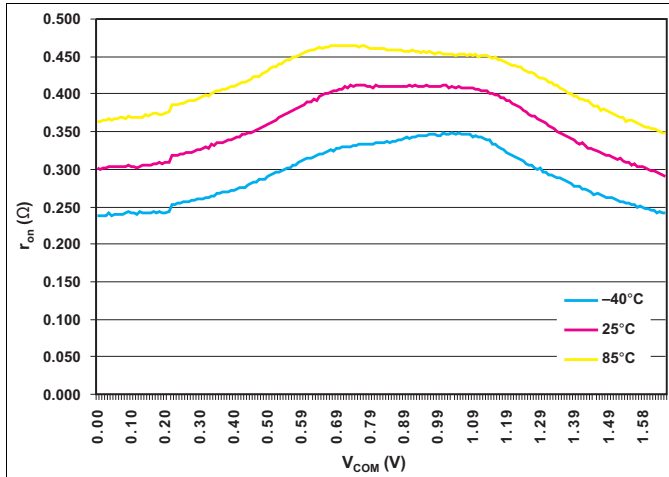
Figure 1. r$_{on}$ vs V$_{COM}$
(V$_{CC}$ = 1.65 V)
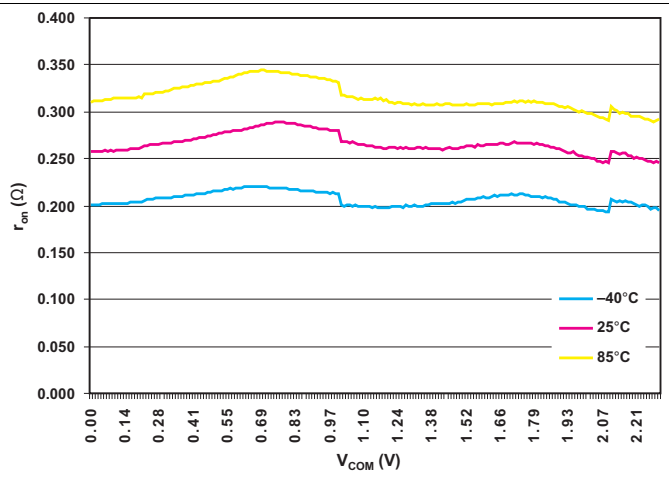
Figure 2. r$_{on}$ vs V$_{COM}$
(V$_{CC}$ = 2.3 V)
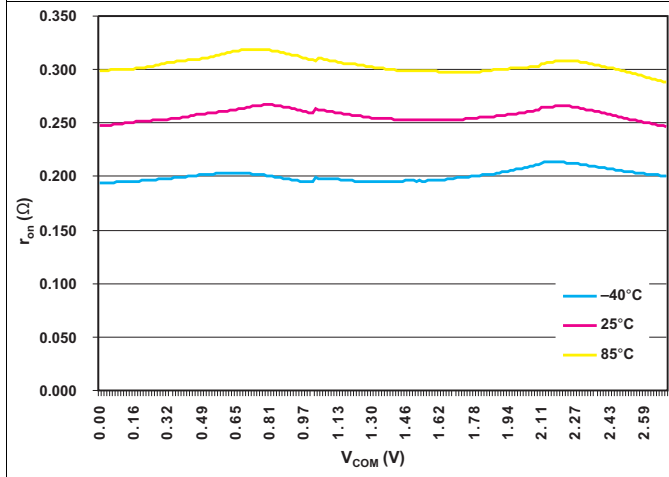
Figure 3. r$_{on}$ vs V$_{COM}$
(V$_{CC}$ = 2.7 V)
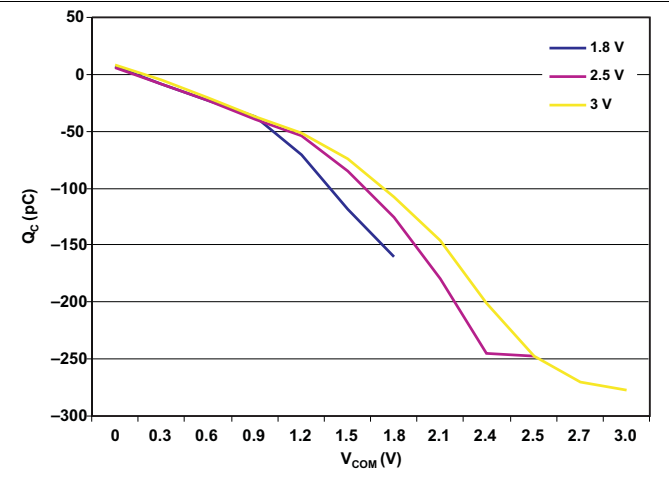
Figure 4. Charge Injection (Q$_C$) vs V$_{COM}$
(T$_A$ = 25°C)
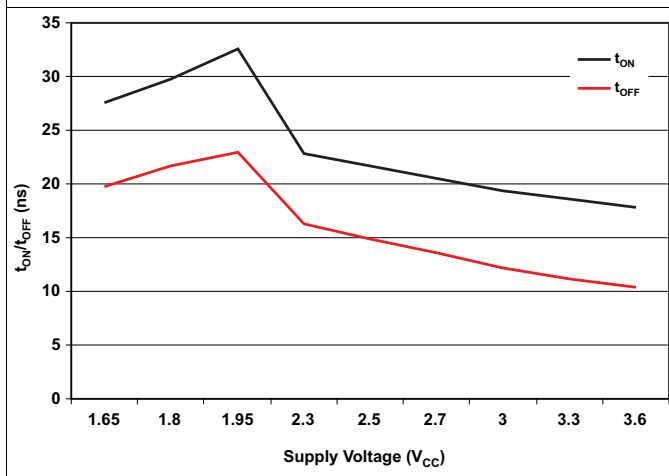
Figure 5. t$_{ON}$ and t$_{OFF}$ vs Supply Voltage
(T$_A$ = 25°C)

Figure 6. Bandwidth

Product Folder Links: TS3A24159
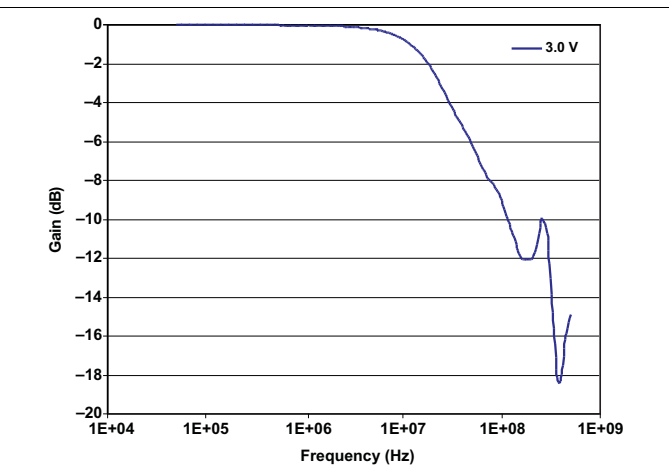
Typical Characteristics (continued)

Figure 7. OFF Isolation

Figure 8. Crosstalk

Figure 9. Total Harmonic Distortion vs Frequency
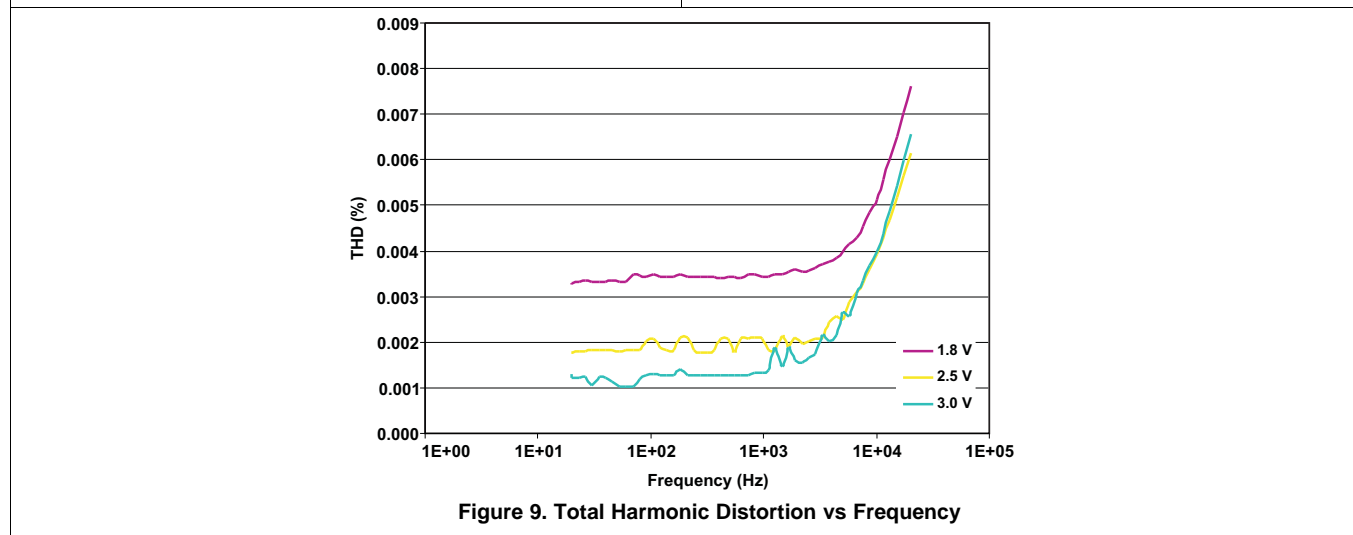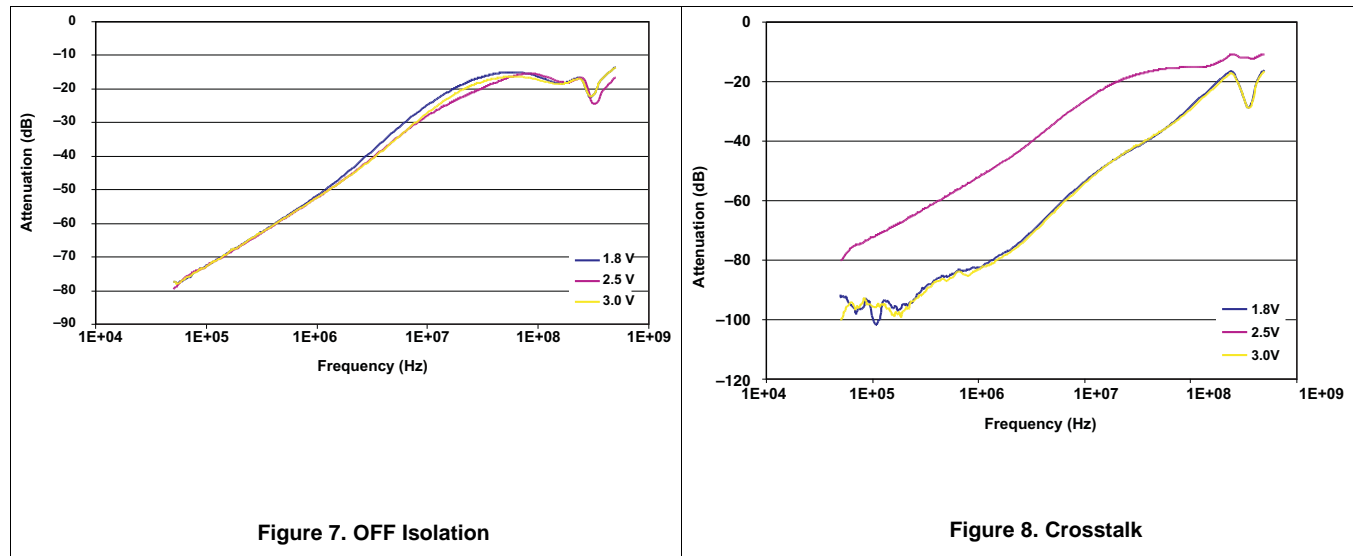
7 Parameter Measurement Information
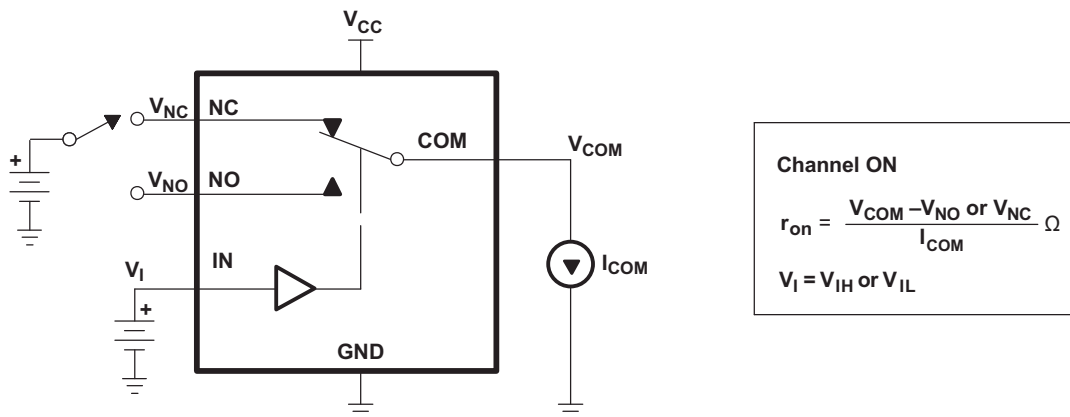
Figure 10. ON-State Resistance

Channel ON

$$r_{on} = \frac{V_{COM} - V_{NO} \text{ or } V_{NC}}{I_{COM}} \ \Omega$$

$V_I = V_{IH} \text{ or } V_{IL}$
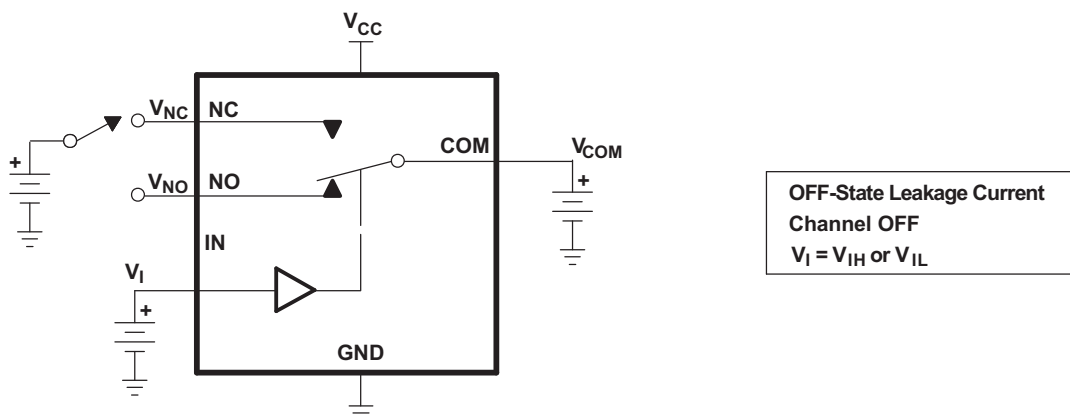
Figure 11. OFF-State Leakage Current
($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

OFF-State Leakage Current
Channel OFF
$V_I = V_{IH} \text{ or } V_{IL}$
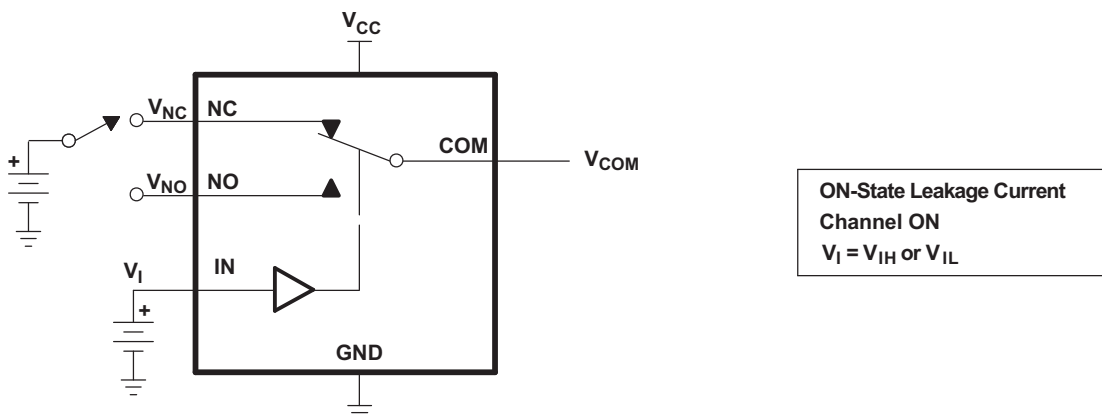
Figure 12. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

ON-State Leakage Current
Channel ON
$V_I = V_{IH} \text{ or } V_{IL}$

Product Folder Links: *TS3A24159*
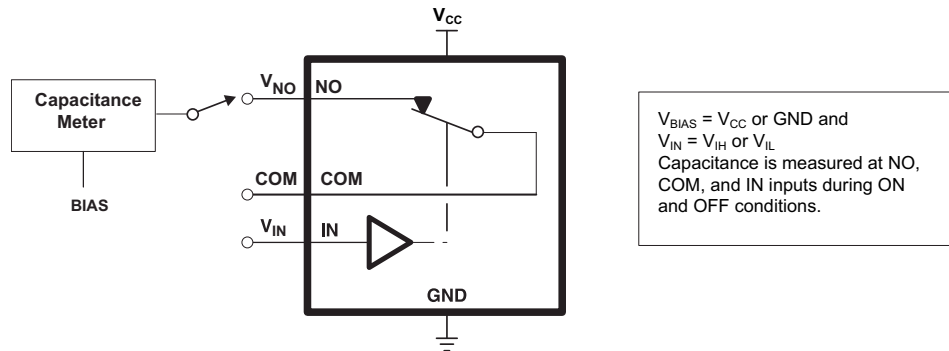
Figure 13. Capacitance C_I, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$
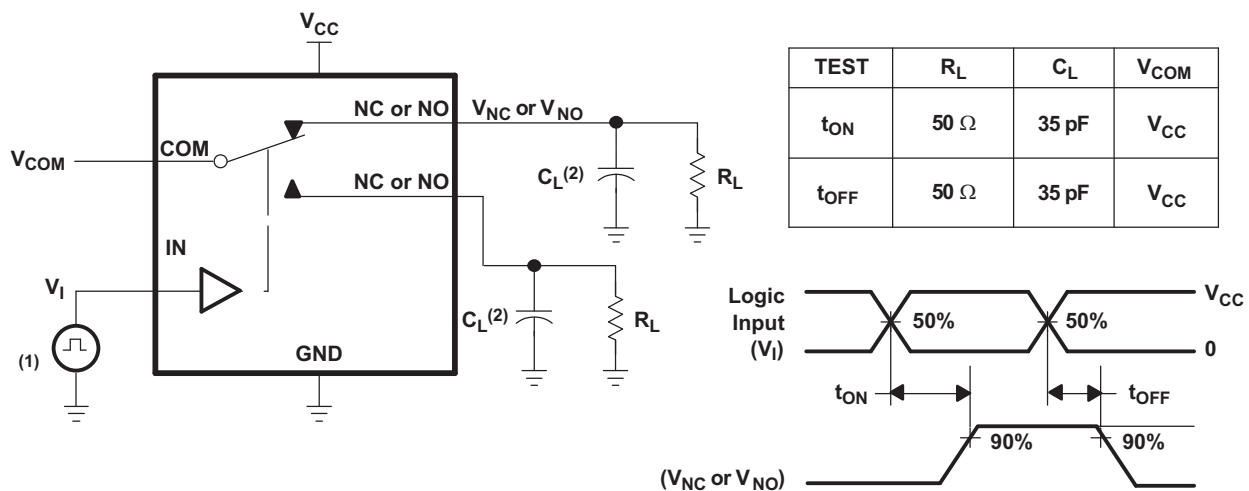
TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_{CC}
t_{OFF}	50 Ω	35 pF	V_{CC}

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 14. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})
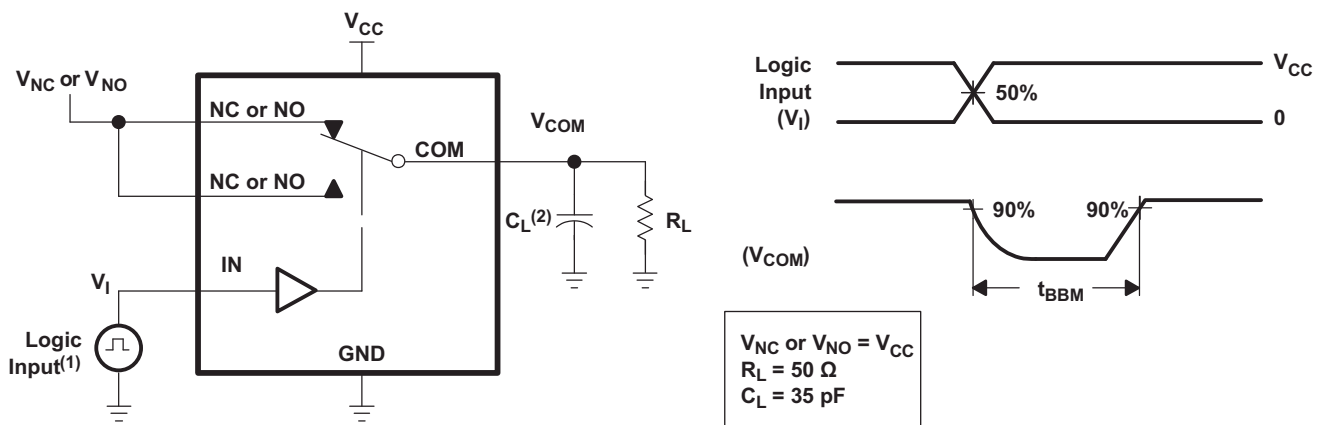
V_{NC} or $V_{NO} = V_{CC}$
R_L = 50 Ω
C_L = 35 pF

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 15. Break-Before-Make Time (t_{BBM})
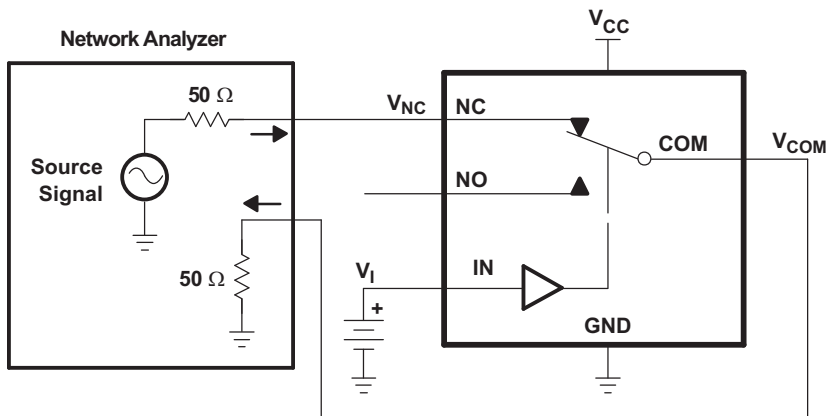
Product Folder Links: *TS3A24159*

Figure 16. Bandwidth (BW)
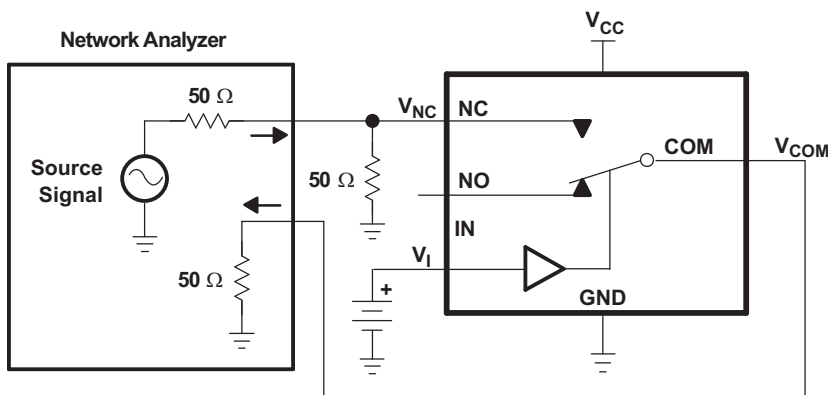
Figure 17. OFF Isolation (O$_{ISO}$)
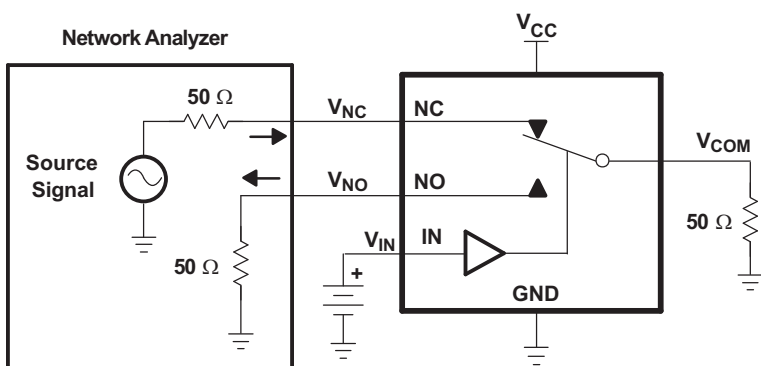
Figure 18. Crosstalk (X$_{TALK}$)

Submit Documentation Feedback 15

Product Folder Links: *TS3A24159*
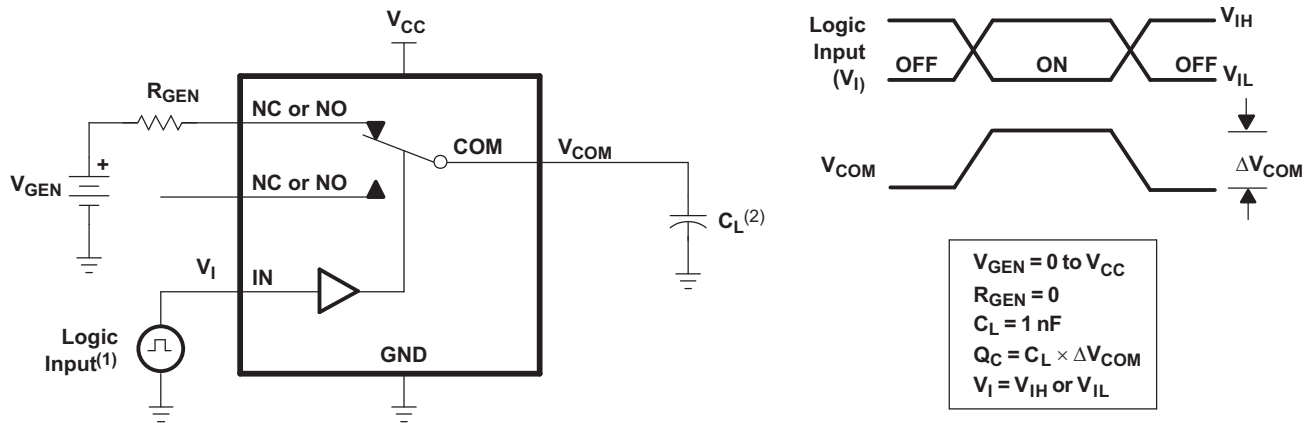
A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 19. Charge Injection (Q_C)
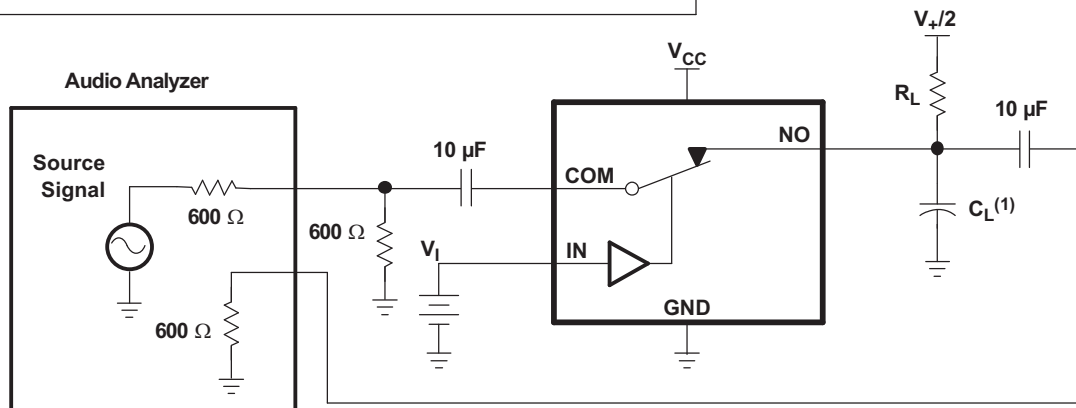
A. C_L includes probe and jig capacitance.

Figure 20. Total Harmonic Distortion (THD)

Product Folder Links: TS3A24159

8 Detailed Description

8.1 Overview

The TS3A24159 is a 2-channel single-pole double-throw (SPDT) bidirectional analog switch that is designed to operate from 1.65 V to 3.6 V. It offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance, low ON-state resistence, and consumes very low power. These are some of the features make this device suitable for a variety of markets and many different applications.

8.2 Functional Block Diagram
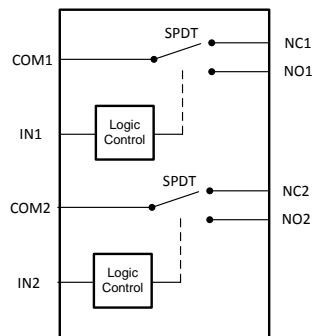
8.3 Feature Description

The TS3A24159 device is bidirectional with two single-pole, double-throw switches. Each of the two switches are controlled independently by two digital signals.

8.4 Device Functional Modes

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The switch of the TS3A23159 device is bidirectional. Hence, NO, NC and COM pins can be used as both inputs or outputs.

9.2 Typical Application
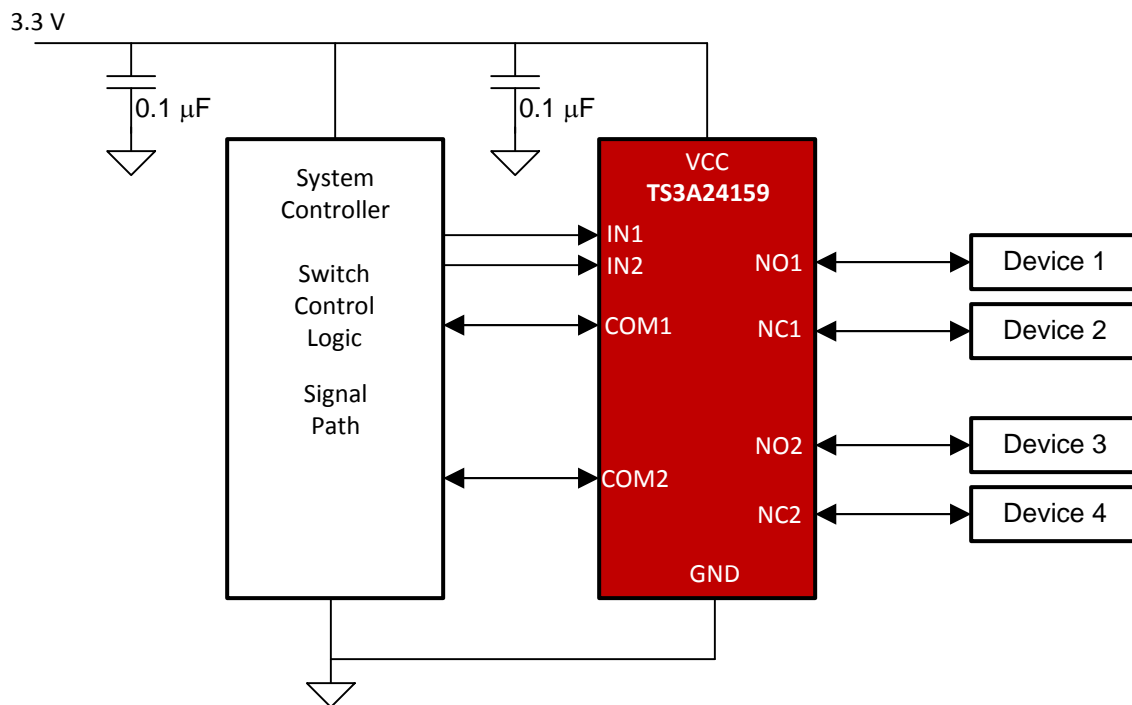
9.2.1 Design Requirements

Ensure that all of the signals passing through the switch are with in the specified ranges to ensure proper performance.

Table 2. Design Parameters

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	1.65	3.6	V
V_{NC} V_{NO} V_{COM}	Signal Voltage	0	V_{CC}	V
V_{IN}	Digital Input Voltage	0	V_{CC}	V

9.2.2 Detailed Design Procedure

The TS3A23159 device can be properly operated without any external components. However, it is recommended that unused pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device. It is also recommended that the digital control pins (IN1 and IN2) be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin.

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS3A23159 input/output signal swing through NO and COM are dependant of the supply voltage VCC.

9.2.3 Application Curve
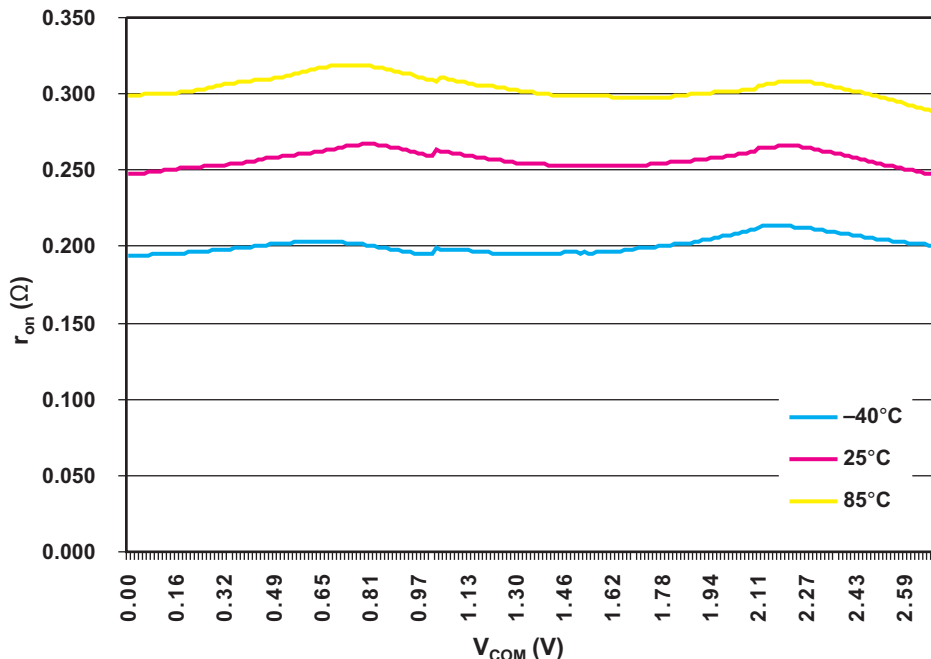
Figure 21. r_{ON} vs V_{COM}

10 Power Supply Recommendations

- Proper power-supply sequencing is recommended for all CMOS devices.
- Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device.
- Always sequence VCC on first, followed by NO or COM.
- Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components.
- A 0.1-µF capacitor, connected from VCC to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended. Bypass capacitors must be used on power supplies. Short trace lengths should be used to avoid excessive loading.

11.2 Layout Example
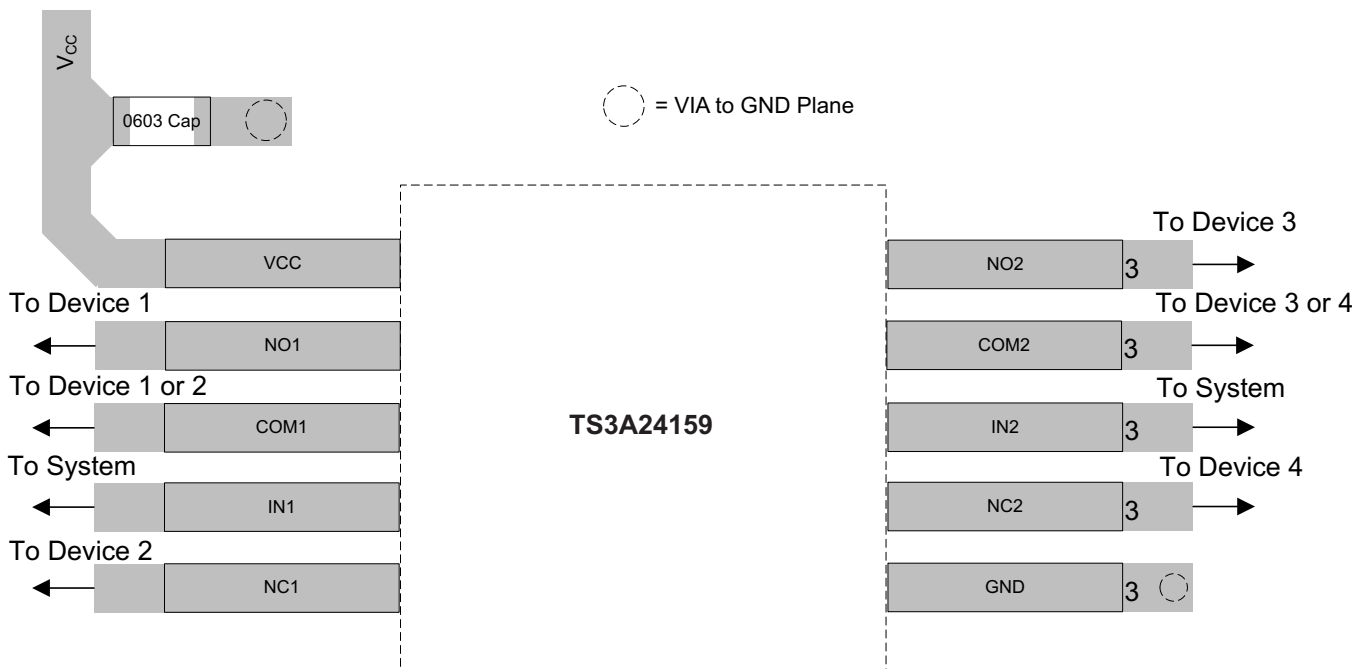
Figure 22. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following: *Implications of Slow or Floating CMOS Inputs*, SCBA004

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A24159DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L8Q ~ L8R)	Samples
TS3A24159DGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L8Q ~ L8R)	Samples
TS3A24159DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWS	Samples
TS3A24159DRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWS	Samples
TS3A24159YZPR	ACTIVE	DSBGA	YZP	10	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	L87	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A24159DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS3A24159DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS3A24159YZPR	DSBGA	YZP	10	3000	178.0	9.2	1.49	1.99	0.63	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A24159DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS3A24159DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TS3A24159YZPR	DSBGA	YZP	10	3000	220.0	220.0	35.0

DGS (S–PDSO–G10)   **PLASTIC SMALL–OUTLINE PACKAGE**

0,50

0,27 / 0,17   ⊕ 0,08 Ⓜ

10   6

3,10 / 2,90   5,05 / 4,75

1   5

3,10 / 2,90

0,23 / 0,13

Gauge Plane

0°–8°

0,25

0,70 / 0,40

1,10 MAX

0,15 / 0,05

Seating Plane

△ 0,10

4073272/C 02/04
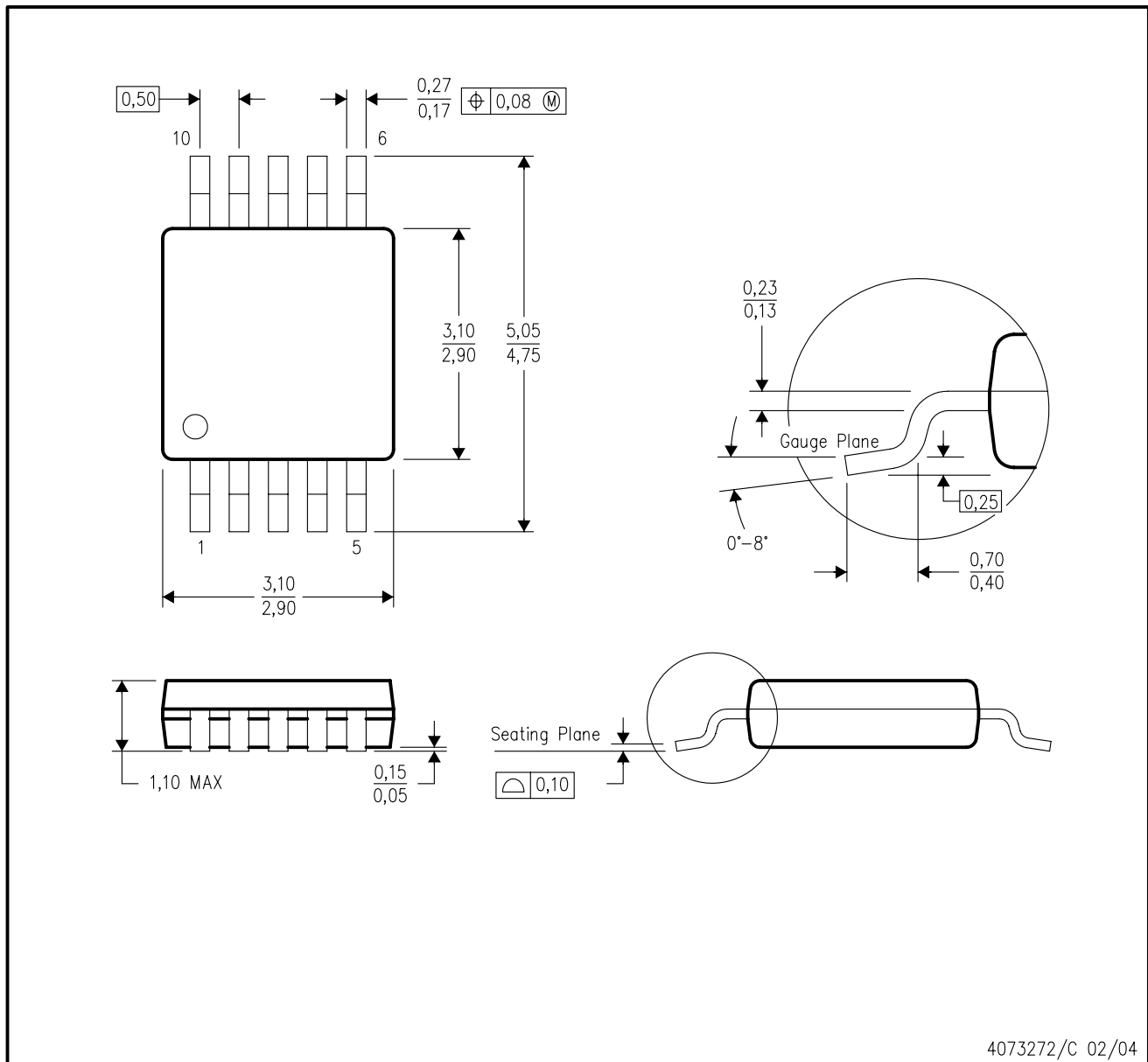
NOTES:
  A. All linear dimensions are in millimeters.
  B. This drawing is subject to change without notice.
  C. Body dimensions do not include mold flash or protrusion.
  D. Falls within JEDEC MO–187 variation BA.
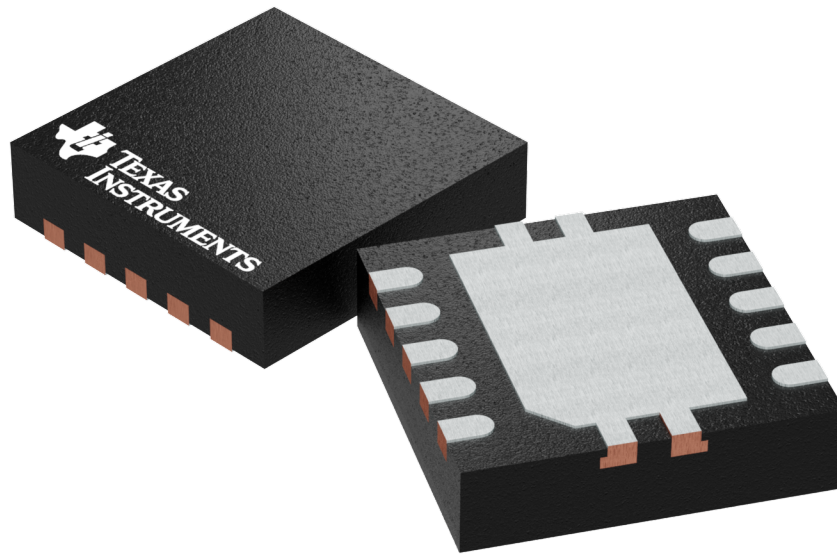
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204102-3/M

TEXAS
INSTRUMENTS

A

3.1
2.9

B

PIN 1 INDEX AREA

3.1
2.9

1.0
0.8

C

SEATING PLANE

0.05
0.00

0.08 C

1.65± 0.1

2X (0.5)

EXPOSED
THERMAL PAD

4X (0.25)

(0.2) TYP

5

6

2X
2

11

SYMM
₵

2.4± 0.1

10

1

8X 0.5

10X 0.30
0.18

PIN 1 ID
(OPTIONAL)

SYMM
₵

0.1 (M) C A B

0.05 (M) C

10X 0.5
0.3

4218878/B   07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

10X (0.6)

1

10X (0.24)

SYMM

8X (0.5)

5

(R0.05) TYP

($\varnothing$ 0.2) VIA
TYP

(1.65)

(0.5)

11

10

(2.4)

(3.4)

(0.95)

6

(0.25)

(0.575)

SYMM

(2.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

0.07 MAX
ALL AROUND

EXPOSED METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

EXPOSED METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED
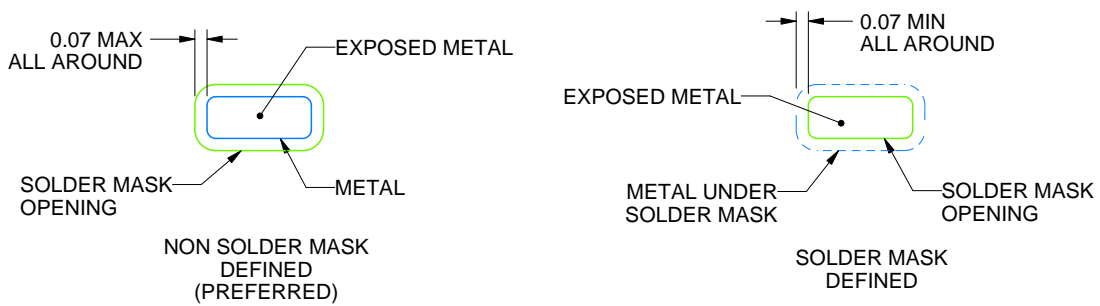
SOLDER MASK DETAILS

4218878/B   07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
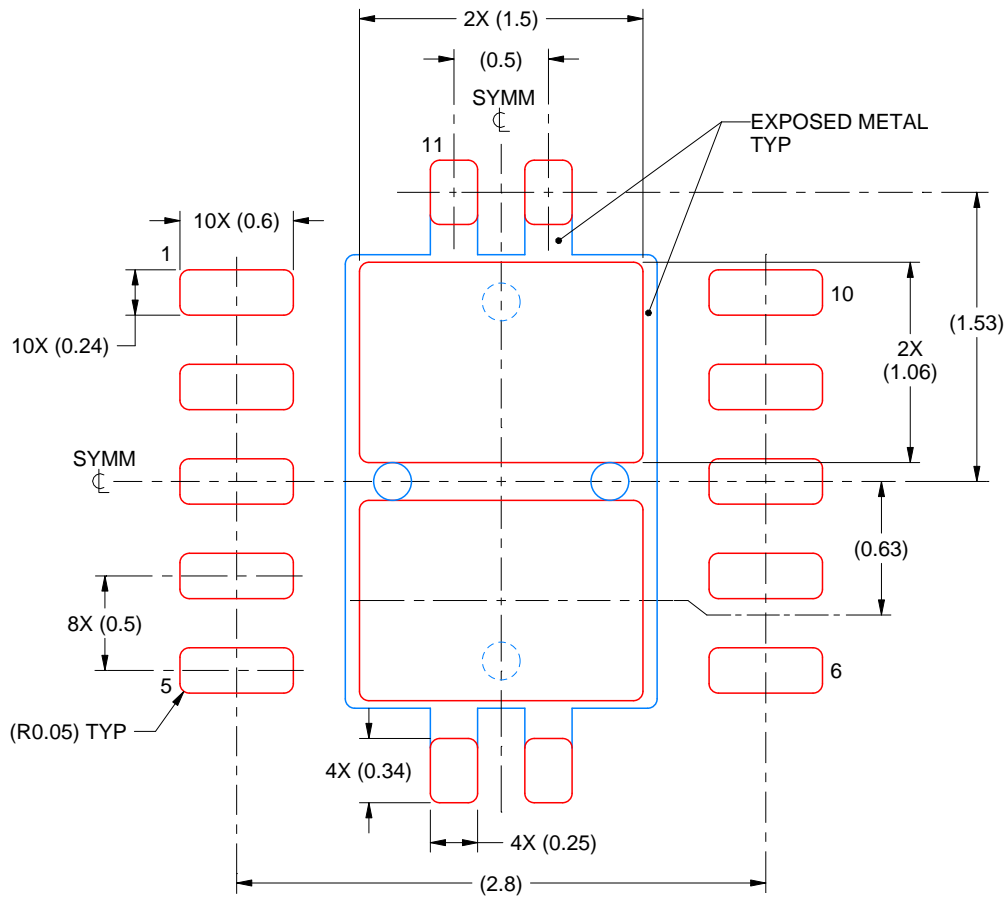
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B   07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
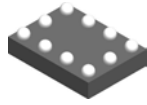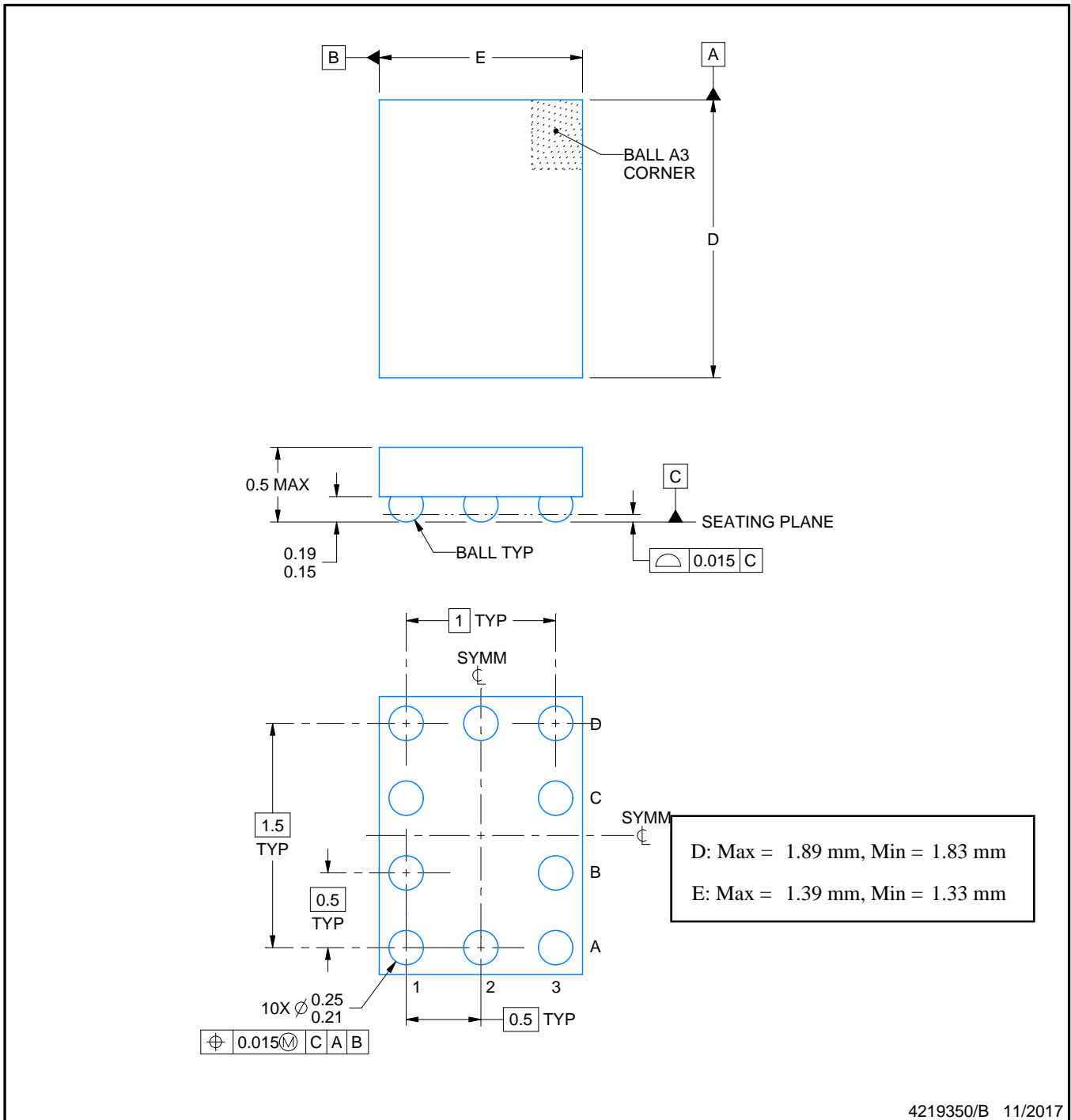
D: Max = 1.89 mm, Min = 1.83 mm

E: Max = 1.39 mm, Min = 1.33 mm

4219350/B   11/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

10X (Ø 0.225)

(0.5) TYP

(0.5) TYP

A

B

C

D

1   2   3

SYMM
℄

SYMM
℄
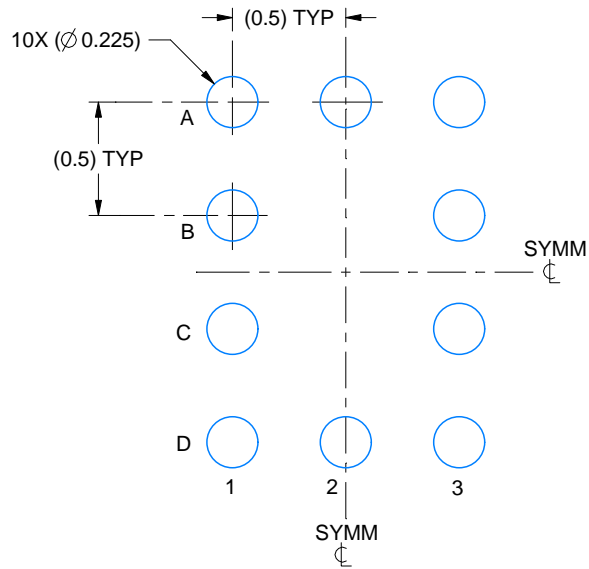
LAND PATTERN EXAMPLE
SCALE:30X

(Ø 0.225)
METAL

0.05 MAX

SOLDER MASK
OPENING

NON-SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN

METAL
UNDER
MASK

(Ø 0.225)
SOLDER MASK
OPENING

SOLDER MASK
DEFINED
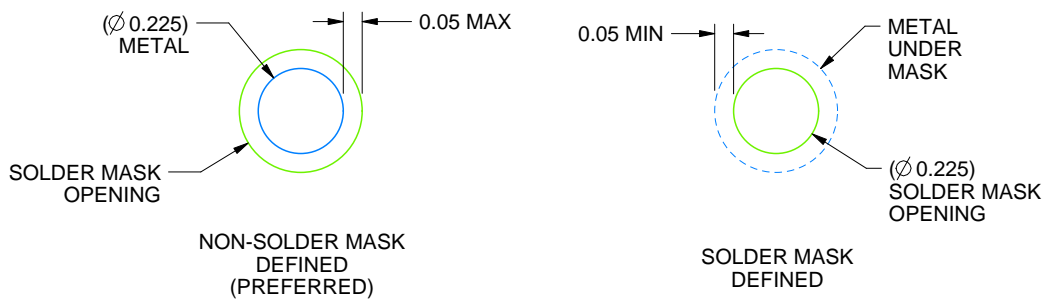
SOLDER MASK DETAILS
NOT TO SCALE

4219350/B   11/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).
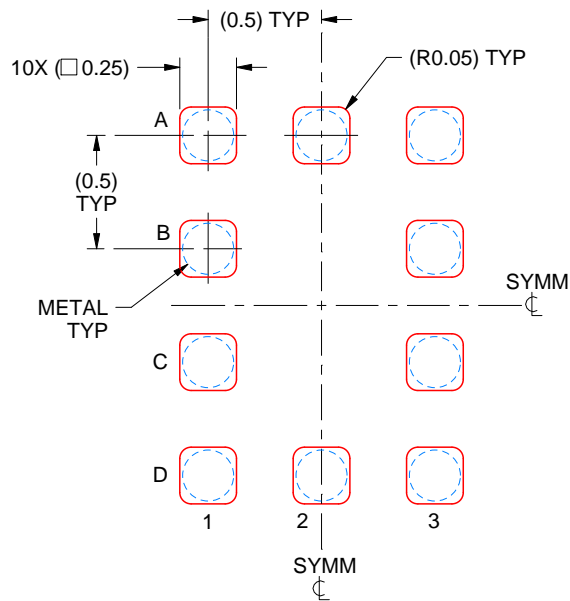
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219350/B   11/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE