24bit, 192kHz Dual Channel Digital to Analog Converter

PRODUCT DESCRIPTION

The MS4344 is a stereo digital-to-analog converter chip, which contains interpolation filter, a multi-bit Δ-Σ modulator, output analog filter. The MS4344 supports most of audio data formats. It is based on the fourth order of a linear analog low pass filter and multi-bit Δ-Σ modulator. The MS4344 can automatically adjust the sample rate from 2kHz and 200kHz by detecting signal frequency and main clock frequency. The MS4344 can operate at 3.3V and 5V. These features make it ideal for wireless devices such as DVD playback decoders and digital communication devices. The MS4344 is available in MSOP10 package.

MSOP10

FEATURES

- Muti-bit ΔΣ Modulator
- 24bit D/A
- Automatic Detection of Signal Frequencies up to 192KHz
- DR:110dB
- THD:0.003%
- Low Clock Jitter Sensitivity
- 3.3V or 5V Operating Voltage
- Linear Filter Output
- MSOP10 Package

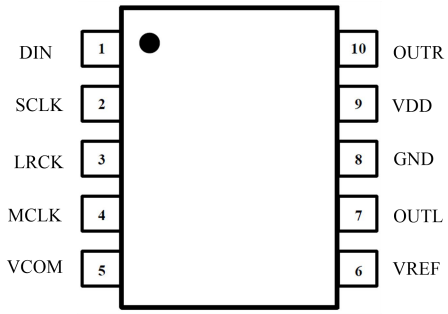
APPLICATIONS

- Digital Communication Equipment
- Car Audio System
- DVD Audio System

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS4344	MSOP10	MS4344

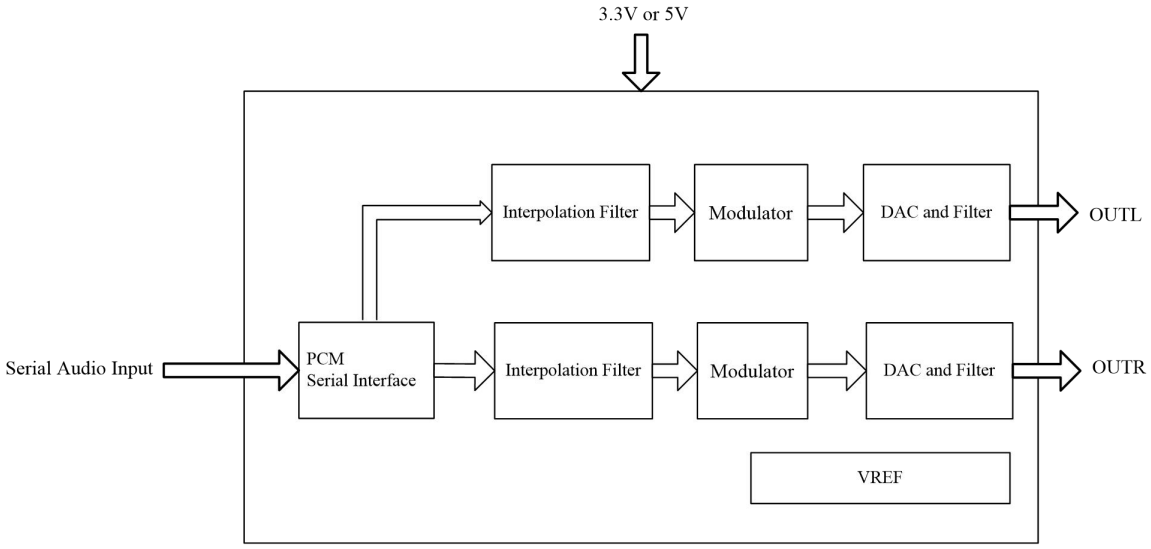
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	DIN	I	Serial Audio Data Input
2	SCLK	I	Serial Clock Input.
3	LRCK	I	Left or Right Serial Audio Data Line.
4	MCLK	I	Clock
5	VCOM	IO	Filter Connection for Internal Voltage.
6	VREF	IO	Positive Reference Voltage
7	OUTL	O	Left Channel Analog Output
8	GND	--	Ground
9	VDD	--	Power
10	OUTR	O	Right Channel Analog Output

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	VDD	-0.3 ~ 7	V
Input Current	I_in	-10 ~ +10	uA
Digital Input Voltage	VIN(D)	-0.3 ~ VDD+0.3	V
Operating Temperature	TOP	-40 ~ 125	°C
Storage Temperature	Tstg	-60 ~ 150	°C

ELECTRICAL CHARACTERISTICS

Recommended Operating Condition

(AGND=0V, All Voltages with respect to Ground)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply	VDD		3.0		5.5	V
Specified Temperature Range	TA	DZZ	-40		+85	°C

DAC Analog Characteristics

TA = 25°C, Full-scale Output Sinusoidal Signal, 997Hz, Fs = 48/96/192kHz;

RL = 3kΩ, CL = 10pF, Test Bandwidth 10Hz to 20kHz.

Parameter			3.3V			Unit
			Min	Typ	Max	
DR	24 bit	A-weighted	100	102		dB
THD	24 bit	0dB	0.003			%
		-60dB	0.1	0.3		%

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Inter channelIsolation (1kHz)			95	100		dB
DC Accuracy						
Interchannel Gain Mismatch				0.1	0.2	dB
Analog Output						
Full Scale Output Voltage			0.63*VDD	0.66*VDD	0.69*VDD	Vpp
Quiescent Voltage	VCOM			0.5*VDD		VDC
Max DC Current draw from OUT	IOUTmax			3.3		mA
Max Current draw from VCOM	IQmax			1		mA
Max AC-Load Resistance	RL			1		kΩ
Max Load Capacitance	CL			1000		pF
Output Impedance	ZOUT			110		Ω

Filter Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode						
PassBand	to -0.1 dB corner		0		0.35	Fs
	to -3 dB corner		0		0.4992	Fs
Frequency Response from 40 Hz to 15 kHz			-0.07		+0.55	dB
StopBand			0.54			Fs
StopBand Attenuation			55			dB
Group Delay		Tgd		10/fs		s
Double-Speed Mode						
PassBand	to -0.1 dB corner		0		0.22	Fs
	to -3 dB corner		0		0.501	Fs
Frequency Response from 40 Hz to 15 kHz			-0.02		+0.2	dB
StopBand			0.54			Fs
StopBand Attenuation			55			dB
Group Delay		Tgd		5/Fs		s
Quad-Speed Mode						
PassBand	to -0.1 dB corner		0		0.11	Fs
	to -3 dB corner		0		0.469	Fs
Frequency Response from 10 Hz to 20 kHz			-0.01		+0.1	dB
StopBand			0.54			Fs
StopBand Attenuation			55			dB
Group Delay		Tgd		2.5/Fs		s

Digital Input Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage(% of VDD)	VIH	VDD-0.6			V
Low-Level Input Voltage(% of VDD)	VIL			0.6	V
Input Leakage Current	Iin		0.02		uA
Input Capacitance			3	8	pF

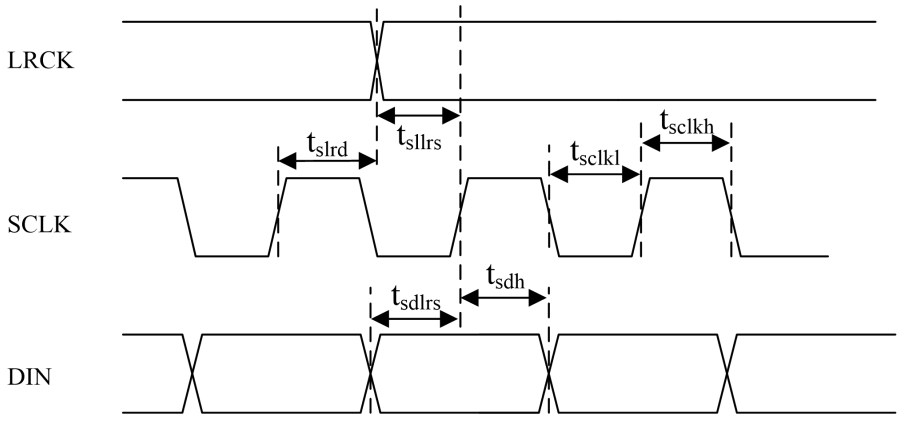
Power Characteristics

Parameters		Symbol	3.3V			Unit
			Min	Typ	Max	
Power Supply Current	Normal Operation	IA		16	21	mA
	Power Down state	IA		100		uA
Power Supply Rejection Ratio	1kHz	PSRR		50		dB
	60Hz	PSRR		40		dB

Switching Characteristics (Serial Port)

Parameters		Symbol	Min	Typ	Max	Units
MCLK Frequency			0.512		50	MHz
MCLK Duty Cycle			45		55	%
Input Sample Rate	MCLK/LRCK	Fs	2		200	kHz
	256x, 384x, 1024x		2		50	kHz
	256x, 384x		84		134	kHz
	512x, 768x		42		67	kHz
	1152x		30		34	kHz
	128x, 192x		50		100	kHz
	64x, 96x		100		200	kHz
	128x, 192x		168		200	kHz
External SCLK Mode						
LRCK Duty Cycle (External SCLK only)			45	50	55	%
SCLK Pulse Width Low		tsclkl	20			ns
SCLK Pulse Width High		tsclkh	20			ns
SCLK Duty Cycle			45	50	55	%
SCLK Rising to LRCK Edge Delay		tslrd	20			ns
SCLK Rising to LRCK Edge Setup Time		tslrs	20			ns
DIN Valid to SCLK Rising Setup Time		tsdlrs	20			ns
SCLK Rising to DIN Hold Time		tsdh	20			ns

External Serial Port Input Timing



FUNCTIONAL DESCRIPTION

The MS4344 accepts standard audio sampling frequency, including 48, 44.1, 32kHz in QSM mode, 96 , 88.2 and 64kHz in DSM mode, 192, 176.4, 128kHz in SSM mode. Audio data is entered through serial input data terminal (DIN). LRCK determines the channel of the current input data. A serial clock is a clock where audio data enters the input data cache.

Master Clock

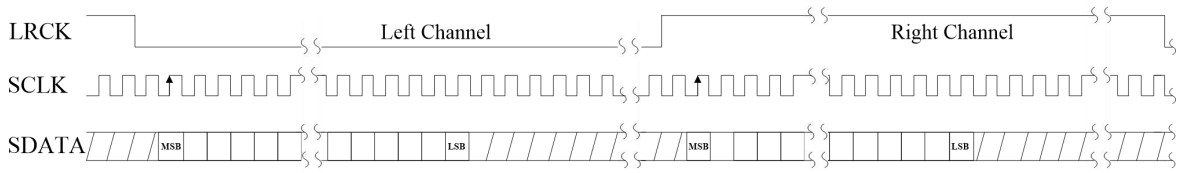
The MCLK/LRCK ratio must be an integer, as shown in table1 below. The frequency of LRCK is equal to the frequency Fs of input data for each channel. The ratio of MCLK to LRCK and the speed mode are initialized by calculating the number of MCLK cycles and the value of MCLK within an LRCK period. A built-in divider will produce a proper clock. The following table lists some of the audio sampling frequencies, along with the corresponding MCLK and LRCK frequencies. Note that although there is no phase requirement, the LRCK and MCLK must be synchronized.

Table 1. Common Clock Frequencies

Mode	LRCK (kHz)	MCLK(MHz)					
		128x	256x	384x	512x	768x	1024x
QSM	32	-	8.192	12.288	16.384	24.576	32.768
	44.1	5.6448	11.2896	16.9344	22.5792	33.868	45.158
	48	6.144	12.288	18.432	24.576	36.864	49.152
DSM	64	8.192	16.384	24.576	32.768	49.152	-
	88.2	11.2896	22.5792	33.868	45.1584	-	-
	96	12.288	24.576	36.864	49.152	-	-
SSM	128	24.576	32.768	49.152	-	-	-
	176.4	22.5792	45.1584	-	-	-	-
	192	24.576	49.152	-	-	-	-

Serial Input Clock

When 16 rising edge pulses are detected continuously at SCLK port during an LRCK cycle, an external serial input clock is entered.



I^2S, up to 24-bit data Data valid on rising edge of SCLK

MS4344 Data Format (I^2S)

Initialization and Power Down

When the system is initially powered up, it enters the power-down state. At this time, the interpolation filter and Δ-Σ modulator are reset. The internal reference voltage, digital-to-analog converter, switched-capacitor filter, and low-pass filter are shut down until the system detects MCLK and LRCK clock. Once MCLK and LRCK are detected, the system starts to calculate the ratio of MCLK to LRCK, then powers up the internal reference voltage, and finally powers up the digital-to-analog converter, the switched-capacitor filter, and outputs the quiescent voltage VCOM.

Output Transient Control

The MS4344 uses Pop-guard technology to reduce transient response during power-up and power-down.

Power On

The DC level at the output terminal is provided by the VCOM pin, which is low when the system is initially powered on. When MCLK detects this, VCOM generates a normal DC voltage. The start-up time is 400ms when a 10uF capacitor terminated to VCOM PIN.

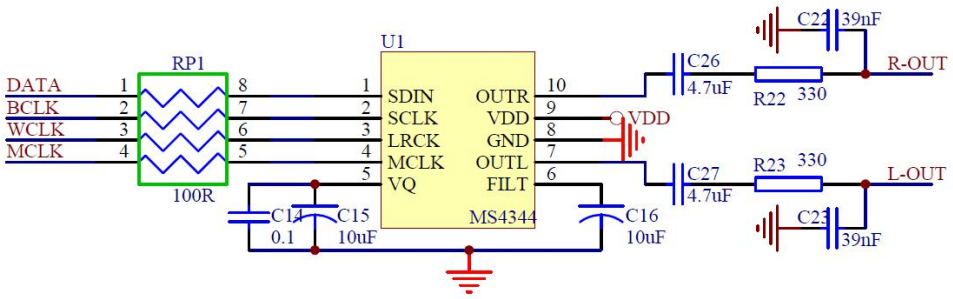
Power Off

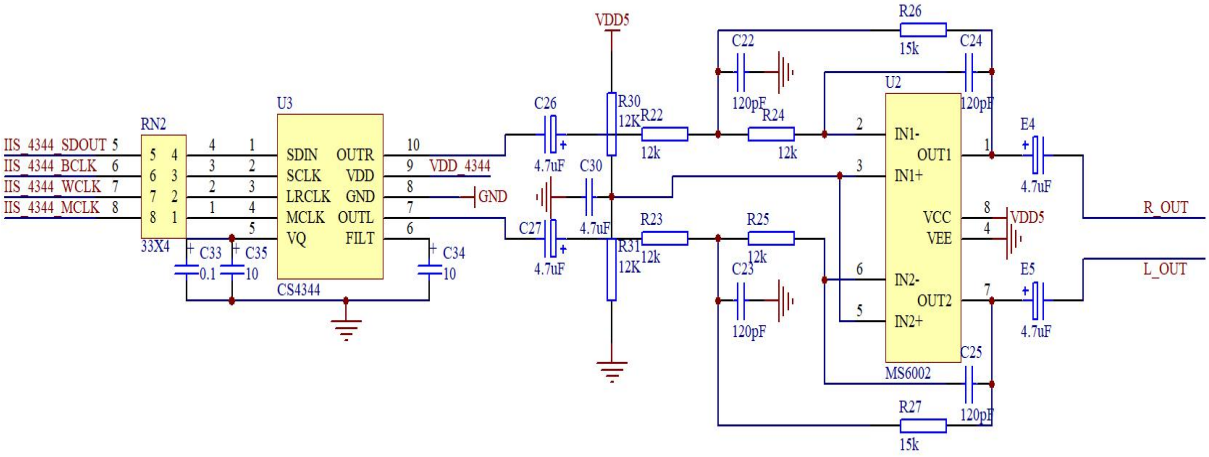
To prevent transient pulses at the output terminal during power down, a 10uF capacitor is connected to the VCOM pin. During this time, the VCOM pin and the output pin gradually descend to GND. When it is necessary to change the clock frequency or sampling frequency, it is better to keep 10 cycles in the LRCK low level signal. The DAC keeps the low level output during the clock transformation.

Ground and Power Supply Decouple

Be careful with ground and power connections to achieve desired performance. For best performance, the decoupling and filter capacitors must be placed as close as possible to the chip.

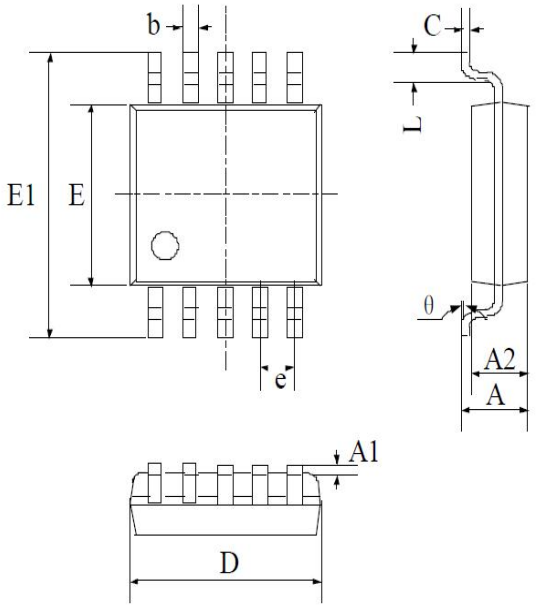
TYPICAL APPLICATIONS





PACKAGE OUTLINE DIMENSIONS

MSOP10



Symbol	Millimeters	
	Min	Max
A	0.800	1.200
A1	0.000	0.200
A2	0.760	0.970
b	0.30TYP	
c	0.152TYP	
D	2.900	3.100
e	0.50TYP	
E	2.900	3.100
E1	4.700	5.100
L	0.410	0.650
θ	0°	6°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

MS4344： Product Name
XXXXXXX： Product Code

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS4344	MSOP10	3000	1	3000	8	24000

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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