XN2101S

650 V Half-Bridge Gate Driver

Features

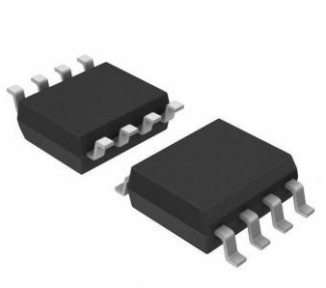
- Fully operational to 650 V
- Floating channel designed for bootstrap operation
- Output source/sink current capability 0.25 A/0.5 A
- Tolerant to negative transient voltage, dV/dt immune
- Matched propagation delay for both channels
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- Shoot-through (cross-conduction) protection
- Built-in dead-time protection: 0.5us
- 3.3 V, 5 V and 15 V input logic compatible
- Outputs in phase with inputs
- SOP8L package available
- RoHS compliant

Product summary

V_{OFFSET}	= 670 V max.
$I_{O+/-}$ (typ.)	= 0.25 A/0.5 A
V_{OUT}	= 10 V - 17.5 V
Internal deadtime	= 350 ns
$t_{on/off}$ (typ.)	= 500 ns/500 ns

Package

SOP8L



Application

- Motor drivers
- Home appliances
- IGBT and power MOS gate drivers for general purpose

Description

The XN2101S is a high voltage, high speed power MOSFET and IGBT driver with independent high-side and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 650 V.

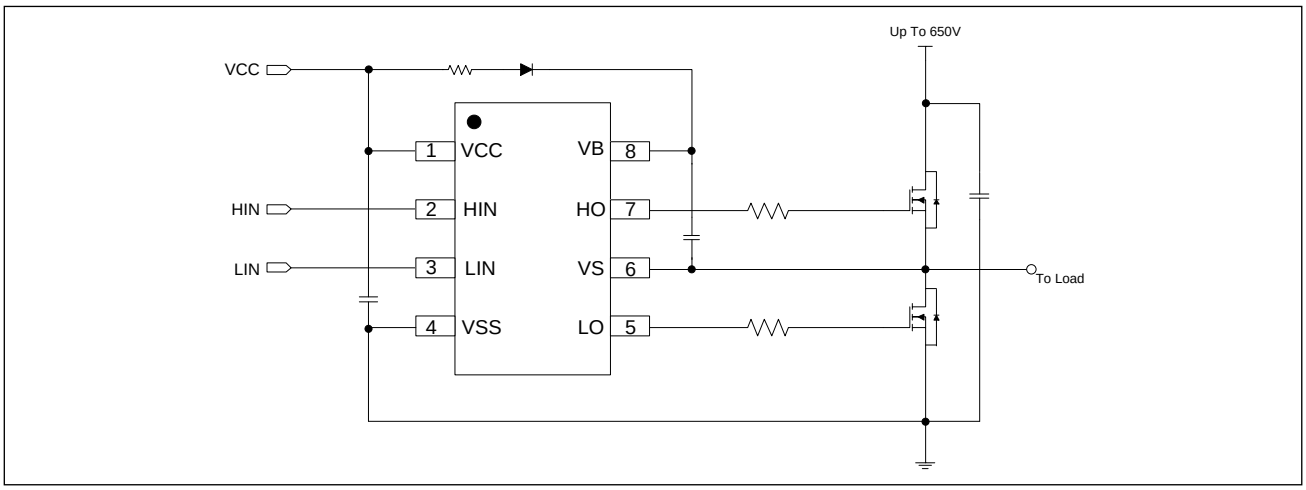


Figure 1 Typical application diagram

Ordering information

Base Part Number	Package	Standard Pack		Orderable Part Number
		Form	Quantity	
XN2101S	SOP8L	Tube/Bulk	95	XN2101S
		Tape and Reel	2500	XN2101STR

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1. Block diagram

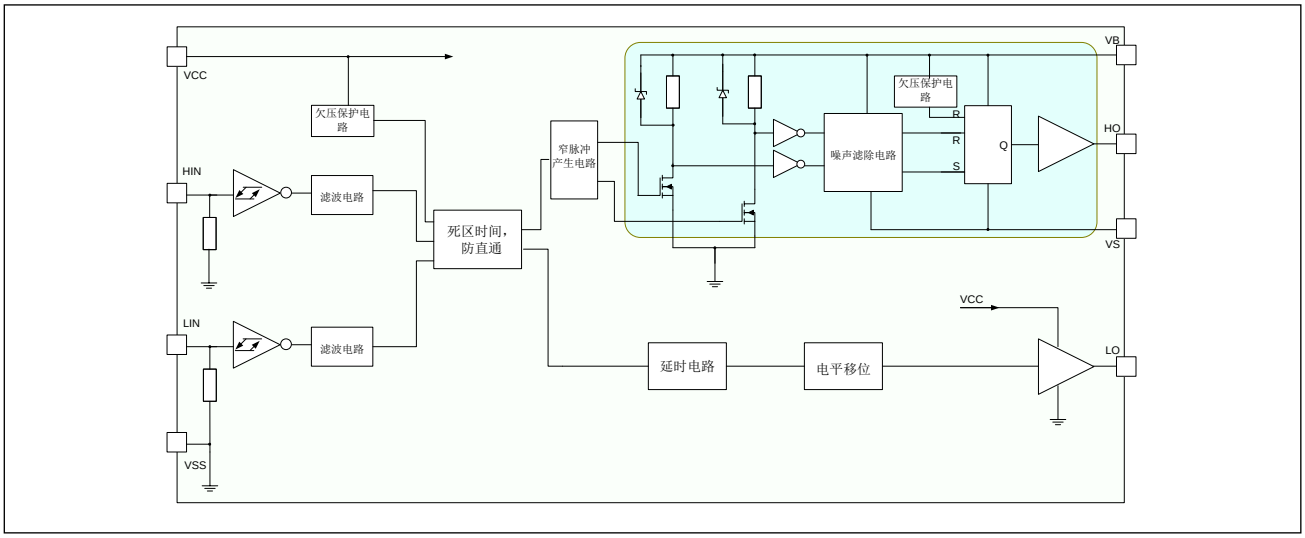


Figure 2 Function block diagram

2. Lead definitions

Table 1 XN2101S lead definitions

Pin no	Name	Function
1	VCC	Low-side and logic supply voltage
2	HIN	Logic input for high-side gate driver output (HO), in phase
3	LIN	Logic input for low-side gate driver output (LO), in phase
4	VSS	Low-side and logic supply voltage
5	LO	Low-side driver output
6	VS	High voltage floating supply return
7	HO	High-side driver output
8	VB	High-side gate drive floating supply

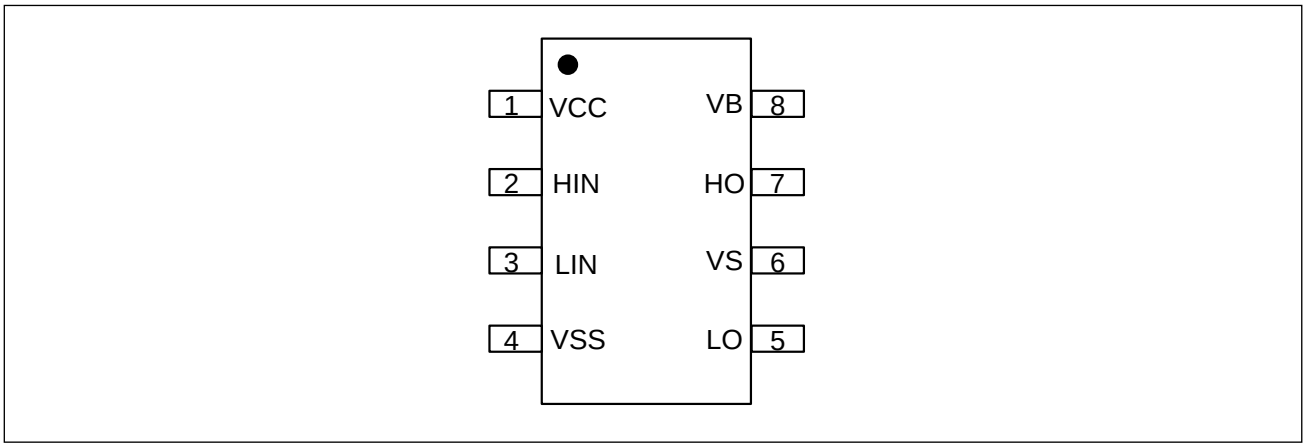


Figure 3 XN2101S lead assignments SOP8L(top view)

3. Electrical parameters

3.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Table 2 Absolute maximum ratings

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating well supply voltage	-0.3	625	V
V_S	High-side floating well supply return voltage	V_B-25	V_B+0.3	
V_{HO}	Floating gate drive output voltage	V_S-0.3	V_B+0.3	
V_{BS}	Floating gate drive voltage supply voltage	-0.3	25	
V_{CC}	Low side supply voltage	-0.3	25	
V_{LO}	Low-side output voltage	-0.3	V_{CC}+0.3	
V_{IN}	Logic input voltage	-0.3	V_{CC}+0.3	
dV_S/dt	Allowable V_S offset supply transient relative to V_{SS}	-	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$ ºC	-	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	-	200	℃/W
T_J	Junction temperature	-	150	℃
T_S	Storage temperature	-50	150	
T_L	Lead temperature (soldering, 10 seconds)	-	300	

3.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The offset rating is tested with supplies of $(V_{CC} – V_{SS}) = (V_B – V_S) = 15$ V.

Table 3 Recommended operating conditions

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating well supply voltage	V_S+10	V_S+20	V
V_S	High-side floating well supply return voltage	Note1	600	
V_{HO}	Floating gate drive output voltage	V_S	V_B	
V_{BS}	Floating gate drive voltage supply voltage	10	20	
V_{CC}	Low side supply voltage	10	20	
V_{LO}	Low-side output voltage	COM	V_{CC}	
V_{IN}	Logic input voltage	COM	V_{CC}	
T_A	Ambient temperature	-40	125	℃
t_{IN}	Pulse width for ON and OFF	0.5	-	us

3.3 Static electrical characteristics

(V_{CC} – V_{SS}) = (V_B – V_S) = 15 V, and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS} and are applicable to the respective input leads: H_{IN} and L_{IN}. The V_O and I_O parameters are referenced to V_{SS}/V_S and are applicable to the respective output leads H_O or L_O. The V_{CCUV} parameters are referenced to V_{SS}. The V_{BSUV} parameters are referenced to V_S.

Table 4 Static electrical characteristics

Symbol	Definition	Min.	TYP.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.2	7.8	8.4	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	6.6	7.2	7.8		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	0.4	0.6	-		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	7.9	8.6	9.3		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.3	8.0	8.7		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	0.4	0.6	-		
I_{LK}	High-side floating well offset supply leakage	-	1	5	uA	V_B = V_S = 600 V
I_{LK}	High-side floating well offset supply leakage	-	5	10		T_J = 125 °C, V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	-	70	100		
I_{QCC}	Quiescent V_{CC} supply current	-	700	1000		
V_{OH}	High level output voltage drop, V_{BIAS}-V_O	-	0.5	1	V	I_O = 20 mA
V_{OL}	Low level output voltage drop, V_O	-	0.15	0.3		
I_{o+}	Peak output current turn-on	-	250	-	mA	V_O = 0 V PW = 10 µs
I_{o-}	Peak output current turn-off	-	500	-		V_O = 15 V PW = 10 µs
V_{IH}	Logic “1” input voltage	2.3	-	-	V	
V_{IL}	Logic “0” input voltage	-	-	0.7		
I_{IN+}	Input bias current (H_O = High)	-	50	-	uA	V_{IN} = 5 V
I_{IN-}	Input bias current (H_O = Low)	-	0	-		V_{IN} = 0 V

3.3 Dynamic electrical characteristics

V_{CC} = V_{BS}= 15 V, V_S = V_{SS}, T_A = 25°C and C_L = 1000 pF unless otherwise specified.

Table 5 Dynamic electrical characteristics

Symbol	Definition	Min.	TYP.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	400	500	600	ns	$V_{LIN/HIN}$ = 0 or 5 V
t_{OFF}	Turn-off propagation delay	400	500	600		
t_R	Turn-on rise time	-	50	80		$V_{LIN/HIN}$ = 0 or 5 V C_L = 1 nF
t_F	Turn-off fall time	-	25	40		
t_{FILIN}	Input filter time	300	350	450		$V_{LIN/HIN}$ = 0 & 5 V
DT	Dead time	300	350	450		$V_{LIN/HIN}$ = 0 & 5 V
MT	Delay matching time	-	-	50		
MDT	Dead time matching time	-	-	50		

4. Switching and timing relationships

The relationship between the input and output signals of the XN2101S are illustrated below. From these figures, we can see the definitions of several timing parameters (i.e.,t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

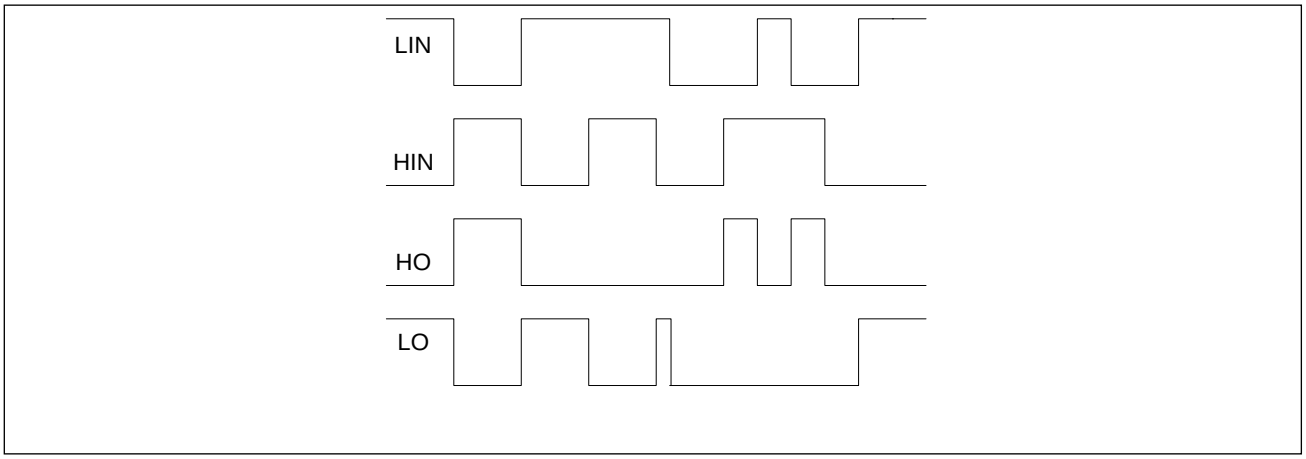


Figure 4 Input/Output timing diagram

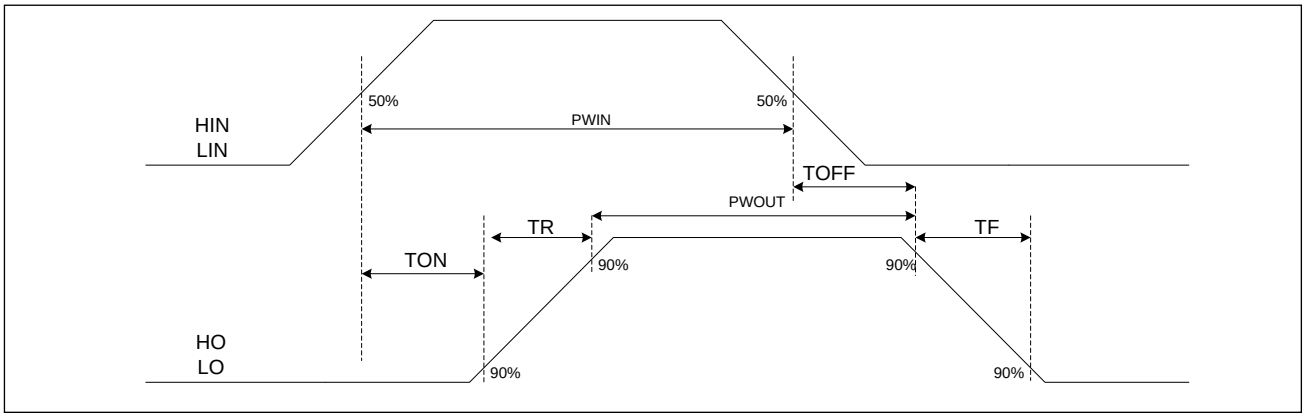


Figure 5 Switching time waveforms

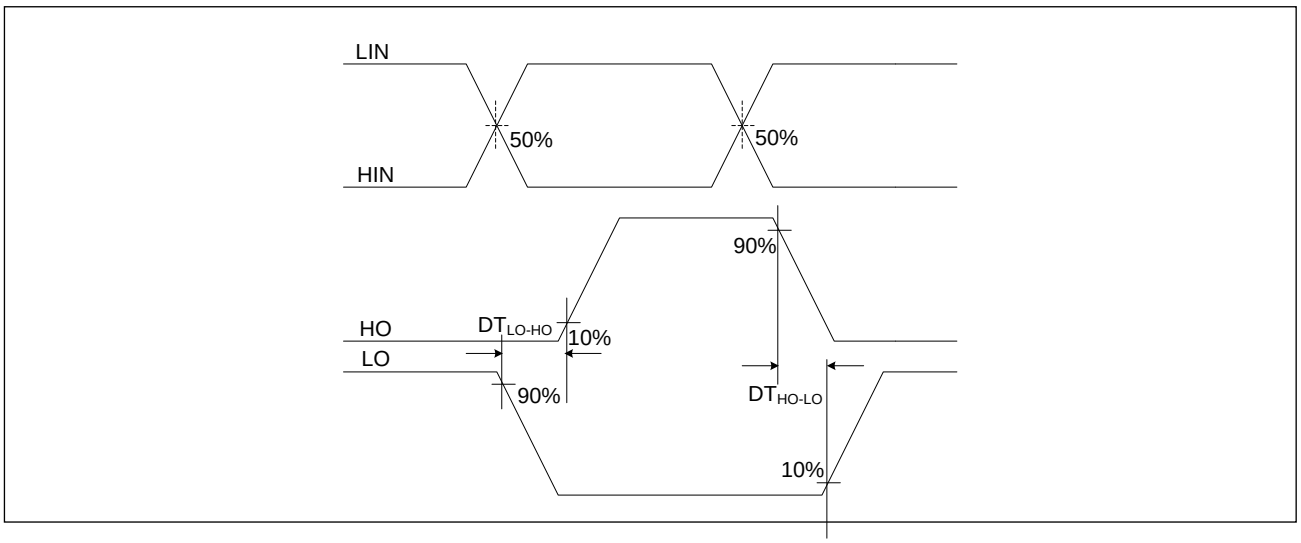
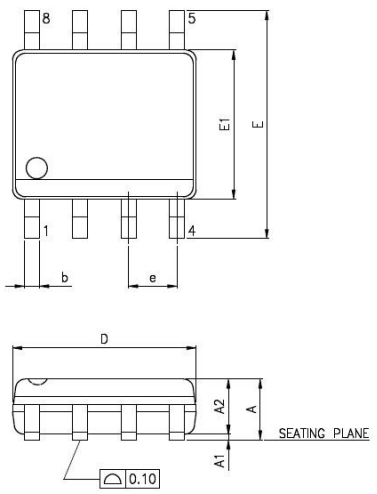


Figure 6 Deadtime waveform definitions

5. Package information SOP8L



	STANDARD		THERMAL	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	—	1.75	—	1.70
A1	0.10	0.25	0.00	0.15
A2	1.25	—	1.25	—
b	0.31	0.51	0.31	0.51
c	0.10	0.25	0.10	0.25
D	4.90 BSC		4.90 BSC	
E	6.00 BSC		6.00 BSC	
E1	3.90 BSC		3.90 BSC	
e	1.27 BSC		1.27 BSC	
L	0.40	1.27	0.40	1.27
h	0.25	0.50	0.25	0.50
θ°	0	8	0	8

UNIT : mm

THERMALLY ENHANCED DIMENSIONS

PAD SIZE	E2		D1	
	MIN.	MAX.	MIN.	MAX.
90X90E	1.94	2.29	1.94	2.29
95X13E	2.05	2.41	2.81	3.30
96X65E(DUAL PAD)	1.78	2.44	2.90	3.56

UNIT : mm

NOTES:
1.JEDEC OUTLINE : MS-012 AA REV.F (STANDARD)
MS-012 BA REV.F (THERMAL)
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3.DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.

Figure 5 Package outline SOP8L

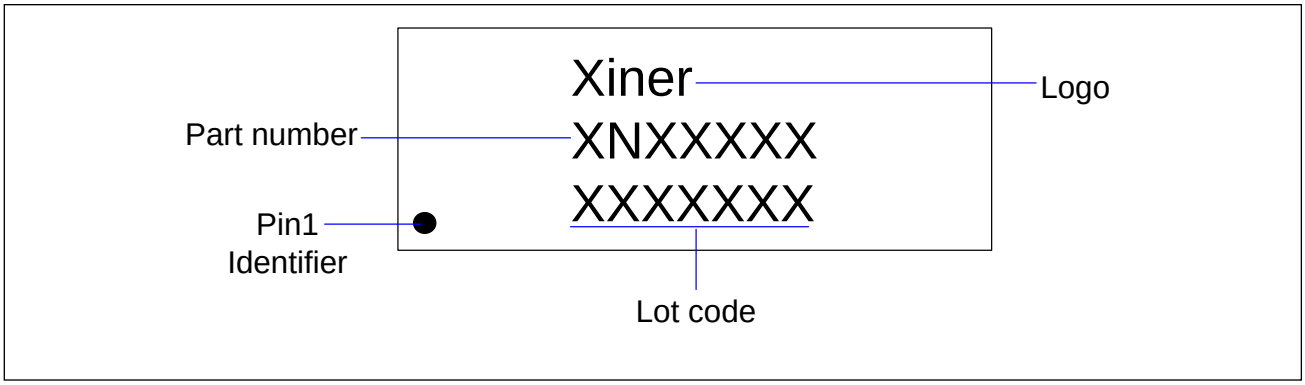
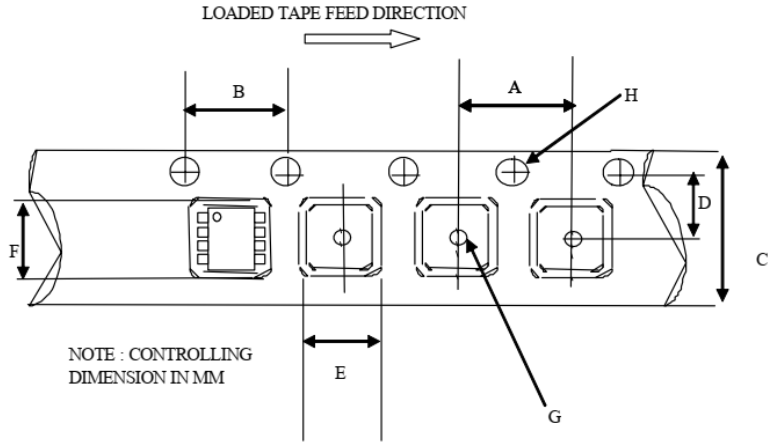
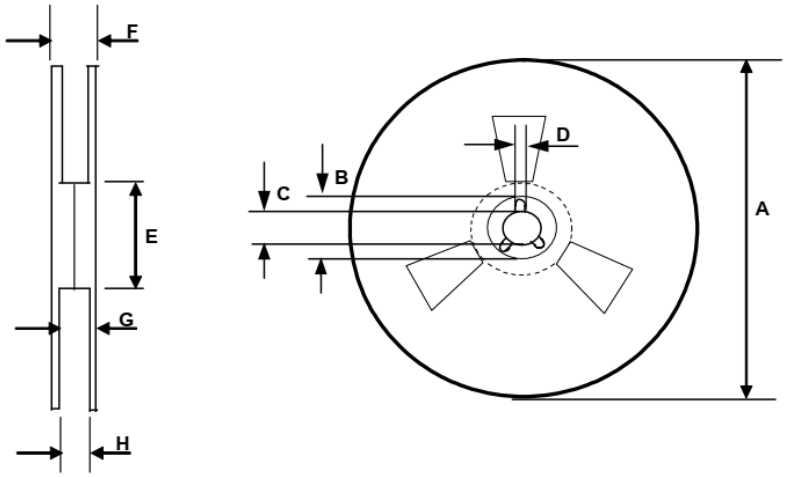


Figure 6 Marking information SOP8L



CARRIER TAPE DIMENSION FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Figure 7 Tape and reel details SOP8L

6. Qualification information

Table 7 Qualification information

Moisture sensitivity level		SOP8L	MSL3, 260°C (per IPC/JEDEC J-STD-020)
ESD	Charged device model	Class C3 (> 1.0 kV) (per JESD22-C101)	
	Human body model	Class 2 (per JEDEC standard JESD22-A114)	
IC latch-up test		Class II Level A (per JESD78)	
RoHS compliant		Yes	

Revision history

Document version	Date of release	Description of changes
1.0	2014-09-22	Preliminary datasheet
2.0	2015-01-06	First release version
2.1	2018-07-19	Product update
2.2	2020-06-19	Product update

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