Single 16-/14-/12-Bit, Low-Power, High-Performance DACs

Features

- Single, 16-/14-/12-Bit Pin-Compatible DACs
  TPC116S1: 16 Bits
  TPC114S1: 14 Bits
  TPC112S1: 12 Bits
- Low Power Consumption (90 μA Typ)
- Differential Nonlinearity: ±1LSB (Max)
- Glitch Energy: 2 nV-s
- Power-on Reset to Zero
- Supply Range: 2.7 V to 5.5 V
- Buffered Rail-to-Rail Output Operation
- Safe Power-on Reset (POR) to Zero DAC Output
- Fast 30-MHz, 3-Wire,
  SPI/QSPI/MICROWIRE-Compatible Serial Interface
- Schmitt-Trigger Inputs for Direct Optocoupler Interface
- SYNC Interrupt Facility
- High-Performance Drop-in Compatible with DAC8551, DAC7512
- Available in a Tiny MSOP8 Package

Applications

- Gain and Offset Adjustment
- 2-Wire Sensors
- Process Control and Servo Loops
- Portable Instrumentation
- Programmable Voltage and Current Sources
- Programmable Attenuators
- Automatic Test Equipment

Description

The TPC116S1/TPC114S1/TPC112S1 are pin-compatible 12-bit, 14-bit, and 16-bit digital-to-analog converters. The series of products are single-channel, low-power, and buffered voltage-out DACs, and are guaranteed monotonic by design. The devices use a precision external reference applied through the high-resistance input for rail-to-rail operation and low system power consumption.

The TPC116S1/TPC114S1/TPC112S1 accept a wide 2.7-V to 5.5-V supply voltage range. The parts incorporate a power-on reset circuit to ensure that the DAC output powers up to 0 V and remains there until a valid write takes place. The parts contain a power-down feature that reduces the current consumption of the devices to 400 nA at 5 V and provides software-selectable output loads while in power-down mode. The power consumption is 0.45 mW at 5 V, reducing to 1 μW in power-down mode.

The on-chip precision output amplifiers of TPC116S1/TPC114S1/TPC112S1 allow rail-to-rail output swing to be achieved. For remote sensing applications, the inverting input of the output amplifier is available to users. The TPC116S1/TPC114S1/TPC112S1 use a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

The TPC116S1/TPC114S1/TPC112S1 are available in the small-sized MSOP8 package. All packages are specified over the −40°C to +125°C extended industrial temperature range.

Typical Application Circuit

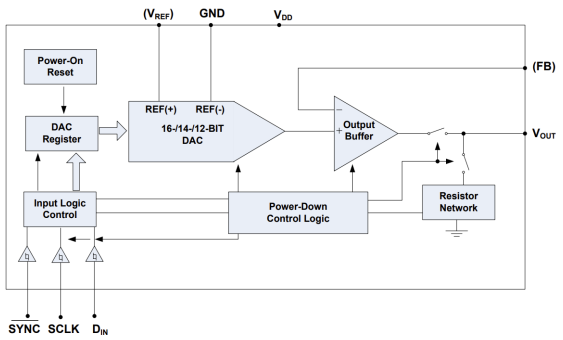


Table of Contents

Revision History

Date	Revision	Notes
2015-06-01	Rev.A.0	Initial release.
2024-12-26	Rev.A.1	Updated to a new datasheet format. Added the Tape and Reel Information. Updated the Package Outline Dimensions.

Pin Configuration and Functions

TPC11xS1
MSOP8 Package
Top View

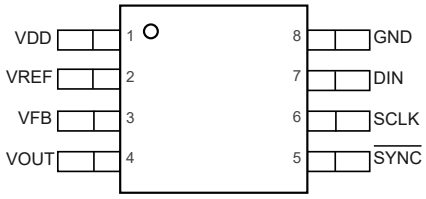


Table 1. Pin Functions: TPC11xS1

Pin No.	Name	I/O	Description
1	VDD		Power supply input, 2.7 V to 5.5 V
2	VREF		Reference voltage input.
3	VFB		Feedback connection for the output amplifier. For voltage output operation, tie to VOUT externally.
4	VOUT		Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
5	$\overline{\text{SYNC}}$		Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 16th/24th clock (unless $\overline{\text{SYNC}}$ is taken HIGH before this edge, in which case the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the TPC112S1/TPC114S1/ TPC116S1). Schmitt-Trigger logic input.
6	SCLK		Serial clock input. Data can be transferred at rates up to 30 MHz. Schmitt-Trigger logic input.
7	DIN		Serial data input. Data is clocked into the 16-/24-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input.
8	GND		Ground reference point for all circuitry on the part.

Specifications

Absolute Maximum Ratings (1)

Parameters	Min	Max	Unit
Supply Voltage: $V^+ - V^-$ (2)		6.5	V
Input Voltage	V^- – 0.3	V^+ + 0.3	
Input Current: +IN, –IN (3)	−20	+20	mA
Output Short-Circuit Duration (4)		Indefinite	
Operating Temperature Range	−40	125	°C
Maximum Junction Temperature		150	°C
Storage Temperature Range	−65	150	°C
Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The supplies must be established simultaneously, with, or before, the application of any input signals.
(3) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500 mV beyond the power supply, the input current should be limited to less than 10 mA.
(4) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	8000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	2000	V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP8	210	45	°C/W

Electrical Characteristics

All test conditions: V_{DD}= 5 V, V_{REF}= 5 V, C_L= 100 pF, R_L= 10 kΩ, T_A= -40°C to +125°C, unless otherwise noted. Typical values are at T_A= +25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Accuracy (1)						
N	Resolution	TPC112S1	12			Bits
		TPC114S1	14			
		TPC116S1	16			
INL	Integral Nonlinearity	TPC112S1 (12-bit) (2)	−2	±0.25	2	LSB
		TPC114S1 (14-bit) (2)	−8	±1	8	
		TPC116S1 (16-bit) (2)	−16	±8	16	
DNL	Differential Nonlinearity	TPC112S1 (12-bit) (2)	−1	±0.05	1	LSB
		TPC114S1 (14-bit) (2)	−1	±0.1	1	
		TPC116S1 (16-bit) (2)	−1	±0.5	1	
OE	Zero Offset Error			6.5	30	mV
	Full-Scale Offset Error		−30	0	30	mV
	Offset-Error Drift			±1		μV/°C
GE	Gain Error		−0.3	±0.13	0.3	%FS
	Gain Temperature Coefficient			±2		ppmFS/°C
Reference Input						
V_{REF}	Reference-Input Voltage Range		2		V_{DD}	V
R_{REF}	Reference-Input Impedance			333		kΩ
DAC Output						
	Output Voltage Range		0		V_{REF}	V
	DC Output Impedance			0.1		Ω
C_L	Capacitive Load (4)	Series resistance = 0 Ω			0.1	nF
		Series resistance = 1 kΩ			15	μF
R_L	Resistive Load (4)		5			kΩ
	Short-Circuit Current	V_{DD} = 5.5 V		35		mA
	Power-Up Time	From power-down mode		25		μs
DIGITAL INPUTS (SCLK, DIN, $\overline{SYNC}$)						
V_{IH}	Input High Voltage	V_{DD} = 5 V	2			V
		V_{DD} = 3.3 V	1.5			V
V_{IL}	Input Low Voltage	V_{DD} = 5 V			0.6	V
		V_{DD} = 3.3 V			0.4	V
I_{IN}	Input Leakage Current	V_{IN} = 0 V or V_{DD}		±0.1	±1	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance			1		pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{HYS}	Hysteresis Voltage			0.15		V
Dynamic Performance (4)						
SR	Voltage-Output Slew Rate	Positive and Negative		1		V/μs
	Voltage-Output Settling Time	1/4 Scale to 3/4 Scale, to ≤ 0.5 LSB, 14-bit		14		μs
	Reference −3-dB Bandwidth	Hex Code = 800 (TPC112S1), Hex Code = 2000 (TPC114S1), Hex Code = 8000 (TPC116S1)		100		kHz
	Digital Feedthrough	Code = 0, All digital inputs from 0 V to VDD, SCLK < 50 MHz		0.5		nV·s
	DAC Glitch Impulse	Major Code Transition		2		nV·s
	Output Noise	10 kHz		90		nV/√Hz
	Integrated Output Noise	0.1 Hz to 10 Hz		45		μV_{P-P}
Power Requirements						
V_{DD}	Supply Voltage		2.7		5.5	V
I_{DD}	Supply Current	No Load; All digital inputs at 0 V or V_{DD}, Supply Current Only; Excludes Reference Input Current, Midscale		90	130	μA
	Power-down Supply Current	No Load, All digital inputs at 0 V or V_{DD}		0.4	1	μA

Serial Write Operation

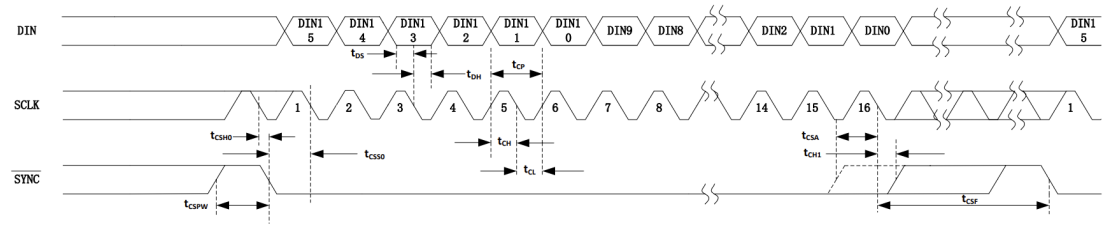


Figure 1. 16-Bit Serial-Interface Timing Diagram (TPC112S1)

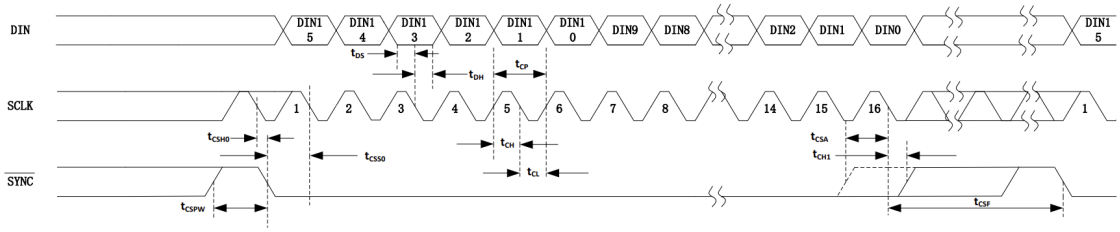


Figure 2. 16-Bit Serial-Interface Timing Diagram (TPC114S1)

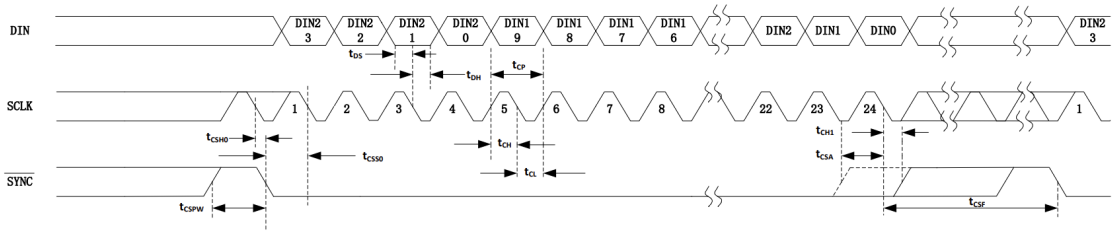


Figure 3. 24-Bit Serial-Interface Timing Diagram (TPC116S1)

Table 2. Timing Characteristics (Figures 1, 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCLK}	Serial Clock Frequency		0		30	MHz
t_{CH}	SCLK Pulse-Width High		8			ns
t_{CL}	SCLK Pulse-Width Low		8			ns
t_{CSS0}	$\overline{SYNC}$ Fall to SCLK Fall Setup Time		8			ns
t_{CSH0}	$\overline{SYNC}$ Fall to SCLK Fall Hold Time		0			ns
t_{CSH1}	$\overline{SYNC}$ Fall to SCLK Fall Hold Time		0			ns
t_{CSA}	$\overline{SYNC}$ Rise to SCLK Fall				12	ns
t_{CSF}	SCLK Fall to $\overline{SYNC}$ Fall		100			ns
t_{DS}	DIN to SCLK Fall Setup Time		5			ns
t_{DH}	DIN to SCLK Fall Hold Time		4.5			ns
t_{CSPW}	$\overline{SYNC}$ Pulse-Width High		20			ns
t_{CLPW}	$\overline{SYNC}$ Pulse-Width High		20			ns
t_{CSC}	$\overline{SYNC}$ Rise to $\overline{SYNC}$ Fall		20			ns

Typical Performance Characteristics

All test conditions: V_S = 5 V, At T_A = +25°C, unless otherwise specified

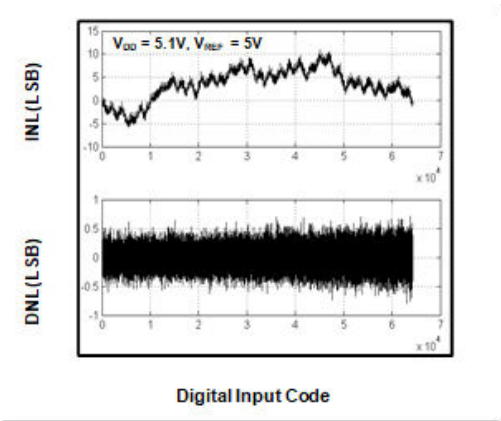


Figure 4. INL and DNL vs. Digital Input Code(+25°C TPC116S1)

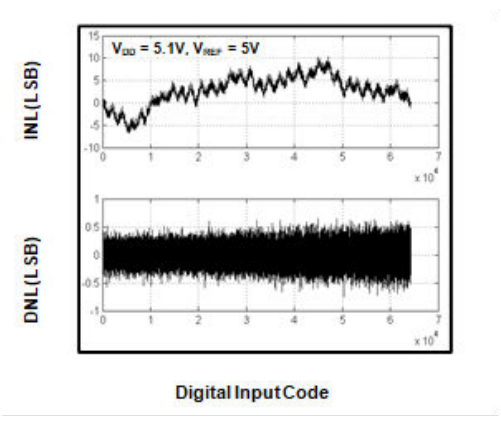


Figure 5. INL and DNL vs. Digital Input Code(-40°C TPC116S1)

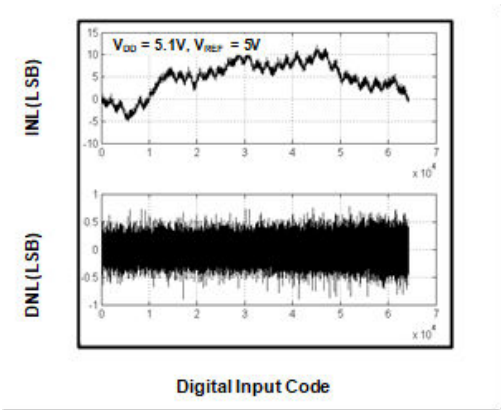


Figure 6. INL and DNL vs. Digital Input Code(+125°C TPC116S1)

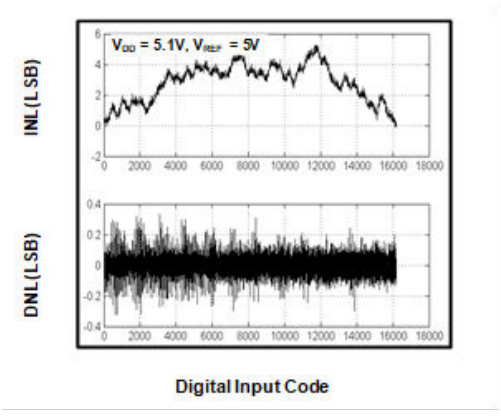


Figure 7. INL and DNL vs. Digital Input Code(+25°C TPC114S1)

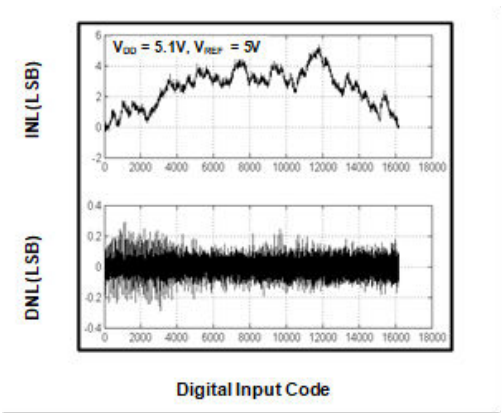


Figure 8. INL and DNL vs. Digital Input Code(-40°C TPC114S1)

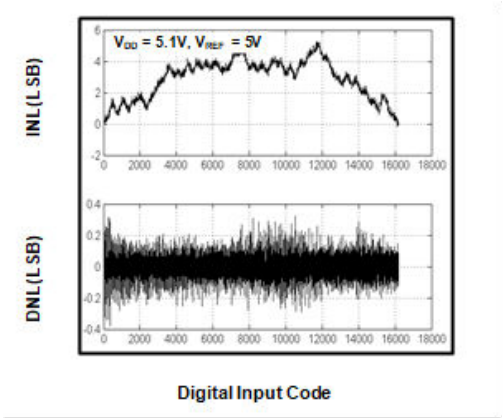


Figure 9. INL and DNL vs. Digital Input Code(+125°C TPC114S1)

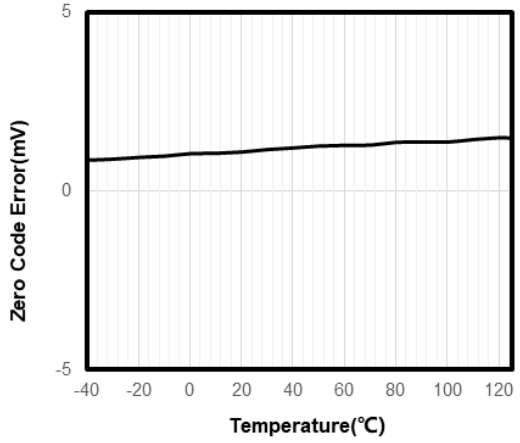


Figure 10. Zero-Scale Error vs. Temperature (TPC112S1)

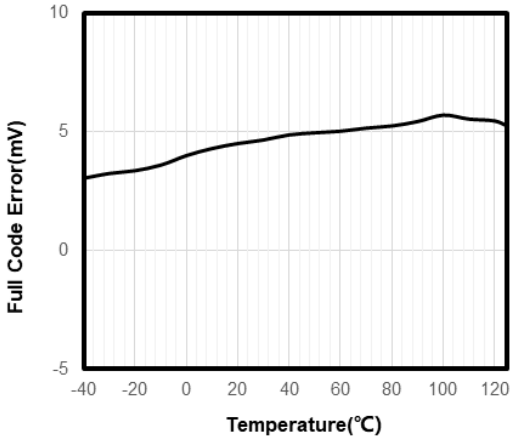


Figure 11. Full-Scale Error vs. Temperature (TPC112S1)

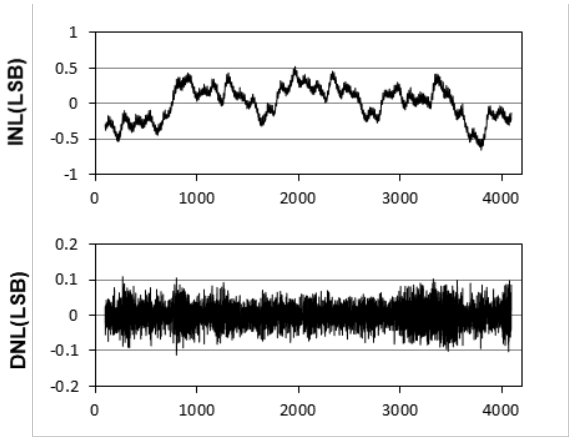


Figure 12. INL and DNL vs. Digital Input Code (-40°C TPC112S1)

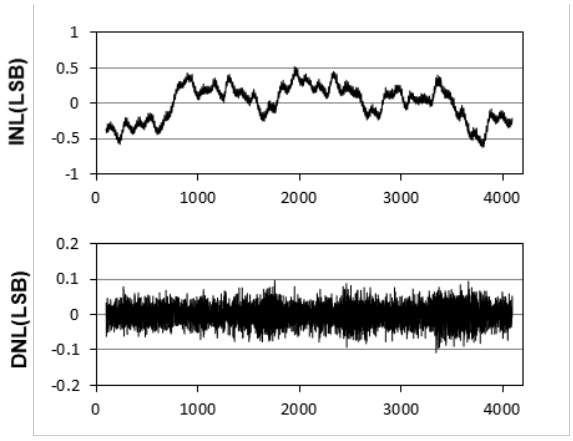


Figure 13. INL and DNL vs. Digital Input Code (25°C TPC112S1)

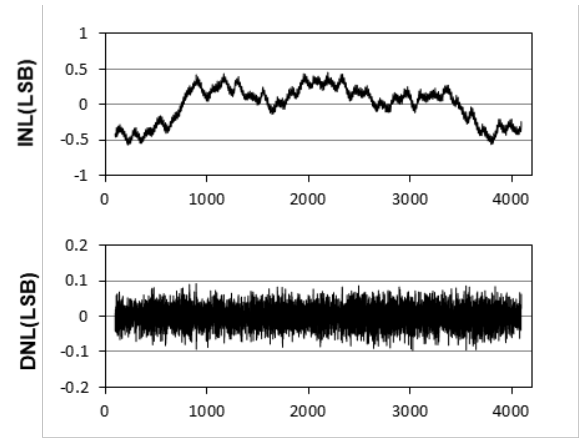


Figure 14. INL and DNL vs. Digital Input Code (125°C TPC112S1)

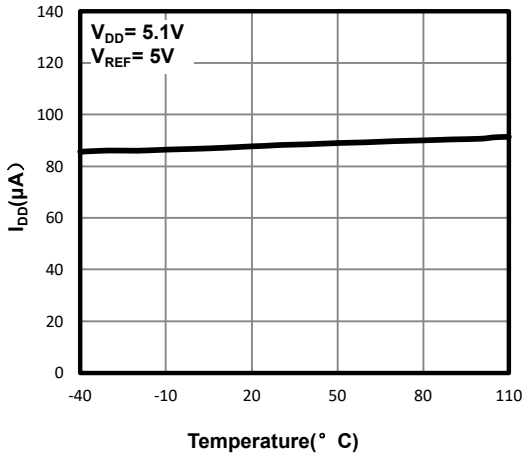


Figure 15. Power-Supply Current vs. Temperature(TPC114S1)

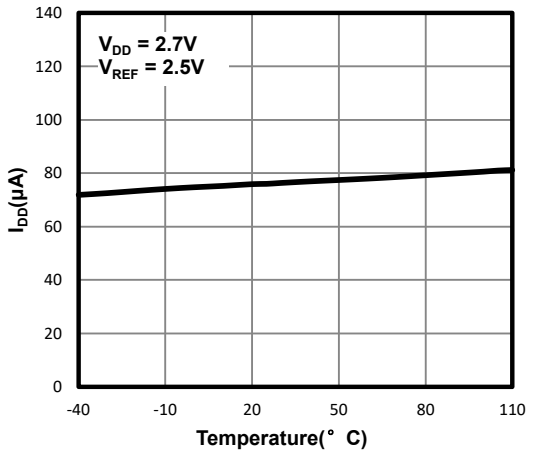


Figure 16. Power-Supply Current vs. Temperature(TPC114S1)

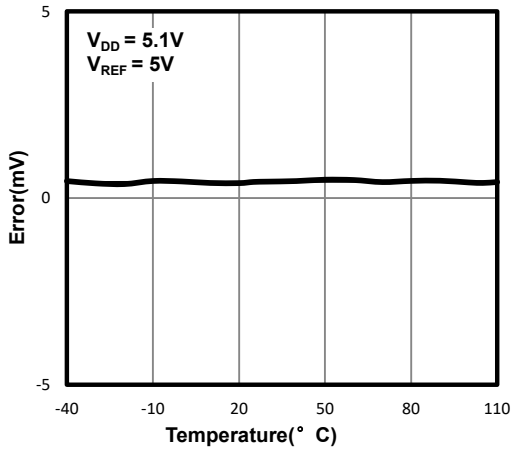


Figure 17. Zero-Scale Error vs. Temperature(TPC114S1)

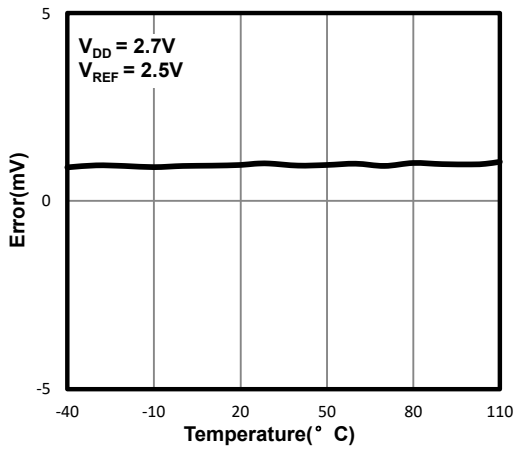


Figure 18. Zero-Scale Error vs. Temperature(TPC114S1)

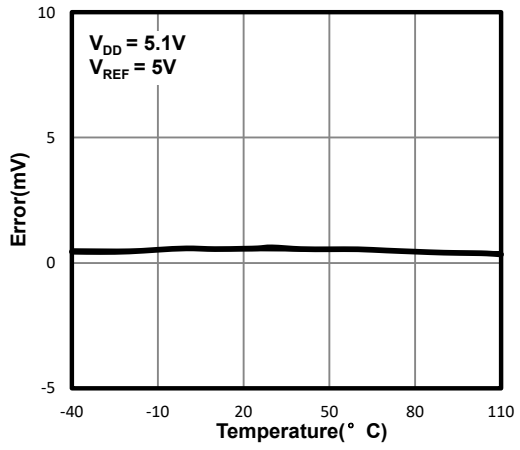


Figure 19. Full-Scale Error vs. Temperature(TPC114S1)

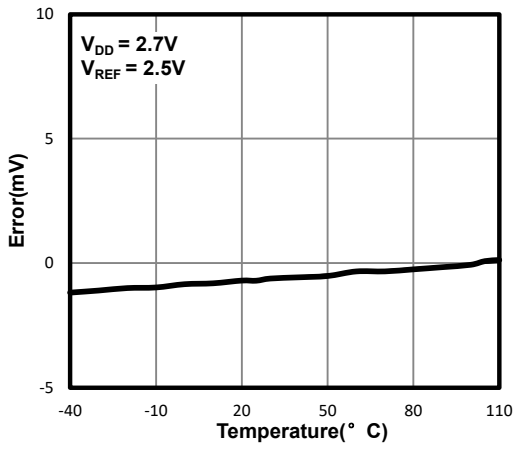


Figure 20. Full-Scale Error vs. Temperature(TPC114S1)

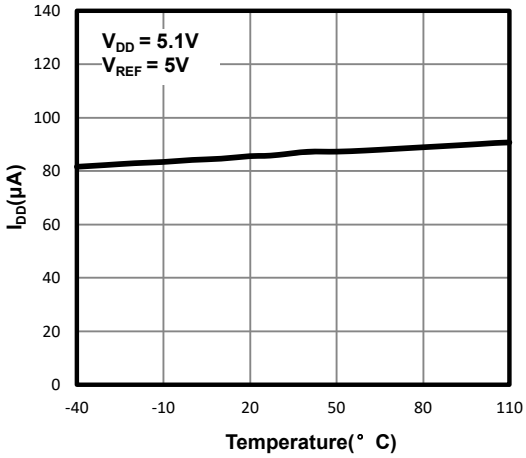


Figure 21. Power-Supply Current vs. Temperature(TPC116S1)

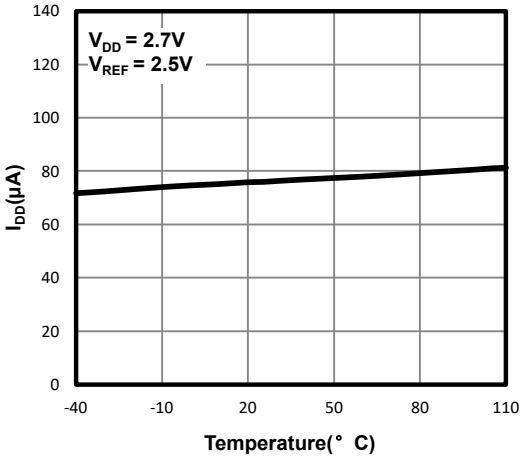


Figure 22. Power-Supply Current vs. Temperature(TPC116S1)

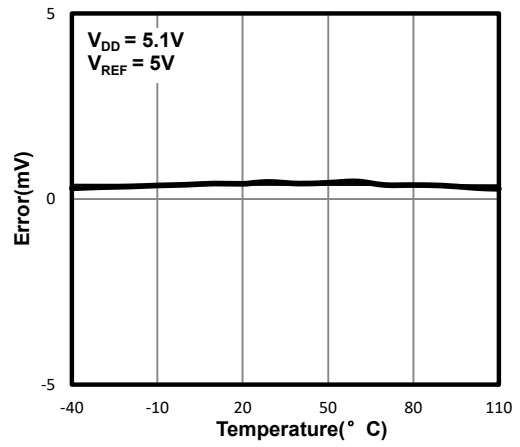


Figure 23. Zero-Scale Error vs. Temperature(TPC116S1)

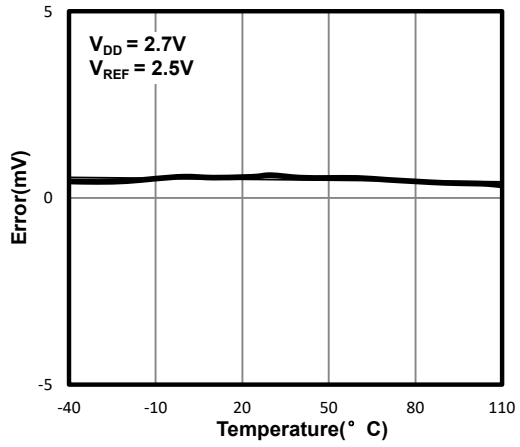


Figure 24. Zero-Scale Error vs. Temperature(TPC116S1)

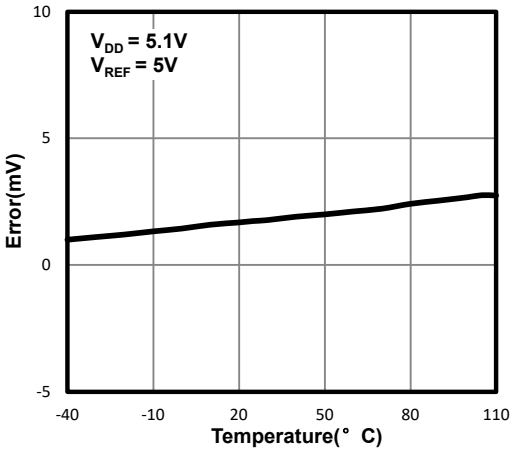


Figure 25. Full-Scale Error vs. Temperature(TPC116S1)

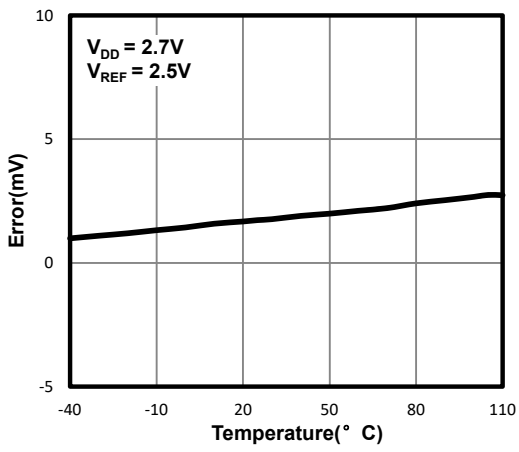


Figure 26. Full-Scale Error vs. Temperature(TPC116S1)

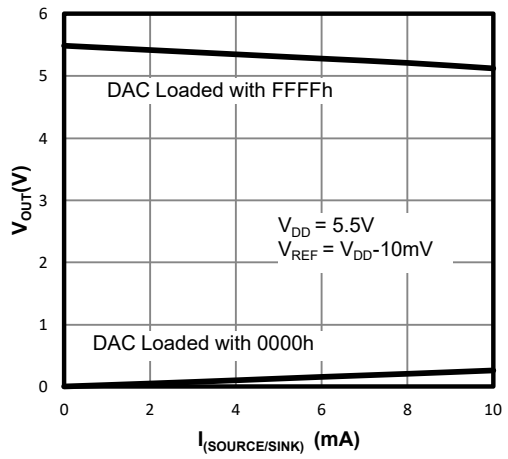


Figure 27. Source and Sink Current Capability(TPC116S1)

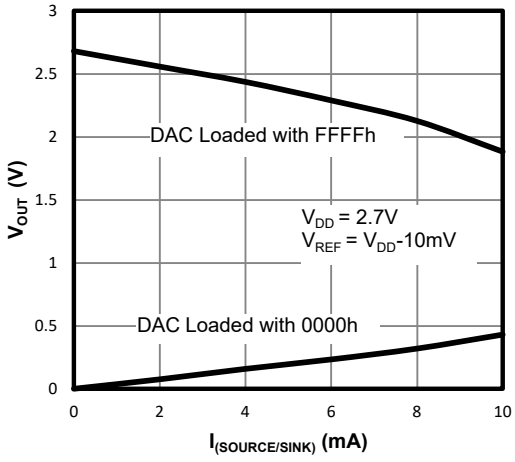


Figure 28. Source and Sink Current Capability(TPC116S1)

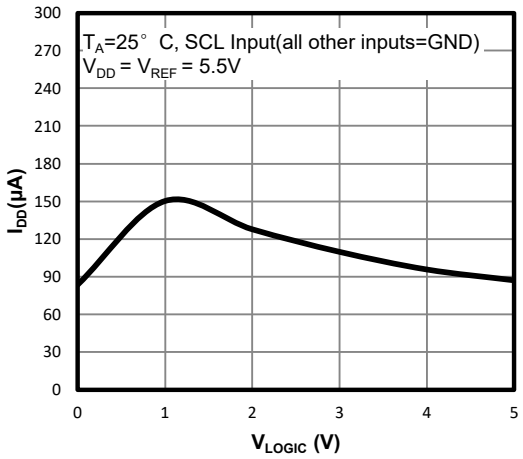


Figure 29. Supply Current vs. Logic Input Voltage(TPC116S1)

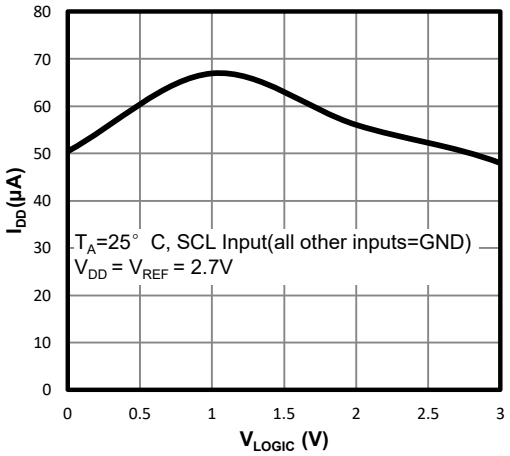


Figure 30. Supply Current vs. Logic Input Voltage(TPC116S1)

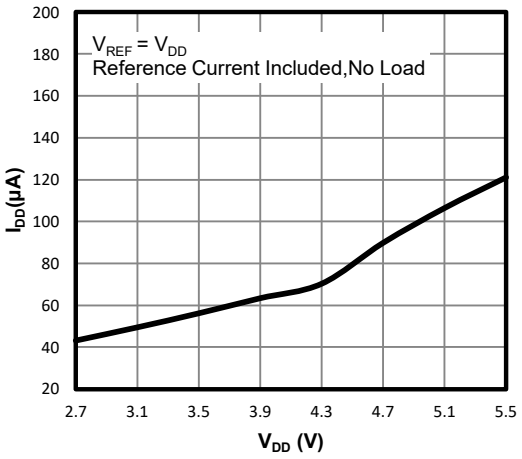


Figure 31. Supply Current vs. Supply Voltage(TPC116S1)

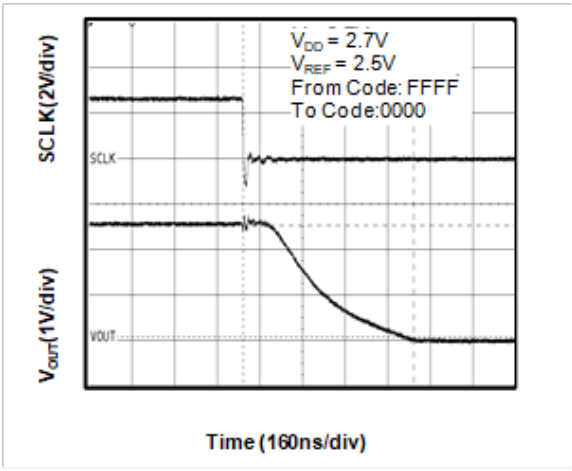


Figure 32. Full-Scale Settling Time(2.7V Falling Edge)

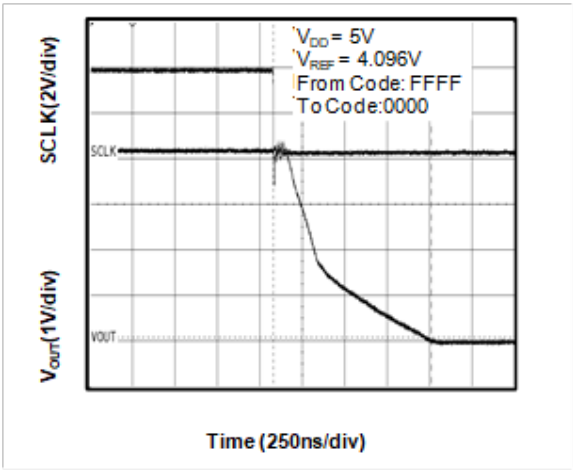


Figure 33. Full-Scale Settling Time(5V Falling Edge)

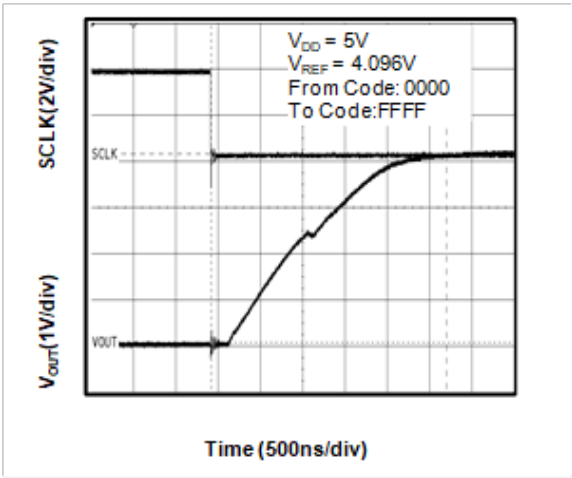


Figure 34. Full-Scale Settling Time(5V Rising Edge)

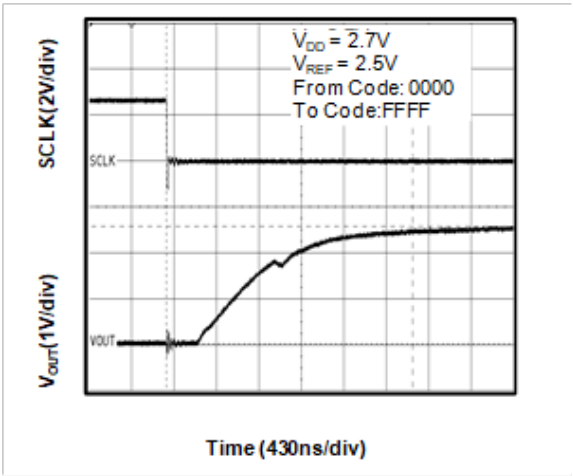


Figure 35. Full-Scale Settling Time(2.7V Rising Edge)

Detailed Description

Overview

The TPC116S1/ TPC114S1/TPC112S1 are pin-compatible and software-compatible 12-bit, 14-bit and 16-bit DACs. The TPC116S1/ TPC114S1/TPC112S1 are single-channel, low-power, high-reference input resistance, and buffered voltage-output DACs. The TPC116S1/ TPC114S1/TPC112S1 minimize the digital noise feedthrough from their inputs to their outputs by powering down the SCLK and DIN input buffers after completion of each data frame. The data frames are 16-bit for the TPC114S1/TPC112S1 and 24-bit for the TPC116S1. On power-up, the TPC116S1/ TPC114S1/TPC112S1 reset the DAC output to zero, providing additional safety for applications that drive valves or other transducers which need to be off on power-up. The TPC116S1/ TPC114S1/TPC112S1 contain a segmented resistor string-type DAC, a serial-in/parallel-out shift register, a DAC register, power-on-reset (POR) circuit, and control logic. On the falling edge of the clock (SCLK) pulse, the serial input (DIN) data is shifted into the device, MSB first.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0 V to VDD. It is capable of driving a load of 2 kW in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics. The slew rate is 1.8 V/ms with a full-scale setting time of 8 ms with the output unloaded.

The inverting input of the output amplifier is brought out to the VFB pin. This configuration allows for better accuracy in critical applications by tying the VFB point and the amplifier output together directly at the load. Other signal conditioning circuitry may also be connected between these points for specific applications.

DAC Reference (REF)

The external reference input features a typical input impedance of 333 kΩ and accepts an input voltage from +2 V to VDD. Connect an external voltage supply between REF and GND to apply an external reference.

Serial Interface

The TPC116S1/ TPC114S1/TPC112S1 3-wire serial interface is compatible with MICROWIRE, SPI, QSPI, and DSP. The interface provides three inputs: SCLK, $\overline{\text{SYNC}}$, and DIN. The chip-select input ($\overline{\text{SYNC}}$) frames the serial data loading at DIN. Following a chip-select input high-to-low transition, the data is shifted synchronously and latched into the input register on each falling edge of the serial-clock input (SCLK). Each serial word is 16-bit for the TPC114S1/ TPC112S1 and 24-bit for the TPC116S1. The first 2 bits are the control bits followed by 12/14 data bits (MSB first) for the TPC114S1/ TPC112S1 and 22 data bits (MSB first) for the TPC116S1 as shown in Tables 1 and 2. The serial input register transfers its contents to the input registers after loading 16/24 bits of data and updates the DAC output immediately after the data is received on the 16-/24-bit falling edge of the clock. To initiate a new data transfer, drive $\overline{\text{SYNC}}$ high and keep SYNC high for a minimum of 20 ns before the next write sequence. The SCLK can be either high or low between $\overline{\text{SYNC}}$ write pulses. Figures 1 and 2 show the timing diagram for the complete 3-wire serial interface transmission. The TPC116S1 DAC code is a unipolar binary with $\text{VOUT} = (\text{code}/16,384) \times \text{VREF}$. The TPC112S1 DAC code is a unipolar binary with $\text{VOUT} = (\text{code}/4096) \times \text{VREF}$.

Table 3. Operating Mode Truth Table (TPC112S1)

16-BIT WORD																Function
MSB		CONTROL BITS		DATA BITS												
				LSB												
D15	D14	PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
X	X	0	0	X	X	X	X	X	X	X	X	X	X	X	X	Normal operation
X	X	-	-	X	X	X	X	X	X	X	X	X	X	X	X	Power-down modes
X	X	0	1	X	X	X	X	X	X	X	X	X	X	X	X	Output typically 1 kΩ to GND
X	X	1	0	X	X	X	X	X	X	X	X	X	X	X	X	Output typically 100 kW to GND
X	X	1	6.51	X	X	X	X	X	X	X	X	X	X	X	X	High-Z

Table 4. Operating Mode Truth Table (TPC114S1)

16-BIT WORD																Function
CONTROL BITS		DATA BITS														
MSB		LSB														
PD1	PD0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Normal operation
-	-	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Power-down modes
0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Output typically 1kΩ to GND
1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Output typically 100kW to GND
1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	High-Z

Table 5. Operating Mode Truth Table (TPC116S1)

24-BIT WORD																Function
CONTROL BITS		DATA BITS														
MSB		LSB														
D23	D22	D21	D20	D19	D18	PD1	PD0	D15	D14	D13	D12	D11	D10	D9	D0~D8	
X	X	X	X	X	X	0	0	X	X	X	X	X	X	X	X	Normal operation
X	X	X	X	X	X	-	-	X	X	X	X	X	X	X	X	Power-down modes
X	X	X	X	X	X	0	1	X	X	X	X	X	X	X	X	Output typically 1kΩ to GND
X	X	X	X	X	X	1	0	X	X	X	X	X	X	X	X	Output typically 100kW to GND

X	X	X	X	X	X	1	1	X	X	X	X	X	X	X	X	High-Z

Power-on Reset

The TPC116S1/ TPC114S1/TPC112S1 contains a power-on-reset circuit that controls the output voltage during power up. On power up, the DAC registers are filled with zeros and the output voltages are 0V; they remain that way until a valid write sequence is made to the DAC. The power-on reset is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

Power-down Modes

The TPC116S1/ TPC114S1/TPC112S1 supports four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. Table 1, 2, and 3 show how the state of the bits corresponds to the mode of operation of the device. When both bits are set to '0', the device works normally with its typical current consumption of 90 μA at 5 V. However, for the three power-down modes, the supply current falls to 400 nA at 5 V (250 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This configuration has the advantage that the output impedance of the device is known while it is in power-down mode. There are three different options. The output is connected internally to GND through a 1 kW resistor, a 100 kW resistor, or it is left open-circuited (High-Z). The output stage is illustrated in Figure 4.

All analog circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 μs for VDD = 5V, and 5 μs for VDD = 3V. See the Typical Characteristics for more information.

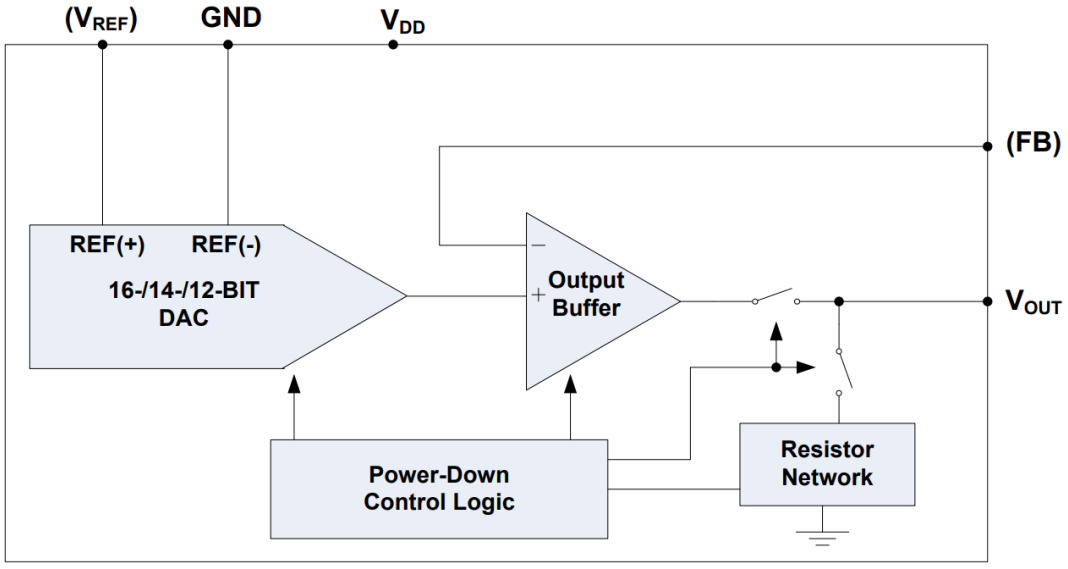
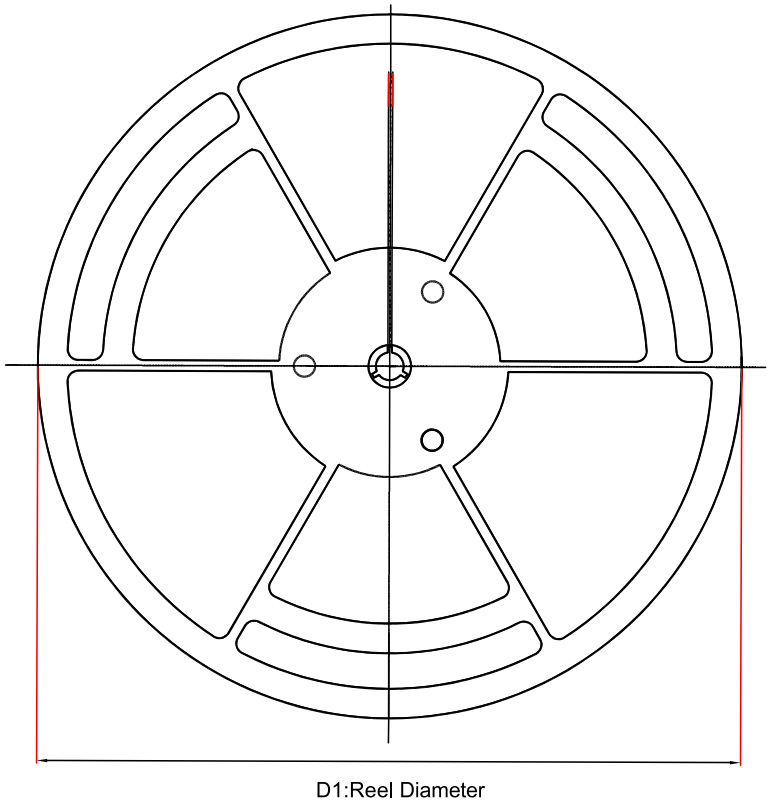
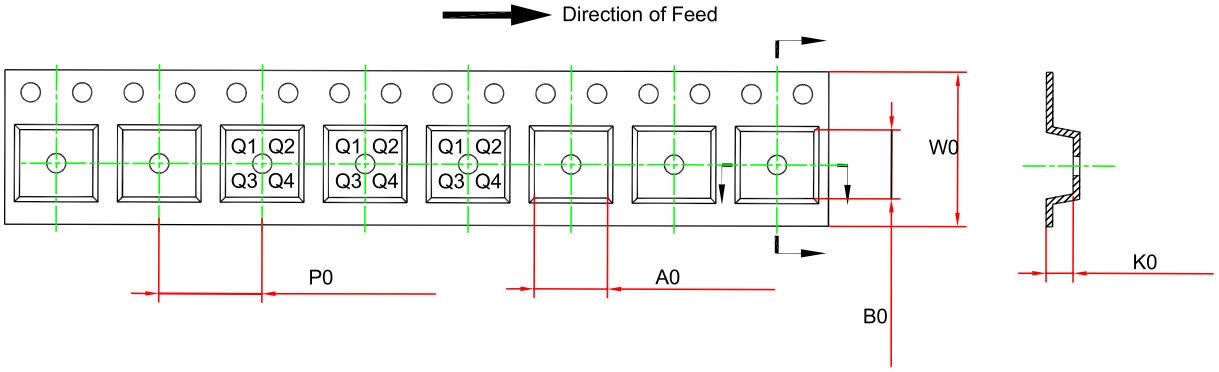


Figure 36. Output Stage During Power-Down

Tape and Reel Information



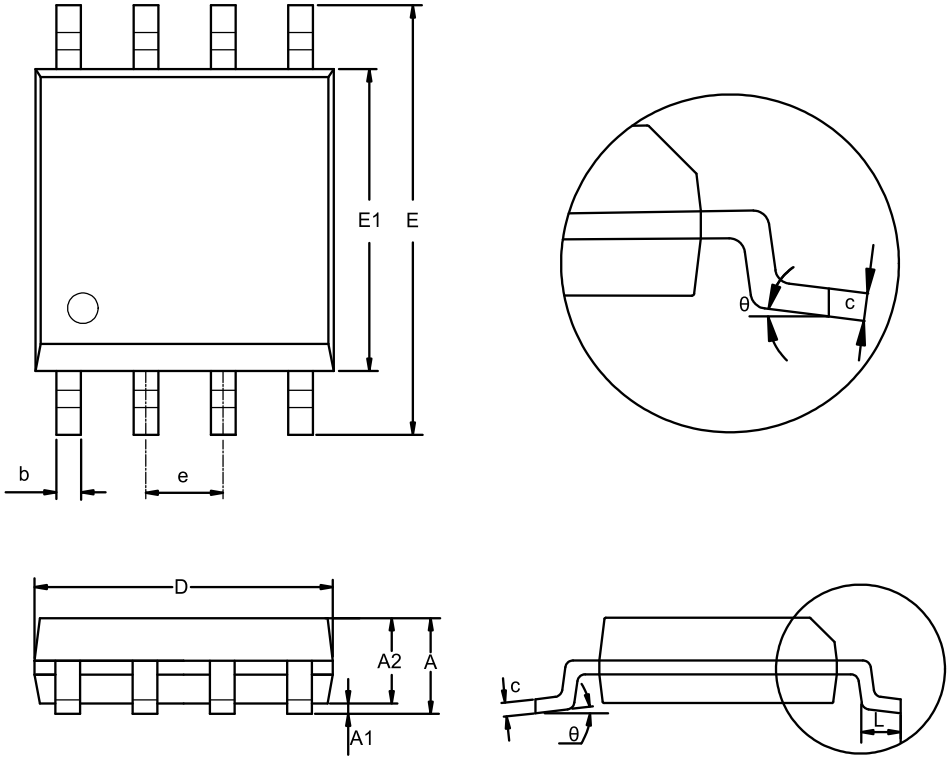


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC112S1-VR	MSOP8	330	17.6	5.3	3.3	1.6	8	12	Q1
TPC114S1-VR	MSOP8	330	17.6	5.3	3.3	1.6	8	12	Q1
TPC116S1-VR	MSOP8	330	17.6	5.3	3.3	1.6	8	12	Q1

Package Outline Dimensions

MSOP8

Package Outline Dimensions VS1(MSOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC112S1-VR	−40 to 125°C	MSOP8	C112S1	3	Tape and Reel, 3,000	Green
TPC114S1-VR	−40 to 125°C	MSOP8	C114S1	3	Tape and Reel, 3,000	Green
TPC116S1-VR	−40 to 125°C	MSOP8	C116S1	3	Tape and Reel, 3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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