TPS54627 4.5-V to 18-V Input, 6-A Synchronous Step-Down Converter

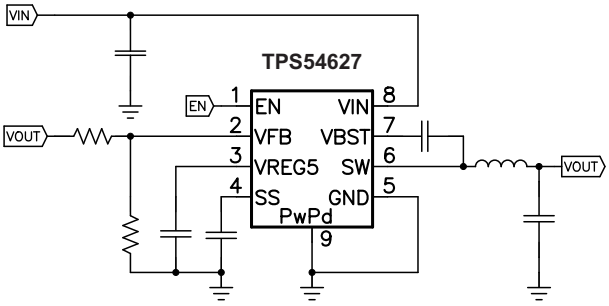
1 Features

- D-CAP2™ Mode Enables Fast Transient Response
- Low-Output Ripple and Allows Ceramic Output Capacitor
- Wide V_{IN} Input-Voltage Range: 4.5 V to 18 V
- Output-Voltage Range: 0.76 V to 5.5 V
- Highly Efficient Integrated FETs Optimized for Lower Duty-Cycle Applications
  - 36 mΩ (High-Side) and 28 mΩ (Low-Side)
- High Efficiency, Less Than 10 μA at Shutdown
- High Initial Bandgap-Reference Accuracy
- Adjustable Soft Start
- Prebiased Soft Start
- 650-kHz Switching Frequency
- Cycle-by-Cycle Overcurrent Limit

2 Applications

- Wide Range of Applications for Low-Voltage System
  - Digital-TV Power Supply
  - High-Definition Blu-ray Disc™ Players
  - Networking Home Terminals
  - Digital Set-Top Boxes (STB)

Simplified Schematic



3 Description

The TPS54627 device is an adaptive on-time D-CAP2 mode synchronous-buck converter. The TPS54627 enables system designers to complete the suite of various end-equipment power-bus regulators with a cost-effective, low-component count, low-standby current solution.

The main control loop for the TPS54627 uses the D-CAP2 mode control that provides a fast transient response with no external compensation components. The TPS54627 also has a proprietary circuit that enables the device to adopt to both low equivalent-series-resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

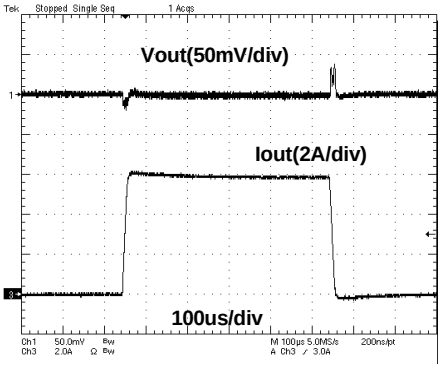
The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.76 V and 5.5 V. The device also features an adjustable soft-start time. The TPS54627 is available in the 8-pin SO PowerPAD package, and designed to operate from –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54627	SO PowerPAD (8)	4.89 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Load Transient Response



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2013) to Revision B **Page**

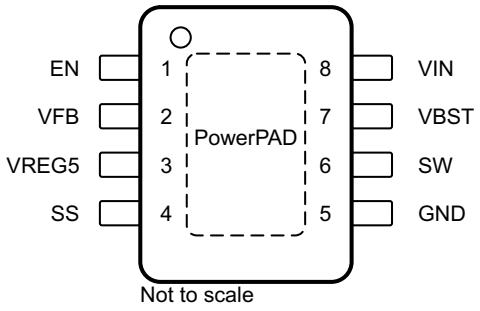
- Added *Device Information* table, *Pin Configuration and Functions* section, *Specifications* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the data sheet ... 1

Changes from Original (April 2013) to Revision A **Page**

- Deleted Deleted Feature: Auto-Skip Eco-mode™ for High Efficiency at Light Load ... 1

5 Pin Configuration and Functions

DDA Package
8-Pin SO PowerPAD
(Top View)



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	1	I	Enable input control. EN is active high and must be pulled up to enable the device.
GND	5	—	Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
SS	4	I	Soft-start control. An external capacitor must be connected to GND.
SW	6	O	Switch node connection between high-side NFET and low-side NFET.
VBST	7	O	Supply input for the high-side FET gate drive circuit. Connect 0.1-µF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
VFB	2	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
VIN	8	I	Input voltage supply pin.
VREG5	3	O	5.5-V power supply output. A capacitor (typical 1 µF) must be connected to GND. VREG5 is not active when EN is low.
—	PowerPAD	—	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN, EN	–0.3	20	V
	VBST	–0.3	26	
	VBST (10-ns transient)	–0.3	28	
	VBST (vs SW)	–0.3	6.5	
	VFB, SS	–0.3	6.5	
	SW	–2	20	
	SW (10-ns transient)	–3	22	
Output voltage	VREG5	–0.3	6.5	V
	GND	–0.3	0.3	
Voltage from GND to thermal pad, V_{DIFF}		–0.2	0.2	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range, (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage		4.5	18	V
	Input voltage	VBST	–0.1	24	V
		VBST (10-ns transient)	–0.1	27	
		VBST (vs SW)	–0.1	6	
		SS	–0.1	5.7	
		EN	–0.1	18	
		VFB	–0.1	5.5	
		SW	–1.8	18	
		SW (10-ns transient)	–3	21	
		GND	–0.1	0.1	
V_O	Output voltage	VREG5	–0.1	5.7	V
I_O	Output current	I_{VREG5}	0	5	mA
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	150	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS54627 DDA (SO PowerPAD) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over operating free-air temperature range, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5 V, V_{FB} = 0.8 V		950	1400	µA
I_{VINSDN}	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V		3	10	µA
LOGIC THRESHOLD						
V_{EN}	EN high-level input voltage	EN	1.6			V
	EN low-level input voltage	EN			0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	200	400	800	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V, continuous mode operation	757	765	773	mV
		T_A = –40 to 85°C, V_O = 1.05 V, continuous mode operation(1)	751	765	779	mV
I_{VFB}	V_{FB} input current	V_{FB} = 0.8 V, T_A = 25°C		0	±0.15	µA
V_{REG5} OUTPUT						
V_{VREG5}	V_{REG5} output voltage	T_A = 25°C, 6 V < V_{IN} < 18 V, 0 < I_{VREG5} < 5 mA	5.2	5.5	5.7	V
I_{VREG5}	Output current	V_{IN} = 6 V, V_{REG5} = 4 V, T_A = 25°C	20			mA
V_{OUT} DISCHARGE						
R_{DISCHG}	V_{OUT} discharge resistance	EN = 0 V, SW = 0.5 V, T_A = 25°C		500	800	Ω
MOSFET						
$R_{DS(on)}$	High-side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V		36		mΩ
	Low-side switch resistance	T_A = 25°C		28		mΩ
CURRENT LIMIT						
I_{OCL}	Current limit	L out = 1.5 µH(1)	6.7	7.3	8.9	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature (1)		165		°C
		Hysteresis (1)		35		
ON-TIME TIMER CONTROL						
t_{ON}	ON time	V_{IN} = 12 V, V_O = 1.05 V		150		ns
$t_{OFF(MIN)}$	Minimum OFF time	T_A = 25°C, V_{FB} = 0.7 V		260	310	ns
SOFT START						
I_{SS}	SS charge current	V_{SS} = 1 V	4.2	6	7.8	µA
	SS discharge current	V_{SS} = 0.5 V	1.5	3.3		mA
HICCUP AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP threshold	OVP Detect (L > H)		125%		
V_{HICCUP}	Output Hiccup threshold	Hiccup detect (H > L)		65%		
$T_{HICCUPDELAY}$	Output Hiccup delay	To hiccup state		250		µs
$T_{HICCUPENDELAY}$	Output Hiccup Enable delay	Relative to soft-start time		×1.7		
UVLO						
UVLO	UVLO threshold	Wake-up V_{REG5} voltage	3.45	3.75	4.05	V
		Hysteresis V_{REG5} voltage	0.13	0.32	0.48	

(1) Not production tested.

6.6 Typical Characteristics

V_{IN} = 12 V, T_A = 25°C (unless otherwise noted).

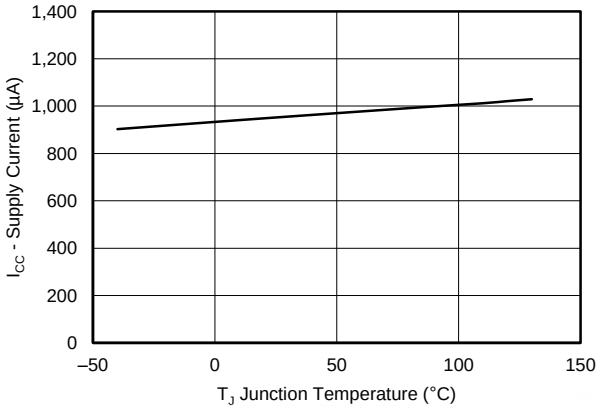


Figure 1. Supply Current vs Junction Temperature

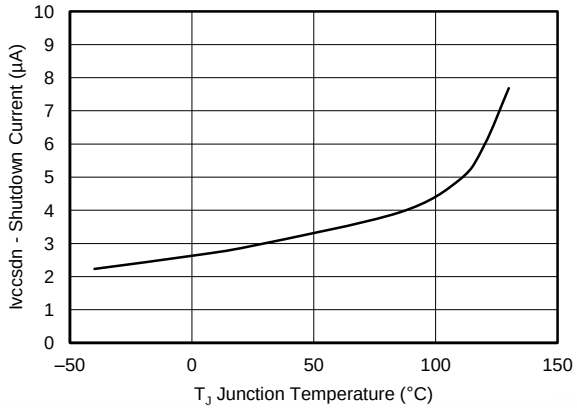


Figure 2. Shutdown Current vs Junction Temperature

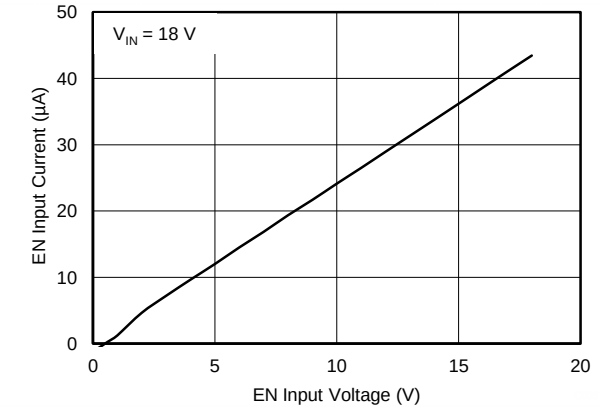


Figure 3. EN Input Current vs EN Input Voltage

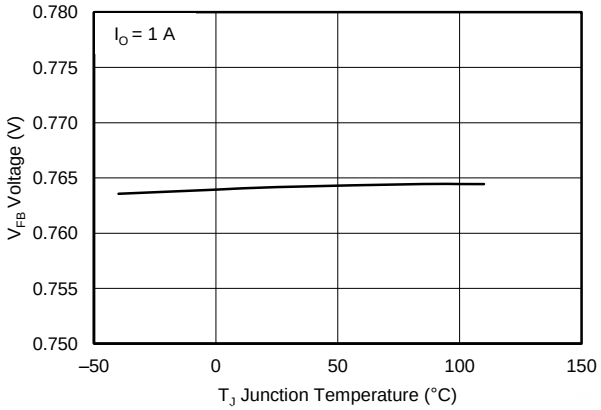


Figure 4. VFB Voltage vs Junction Temperature

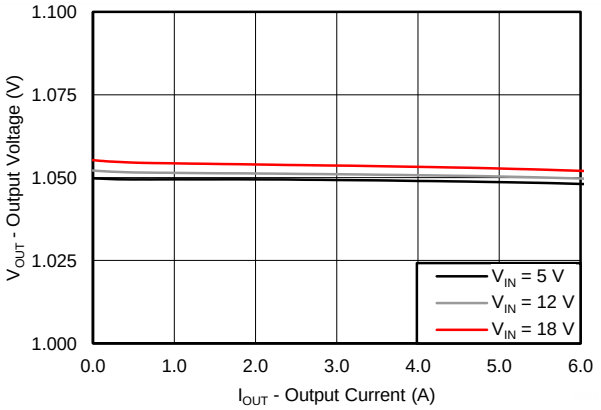


Figure 5. 1.05-V Output Voltage vs Output Current

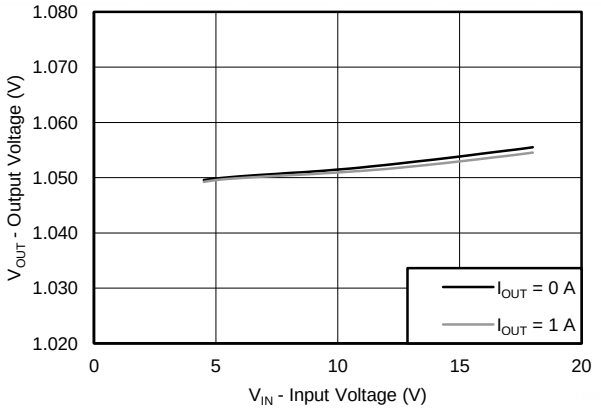


Figure 6. 1.05-V Output Voltage vs Input Voltage

Typical Characteristics (continued)

V_{IN} = 12 V, T_A = 25°C (unless otherwise noted).

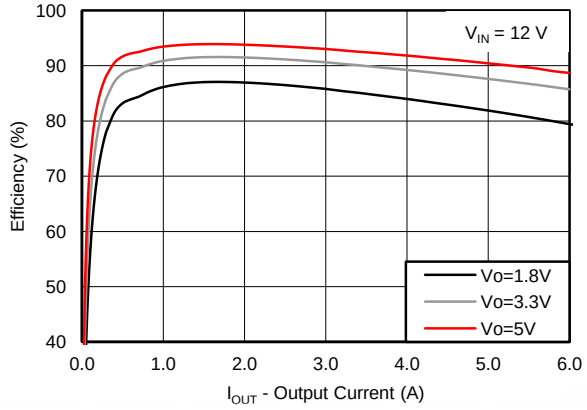


Figure 7. Efficiency vs Output Current

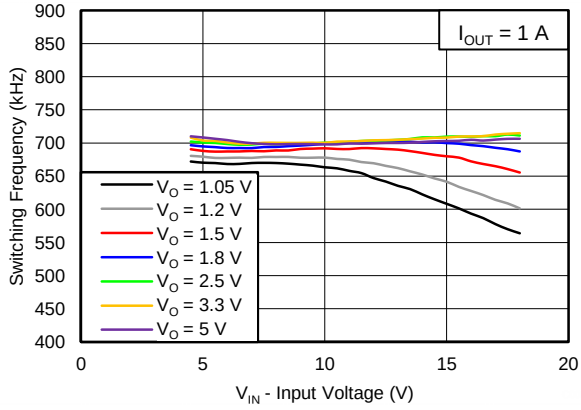


Figure 8. Switching Frequency vs Input Voltage

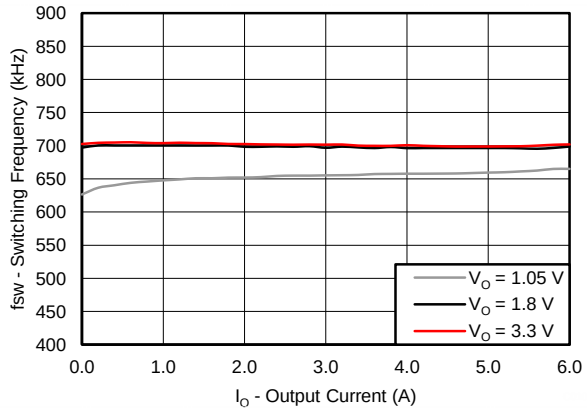


Figure 9. Switching Frequency vs Output Current

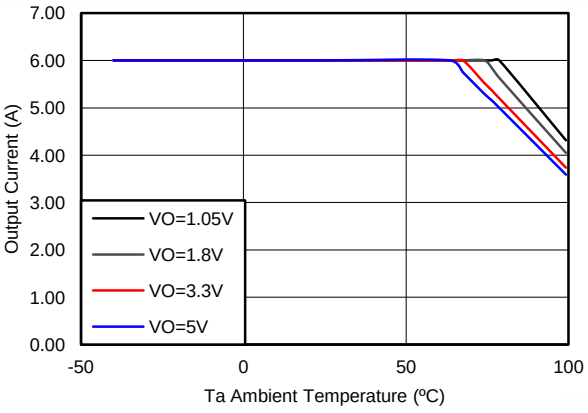


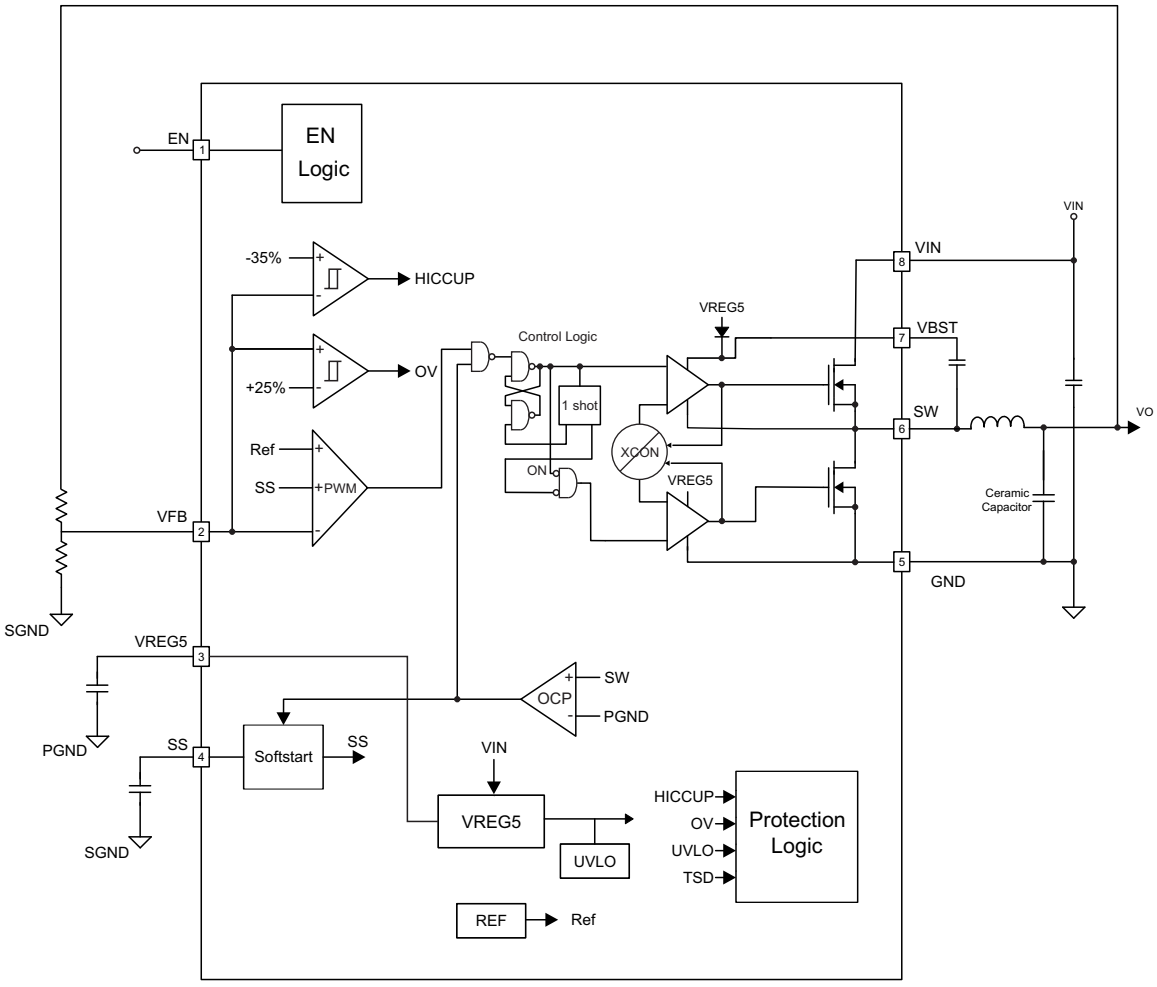
Figure 10. Output Current vs Ambient Temperature

7 Detailed Description

7.1 Overview

The TPS54627 is a 6-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2 mode control. The fast transient response of D-CAP2 control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low-ESR output capacitors including ceramic and special polymer types.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft Start and Prebiased Soft Start

The soft-start function is adjustable. When the EN pin becomes high, 6-µA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start-up. The equation for the slow start time is shown in Equation 1. VFB voltage is 0.765 V and SS pin source current is 6 µA.

$$t_{SS}(ms) = \frac{C6(nF) \times V_{FB} \times 1.1}{I_{SS}(\mu A)} = \frac{C6(nF) \times 0.765 \times 1.1}{6} \quad (1)$$

The TPS54627 contains a unique circuit to prevent current from being pulled from the output during start-up if the output is prebiased. When the soft start commands a voltage higher than the prebias level—internal soft start becomes greater than feedback voltage (V_{FB})—the controller slowly activates synchronous rectification by starting the first low-side FET gate driver, which pulses with a narrow on time. The controller then increments that on time on a cycle-by-cycle basis until it coincides with the time dictated by (1 – D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the prebias output, ensures that the out voltage starts and ramps up smoothly into regulation, and provides the control loop time to transition from prebiased start-up to normal mode operation.

7.3.2 Output Discharge Control

TPS54627 discharges the output when EN is low or if the controller is turned off by the UVLO protection. The internal low-side MOSFET is not turned on for the output discharge operation to avoid the possibility of causing negative voltage at the output.

7.3.3 Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between SW and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_O, the on time, and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current (I_O). The TPS54627 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch ON until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on time is set to a fixed value and the current is monitored in the same manner. If the overcurrent condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of overcurrent protection. The peak current is the average load current plus one half of the peak-to-peak inductor current. The valley current is the average load current minus one half of the peak-to-peak inductor current. Because the valley current is used to detect the overcurrent threshold, the load current is higher than the overcurrent threshold. Also, when the current is being limited, the output voltage tends to fall. When the VFB voltage becomes lower than 65% of the target voltage, the UVP comparator detects it. If the undervoltage condition persists for 250 µs, the device shuts down and restarts in hiccup mode after 7 times the SS period. When the overcurrent condition is removed, the output voltage returns to the regulated value. This protection is non-latching.

7.3.4 Overvoltage Protection

TPS54627 detects overvoltage and undervoltage conditions by monitoring the feedback voltage (V_{FB}). This function is enabled after approximately 1.7 times the soft-start time. When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and both the high-side MOSFET driver and the low-side MOSFET driver turn off. This function is a non-latching operation.

Feature Description (continued)

7.3.5 UVLO Protection

Undervoltage lockout protection (UVLO) monitors the voltage of the VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the TPS54627 is shut off. This protection is non-latching.

7.3.6 Thermal Shutdown

TPS54627 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latching protection.

7.4 Device Functional Modes

7.4.1 PWM Operation

The main control loop of the TPS54627 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 mode control. D-CAP2 mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one shot is set by the converter input voltage (V_{IN}) and the output voltage (V_O) to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 mode control.

7.4.2 PWM Frequency and Adaptive On-Time Control

TPS54627 uses an adaptive on-time control scheme and does not have a dedicated onboard oscillator. The TPS54627 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on time is inversely proportional to the input voltage and proportional to the output voltage; therefore, when the duty ratio is V_O / V_{IN}, the frequency is constant.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54627 is designed to provide up to 6-A output current from an input voltage source ranging from 4.5 V to 18 V. The output voltage ins configurable from 0.76 V to 5.5 V. The TPS54627 is designed to provide up to a 6-A output current from an input voltage source ranging from 4.5 V to 18 V. The output voltage is configurable from 0.76 V to 5.5 V. A simplified design procedure for a 1.05-V output is shown below.

8.2 Typical Application

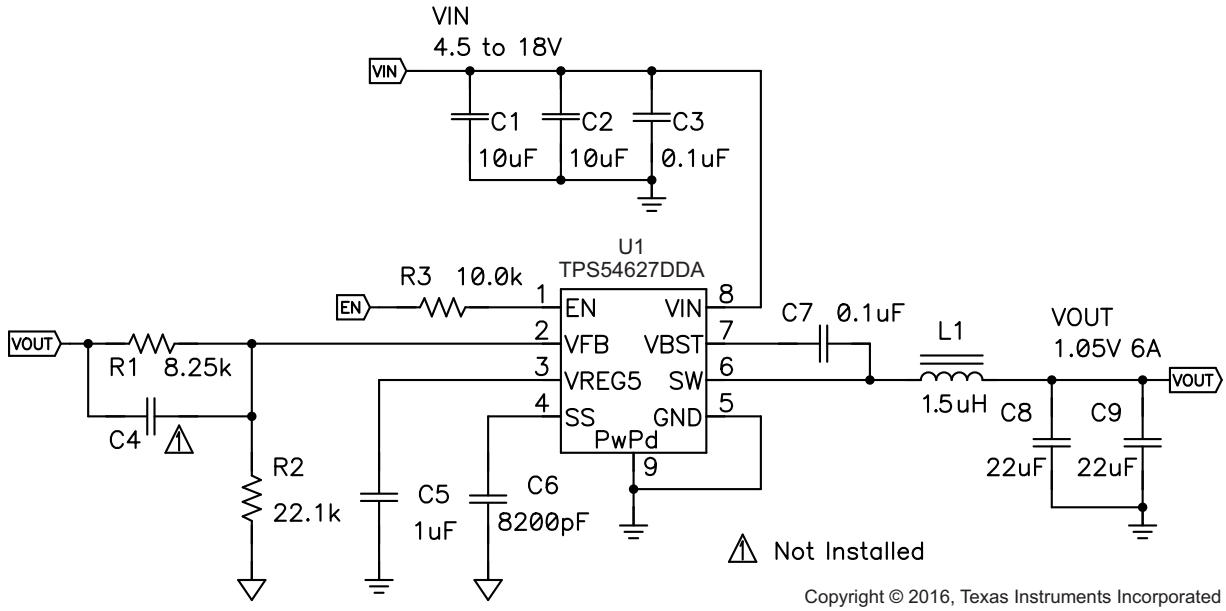


Figure 11. Simplified Application Schematic

8.2.1 Design Requirements

To begin the design process, the user must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends using 1% tolerance or better divider resistors. Start by using Equation 2 to calculate V_O.

To improve efficiency at light loads consider using larger value resistors, high resistance is more susceptible to noise, and the voltage errors from the VFB input current are more noticeable.

Typical Application (continued)

$$V_O = 0.765 \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

8.2.2.2 Output Filter Selection

The output filter used with the TPS54627 is an LC circuit. This LC filter has double pole at Equation 3.

$$F_P = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54627. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. Table 1 provides recommended inductor and capacitor values to meet this requirement.

Table 1. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)(1)			L1 (µH)			C8 + C9 (µF)	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX
1	6.81	22.1	5	150	220	1	1.5	4.7	22	68
1.05	8.25	22.1	5	150	220	1	1.5	4.7	22	68
1.2	12.7	22.1	5		100	1	1.5	4.7	22	68
1.5	21.5	22.1	5		68	1	1.5	4.7	22	68
1.8	30.1	22.1	5		22	1.2	1.5	4.7	22	68
2.5	49.9	22.1	5		22	1.5	2.2	4.7	22	68
3.3	73.2	22.1	2		22	1.8	2.2	4.7	22	68
5	124	22.1	2		22	2.2	3.3	4.7	22	68

(1) Optional

Because the DC gain is dependent on the output voltage, the required inductor value increases as the output voltage increases. Additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1. The feed forward capacitor is most effective for output voltages at or above 1.8 V.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5, and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 650 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

$$I_{IPP} = \frac{V_O}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_O}{L_O \times f_{SW}} \quad (4)$$

$$I_{Ipeak} = I_O + \frac{I_{IPP}}{2} \quad (5)$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} \times I_{IPP}^2} \quad (6)$$

For this design example, the calculated peak current is 6.51 A and the calculated RMS current is 6.01 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54627 is intended for use with ceramic or other low ESR capacitors. TI recommends the values range from 22 µF to 68 µF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{Co(RMS)} = \frac{V_O \times (V_{IN} - V_O)}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.284 A and each output capacitor is rated for 4 A.

8.2.2.3 Input Capacitor Selection

The TPS54627 requires an input decoupling capacitor, and a bulk capacitor may be required depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from VIN to ground is optional to provide additional high-frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST and SW pins for proper operation. TI recommends using a ceramic capacitor.

8.2.2.5 VREG5 Capacitor Selection

A 1-µF ceramic capacitor must be connected between the VREG5 and GND pins for proper operation. TI recommends using a ceramic capacitor.

8.2.3 Application Curves

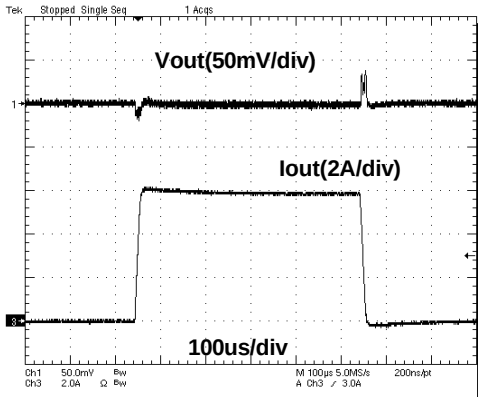


Figure 12. 1.05-V Load Transient Response

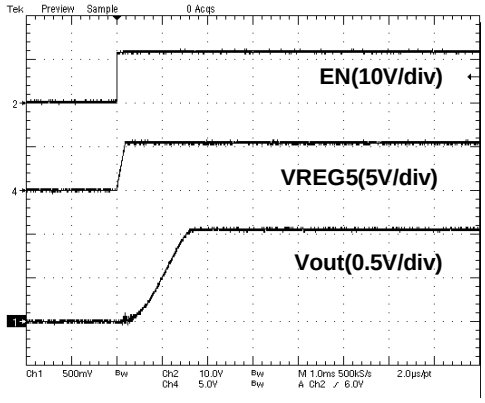
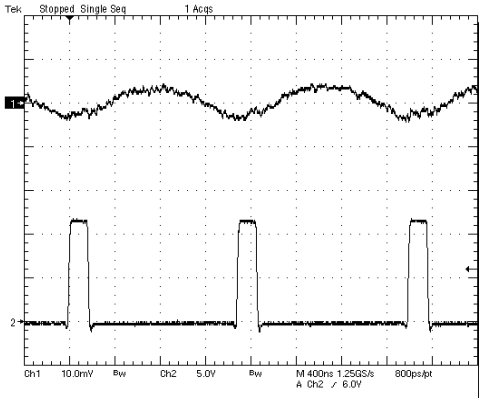
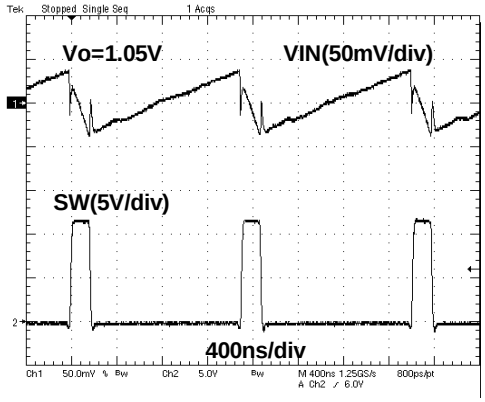


Figure 13. Start-Up Waveform



I_O = 6 A

Figure 14. Voltage Ripple at Output



I_O = 6 A

Figure 15. Voltage Ripple at Input

9 Power Supply Recommendations

The input voltage range is from 4.5 V to 18 V. The input power supply and the input capacitors must be placed as close to the device as possible to minimize the impedance of the power-supply line.

10 Layout

10.1 Layout Guidelines

The grounding and PCB circuit layout considerations are.

- The TPS54627 can supply large load currents up to 6 A, so heat dissipation may be a concern. The top-side area adjacent to the TPS54627 must be filled with ground as much as possible to dissipate heat.
- The bottom side area directly below the IC must a dedicated ground area and must be directly connected to the thermal pad of the device using vias as shown. The ground area must be as large as practical. Additional internal layers can be dedicated as ground planes and connected to the vias as well.
- Keep the input switching current loop as small as possible.
- Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections must be brought from the output to the feedback pin of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.
- Exposed thermal pad of device must be connected to PGND with solder.
- VREG5 capacitor must be placed near the device, and connected PGND.
- Output capacitor must be connected to a broad pattern of the PGND.
- Voltage feedback loop must be as short as possible, and preferably with ground shield.
- The lower resistor of the voltage divider, which is connected to the VFB pin, must be tied to SGND.
- Providing sufficient via is required for VIN, SW, and PGND connections.
- PCB pattern for VIN, SW, and PGND must be as broad as possible.
- VIN capacitor must be placed as near to the device as possible.

10.2 Layout Example

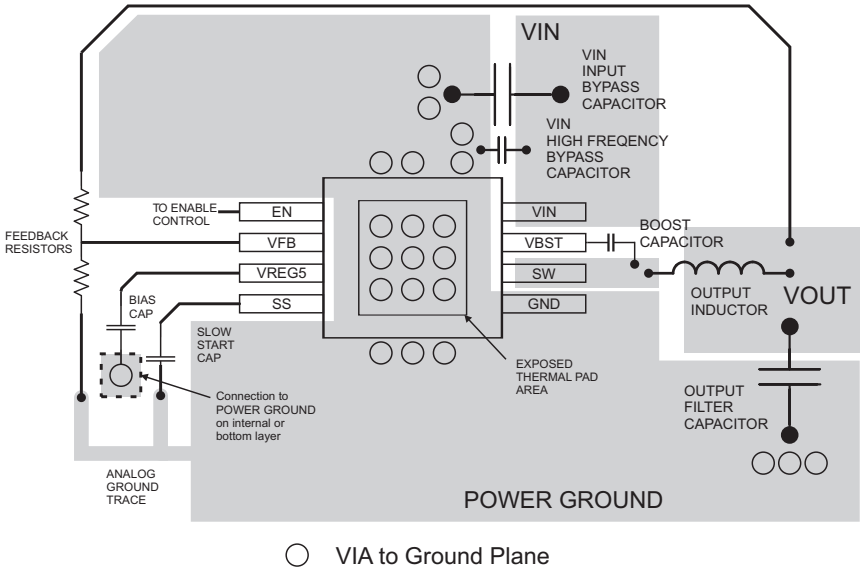


Figure 16. PCB Layout

10.3 Thermal Considerations

This 8-pin SO-PowerPAD package incorporates an exposed thermal pad that is designed to be directly connected to an external heat sink. The thermal pad must be soldered directly to the printed-circuit board (PCB). After soldering, the PCB can be used as a heat sink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, see *PowerPAD Thermally Enhanced Package* (SLMA002) and *PowerPAD Made Easy* (SLMA004).

The exposed thermal pad dimensions for this package are shown in Figure 17.

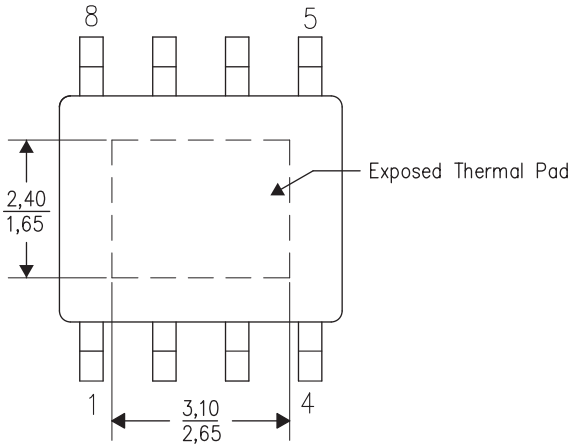


Figure 17. Thermal Pad Dimensions

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *TPS54627EVM-052, 6-A, Regulator Evaluation Module* (SLVU889)
- *PowerPAD Thermally Enhanced Package* (SLMA002)
- *PowerPAD Made Easy* (SLMA004)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54627DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-2-260C-1 YEAR	-40 to 125	54627	Samples
TPS54627DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-2-260C-1 YEAR	-40 to 125	54627	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

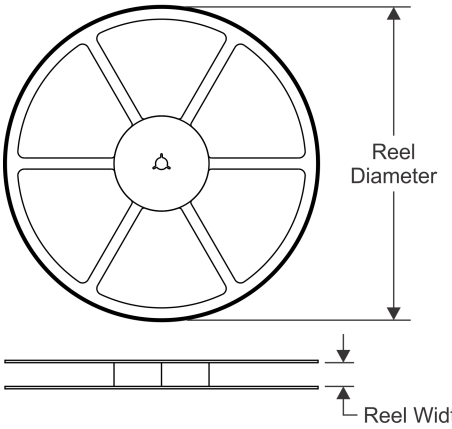
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

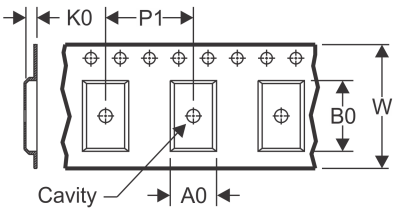
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

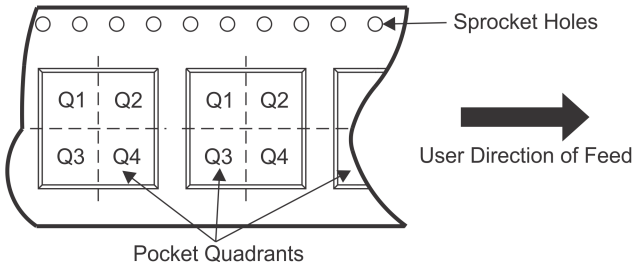


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

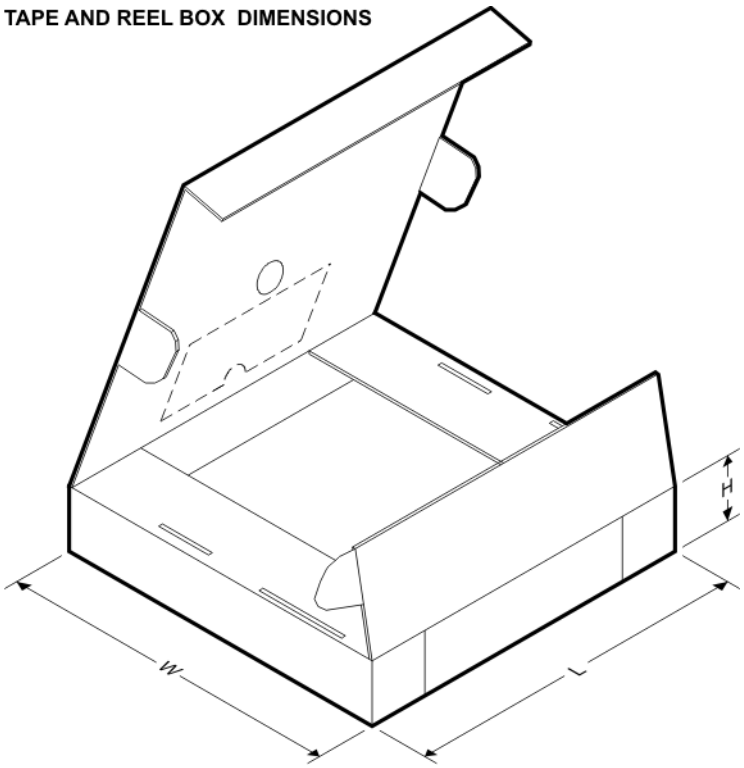
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54627DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

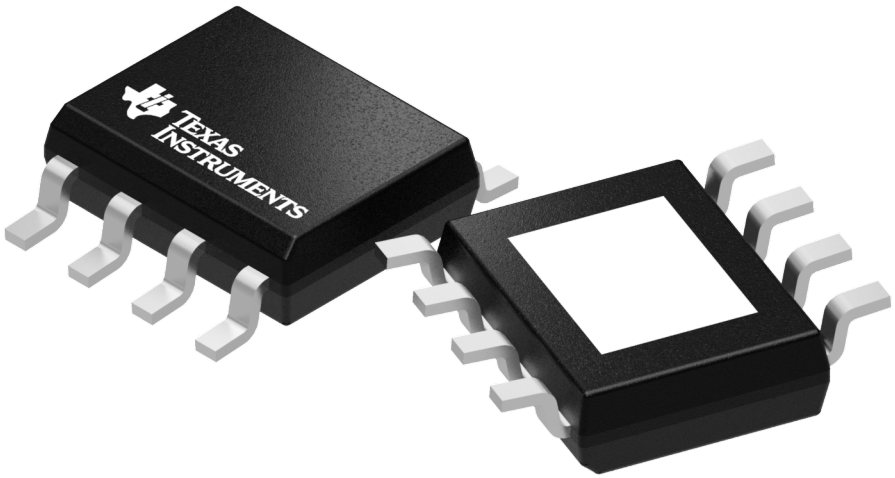


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54627DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

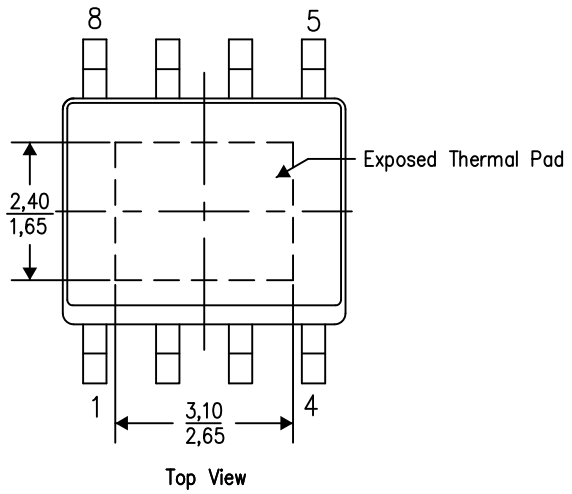
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



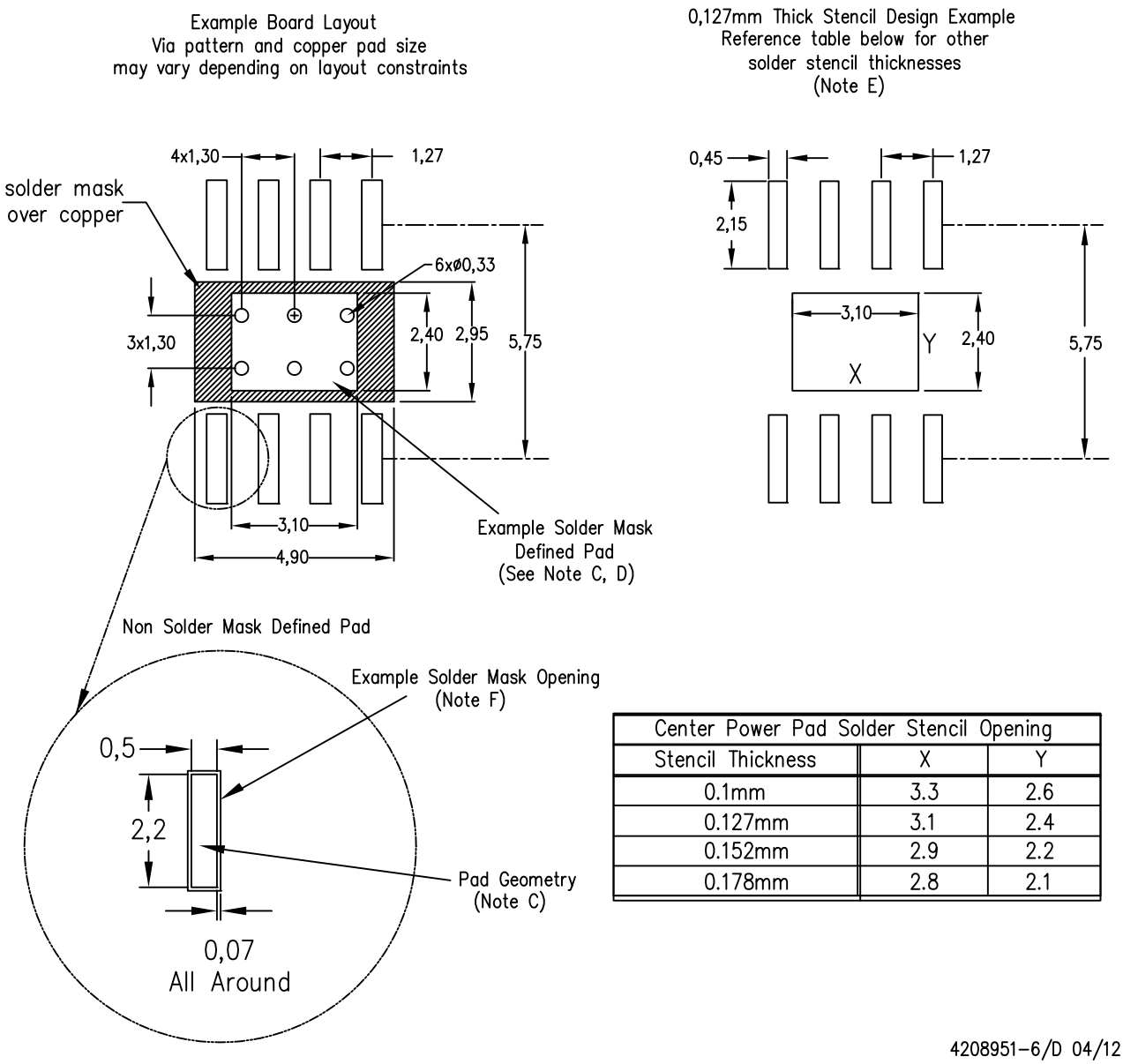
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

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