USX2064

USB 2.0 Hi-Speed 4-Port Hub Controller with Battery Charging

PRODUCT FEATURES

Datasheet

General Description

The SMSC 4-Port Hub is a low-power, OEM configurable, MTT (multi transaction translator) hub controller IC with 4 downstream ports for embedded USB solutions. The 4-port hub supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

General Features

- High-performance, low-power, small footprint hub controller IC with 4 downstream ports
- Fully compliant with the USB 2.0 Specification
- Enhanced OEM configuration options available through either a single serial I²C® EEPROM or SMBus slave port
- 36-pin (6x6 mm) QFN lead-free, RoHS compliant package

- MultiTRAK™ Technology
  - High-performance multi transaction translator which provides one transaction translator per port
- PortMap
  - Flexible port mapping and port disable sequencing
- PortSwap
  - Programmable USB differential-pair pin locations ease PCB design by aligning USB signal lines directly to connectors
- PHYBoost
  - Programmable USB signal drive strength for recovering signal integrity using 4-level driving strength resolution

Hardware Features

- Full power management with individual or ganged power control of each downstream port
- Integrated 1.8 V core regulator
- Fully integrated USB termination and pull-up/pull-down resistors
- Onboard 24 MHz crystal driver, ceramic resonator, or external 24 MHz clock input

OEM Selectable Features

- Customize the vendor ID, product ID, and device ID
- Select whether or not the hub is part of a compound device
- Configure the delay time for filtering the over-current sense inputs
- Select the presence of a permanently hardwired USB peripheral device on a port-by-port basis
- Indicate the maximum current that the 4-port hub consumes from the USB upstream port
- Indicate the maximum current required for the hub controller
- Supports self- and bus-powered operation
- Supports the USB Battery Charging specification Rev. 1.1 for Charging Downstream Ports (CDP)
- Customizable string descriptors up to 31 characters in length for:
  - Product String
  - Manufacturer String
  - Serial Number String

- Pin selectable options for default configuration
  - Downstream Ports as Disabled Ports
  - USB Differential Pair Pin location

Applications

- LCD monitors and TVs
- Multi-function USB peripherals
- PC mother boards
- Set-top boxes, DVD players, DVR/PVR
- Printers and scanners
- PC media drive bay
- Portable hub boxes
- Mobile PC docking
- Embedded systems

ORDER NUMBERS:

36-PIN QFN LEAD-FREE ROHS COMPLIANT PACKAGE

ORDER NUMBERS	PACKAGE OPTION
USX2064-AEZG	14 x 35 = 490 pieces/tray
USX2064-AEZG-TR	2500 pieces/tape and reel

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

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Chapter 1 Acronyms

ESD: Electrostatic Discharge

I²C: Inter-Integrated Circuit[1]

OCS: Over-current sense

PCB: Printed Circuit Board

PHY: Physical Layer

PLL: Phase-Locked Loop

QFN: Quad Flat No Leads

RoHS: Restriction of Hazardous Substances Directive

SCK: Serial Clock

SIE: Serial Interface Engine

SMBus: System Management Bus

TT: Transaction Translator

1. I²C is a registered trademark of Philips Corporation.

Chapter 2 Pin Configuration

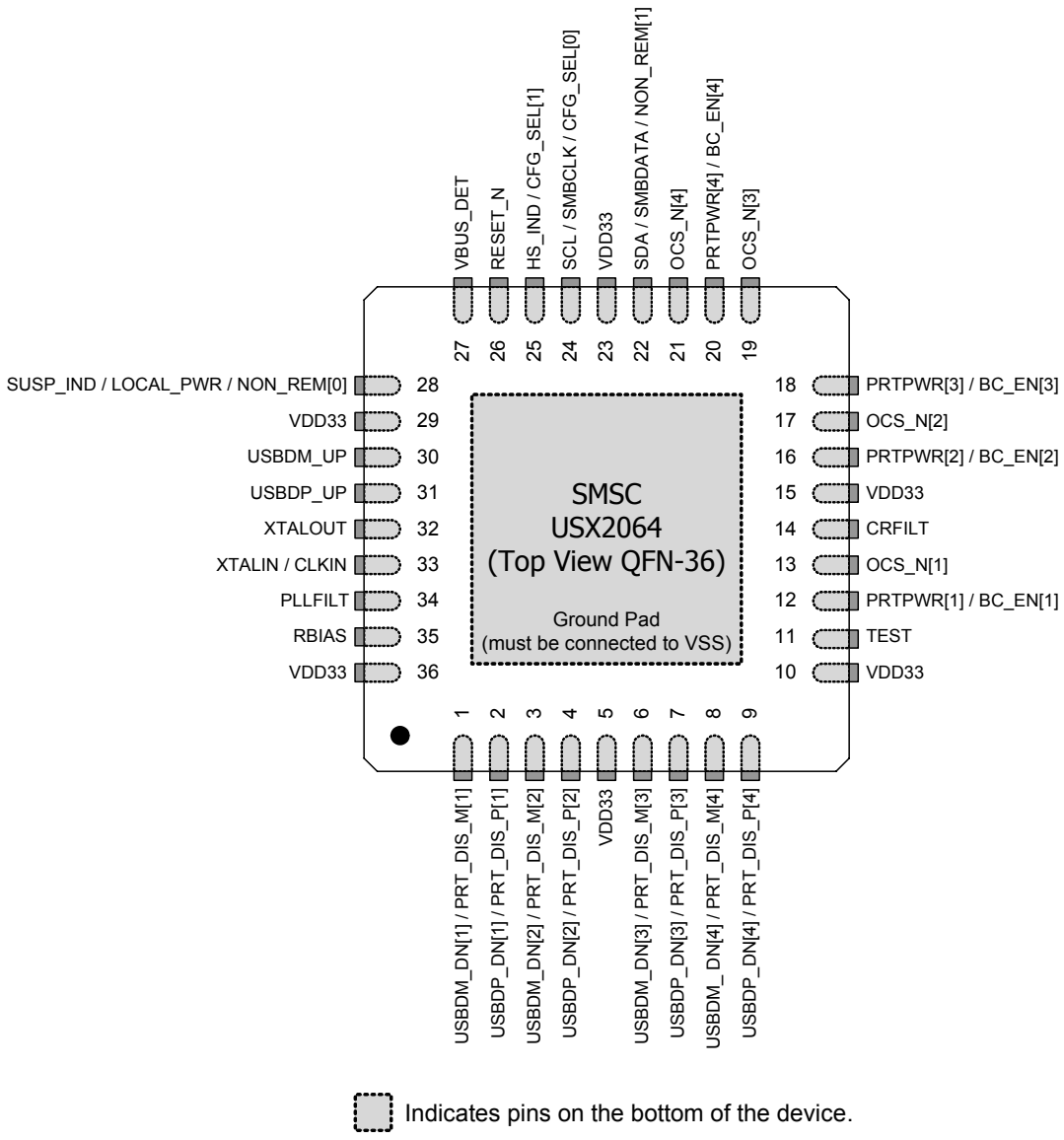


Figure 2.1 USX2064 36-Pin QFN

Chapter 3 Block Diagram

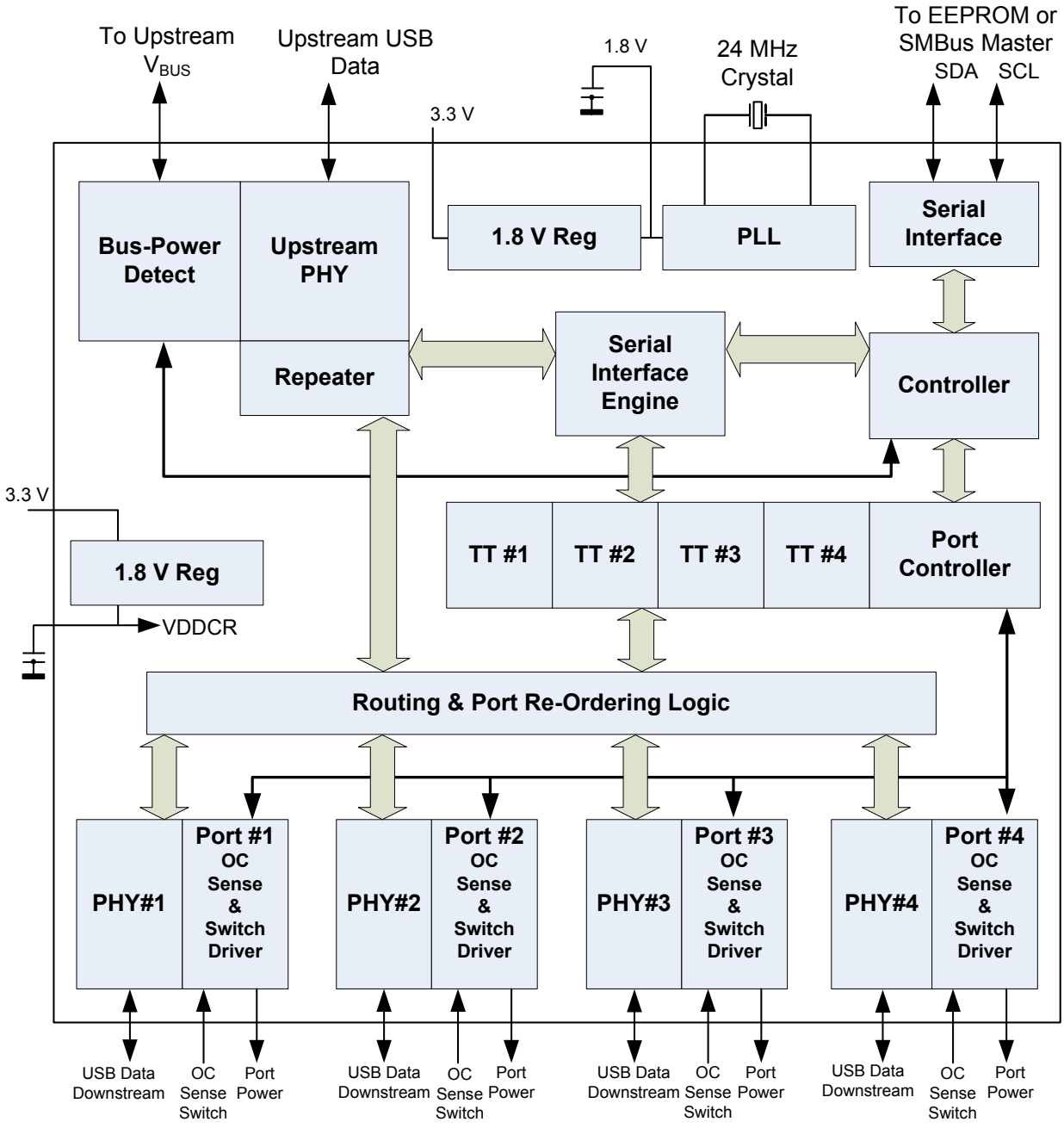


Figure 3.1 USX2064 Block Diagram

Chapter 4 Pin Descriptions

4.1 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “N” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “N” is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Table 4.1 USX2064 Pin Descriptions

SYMBOL	36 QFN	BUFFER TYPE (Table 4.3)	DESCRIPTION
UPSTREAM USB INTERFACES			
USBDP_UP USBDM_UP	31 30	IO-U	USB Bus Data These pins connect to the upstream USB bus data signals (host port, or upstream hub).
VBUS_DET	27	I/O12	Detect Upstream VBUS Power Detects the state of upstream VBUS power. The SMSC hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor which signals a connect event. When designing a detachable hub, this pin must be connected to the VBUS on the upstream port via a 2 to 1 voltage divider. For self-powered applications with a permanently attached host, this pin must be connected to 3.3 V (typically VDD33).
DOWNSTREAM 4-PORT USB 2.0 INTERFACE			
USBDP_DN[4:1]/ PRT_DIS_P[4:1] &	9 7 4 2	IO-U	Hi-Speed USB Data These pins connect to the downstream USB peripheral devices attached to the hub’s port. To disable, pull up with a 10 K resistor to 3.3 V.
USBDM_DN[4:1]/ PRT_DIS_M[4:1]	8 6 3 1		Downstream Port Disable Strap Option If this strap is enabled by package and configuration settings (See Table 5.1, "Hub Configuration Options"), this pin will be sampled at RESET_N negation to determine if the port is disabled. To disable a port, pull up both PRT_DIS_M[x:1] and PRT_DIS_P[x:1] pins corresponding to the port numbers.

Table 4.1 USX2064 Pin Descriptions (continued)

SYMBOL	36 QFN	BUFFER TYPE (Table 4.3)	DESCRIPTION
PRTPWR[4:1] /	20 18 16 12	O12	USB Port Power Enable Enables power to downstream USB peripheral devices. **Note:** The hub will only support active high controllers.
BC_EN[4:1]			Battery Charging Strap Option If this strap is enabled by package and configuration settings, (see Table 5.1, "Hub Configuration Options"), this pin will be sampled at RESET_N negation to determine if ports [x:1] support the battery charging protocol (and thus the supporting external port power controllers) that would enable a device to draw the currents per the USB battery charging specification. BC_EN[x] = '1': Battery charging feature is supported for port x BC_EN[x] = '0': Battery charging feature is not supported for port x
OCS[4:1]_N	21 19 17 13	IPU	Over-current Sense Input from external current monitor indicating an over-current condition.
RBIAS	35	I-R	USB Transceiver Bias A 12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
SERIAL PORT INTERFACE			
SDA/	22	I/OSD12	Serial Data signal (SDA)
SMBDATA/			Server Message Block Data signal (SMBDATA)
NON_REM[1]			Non-removable Port Strap Option If this strap is enabled by package and configuration settings (See Table 5.1, "Hub Configuration Options"), this pin will be sampled (in conjunction with SUSP_IND / LOCAL_PWR / NON_REM[0]) at RESET_N negation to determine if ports [4:1] contain permanently attached (non-removable) devices: NON_REM[1:0] = '00', All ports are removable, NON_REM[1:0] = '01', Port 1 is non-removable, NON_REM[1:0] = '10', Ports 1 & 2 are non-removable, NON_REM[1:0] = '11', Ports 1, 2 & 3 are non-removable
SCL/	24	I/OSD12	Serial Clock (SCL)
SMBCLK/			System Management Bus Clock (SMBCLK)
CFG_SEL[0]			Configuration Select: The logic state of this multifunction pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in Table 5.1, "Hub Configuration Options".

Table 4.1 USX2064 Pin Descriptions (continued)

SYMBOL	36 QFN	BUFFER TYPE (Table 4.3)	DESCRIPTION
HS_IND/	25	I/O12	Hi-Speed Upstream Port Indicator HS_IND: Hi-Speed Indicator for upstream port connection speed. The active state of the LED will be determined as follows: CFG_SEL[1] = '0', HS_IND is active high, CFG_SEL[1] = '1', HS_IND is active low, 'Asserted' = the hub is connected at HS 'Negated' = the hub is connected at FS
CFG_SEL[1]			Configuration Programming Select CFG_SEL[1]: The logic state of this pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in Table 5.1, "Hub Configuration Options".
MISC			
XTALIN	33	ICLKx	Crystal Input 24 MHz crystal. This pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used.
CLKIN			External Clock Input This pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used. When used with an external clock, a resistor divider must be used to provide a 1.8 V signal.
XTALOUT	32	OCLKx	Crystal Output 24 MHz crystal. This is the other terminal of the crystal, or a no connect pin, when an external clock source is used to drive XTALIN/CLKIN.
RESET_N	26	IS	RESET Input The system can reset the chip by driving this input low. The minimum active low pulse is 1 µs after all power supply voltages are at nominal levels.

Table 4.1 USX2064 Pin Descriptions (continued)

SYMBOL	36 QFN	BUFFER TYPE (Table 4.3)	DESCRIPTION
SUSP_IND/ LOCAL_PWR/ NON_REM[0]	28	I/O12	Active/Suspend status LED Suspend Indicator: Indicates USB state of the hub 'negated' = Unconfigured, or configured and in USB Suspend 'asserted' = The hub is configured, and is active (i.e., not in suspend) Local power: Detects availability of local self-power source. Low = Self/local power source is NOT available (i.e., the hub gets all power from upstream USB VBus). High = Self/local power source is available. Non-Removable Strap Option NON_REM0: If this strap is enabled by package and configuration settings (See Table 5.1, "Hub Configuration Options"), this pin will be sampled (in conjunction with NON_REM1) at RESET_N negation to determine if ports [4:1] contain permanently attached (non-removable) devices. Also, the active state of the LED will be determined as follows: NON_REM[1:0] = '00', All ports are removable, and the LED is active high NON_REM[1:0] = '01', Port 1 is non-removable, and the LED is active low NON_REM[1:0] = '10', Ports 1 & 2 are non-removable, and the LED is active high NON_REM[1:0] = '11', Ports 1, 2 & 3 are non-removable, and the LED is active low
TEST	11	IPD	TEST pin User must treat as a no connect pin or connect to ground. No trace or signal should be routed or attached to this pin.

Table 4.2 USX2064 Power, Ground, No Connect Pins

PACKAGE SYMBOL	36 QFN	FUNCTION
CRFILT	14	VDD Core Regulator Filter Capacitor This pin must have a 1.0 μF (or greater) ±20% (ESR <0.1 Ω) capacitor to VSS.
VDD33	36 29 23 15 10 5	3.3 V Power
PLLFILT	34	PLL Regulator Filter Capacitor This pin must have a 1.0 μF (or greater) ±20% (ESR <0.1 Ω) capacitor to VSS.
VSS		Ground Pad / ePad The package slug is the only VSS for the device and must be tied to ground with multiple vias.

4.2 Buffer Type Descriptions

Table 4.3 USX2064 Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input.
IPD	Input with internal weak pull-down resistor.
IPU	Input with internal weak pull-up resistor.
IS	Input with Schmitt trigger.
O12	Output 12 mA.
I/O12	Input/Output buffer with 12 mA sink and 12 mA source.
I/OSD12	Open drain with Schmitt trigger and 12 mA sink. Meets I^2C-Bus specification (Version 2.1) requirements.
ICLKx	XTAL clock input.
OCLKx	XTAL clock output.
I-R	RBIAS.
IO-U	Analog input/output defined in USB 2.0 specification.

Chapter 5 Configuration Options

5.1 4-Port Hub

SMSC's USB 2.0 4-Port Hub is fully compliant to the Universal Serial Bus Specification (Version 2.0) from April 27, 2000 (12/7/2000 and 5/28/2002 Errata). Please reference Chapter 11 (Hub specification) for general details regarding hub operation and functionality.

The 4-port hub provides 1 Transaction Translator (TT) per port (defined as Single-TT configuration), divided into 4 non-periodic buffers per TT.

5.1.1 Hub Configuration Options

The SMSC hub supports a large number of features (some are mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. There are three principal ways to configure the hub: SMBus, EEPROM, or by internal default settings (with or without pin strapping option overrides). In all cases, the configuration method will be determined by the CFG_SEL[1] and CFG_SEL[0] pins immediately after RESET_N negation. Please refer to Table 5.1, "Hub Configuration Options" for more information.

5.1.2 SMBus or EEPROM Interface

Table 5.1 Hub Configuration Options

CFG_SEL[1]	CFG_SEL[0]	DESCRIPTION
0	0	Internal Default Configuration without any over-rides ▪ Strap options enabled ▪ Self-powered operation enabledIndividual power switching ▪ Individual over-current sensing
0	1	Configures as an SMBus slave for external download of user-defined descriptors ▪ SMBus slave address 58 (0101100x) ▪ Strap options disabled ▪ All settings are controlled by registers as set by the user
1	0	Internal Default Configuration ▪ Strap options enabled ▪ Bus-power operationIndividual power switching ▪ Individual over-current sensing
1	1	Supports 2-Wire I^2C EEPROMS ▪ Strap options disabled ▪ All settings controlled by registers as set by the user

5.1.2.1 Power Switching Polarity

Note: The hub only supports "active high" port power controllers.

5.2 VBus Detect

According to Section 7.2.1 of the USB 2.0 Specification, a downstream port can never provide power to its D+ or D- pull up resistors unless the upstream port's VBUS is in the asserted (powered) state. The VBUS_DET pin on the hub monitors the state of the upstream VBUS signal and will not pull up

the D+ resistor if VBUS is not active. If VBUS goes from an active to an inactive state (not powered), the hub will remove power from the D+ pull up resistor within 10 seconds.

5.3 EEPROM Interface

The SMSC hub can be configured via a 2-wire (I^2C) EEPROM (256x8). (Please see Table 5.1, "Hub Configuration Options" for specific details on how to enable configuration via an I^2C EEPROM).

The internal state machine will (when configured for EEPROM support) read the external EEPROM for configuration data. The hub will then “attach” to the upstream USB host.

The hub does not have the capacity to write, or “Program,” an external EEPROM. The hub only has the capability to read external EEPROMs. The external EEPROM will be read (even if it is blank or non-populated), and the hub will be “configured” with the values that are read.

Each register has read/write capability via SMBus. SMBus and EEPROM Reset Values are 0x00. Reserved registers should be written ‘0’ unless specified otherwise.

Note: The hub does not have the capability to write, or “Program”, an external EEPROM. The Hub only has the capability to read external EEPROMs. The external eeprom will be read (even if it is blank or non-populated), and the hub will be “configured” with the values that are read.

Please see the Internal Register Set (Common to EEPROM and SMBus) for a list of available data fields. Please visit www.smsc.com/ftpdocs/usb.html to download the configuration utility for hub EEPROM data. Select the “e2prommap.msi” link to download the tool.

Each register has R/W capability. SMBUS and EEPROM Reset Values are 0x00. Reserved registers should be written to ‘0’ unless otherwise specified.

5.3.1 Internal Register Set (Common to EEPROM and SMBus)

Table 5.2 Internal Default, EEPROM and SMBus Register Memory Map

REG ADDR	REGISTER DESCRIPTION	REGISTER NAME	INTERNAL DEFAULT ROM
00h	Vendor ID Least Significant Byte	VID_LSB	24h
01h	Vendor ID Most Significant Byte	VID_MSB	04h
02h	Product ID Least Significant Byte	PID_LSB	14h
03h	Product ID Most Significant Byte	PID_MSB	25h
04h	Device ID Least Significant Byte	DID_LSB	A0h
05h	Device ID Most Significant Byte	DID_MSB	0Bh
06h	Configuration Data Byte 1	CFG1	9Bh
07h	Configuration Data Byte 2	CFG2	20h
08h	Configuration Data Byte 3	CFG3	02h
09h	Non-Removable Devices	NR_DEVICE	00h
0Ah	Port Disable (Self)	PORT_DIS_SP	00h
0Bh	Port Disable (Bus)	PORT_DIS_BP	00h
0Ch	Max Power (Self)	MAX_PWR_SP	01h
0Dh	Max Power (Bus)	MAX_PWR_BP	32h

Table 5.2 Internal Default, EEPROM and SMBus Register Memory Map (continued)

REG ADDR	REGISTER DESCRIPTION	REGISTER NAME	INTERNAL DEFAULT ROM
0Eh	Hub Controller Max Current (Self)	HC_MAX_C_SP	01h
0Fh	Hub Controller Max Current (Bus)	HC_MAX_C_BP	32h
10h	Power-on Time	PWR_ON_TIME	32h
11h	Language ID High	LANG_ID_H	00h
12h	Language ID Low	LANG_ID_L	00h
13h	Manufacturer String Length	MFR_STR_LEN	00h
14h	Product String Length	PRD_STR_LEN	00h
15h	Serial String Length	SER_STR_LEN	00h
16h-53h	Manufacturer String	MFR_STR	00h
54h-91h	Product String	PRD_STR	00h
92h-CFh	Serial String	SER_STR	00h
D0h	Battery Charging Enable	BC_EN	00h
D1h-F5h	Reserved	N/A	00h
F6h	Boost_Up	BOOSTUP	00h
F7h	Reserved	N/A	00h
F8h	Boost_4:0	BOOST40	00h
F9h	Reserved	N/A	00h
FAh	Port Swap	PRTSP	00h
FBh	Port Map 12	PRTM12	00h
FCh	Port Map 34	PRTM34	00h
FDh-FEh	Reserved	N/A	00h
FFh	Status/Command **Note:** SMBus register only	STCD	00h

5.3.1.1 Register 00h: Vendor ID (LSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	VID_LSB	Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the OEM using either the SMBus or EEPROM interface options.

5.3.1.2 Register 01h: Vendor ID (MSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	VID_MSB	Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the OEM using either the SMBus or EEPROM interface options.

5.3.1.3 Register 02h: Product ID (LSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PID_LSB	Least Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options.

5.3.1.4 Register 03h: Product ID (MSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PID_MSB	Most Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options.

5.3.1.5 Register 04h: Device ID (LSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	DID_LSB	Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options.

5.3.1.6 Register 05h: Device ID (MSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	DID_MSB	Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options.

5.3.1.7 Register 06h: Configuration Data Byte 1

BIT NUMBER	BIT NAME	DESCRIPTION
7	SELF_BUS_PWR	Self- or Bus-Power: Selects between Self- and Bus-Powered operation. The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller). When configured as a bus-powered device, the SMSC hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered SMSC hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 specifications are not violated. When configured as a self-powered device, <1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current. This field is set by the OEM using either the SMBus or EEPROM interface options. Please see the description of the dynamic bit (reg 07h, bit 7) for the self-or bus-power functionality when dynamic power switching is enabled. ‘0’ = Bus-powered operation ‘1’ = Self-powered operation If dynamic power switching is enabled, this bit is ignored and the LOCAL_PWR pin is used to determine if the hub is operating from self or bus power.
6	Reserved	Reserved
5	HS_DISABLE	Hi-Speed Disable: Disables the capability to attach as either a Hi/Full-speed device, and forces attachment as Full-speed only (i.e. no Hi-Speed support). ‘0’ = Hi-/Full-Speed ‘1’ = Full-Speed-Only (Hi-Speed disabled!)
4	MTT_ENABLE	Multi-TT enable: Enables one transaction translator per port operation. Selects between a mode where only one transaction translator is available for all ports (Single-TT), or each port gets a dedicated transaction translator (Multi-TT). ‘0’ = single TT for all ports ‘1’ = one TT per port (multiple TT’s supported)
3	EOP_DISABLE	EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the USB 2.0 Specification for additional details. ‘0’ = EOP generation is normal ‘1’ = EOP generation is disabled
2:1	CURRENT_SNS	Over-current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a port or ganged basis is hardware implementation dependent. ‘00’ = Ganged sensing (all ports together) ‘01’ = Individual port-by-port ‘1x’ = Over-current sensing not supported (must only be used with bus-powered configurations!)

BIT NUMBER	BIT NAME	DESCRIPTION
0	PORT_PWR	Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port- by-port basis (individual). The ability to support power enabling on a port or ganged basis is hardware implementation dependent. ‘0’ = Ganged switching (all ports together) ‘1’ = Individual port-by-port switching

5.3.1.8 Register 07h: Configuration Data Byte 2

BIT NUMBER	BIT NAME	DESCRIPTION
7	DYNAMIC	Dynamic Power Switching Enable: Controls the ability of the hub to automatically change from self-powered operation to bus-powered operation if the local power source is removed or is unavailable (and from bus-powered to self-powered if the local power source is restored). When dynamic power switching is enabled, the hub detects the availability of a local power source by monitoring the external LOCAL_PWR pin. If the hub detects a change in power source availability, the hub immediately disconnects and removes power from all downstream devices and disconnects the upstream port. The hub will then re-attach to the upstream port as either a bus-powered hub (if local power is unavailable) or a self-powered hub (if local power is available). ‘0’ = No dynamic auto-switching ‘1’ = Dynamic auto-switching capable
6	Reserved	Reserved
5:4	OC_TIMER	Over-Current Timer: Over-Current Timer delay. ‘00’ = 0.1 ms ‘01’ = 4.0 ms ‘10’ = 8.0 ms ‘11’ = 16.0 ms
3	COMPOUND	Compound Device: Allows the OEM to indicate that the hub is part of a compound (see the USB Specification for definition) device. The applicable port(s) must also be defined as having a "Non-Removable Device". **Note:** When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. ‘0’ = No ‘1’ = Yes, the hub is part of a compound device
2:0	Reserved	Reserved

5.3.1.9 Register 08h: Configuration Data Byte 3

BIT NUMBER	BIT NAME	DESCRIPTION
7:4	Reserved	Reserved
3	PRTMAP_EN	Port Re-mapping enable: Selects the method used by the hub to assign port numbers and disable ports. '0' = Standard mode '1' = Port re-map mode
2:1	Reserved	Reserved
0	STRING_EN	Enables String Descriptor Support '0' = String support disabled '1' = String support enabled

5.3.1.10 Register 09h: Non-Removable Device

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	NR_DEVICE	Non-Removable Device: Indicates which port(s) include non-removable devices. '0' = port is removable '1' = port is non-removable Informs the host if one of the active ports has a permanent device that is undetachable from the hub. **Note:** The device must provide its own descriptor data. When using the internal default option, the NON_REM[1:0] pins will designate the appropriate ports as being non-removable. Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Controls Physical Port 4 Bit 3= Controls Physical Port 3 Bit 2= Controls Physical Port 2 Bit 1= Controls Physical Port 1 Bit 0 is Reserved, always = '0'

5.3.1.11 Register 0Ah: Port Disable For Self-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PORT_DIS_SP	Port Disable Self-Powered: Disables 1 or more contiguous ports. ‘0’ = Port is available ‘1’ = Port is disabled During self-powered operation when remapping mode is disabled (PRTMAP_EN='0'), this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a host controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB host, and will reorder the active ports in order to ensure proper function. When using the internal default option, the PRT_DIS_P[x:1] and PRT_DIS_M[x:1] pins will disable the appropriate ports. Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Controls Port 4 Bit 3= Controls Port 3 Bit 2= Controls Port 2 Bit 1= Controls Port 1 Bit 0 is Reserved, always = ‘0’

5.3.1.12 Register 0Bh: Port Disable For Bus-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PORT_DIS_BP	Port Disable Bus-Powered: Disables 1 or more contiguous ports. ‘0’ = Port is available ‘1’ = Port is disabled During self-powered operation when remapping mode is disabled (PRTMAP_EN='0'), this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a host controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB host, and will reorder the active ports in order to ensure proper function. When using the internal default option, the PRT_DIS_P[4:1] and PRT_DIS_M[4:1] pins will disable the appropriate ports. Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Controls Port 4 Bit 3= Controls Port 3 Bit 2= Controls Port 2 Bit 1= Controls Port 1 Bit 0 is Reserved, always = ‘0’

5.3.1.13 Register 0Ch: Max Power For Self-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	MAX_PWR_SP	Max Power Self_Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0mA in its descriptors. **Note:** The USB 2.0 Specification does not permit this value to exceed 100 mA.

5.3.1.14 Register 0Dh: Max Power For Bus-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	MAX_PWR_BP	Max Power Bus_Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors.

5.3.1.15 Register 0Eh: Hub Controller Max Current For Self-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	HC_MAX_C_SP	Hub Controller Max Current Self-Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. **Note:** The USB 2.0 Specification does not permit this value to exceed 100 mA. A value of 50 (decimal) indicates 100 mA, which is the default value.

5.3.1.16 Register 0Fh: Hub Controller Max Current For Bus-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	HC_MAX_C_BP	Hub Controller Max Current Bus-Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value will NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. A value of 50 (decimal) would indicate 100 mA, which is the default value.

5.3.1.17 Register 10h: Power-On Time

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PWR_ON_TIME	Power-On Time: The length of time that it takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is stable on that port.

5.3.1.18 Register 11h: Language ID High

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	LANG_ID_H	USB LANGUAGE ID (Upper 8 bits of a 16-bit ID field)

5.3.1.19 Register 12h: Language ID Low

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	LANG_ID_L	USB LANGUAGE ID (Lower 8 bits of a 16-bit ID field)

5.3.1.20 Register 13h: Manufacturer String Length

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	MFR_STR_LEN	Manufacturer String Length Maximum string length is 31 characters

5.3.1.21 Register 14h: Product String Length

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PRD_STR_LEN	Product String Length Maximum string length is 31 characters

5.3.1.22 Register 15h: Serial String Length

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	SER_STR_LEN	Serial String Length Maximum string length is 31 characters

5.3.1.23 Register 16h-53h: Manufacturer String

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	MFR_STR	Manufacturer String, UNICODE UTF-16LE per USB 2.0 Specification Maximum string length is 31 characters (62 bytes) **Note:** The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Some EEPROM programmers may transpose the MSB and LSB, thus reversing the Byte order. Please pay careful attention to the byte ordering or your selected programming tools.

5.3.1.24 Register 54h-91h: Product String

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PRD_STR	Product String, UNICODE UTF-16LE per USB 2.0 Specification Maximum string length is 31 characters (62 bytes) **Note:** The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Some EEPROM programmers may transpose the MSB and LSB, thus reversing the Byte order. Please pay careful attention to the byte ordering or your selected programming tools.

5.3.1.25 Register 92h-CFh: Serial String

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	SER_STR	Serial String, UNICODE UTF16LE per USB 2.0 Specification Maximum string length is 31 characters (62 bytes) **Note:** The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Some EEPROM programmers may transpose the MSB and LSB, thus reversing the Byte order. Please pay careful attention to the byte ordering or your selected programming tools.

5.3.1.26 Register D0h: Battery Charging Enable

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	BC_EN	Battery Charging Enable: Enables the battery charging feature. '0' = Battery Charging support is not enabled '1' = Battery Charging support is enabled Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Controls Port 4 Bit 3= Controls Port 3 Bit 2= Controls Port 2 Bit 1= Controls Port 1 Bit 0= Reserved

5.3.1.27 Register F6h: Boost_Up

BIT NUMBER	BIT NAME	DESCRIPTION
7:2	Reserved	Reserved
1:0	BOOST_IOUT	USB electrical signaling drive strength Boost Bit for Upstream Port. '00' = Normal electrical drive strength = No boost '01' = Elevated electrical drive strength = Low (approximately 4% boost) '10' = Elevated electrical drive strength = Medium (approximately 8% boost) '11' = Elevated electrical drive strength = High (approximately 12% boost)

Note: "Boost" could result in non-USB Compliant parameters, the OEM should use a '00' value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.

5.3.1.28 Register F8h: Boost_4:0

BIT NUMBER	BIT NAME	DESCRIPTION
7:6	BOOST_IOUT_4	USB electrical signaling drive strength Boost Bit for Downstream Port '4'. '00' = Normal electrical drive strength = No boost '01' = Elevated electrical drive strength = Low (~ 4% boost) '10' = Elevated electrical drive strength = Medium (~ 8% boost) '11' = Elevated electrical drive strength = High (~ 12% boost)
5:4	BOOST_IOUT_3	USB electrical signaling drive strength Boost Bit for Downstream Port '3'. '00' = Normal electrical drive strength = No boost '01' = Elevated electrical drive strength = Low (~ 4% boost) '10' = Elevated electrical drive strength = Medium (~ 8% boost) '11' = Elevated electrical drive strength = High (~ 12% boost)
3:2	BOOST_IOUT_2	USB electrical signaling drive strength Boost Bit for Downstream Port '2'. '00' = Normal electrical drive strength = No boost '01' = Elevated electrical drive strength = Low (~ 4% boost) '10' = Elevated electrical drive strength = Medium (~ 8% boost) '11' = Elevated electrical drive strength = High (~ 12% boost)

BIT NUMBER	BIT NAME	DESCRIPTION
1:0	BOOST_IOUT_1	USB electrical signaling drive strength Boost Bit for Downstream Port ‘1’. ‘00’ = Normal electrical drive strength = No boost ‘01’ = Elevated electrical drive strength = Low (~ 4% boost) ‘10’ = Elevated electrical drive strength = Medium (~ 8% boost) ‘11’ = Elevated electrical drive strength = High (~ 12% boost)

Note: “Boost” could result in non-USB Compliant parameters, the OEM should use a ‘00’ value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.

5.3.1.29 Register FAh: Port Swap

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PRTSP	Port Swap: Swaps the Upstream and Downstream USB DP and DM Pins for ease of board routing to devices and connectors. ‘0’ = USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. ‘1’ = USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin. Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Controls Port 4 Bit 3= Controls Port 3 Bit 2= Controls Port 2 Bit 1= Controls Port 1 Bit 0= ‘1’ the Upstream Port DP/DM is swapped

5.3.1.30 Register FBh: PortMap 12

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PRTM12	PortMap register for ports 1 & 2 When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number '1', up to the number of ports that the hub recognizes. The host's port number is referred to as "Logical Port Number" and the physical port on the hub is the “Physical Port Number". When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host). **Note:** The OEM must ensure that contiguous logical port numbers are used, starting from #1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a Host will communicate with the ports.

Table 5.3 Port Map Register for Ports 1 & 2

Bit [7:4]	‘0000’	Physical Port 2 is Disabled
	‘0001’	Physical Port 2 is mapped to Logical Port 1
	‘0010’	Physical Port 2 is mapped to Logical Port 2
	‘0011’	Physical Port 2 is mapped to Logical Port 3
	‘0100’	Physical Port 2 is mapped to Logical Port 4
	‘0101’ to ‘1111’	Reserved, will default to ‘0000’ value
Bit [3:0]	‘0000’	Physical Port 1 is Disabled
	‘0001’	Physical Port 1 is mapped to Logical Port 1
	‘0010’	Physical Port 1 is mapped to Logical Port 2
	‘0011’	Physical Port 1 is mapped to Logical Port 3
	‘0100’	Physical Port 1 is mapped to Logical Port 4
	‘0101’ to ‘1111’	Reserved, will default to ‘0000’ value

5.3.1.31 Register FCh: PortMap 34

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PRTM34	PortMap register for ports 3 & 4 When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The Host Controller will number the downstream ports of the hub starting with the number '1', up to the number of ports that the hub recognizes. The host's port number is referred to as "Logical Port Number" and the physical port on the hub is the “Physical Port Number". When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host). **Note:** The OEM must ensure that contiguous logical port numbers are used, starting from #1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a Host will communicate with the ports.

Table 5.4 Port Map Register for Ports 3 & 4

Bit [7:4]	‘0000’	Physical Port 4 is Disabled
	‘0001’	Physical Port 4 is mapped to Logical Port 1
	‘0010’	Physical Port 4 is mapped to Logical Port 2
	‘0011’	Physical Port 4 is mapped to Logical Port 3
	‘0100’	Physical Port 4 is mapped to Logical Port 4
	‘0101’ to ‘1111’	Reserved, will default to ‘0000’ value
Bit [3:0]	‘0000’	Physical Port 3 is Disabled
	‘0001’	Physical Port 3 is mapped to Logical Port 1
	‘0010’	Physical Port 3 is mapped to Logical Port 2
	‘0011’	Physical Port 3 is mapped to Logical Port 3
	‘0100’	Physical Port 3 is mapped to Logical Port 4
	‘0101’ to ‘1111’	Reserved, will default to ‘0000’ value

5.3.1.32 Register FFh: Status/Command

BIT NUMBER	BIT NAME	DESCRIPTION
7:3	Reserved	Reserved
2	INTF_PW_DN	SMBus Interface Power Down '0' = Interface is active '1' = Interface power down after ACK has completed
1	RESET	Reset the SMBus Interface and internal memory back to RESET_N assertion default settings. '0' = Normal Run/Idle State '1' = Force a reset of registers to their default state
0	USB_ATTACH	USB Attach (and write protect) '0' = SMBus slave interface is active '1' = the hub will signal a USB attach event to an upstream device. The internal memory (address range 00h-FEh) is "write-protected" to prevent unintentional data corruption.

5.3.2 I²C EEPROM

The I²C EEPROM interface implements a subset of the I²C Master Specification (Please refer to the Philips Semiconductor Standard I²C-Bus Specification for details on I²C bus protocols). The hub's I²C EEPROM interface is designed to attach to a single "dedicated" I²C EEPROM, and conforms to the Standard-mode I²C Specification (100 kbit/s transfer rate and 7-bit addressing) for protocol and electrical compatibility.

Note: Extensions to the I²C Specification are not supported.

The hub acts as the master and generates the serial clock SCL, controls the bus access (determines which device acts as the transmitter and which device acts as the receiver), and generates the START and STOP conditions.

5.3.2.1 Implementation Characteristics

The hub will only access an EEPROM using the sequential read protocol.

5.3.2.2 Pull-Up Resistor

The circuit board designer is required to place external pull-up resistors (10 kΩ recommended) on the SDA / SMBDATA and SCL / SMBCLK / CFG_SEL0 lines (per SMBus 1.0 Specification, and EEPROM manufacturer guidelines) to VDD33 in order to assure proper operation.

5.3.2.3 I²C EEPROM Slave Address

Slave address is 1010000.

Note: 10-bit addressing is NOT supported.

5.3.3 In-Circuit EEPROM Programming

The EEPROM can be programmed via ATE (automatic test equipment) by pulling RESET_N low (which tri-states the hub's EEPROM interface and allows an external source to program the EEPROM).

5.4 SMBus Slave Interface

Instead of loading User-Defined Descriptor data from an external EEPROM, the SMSC hub can be configured to receive a code load from an external processor via an SMBus interface. The SMBus interface shares the same pins as the EEPROM interface; if CFG_SEL1 & CFG_SEL0 activates the SMBus interface, external EEPROM support is no longer available (and the user-defined descriptor data must be downloaded via the SMBus). The SMSC hub waits indefinitely for the SMBus code load to complete and only “appears” as a newly connected device on USB after the code load is complete.

The hub’s SMBus implementation is a *slave-only* SMBus device. The implementation only supports Read Block and Write Block protocols.The hub responds to other protocols as described in Section 5.4.2, "Invalid Protocol Response Behavior," on page 31. Please reference the System Management Bus Specification, Rev 1.0.

The SMBus interface is used to read and write the registers in the device. The register set is shown in Section 5.3.1, "Internal Register Set (Common to EEPROM and SMBus)," on page 15.

5.4.1 Bus Protocols

Typical Write Block and Read Block protocols are shown below. Register accesses are performed using 7-bit slave addressing, an 8-bit register address field, and an 8-bit data field. The shading indicates the hub driving data on the SMBDATA line; otherwise, host data is on the SDA/SMBDATA line.

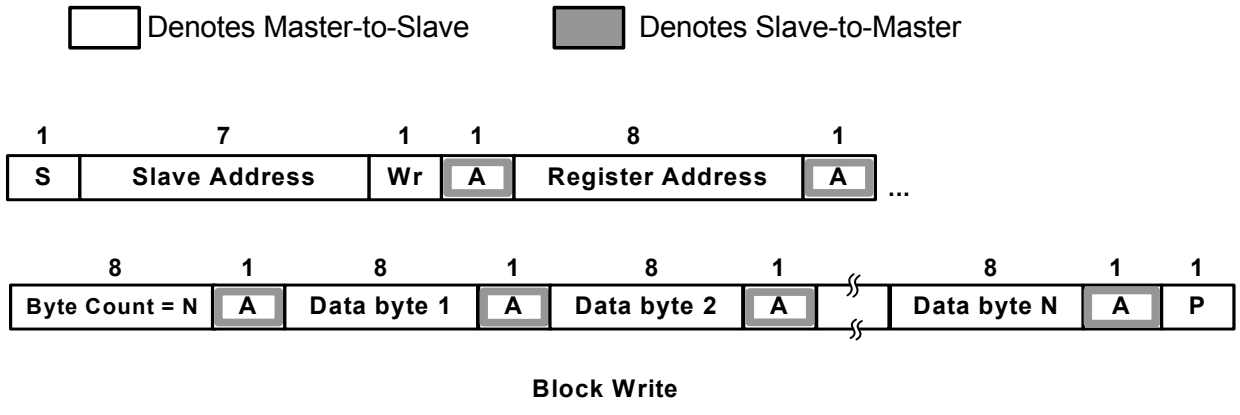
The slave address is the unique SMBus Interface Address for the hub that identifies it on SMBus. The register address field is the internal address of the register to be accessed. The register data field is the data that the host is attempting to write to the register or the contents of the register that the host is attempting to read.

Note: Data bytes are transferred MSB first (msb first).

5.4.1.1 Block Read/Write

The Block Write begins with a slave address and a write condition. After the command code, the host issues a byte count which describes how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A Block Read or Write is allowed to transfer a maximum of 32 data bytes.

Note: For the following SMBus tables:

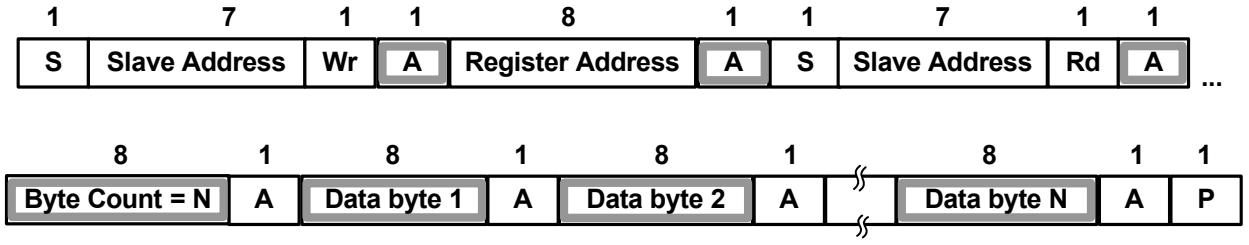


Block Write

Figure 5.1 Block Write

5.4.1.2 Block Read

A Block Read differs from a block write in that the repeated start condition exists to satisfy the I^2C specification's requirement for a change in the transfer direction.



Block Read

Figure 5.2 Block Read

5.4.2 Invalid Protocol Response Behavior

Registers that are accessed with an invalid protocol are not updated. A register is only updated following a valid protocol. The only valid protocols are Write Block and Read Block, which are described above. The hub only responds to the hardware selected Slave Address (0101100x).

Attempting to communicate with the hub over SMBus with an invalid slave address or invalid protocol results in no response, and the SMBus Slave Interface returns to the idle state.

The only valid registers that are accessible by the SMBus slave address are the registers defined in the Registers Section. The hub does not respond to undefined registers.

5.4.3 General Call Address Response

The hub does not respond to a general call address of 0000_000b.

5.4.4 Slave Device Time-Out

According to the SMBus Specification (Version 1.0) devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25 ms ($T_{TIMEOUT, MIN}$). Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than 35 ms ($T_{TIMEOUT, MAX}$).

Note: Some simple devices do not contain a clock low drive circuit; this simple kind of device typically resets its communications port after a start or stop condition. The Slave Device Time-Out must be implemented.

5.4.5 Stretching the SCLK Signal

The hub supports stretching of the SCLK by other devices on the SMBus. The hub does not stretch the SCLK.

5.4.6 SMBus Timing

The SMBus Slave Interface complies with the SMBus AC Timing specification. See the SMBus timing in the "Timing Diagram" section.

5.4.7 Bus Reset Sequence

The SMBus slave Interface resets and returns to the idle state upon a START field followed immediately by a STOP field.

5.4.8 SMBus Alert Response Address

The SMBALERT# signal is not supported by the hub.

5.4.8.1 Undefined Registers

The registers shown in Table 5.2 are the defined registers in the hub. Reads to undefined registers return to 00h. Writes to undefined registers have no effect and do not return an error.

5.4.8.2 Reserved Registers

Reserved registers should be written to ‘0’ unless otherwise specified. Contents read should be ignored.

5.5 Default Configuration Option

To confiture the SMSC hub in its default configuration, strap CFG_SEL[1:0] to 00h. This procedure configures the hub to the internal defaults and enables the strapping options. Please see Section 5.3.1, "Internal Register Set (Common to EEPROM and SMBus)" for the list of the default values. For specific pin strapping options, please see Chapter 4, Pin Descriptions for instructions on how to modify the default values. Options include port disable and non-removable pin strapping.

5.6 Default Strapping Options

The USX2064 can be configured via a combination of internal default values and pin strap options. Please see Table 4.1, "USX2064 Pin Descriptions" and Table 5.1, "Hub Configuration Options" for specific details on how to enable the default/pin-strap configuration option.

The strapping option pins only cover a limited sub-set of the configuration options. The internal default values will be used for the bits and registers that are not controlled by a strapping option pin. Please refer to Table 5.1, "Hub Configuration Options" for the internal default values that are loaded when this option is selected.

5.7 Strap Options

5.7.1 Non-Removable Strap Option

The strap function of the NON_REM[1:0] pins are enabled through the internal default configuration. The driver type of each strap pin is I/O (no internal pull-up or pull-down for the input function). Use this type of strap option for NON_REM[1:0]. Figure 5.3, "Non-Removable Pin Strap Example" shows an example of Strap High and Strap Low. Use the Strap High configuration to set the strap option value to a ‘1’. Use the Strap Low configuration to set the strap option value to ‘0’.

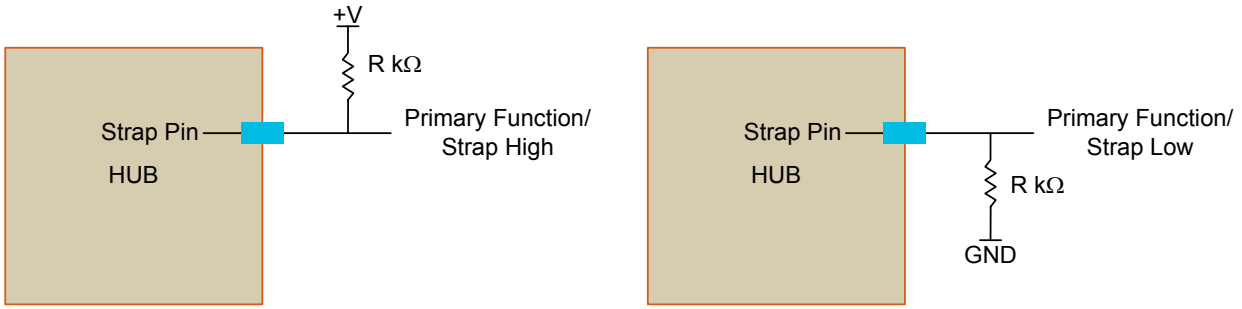


Figure 5.3 Non-Removable Pin Strap Example

5.7.2 Internal Pull-Down

If a pin's strap function is enabled through hub configuration selection (Table 5.1, "Hub Configuration Options") and the strap pins driver type is IPD/O (internal pull-down for the Input function), use this type of strap option.

Figure 5.4, "Pin Strap Option wit IPD Pin Example" shows an example of Strap High and Strap Low. Use the Strp High configuration to set the strap option value to a '1'. Use the Strap Low configuration to set the strap option value to '0'.

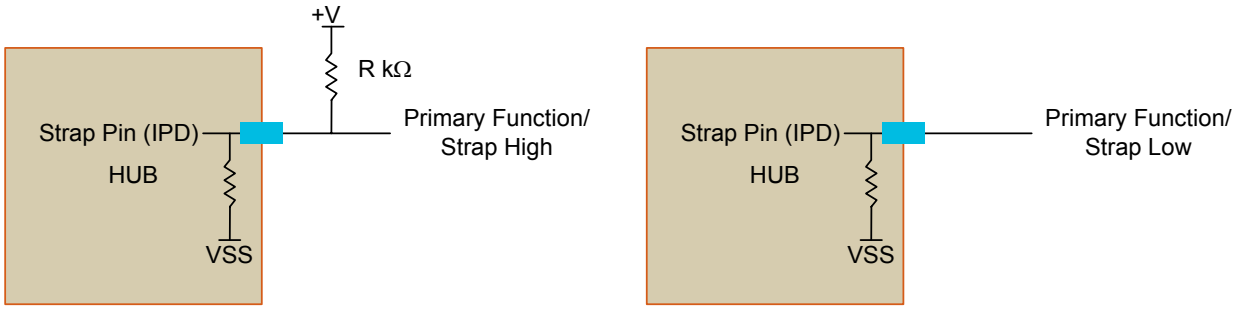


Figure 5.4 Pin Strap Option wit IPD Pin Example

5.8 Reset

There are two different resets that the hub experiences. One is a hardware reset via the RESET_N pin and the second is a USB Bus Reset.

5.8.1 External Hardware RESET_N

A valid hardware reset is defined as assertion of RESET_N for a minimum of 1 µs after all power supplies are within operating range. While reset is asserted, the hub (and its associated external circuitry) consumes less than 500 µA of current from the upstream USB power source.

Assertion of RESET_N (external pin) causes the following:

1. All downstream ports are disabled, and PRTPWR power to downstream devices is removed (unless BC_EN is enabled).
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases 00(h)).
5. The external crystal oscillator is halted.

6. The PLL is halted.
7. LED indicators are disabled.

The hub is “operational” 500 µs after RESET_N is negated. Once operational, the hub immediately reads OEM-specific data from the external EEPROM (if the SMBus option is not disabled).

5.8.1.1 RESET_N for Strapping Option Configuration

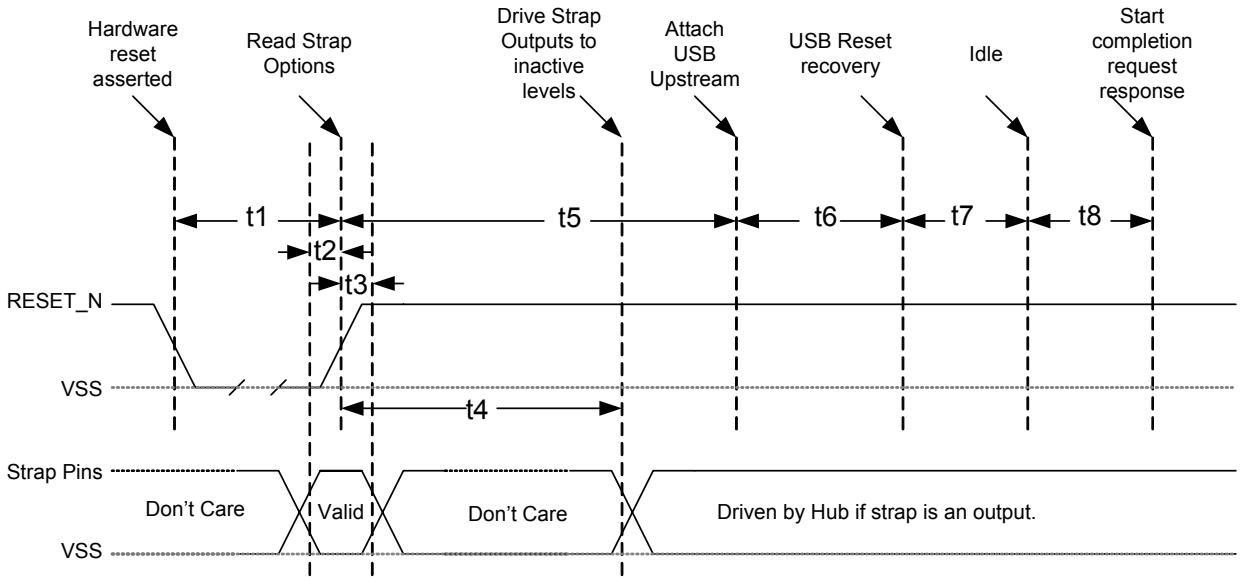


Figure 5.5 Reset_N Timing for Default/Strap Option Mode

Table 5.5 Reset_N Timing for Default/Strap Option Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	RESET_N Asserted.	1			µsec
t2	Strap Setup Time	16.7			nsec
t3	Strap Hold Time.	16.7		1400	nsec
t4	Hub outputs driven to inactive logic states.		1.5	2	µsec
t5	USB Attach (See Note).			100	msec
t6	Host acknowledges attach and signals USB Reset.	100			msec
t7	USB Idle.		undefined		msec
t8	Completion time for requests (with or without data stage).			5	msec

Notes:

- When in bus-powered mode, the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t1+t5.
- All power supplies must have reached the operating levels mandated in Chapter 6, DC Parameters, prior to (or coincident with) the assertion of RESET_N.

5.8.1.2 RESET_N for EEPROM Configuration

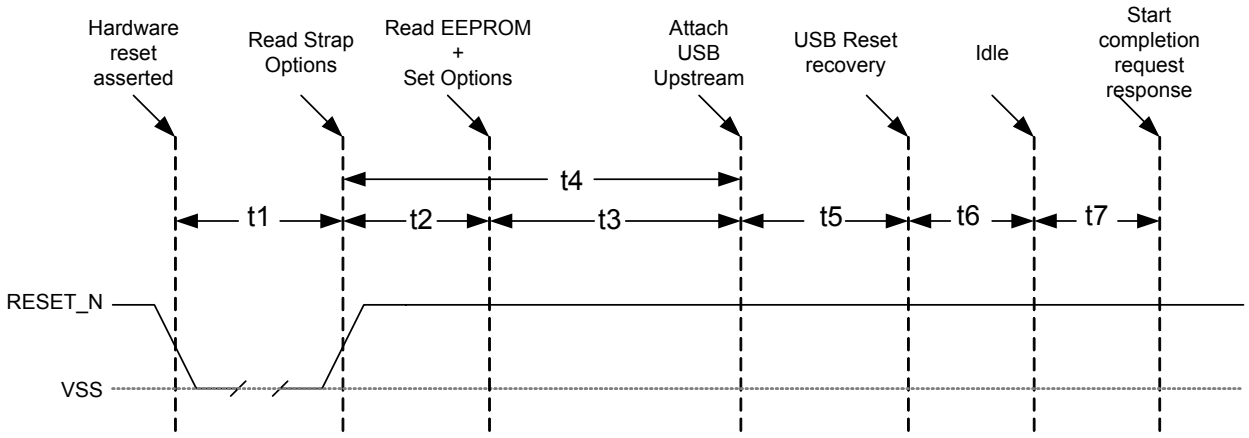


Figure 5.6 Reset_N Timing for EEPROM Mode

Table 5.6 Reset_N Timing for EEPROM Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	RESET_N Asserted.	1			µsec
t2	Hub Recovery/Stabilization.			500	µsec
t3	EEPROM Read / Hub Config.		2.0	99.5	msec
t4	USB Attach (See Note).			100	msec
t5	Host acknowledges attach and signals USB Reset.	100			msec
t6	USB Idle.		undefined		msec
t7	Completion time for requests (with or without data stage).			5	msec

Notes:

- When in bus-powered mode, the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t4+t5+t6+t7.
- All Power Supplies must have reached the operating levels mandated in Chapter 6, DC Parameters, prior to (or coincident with) the assertion of RESET_N.

5.8.1.3 RESET_N for SMBus Slave Configuration

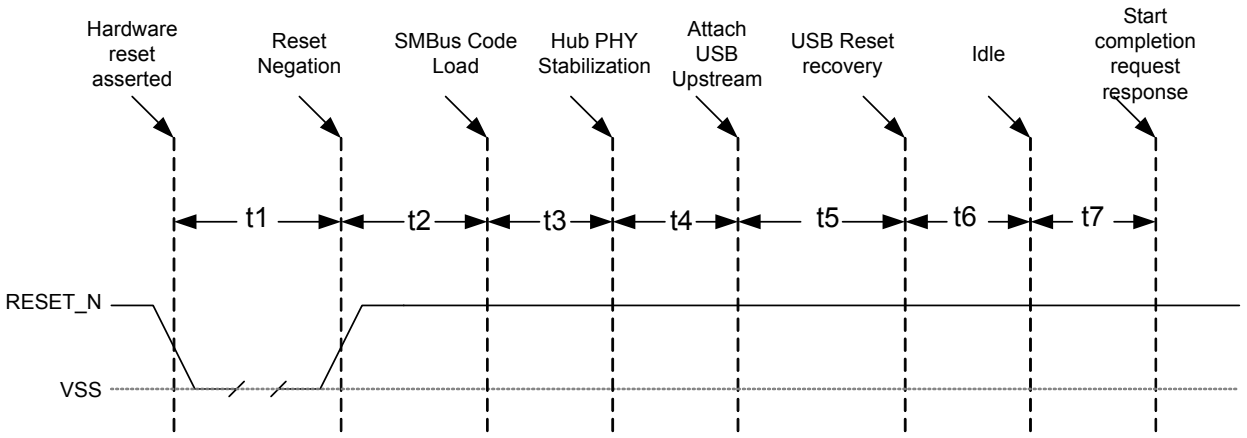


Figure 5.7 Reset_N Timing for SMBus Mode

Table 5.7 Reset_N Timing for SMBus Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	RESET_N Asserted.	1			µsec
t2	Hub Recovery/Stabilization.			500	µsec
t3	SMBus Code Load (See Note).		250	300	msec
t4	Hub Configuration and USB Attach.			100	msec
t5	Host acknowledges attach and signals USB Reset.	100			msec
t6	USB Idle.		Undefined		msec
t7	Completion time for requests (with or without data stage).			5	msec

Notes:

- For bus-powered configurations, the 99.5 ms (MAX) is required, and the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t2+t3+t4+t5+t6+t7. For self-powered configurations, t3 MAX is not applicable and the time to load the configuration is determined by the external SMBus host.
- All power supplies must have reached the operating levels mandated in Chapter 6, DC Parameters, prior to (or coincident with) the assertion of RESET_N.

5.8.2 USB Bus Reset

In response to the upstream port signaling a reset to the hub, the hub does the following:

Note: The hub does not propagate the upstream USB reset to downstream devices.

1. Sets default address to ‘0’.
2. Sets configuration to: Unconfigured.
3. Negates PRTPWR[4:1] to all downstream ports unless battery charging (BC_EN) is enabled.
4. Clears all TT buffers.
5. Moves device from suspended to active (if suspended).

6. Complies with Section 11.10 of the USB 2.0 Specification for behavior after completion of the reset sequence.

Note: The hub does not propagate the upstream USB reset to downstream devices.

Chapter 6 DC Parameters

6.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	T_{STOR}	-55	150	°C	
Lead Temperature			325	°C	Refer to JEDEC Specification J-STD_020D.
3.3 V supply voltage	V_{DD33}, PLLFILT, CRFILT		4.6	V	Applies to all parts.
Voltage on any I/O pin		-0.5	5.5	V	
Voltage on XTALIN		-0.5	4.0	V	
Voltage on XTALOUT		-0.5	2.5	V	

Note 6.1 Stresses above the specified parameters could cause permanent damage to the device. These are only stress ratings. Functional operation of the device at any condition above these parameters in the operation sections of this specification are not implied.

Note 6.2 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

6.2 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Operating Temperature	T_A	0	70	°C	Ambient temperature in still air.
1.8 V supply voltage	$V_{DD18PLL}$ V_{DD18}	1.62	1.98	V	
3.3 V supply voltage	V_{DDA33} $V_{DDA33PLL}$ V_{DD33} V_{DD33CR}	3.0	3.6	V	
3.3 V supply rise time	t_{RT}		400	µs	(See Figure 6.1, "Supply Rise Time Model")

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Voltage on any I/O pin		-0.3	5.5	V	If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes: (3.3 V supply voltage) + 0.5
Voltage on XTALIN		-0.3	0.2	V	
Voltage on XTALOUT		-0.3	0.2	V	

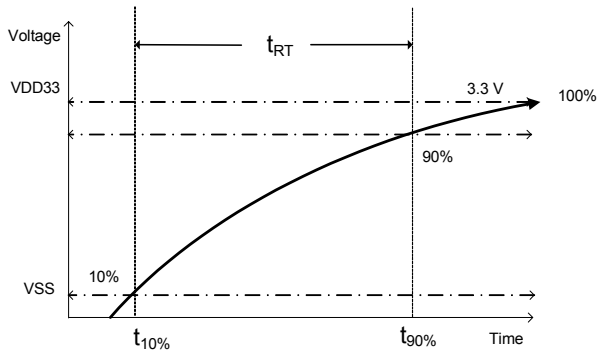


Figure 6.1 Supply Rise Time Model

Table 6.1 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I, IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0 to V_{DD33}
Hysteresis (‘IS’ Only)	V_{HYSI}	250		350	mV	
Input Buffer with Pull-Up (IPU)						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Low Input Leakage	I_{ILL}	+35		+90	µA	V_{IN} = 0
High Input Leakage	I_{IHL}	-10		+10	µA	V_{IN} = V_{DD33}
Input Buffer with Pull-Down (IPD)						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Low Input Leakage	I_{ILL}	+10		-10	µA	V_{IN} = 0
High Input Leakage	I_{IHL}	-35		-90	µA	V_{IN} = V_{DD33}

Table 6.1 DC Electrical Characteristics (continued)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.5	V	
High Input Level	V_{IHCK}	1.4			V	
Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0 to V_{DD33}
O12, I/O12 & I/OSD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA @ V_{DD33} = 3.3 V
High Output Level	V_{OH}	2.4			V	I_{OH} = -12 mA @ V_{DD33} = 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 6.3)
Hysteresis ('SD' pad only)	V_{HYSC}	250		350	mV	
IO-U (Note 6.4)						
Supply Current Unconfigured						
Hi-Speed Host Full-Speed Host	$I_{CCINTHS}$ $I_{CCINITFS}$		95 80	105 90	mA mA	
Supply Current Configured (Hi-Speed Host)						All supplies combined
1 Port HS, 1 Port LS/FS 2 Ports @ LS/FS 2 Ports @ HS 3 Ports @ HS 4 Ports @ HS	I_{HCH1C1} I_{HCC2} I_{HCH2} I_{HCH3} I_{HCH4}		150 150 160 170 175	170 160 275 290 305	mA mA mA mA mA	
Supply Current Configured (Full-Speed Host)						All supplies combined
1 Port 2 Ports 3 Ports 4 Ports	I_{FCC1} I_{FCC2} I_{FCC3} I_{FCC4}		140 140 140 140	150 150 150 150	mA mA mA mA	
Supply Current Suspend	I_{CSBY}		310	420	µA	All supplies combined
Supply Current Reset	I_{CRST}		100	275	µA	All supplies combined

Note 6.3 Output leakage is measured with the current pins in high impedance.

Note 6.4 See USB 2.0 Specification for USB DC electrical characteristics.

CAPACITANCE T_A = 25°C; fc = 1 MHz; V_{DD33} = 3.3 V

Table 6.2 Pin Capacitance

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{XTAL}			2	pF	All pins except USB pins (and pins under test tied to AC ground)
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Chapter 7 AC Specifications

7.1 Oscillator/Crystal

Parallel Resonant, Fundamental Mode, 24 MHz ± 350 ppm.

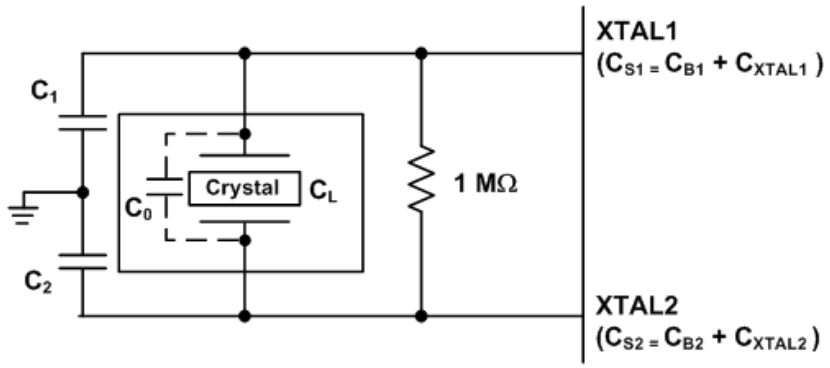


Figure 7.1 Typical Crystal Circuit

Table 7.1 Crystal Circuit Legend

IN ACCORDANCE WITH	SYMBOL	DESCRIPTION
Crystal manufacturer's specification	C_0	Crystal shunt capacitance
	C_L	Crystal load capacitance
OEM board design	C_B	Total board or trace capacitance
SMSC IC and OEM board design	C_S	Stray capacitance
SMSC IC	C_{XTAL}	XTAL pin input capacitance

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

Figure 7.2 Capacitance Formulas

7.2 Ceramic Resonator

24 MHz ± 350 ppm

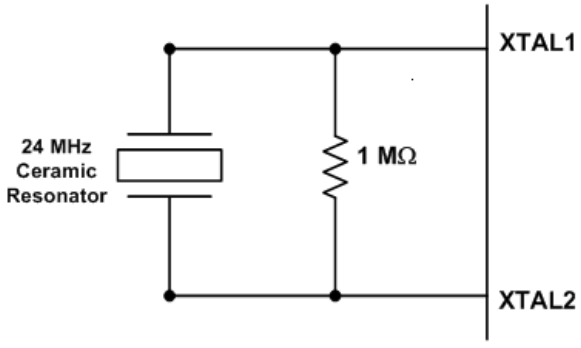


Figure 7.3 Ceramic Resonator Usage with SMSC IC

7.3 External Clock

50% Duty cycle ± 10%, 24 MHz ± 350 ppm, Jitter < 100 ps rms.

The external clock is recommended to conform to the signaling level designated in the JESD76-2 specification on 1.8 V CMOS Logic. XTAL2 should be treated as a no connect.

7.3.1 SMBus Interface

The SMSC Hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the SMBus 1.0 Specification for Slave-Only devices (except as noted in Section 5.4, "SMBus Slave Interface").

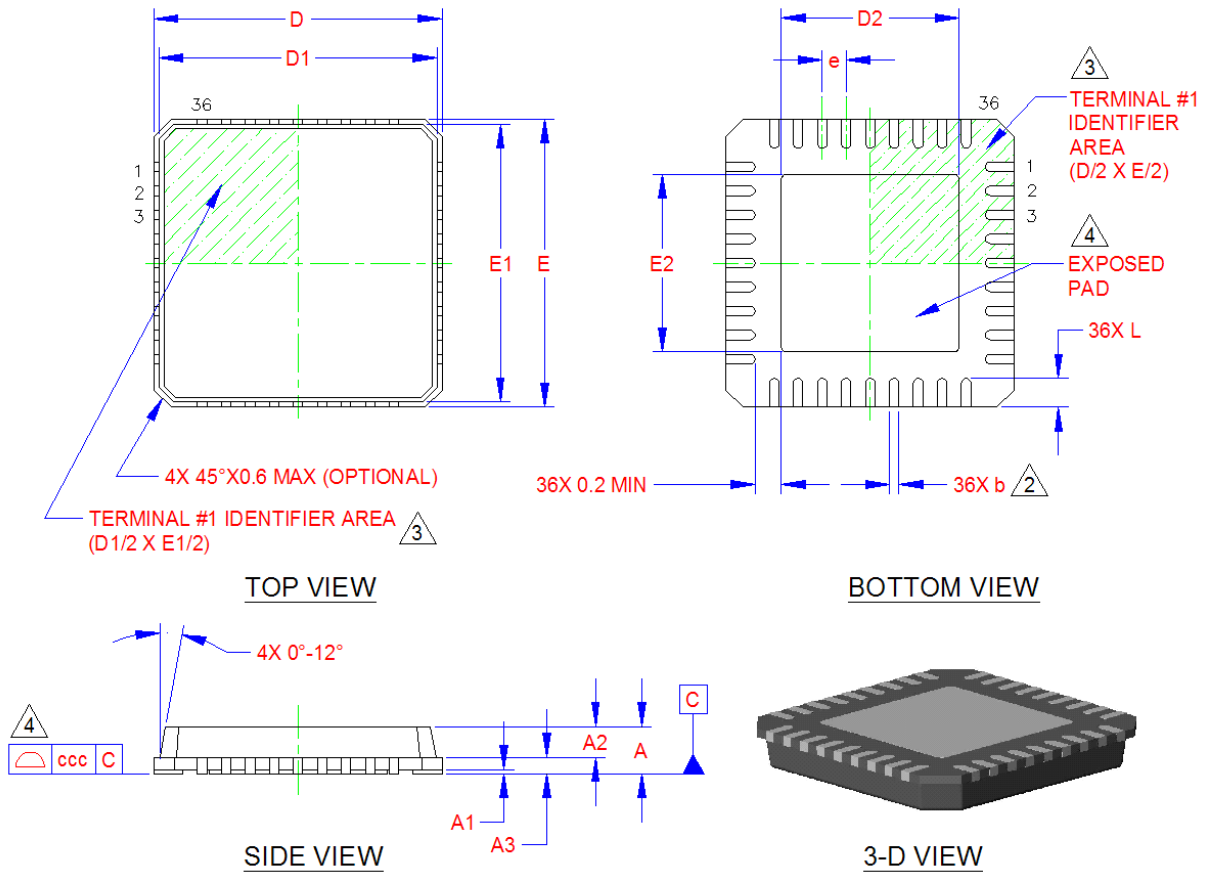
7.3.2 I^2C EEPROM

Frequency is fixed at 58.6 kHz ± 20%.

7.3.3 USB 2.0

The SMSC device conforms to all voltage, power, and timing characteristics and specifications as set forth in the USB 2.0 Specification. Please refer to the USB 2.0 Specification for more information.

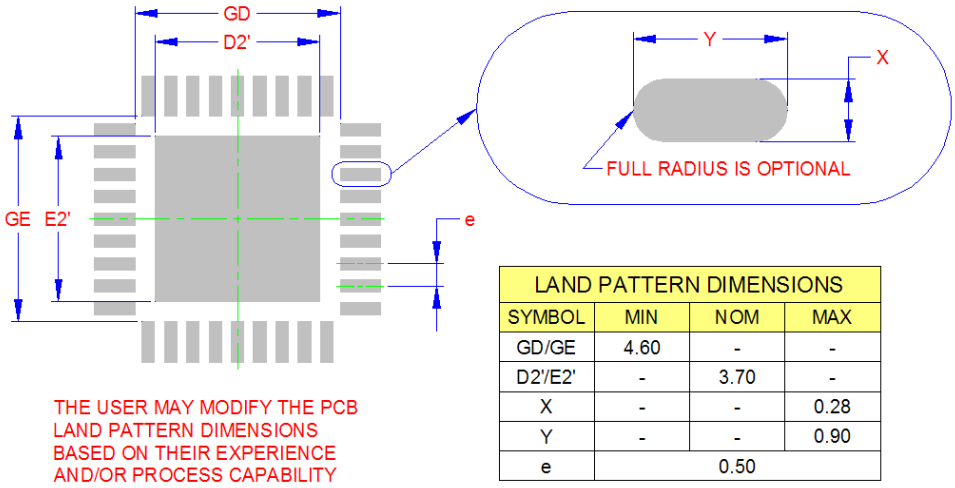
Chapter 8 Package Outline



COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	-	1.00	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A2	0.60	-	0.80	-	MOLD CAP THICKNESS
A3	0.20 REF			-	LEADFRAME THICKNESS
D/E	5.85	6.00	6.15	-	X/Y BODY SIZE
D1/E1	5.55	-	5.95	-	X/Y MOLD CAP SIZE
D2/E2	3.55	3.70	3.85	2	X/Y EXPOSED PAD SIZE
L	0.50	0.60	0.75	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
e	0.50 BSC			-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.
4. COPLANARITY ZONE APPLIES TO EXPOSED PAD AND TERMINALS.

Figure 8.1 36-Pin QFN, 6x6 mm Body, 0.5 mm Pitch



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	4.60	-	-
D2'/E2'	-	3.70	-
X	-	-	0.28
Y	-	-	0.90
e	0.50		

RECOMMENDED PCB LAND PATTERN

Figure 8.2 36-Pin QFN Footprint