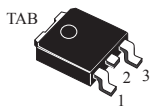
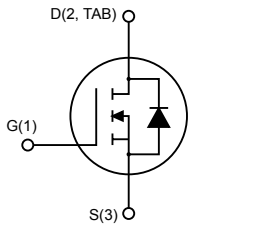
Automotive-grade N-channel 55 V, 6.5 mΩ typ., 80 A STripFET F3 Power MOSFET in a DPAK package



DPAK



Features

Type	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD65N55F3	55 V	8.5 mΩ	80 A	110 W

- AEC-Q101 qualified
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STripFET™ F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

Product status
STD65N55F3

Product summary	
Order code	STD65N55F3
Marking	65N55F3
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	55	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	80	A
	Drain current (continuous) at T_C = 100 °C	56	A
I_{DM}(1)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
dv/dt(2)	Peak diode recovery	11	V/ns
E_{AS}(3)	Single pulse avalanche energy	390	mJ
T_j	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 65A, di/dt ≤ 300 A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{jmax}*
3. *Starting T_j = 25°C, I_D = 32 A, V_{DD} = 25 V*

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.36	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	50	°C/W

1. *When mounted on an 1- inch² FR-4 board, 2oz Cu.*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 3. Static characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	55			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 55 V			10	µA
		V_{GS} = 0 V, V_{DS} = 55 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 32 A		6.5	8.5	mΩ

1. *Defined by design, not subject to production test.*

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	2200		pF
C_{oss}	Output capacitance		-	500		pF
C_{rss}	Reverse transfer capacitance		-	25		pF
Q_g	Total gate charge	V_{DD} = 27 V, I_D = 65 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	33.5	45	nC
Q_{gs}	Gate-source charge		-	12.5		nC
Q_{gd}	Gate-drain charge		-	9.5		nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 27 V, I_D = 32 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	20	-	ns
t_r	Rise time		-	50	-	ns
$t_{d(off)}$	Turn-off delay time		-	35	-	ns
t_f	Fall time		-	11.5	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				80	A
I_{SDM}(1)	Source-drain current (pulsed)				320	A
V_{SD}	Forward on voltage	I_{SD} = 65 A, V_{GS} = 0 V	-		1.5	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	I_{SD} = 65 A, di/dt = 100 A/µs,	-	47		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 25 V, T_j = 150 °C	-	87		nC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	3.7		A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

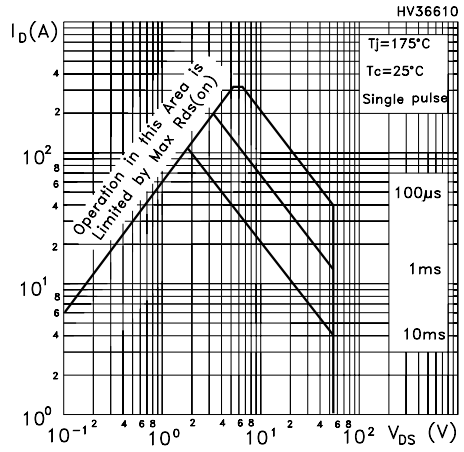


Figure 2. Thermal impedance

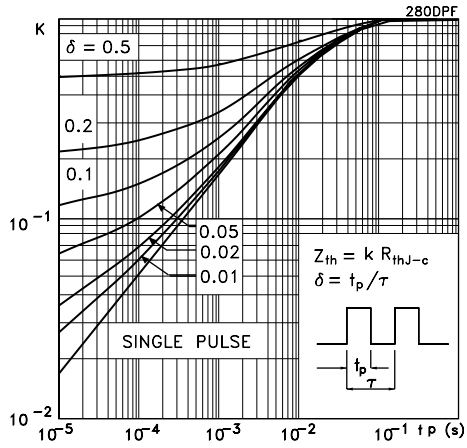


Figure 3. Output characteristics

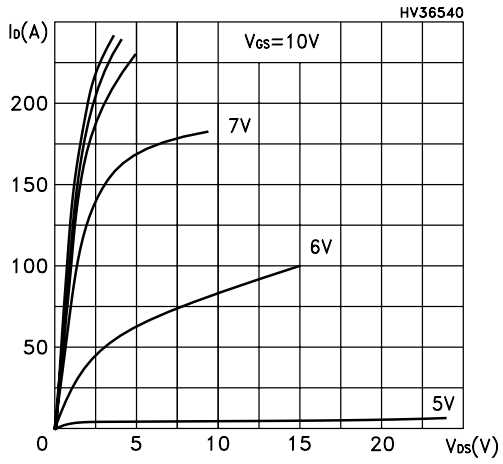


Figure 4. Transfer characteristics

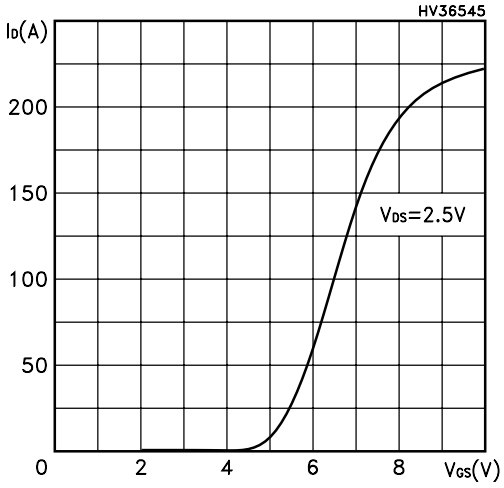


Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

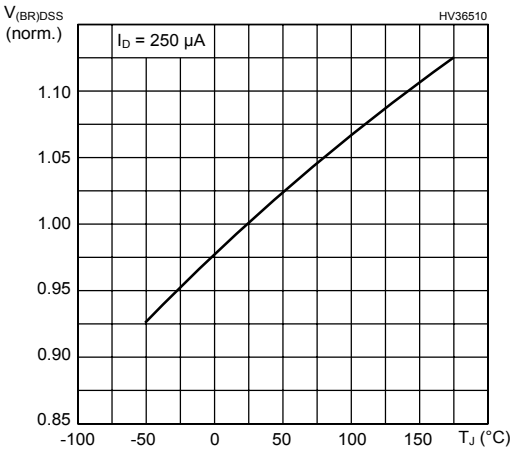


Figure 6. Static drain-source on-resistance

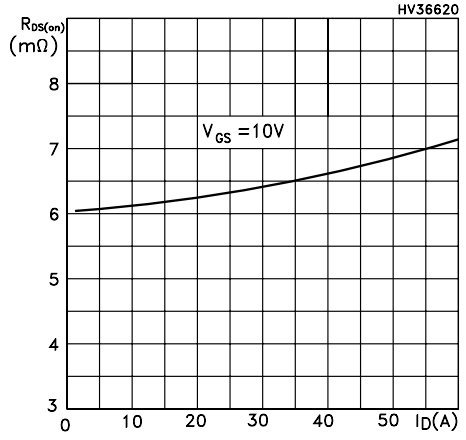


Figure 7. Gate charge vs gate-source voltage

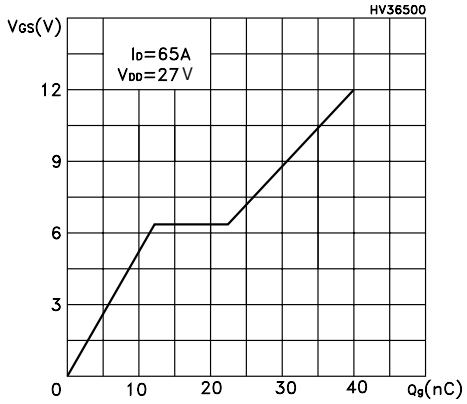


Figure 8. Capacitance variations

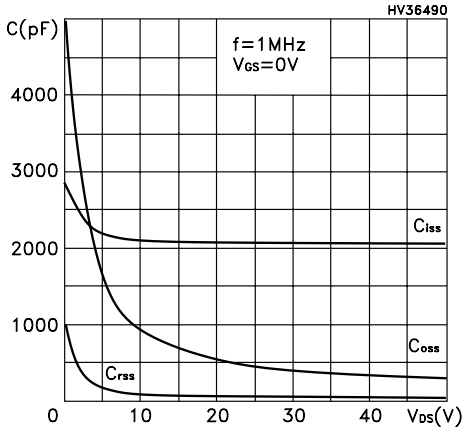


Figure 9. Normalized gate threshold voltage vs temperature

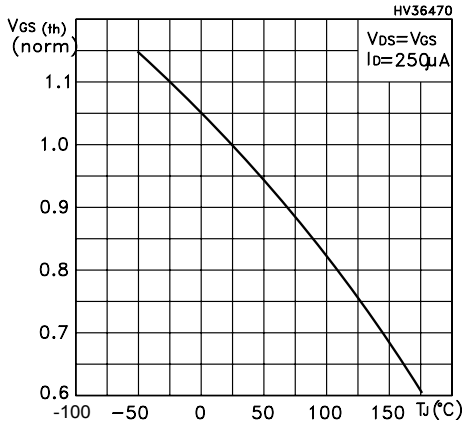


Figure 10. Normalized on-resistance vs temperature

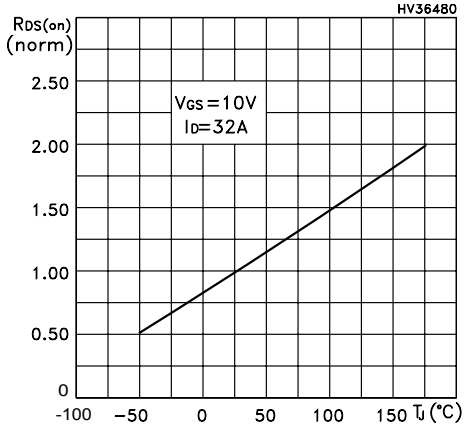
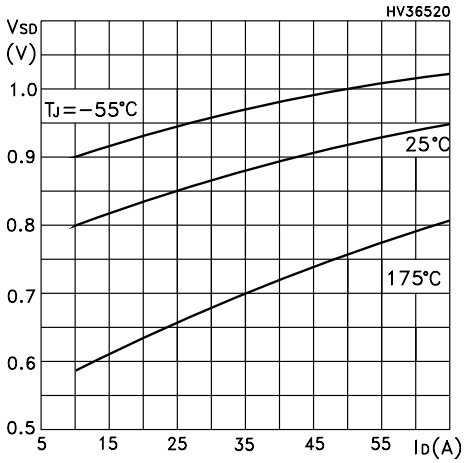


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

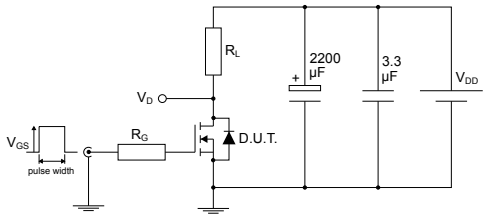


Figure 13. Test circuit for gate charge behavior

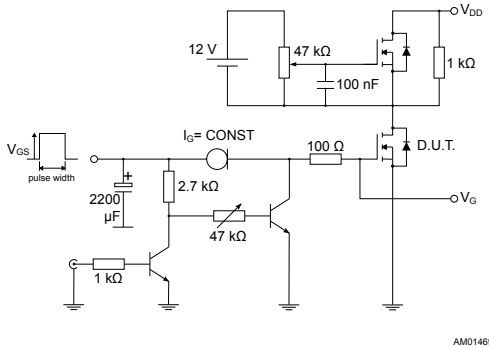


Figure 14. Test circuit for inductive load switching and diode recovery times

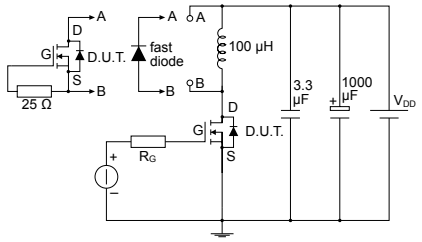


Figure 15. Unclamped inductive load test circuit

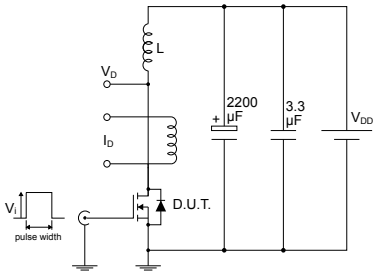


Figure 16. Unclamped inductive waveform

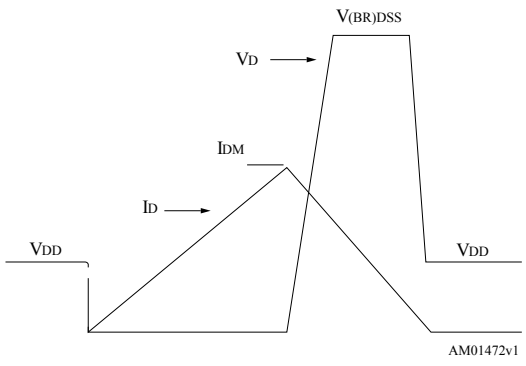
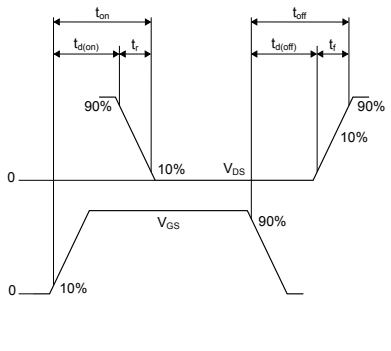


Figure 17. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 18. **DPAK (TO-252) type A2 package outline**

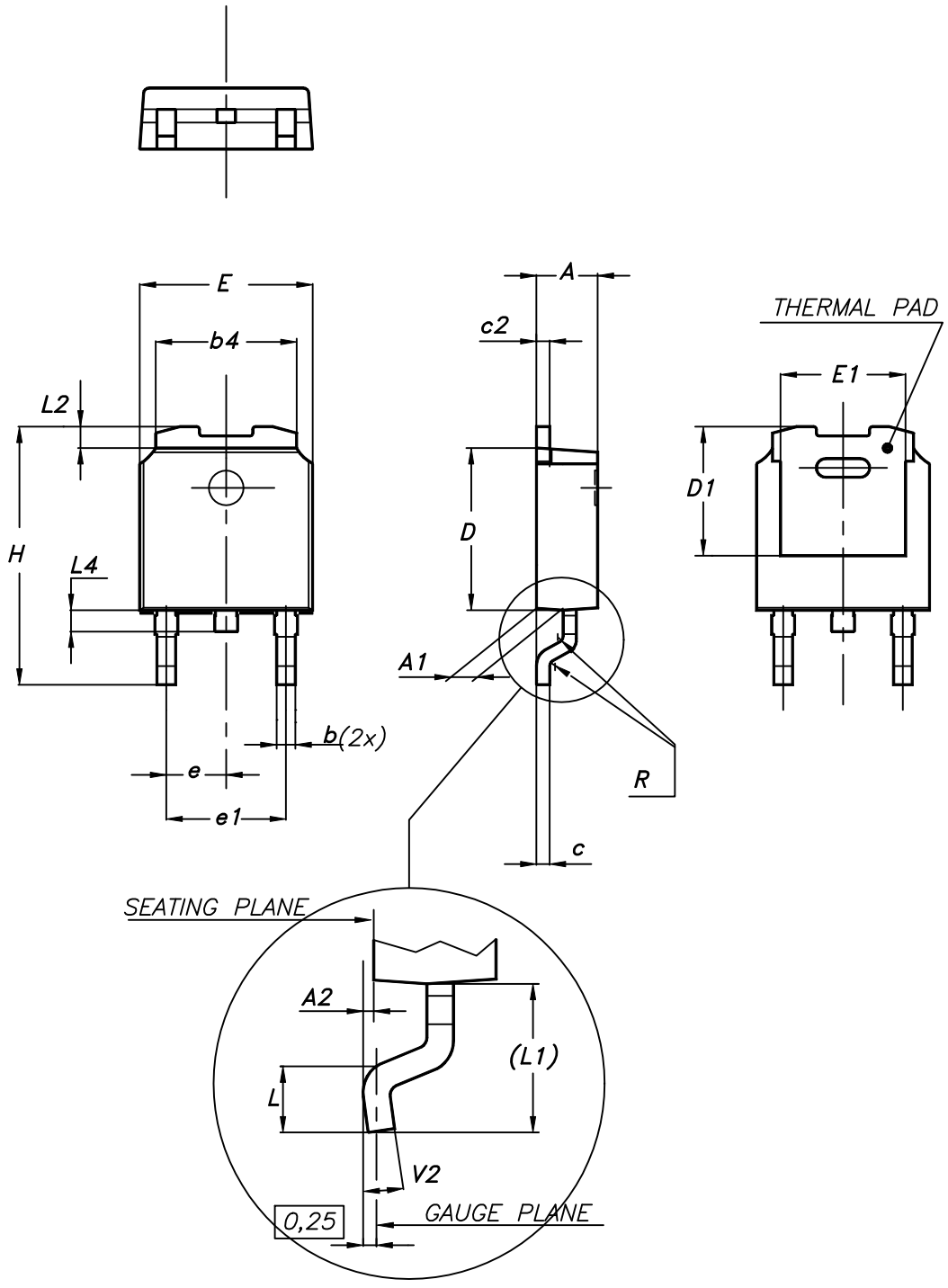
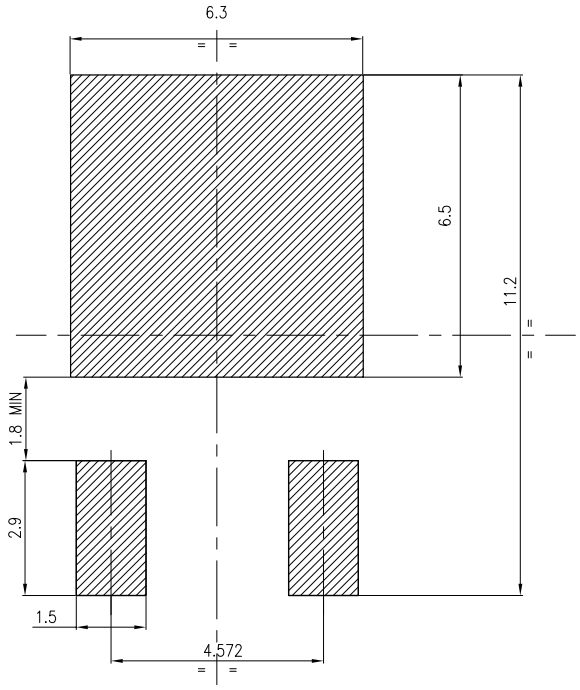


Table 7. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 19. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



4.2 DPAK (TO-252) packing information

Figure 20. **DPAK (TO-252) tape outline**

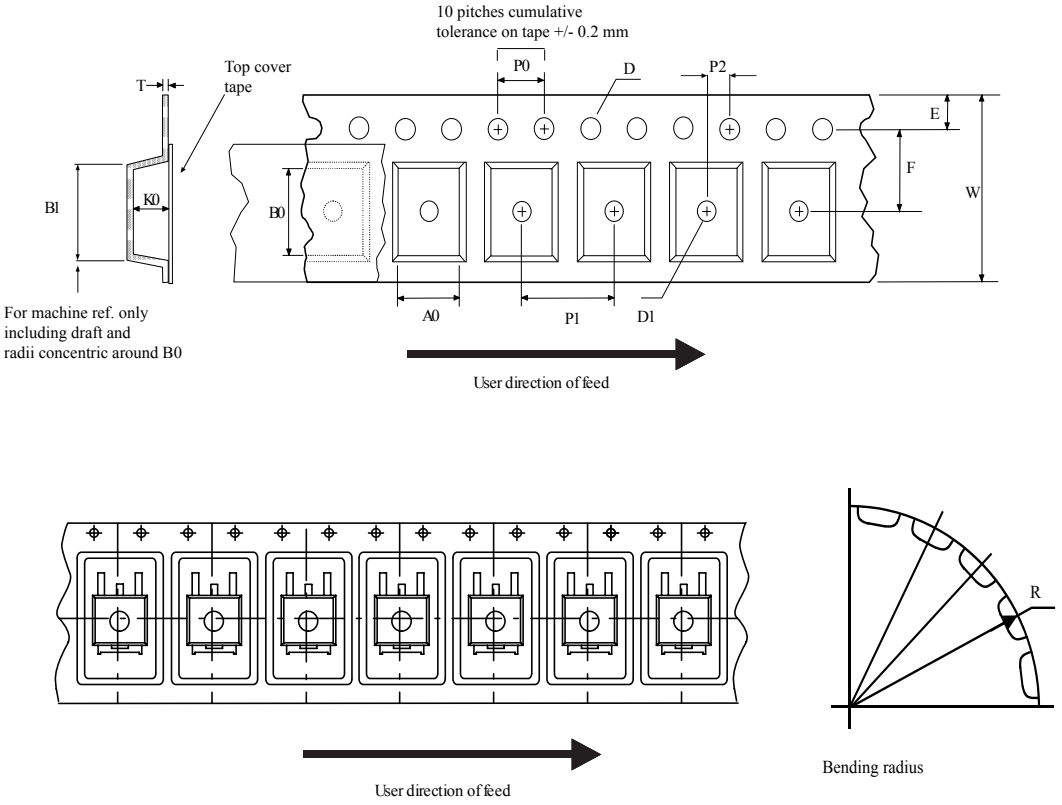


Figure 21. **DPAK (TO-252) reel outline**

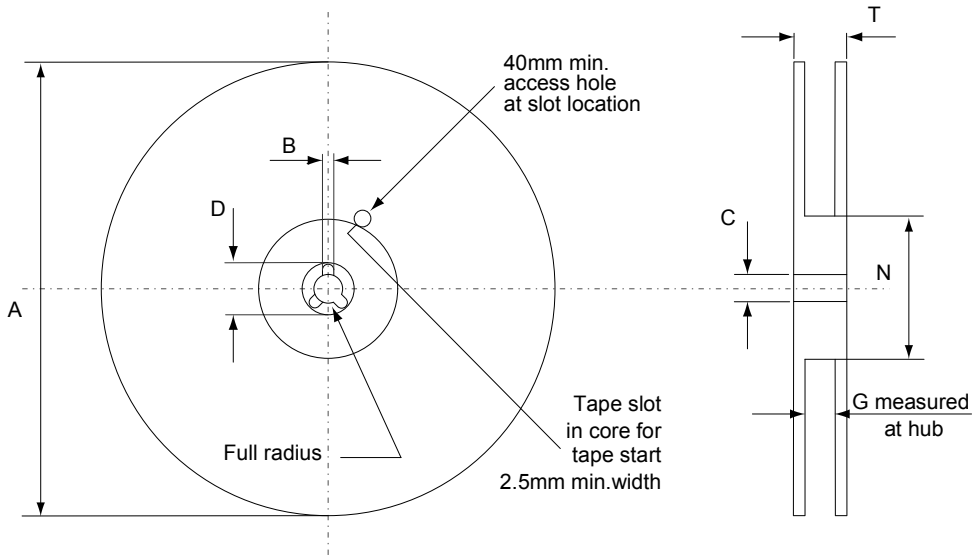


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Table 8. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 9. **Document revision history**

Date	Version	Changes
08-Feb-2007	1	First release.
22-Feb-2007	2	Description has been changed
11-May-2007	3	Improved current values
13-Feb-2018	4	Updated information on cover page. Updated Section 1 Electrical ratings and Section 2 Electrical characteristics. Updated Section 4.1 DPAK (TO-252) type A2 package information. Minor text changes

Contents

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