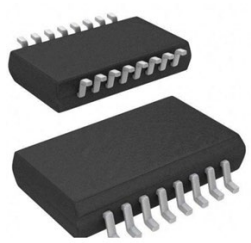
Four Channel Differential Line Receiver

PRODUCT DESCRIPTION

The MS2575/MS2575T is a low-dissipation four channel line receiver, which is applied to equalized or unequalized digital signal transmission. Four receivers all have enable function, which supports two optional inputs: active-high select and active-low select. Tri-state outputs ensure receiver directly connects to bus-structure system. And fail-safe design ensures that all output pins maintain high level when inputs are open. The MS2575 has lead SOP16 package, while MS2575T has lead TSSOP16 package.



SOP16

TSSOP16

FEATURES

- Meet or Exceed the demands of ANSI TIA/EIA-422-B,TIA/EIA-423-B and ITU Suggestion V.10 and V.11
- Low Dissipation
- ±15V Common-Mode Input Range with ±200mV Sensitivity
- Input Hysteresis: 60mV Typical Value
- Power Supply: 2.5V-5.5V
- Tri-State Outputs
- Fail-safe for Open Input
- SOP16 or TSSOP16 Package

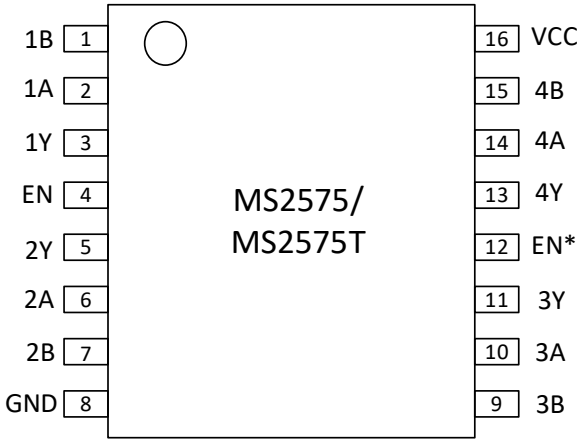
APPLICATIONS

- Reliability Automobile
- Factory Automation Equipment
- ATM and Cash Counter
- Smart Power Grid
- AC and Servo Motor Driver

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS2575	SOP16	MS2575
MS2575T	TSSOP16	MS2575T

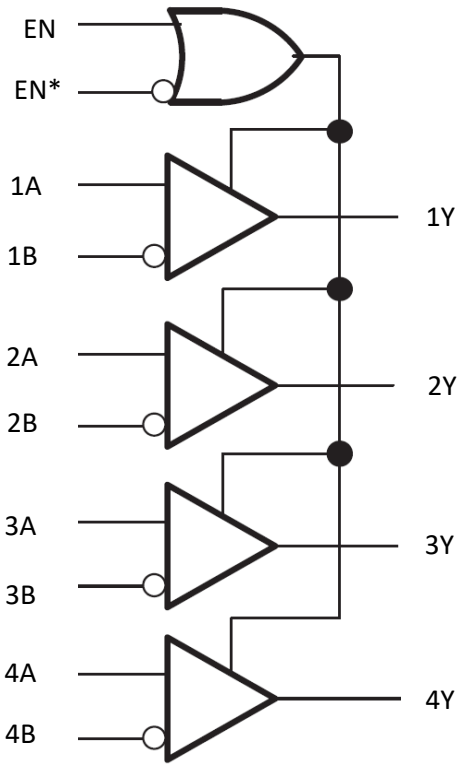
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	1B	I	Inverting Input Terminal (Channel 1)
2	1A	I	Non-inverting Input Terminal (Channel 1)
3	1Y	O	Output Terminal (Channel 1)
4	EN	I	Enable Terminal for Non-Inverting Input
5	2Y	O	Output Terminal (Channel 2)
6	2A	I	Non-inverting Input Terminal (Channel 2)
7	2B	I	Inverting Input Terminal (Channel 2)
8	GND	-	Ground
9	3B	I	Inverting Input Terminal (Channel 3)
10	3A	I	Non-inverting Input Terminal (Channel 3)
11	3Y	O	Output Terminal (Channel 3)
12	EN*	I	Enable Terminal for Inverting Input
13	4Y	O	Output Terminal (Channel 4)
14	4A	I	Non-inverting Input Terminal (Channel 4)
15	4B	I	Inverting Input Terminal (Channel 4)
16	VCC	-	Power Supply

BLOCK DIAGRAM



Function Table

Enable		Input	Output
EN	EN*	(A)-(B)	Y
L	H	X	Z
Other Conditions		VID ≥+0.2V	H
		VID ≤-0.2V	L
		-0.2V<VID<+0.2V	?
		Open	H

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply Voltage	VCC	-0.3V ~ 6V	V
Input Voltage	(A, B)	-15 ~ +15	V
EN Input Voltage	(EN, EN*)	-0.3 ~ Vcc+0.3	V
Output Voltage	(Y)	-0.3 ~ Vcc+0.3	V
Maximum Junction Temperature		+150	°C
Storage Temperature	T_{stg}	-60 ~ 150	°C
ESD Susceptibility (HBM) (bus A,B pin)		±20K	V

ELECTRICAL CHARACTERISTICS

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	2.5	5	5.5	V
High-Level Input Voltage	VIH	2		VCC	V
Low-Level Input Voltage	VIL	0		0.8	V
Common-Mode Input Voltage	VIC	-15		+15	V
High-Level Output Current	IOH			-6	mA
Low-Level Output Current	IOL			+6	mA
Operating Temperature		-40	25	125	°C

At power supply and operating temperature range,see Note 1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Differential Input High-Level Threshold Voltage	VIT+	VIC=-7V to 7V			0.2	V
		VIC=0V to 5.5V			0.1	
Differential Input Low-Level Threshold Voltage	VIT-	VIC=-7V to 7V	-0.2			V
		VIC=0V to 5.5V	-0.1			
Input Hysteresis		(VIT+)-(VIT-)		60		mV
Enable Input Clamp Voltage	VIK	VCC=4.5V, Iin=-18mA		-0.8	-1.5	V
High-Level Output Voltage	VOH	IOH = −6mA, VID = +200 mV	3.8			V
Low-Level Output Voltage	VOL	IOL = 6 mA, VID = −200 mV		0.2	0.3	V
Tri-State Output Current	IOZ	Vout = 0V or Vcc	-10	±1	+10	μA
Input Current (A, B Pin)	Ii	Vi=15V, other PIN inputs 0V		0.15		mA
		Vi=-15V, other PIN inputs 0V		-0.2		mA
High-Level Enable Current		Vi=2.7V		120	200	μA
Low--Level Enable Current		Vi=0.4V		130	-200	μA
Input Resistance		PIN to GND	130	150		kΩ
Supply Current	ICC	VCC=5.5V		0.8	1	mA

Switch Characteristics

VCC = +5.0V, TA = +25°C, Note 2,3,4,5,6

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Propagation Delay Time, High-to-Low-Level	t_{PHLD}	CL=15pF VID=200mV (Figure 1and Figure2)	80	100	110	ns
Propagation Delay Time, Low-to-High-Level	t_{PLHD}		80	100	110	ns
Delay Offset | t_{PHLD}–t_{PLHD} |	t_{SKD}		0	10	20	ps
Channel Delay Offset	t_{SK1}		0	2	5	ns
Propagation Delay						
High-Level to Hi-Z	t_{PHZ}	CL=15pF (Figure 3 and Figure 4)		35	40	ns
Low-Level to Hi-Z	t_{PLZ}			35	40	ns
Hi-Z to High-Level	t_{PZH}			4	10	ns
Hi-Z to Low-Level	t_{PZL}			4	10	ns

Note: 1. Positive Current is defined as the current flowing into device, while negative current flowing out of device. All voltage values are relative to ground shown in the table.

2. All typical values are at VCC =+5.0V, TA=+25°C.

3. The wave is added to test circuit: For input signal, f=1MHz, ZO=50Ω, tr, tf (0%–100%)≤ 1ns;

For EN and EN* signal, tr, tf≤6ns.

4. Channel Delay Offset is, for the same input signal, the difference among different channel delay time.

5. Chip Delay Offset is, for the same input signal, the difference among different chip delay time.

6. Load Capacitor includes meter pen and soldering terminal.

TEST CIRCUIT

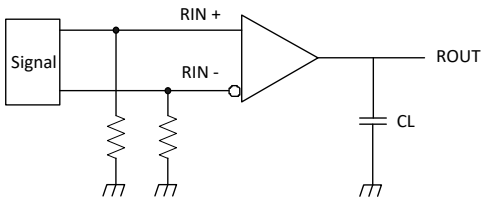


Figure 1. Propagation Delay and Switch TIme Test Circuit

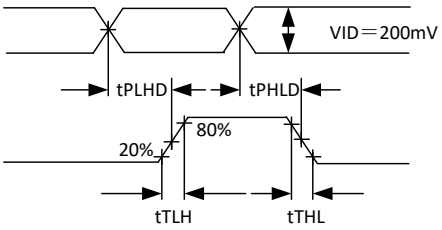


Figure 2. Propagation Delay and Switch TIme Waveform

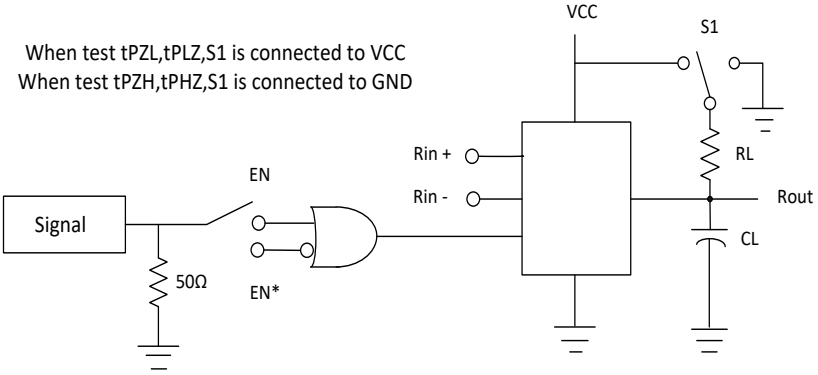


Figure 3. Tri-State Delay Test Circuit

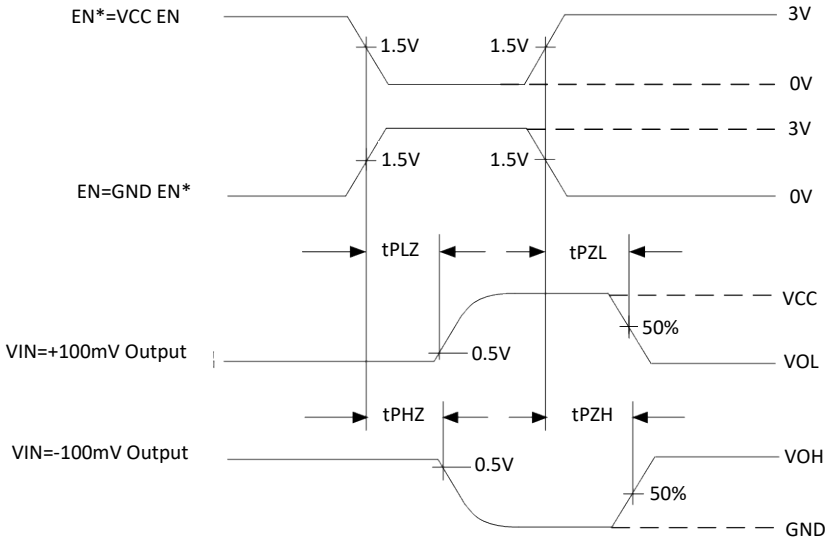
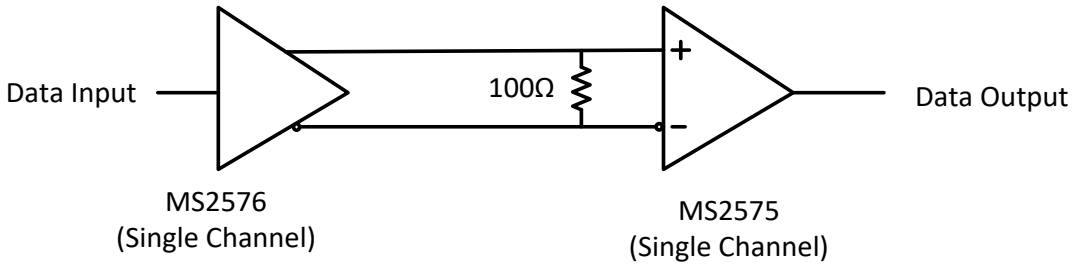


Figure 4. Tri-State Propagation Waveform

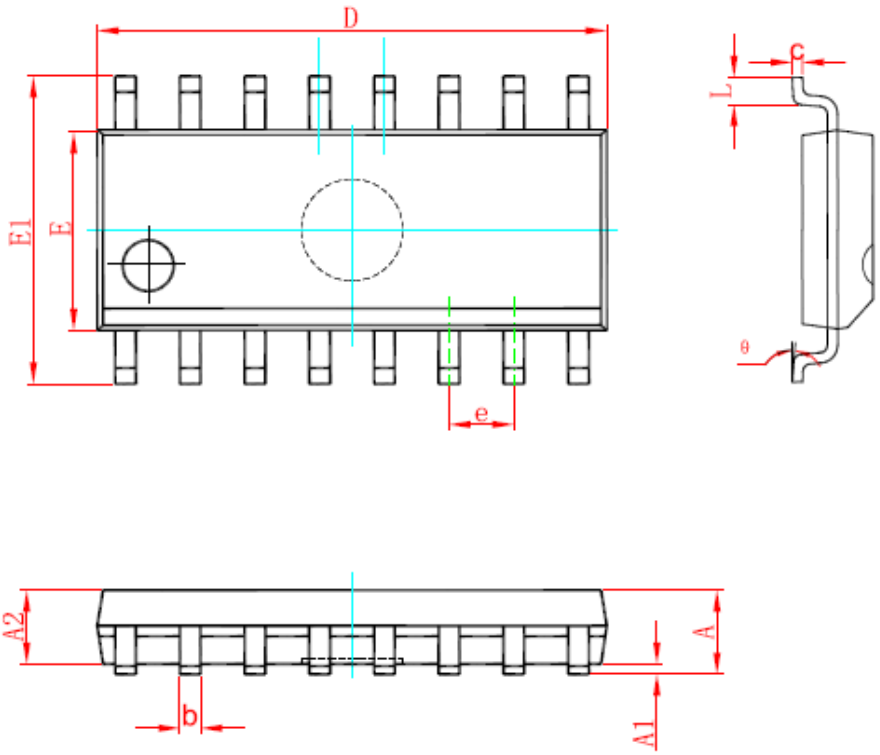
TYPICAL APPLICATION DIAGRAM



The chip is mainly applied to simple point-to-point structure shown in above figure. The structure offers signal clean transmission environment for. And transmission medium can be twisted-pair, cable and PCB trace. The typical transmission medium impedance is less than 100Ω.In order to match transmission medium impedance, differential input terminal is connected to 100Ω terminal resistance, which is as close as possible to device input terminal. The terminal resistance transforms current signal into voltage signal, which is provided for MS2575/MS2575T. For other multi-receiver structure, must consider match impedance and noise threshold range of middle connector and cable interface.

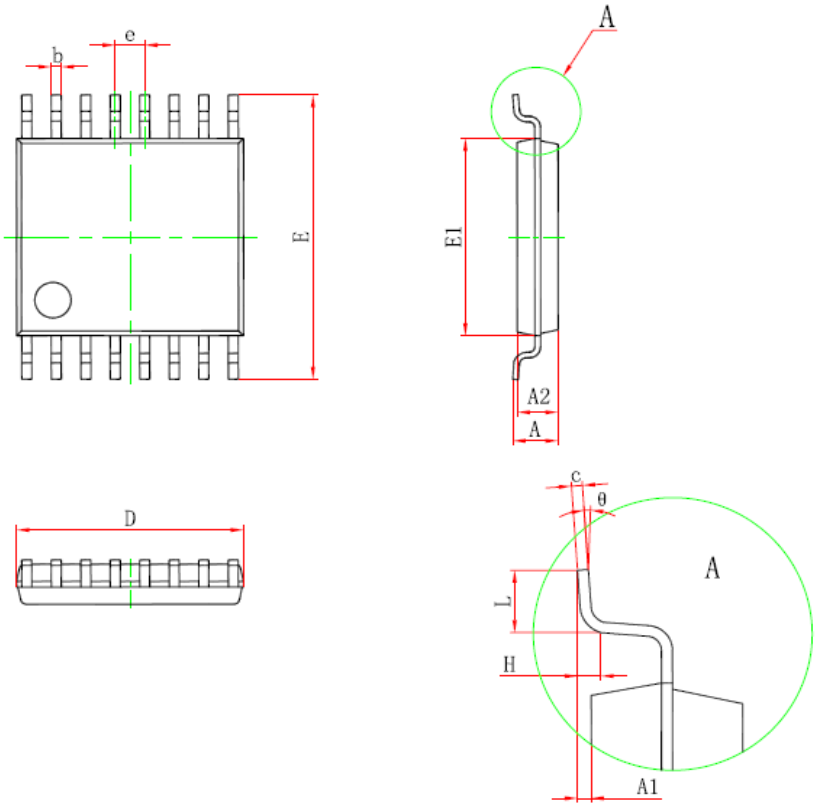
PACKAGE OUTLINE DIMENSIONS

SOP16



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

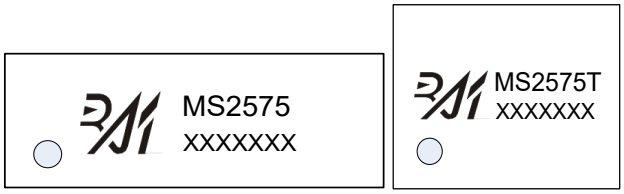
TSSOP16



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	6.250	6.550	0.246	0.258
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	4.300	4.500	0.169	0.177
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.400	1.270	0.016	0.050
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name: MS2575, MS2575T

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS2575	SOP16	4000	1	4000	8	32000
MS2575T	TSSOP16	3000	1	3000	8	24000

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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