

MX25L3233F- J/K Grade

3V, 32M-BIT [x 1/x 2/x 4]
CMOS MXSMIO[®] (SERIAL MULTI I/O)
FLASH MEMORY

Key Features

- *J Grade (Temperature = -40°C to 105°C)*
- *K Grade (Temperature = -40°C to 125°C)*
- *Hold Feature*
- *Multi I/O Support - Single I/O, Dual I/O and Quad I/O*
- *Program Suspend/Resume & Erase Suspend/Resume*

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**32M-BIT [x 1 / x 2 / x 4] CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY**

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 33,554,432 x 1 bit structure
or 16,777,216 x 2 bits (two I/O read mode) structure
or 8,388,608 x 4 bits (four I/O mode) structure
- 1024 Equal Sectors with 4K bytes each
 - Any Sector can be erased individually
- 128 Equal Blocks with 32K bytes each
 - Any Block can be erased individually
- 64 Equal Blocks with 64K bytes each
 - Any Block can be erased individually
- Power Supply Operation
 - 2.65 ~ 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Conform with AEC-Q100
- Fast read for SPI mode
 - Support Fast Read, 2READ, DREAD, 4READ, QREAD instructions
 - Configurable dummy cycle number for fast read operation
- Programming: 256byte page buffer
- Minimum 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
 - 1-byte Command code
- Advanced Security Features
 - Block Lock Protection

The BP0-BP3 and T/B status bits define the site of the area to be protected against program and erase instructions.
- Additional 4K bits secured OTP
 - Features unique identifier
 - Factory locked identifiable and customer lockable

- Auto Erase and Auto Program Algorithms
 - Automatically erases and verifies data at selected sector
 - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse width (Any page to be programmed should have page in the erased state first.)
- Status Register Feature
- Command Reset
- Program/Erase Suspend
- Program/Erase Resume
- Electronic Identification
 - JEDEC 1-byte Manufacturer ID and 2-byte Device ID
 - RES command for 1-byte Device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
 - Serial clock input
- SI/SIO0
 - Serial Data Input or Serial Data Input/Output for 2 x I/O mode or Serial Data Input/Output for 4 x I/O mode
- SO/SIO1
 - Serial Data Output or Serial Data Input/Output for 2 x I/O mode or Serial Data Input/Output for 4 x I/O mode
- WP#/SIO2
 - Hardware Write Protection or Serial Data Input/Output for 4 x I/O mode
- HOLD#/SIO3
 - To pause the device without deselecting the device or Serial Data Input/Output for 4 x I/O mode
- PACKAGE
 - 8-pin SOP (150mil)
 - 8-pin SOP (200mil)
 - 16-SOP (300mil)
 - 6x5mm 8-WSON
 - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX25L3233F is 32Mb bits Serial NOR Flash memory, which is configured as 4,194,304 x 8 internally. When it is in four I/O mode, the structure becomes 8,388,608 bits x 4. When it is in two I/O mode, the structure becomes 16,777,216 bits x 2.

MX25L3233F features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

MX25L3233F, MXSMIO[®] (Serial Multi I/O) flash memory, provides sequential read operation on the whole chip and multi-I/O features.

When it is in quad I/O mode, the SI pin, SO pin, WP# pin and HOLD# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data Input/Output.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis. Erase command is executed on 4K-byte sector, 32K-byte/64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

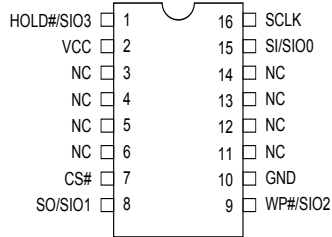
When the device is not in operation and CS# is high, it is put in standby mode.

The MX25L3233F utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

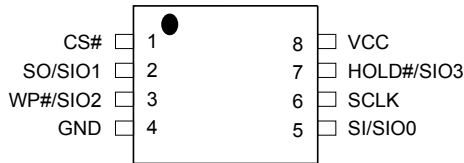
For detailed electrical specifications, please refer to MX25L3233F datasheet.

3. PIN CONFIGURATION

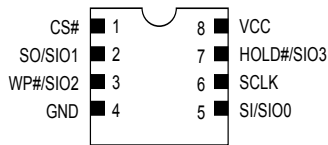
16-PIN SOP (300mil)



8-PIN SOP (150mil/200mil)



8-LAND WSON (6x5mm)



4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1xI/O)/ Serial Data Input & Output (for 2xI/O mode and 4xI/O mode)
SO/SIO1	Serial Data Output (for 1xI/O)/Serial Data Input & Output (for 2xI/O mode and 4xI/O mode)
SCLK	Clock Input
WP#/SIO2	Write protection Active Low or Serial Data Input & Output (for 4xI/O mode)
HOLD#/SIO3	To pause the device without deselecting the device or Serial data Input/Output for 4 x I/O mode
VCC	+ 3.0V Power Supply
GND	Ground
NC	No Connection

Note:

1. The pin of HOLD#/SIO3 or WP#/SIO2 will remain internal pull up function while this pin is not physically connected in system configuration. However, the internal pull up function will be disabled if the system has physical connection to HOLD#/SIO3 or WP#/SIO2 pin.

5. CONFIGURATION REGISTER

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

ODS bit

The output driver strength ODS bit are volatile bits, which indicate the output driver level of the device. The Output Driver Strength is defaulted=1 when delivered from factory. To write the ODS bit requires the Write Status Register (WRSR) instruction to be executed.

TB bit

The Top/Bottom (TB) bit is a OTP bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as "0", which means Top area protect. When it is set as "1", the protect area will change to Bottom area of the memory device. To write the TB bit requires the Write Status Register (WRSR) instruction to be executed.

Table 1. Configuration Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	DC (Dummy Cycle)	Reserved	Reserved	TB (top/bottom selected)	Reserved	Reserved	ODS
x	2READ/ 4READ Dummy Cycle	x	x	0=Top area protect 1=Bottom area protect (Default=0)	x	x	0,Output driver strength=1 1,Output driver strength=1/4 (Default=0)
x	volatile	x	x	OTP	x	x	volatile

Note: Please refer to "[Table 2. Dummy Cycle Table](#)", with "Don't Care" on other Reserved Configuration Registers.

Table 2. Dummy Cycle Table

	DC	Numbers of Dummy Cycles	Freq. (MHz)
2READ	0 (default)	4	104
	1	8	133
4READ	0 (default)	6	104
	1	10	133

6. Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC Standard, JESD216.

Figure 1. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence

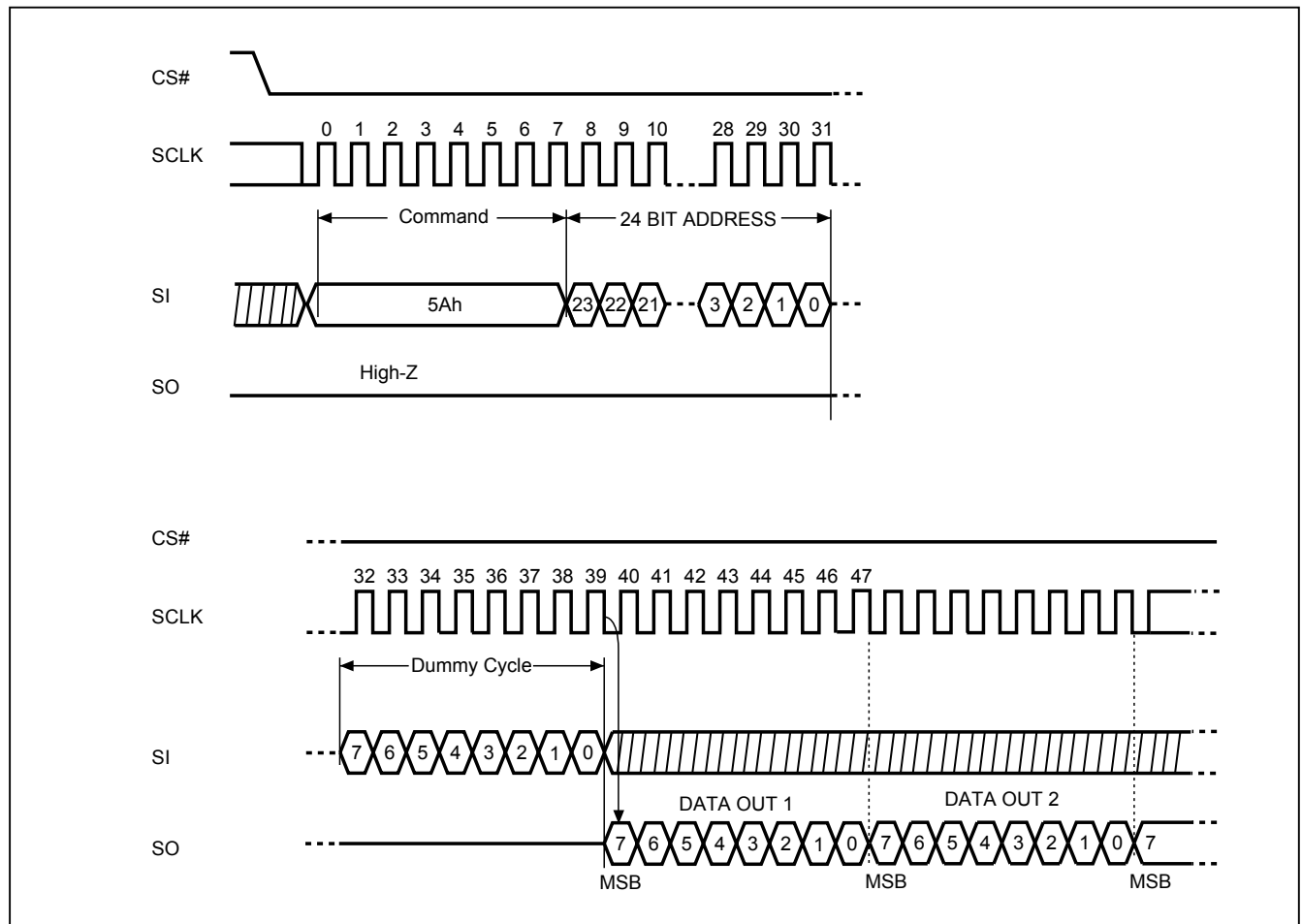


Table 3. Signature and Parameter Identification Data Values

SFDP Table (JESD216) below is for MX25L3233FM2J-08G

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
SFDP Signature	Fixed: 50444653h	00h	07:00	53h	53h
		01h	15:08	46h	46h
		02h	23:16	44h	44h
		03h	31:24	50h	50h
SFDP Minor Revision Number	Start from 00h	04h	07:00	00h	00h
SFDP Major Revision Number	Start from 01h	05h	15:08	01h	01h
Number of Parameter Headers	This number is 0-based. Therefore, 0 indicates 1 parameter header.	06h	23:16	01h	01h
Unused		07h	31:24	FFh	FFh
ID number (JEDEC)	00h: it indicates a JEDEC specified header.	08h	07:00	00h	00h
Parameter Table Minor Revision Number	Start from 00h	09h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	0Ah	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0Bh	31:24	09h	09h
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0Ch	07:00	30h	30h
		0Dh	15:08	00h	00h
		0Eh	23:16	00h	00h
Unused		0Fh	31:24	FFh	FFh
ID number (Macronix manufacturer ID)	it indicates Macronix manufacturer ID	10h	07:00	C2h	C2h
Parameter Table Minor Revision Number	Start from 00h	11h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	12h	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13h	31:24	04h	04h
Parameter Table Pointer (PTP)	First address of Macronix Flash Parameter table	14h	07:00	60h	60h
		15h	15:08	00h	00h
		16h	23:16	00h	00h
Unused		17h	31:24	FFh	FFh

Table 4. Parameter Table (0): JEDEC Flash Parameter Tables

SFDP Table below is for MX25L3233FM2J-08G

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Block/Sector Erase sizes	00: Reserved, 01: 4KB erase, 10: Reserved, 11: not support 4KB erase	30h	01:00	01b	E5h
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Required for Writing to Volatile Status Registers	0: not required 1: required 00h to be written to the status register		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: use 50h opcode, 1: use 06h opcode Note: If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31h	15:08	20h	20h
(1-1-2) Fast Read (Note2)	0=not support 1=support	32h	16	1b	F1h
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) Clocking	0=not support 1=support		19	0b	
(1-2-2) Fast Read	0=not support 1=support		20	1b	
(1-4-4) Fast Read	0=not support 1=support		21	1b	
(1-1-4) Fast Read	0=not support 1=support		22	1b	
Unused			23	1b	
Unused		33h	31:24	FFh	FFh
Flash Memory Density		37h:34h	31:00	01FF FFFFh	
(1-4-4) Fast Read Number of Wait states (Note3)	0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8	38h	04:00	0 0100b	44h
(1-4-4) Fast Read Number of Mode Bits (Note4)	Mode Bits: 000b: Not supported; 010b: 2 bits		07:05	010b	
(1-4-4) Fast Read Opcode		39h	15:08	EBh	EBh
(1-1-4) Fast Read Number of Wait states	0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8	3Ah	20:16	0 1000b	08h
(1-1-4) Fast Read Number of Mode Bits	Mode Bits: 000b: Not supported; 010b: 2 bits		23:21	000b	
(1-1-4) Fast Read Opcode		3Bh	31:24	6Bh	6Bh

SFDP Table below is for MX25L3233FM2J-08G

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
(1-1-2) Fast Read Number of Wait states	0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8	3Ch	04:00	0 1000b	08h
(1-1-2) Fast Read Number of Mode Bits	Mode Bits: 000b: Not supported; 010b: 2 bits		07:05	000b	
(1-1-2) Fast Read Opcode		3Dh	15:08	3Bh	3Bh
(1-2-2) Fast Read Number of Wait states	0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8	3Eh	20:16	0 0100b	04h
(1-2-2) Fast Read Number of Mode Bits	Mode Bits: 000b: Not supported; 010b: 2 bits		23:21	000b	
(1-2-2) Fast Read Opcode		3Fh	31:24	BBh	BBh
(2-2-2) Fast Read	0=not support 1=support	40h	00	0b	EEh
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	0b	
Unused			07:05	111b	
Unused		43h:41h	31:08	FFh	FFh
Unused		45h:44h	15:00	FFh	FFh
(2-2-2) Fast Read Number of Wait states	0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8	46h	20:16	0 0000b	00h
(2-2-2) Fast Read Number of Mode Bits	Mode Bits: 000b: Not supported; 010b: 2 bits		23:21	000b	
(2-2-2) Fast Read Opcode		47h	31:24	FFh	FFh
Unused		49h:48h	15:00	FFh	FFh
(4-4-4) Fast Read Number of Wait states	0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8	4Ah	20:16	0 0000b	00h
(4-4-4) Fast Read Number of Mode Bits	Mode Bits: 000b: Not supported; 010b: 2 bits		23:21	000b	
(4-4-4) Fast Read Opcode		4Bh	31:24	FFh	FFh
Sector Type 1 Size	Sector/block size = 2 ^N bytes (Note5) 0Ch: 4KB; 0Fh: 32KB; 10h: 64KB	4Ch	07:00	0Ch	0Ch
Sector Type 1 erase Opcode		4Dh	15:08	20h	20h
Sector Type 2 Size	Sector/block size = 2 ^N bytes 00h: N/A; 0Fh: 32KB; 10h: 64KB	4Eh	23:16	0Fh	0Fh
Sector Type 2 erase Opcode		4Fh	31:24	52h	52h
Sector Type 3 Size	Sector/block size = 2 ^N bytes 00h: N/A; 0Fh: 32KB; 10h: 64KB	50h	07:00	10h	10h
Sector Type 3 erase Opcode		51h	15:08	D8h	D8h
Sector Type 4 Size	00h: N/A, This sector type doesn't exist	52h	23:16	00h	00h
Sector Type 4 erase Opcode		53h	31:24	FFh	FFh

Table 5. Parameter Table (1): Macronix Flash Parameter Tables

SFDP Table below is for MX25L3233FM2J-08G

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)	
Vcc Supply Maximum Voltage	2000h=2.000V 2700h=2.700V 3600h=3.600V	61h:60h	07:00 15:08	00h 36h	00h 36h	
Vcc Supply Minimum Voltage	1650h=1.650V, 1750h=1.750V 2250h=2.250V, 2300h=2.300V 2350h=2.350V, 2650h=2.650V 2700h=2.700V	63h:62h	23:16 31:24	50h 26h	50h 26h	
H/W Reset# pin	0=not support 1=support	65h:64h	00	0b	F99Eh	
H/W Hold# pin	0=not support 1=support		01	1b		
Deep Power Down Mode	0=not support 1=support		02	1b		
S/W Reset	0=not support 1=support		03	1b		
S/W Reset Opcode	Reset Enable (66h) should be issued before Reset Opcode		11:04	1001 1001b (99h)		
Program Suspend/Resume	0=not support 1=support		12	1b		
Erase Suspend/Resume	0=not support 1=support		13	1b		
Unused			14	1b		
Wrap-Around Read mode	0=not support 1=support		15	1b		
Wrap-Around Read mode Opcode			66h	23:16		77h
Wrap-Around Read data length	08h:support 8B wrap-around read 16h:8B&16B 32h:8B&16B&32B 64h:8B&16B&32B&64B	67h	31:24	64h	64h	
Individual block lock	0=not support 1=support	6Bh:68h	00	0b	CFFEh	
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	1b		
Individual block lock Opcode			09:02	1111 1111b (FFh)		
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	1b		
Secured OTP	0=not support 1=support		11	1b		
Read Lock	0=not support 1=support		12	0b		
Permanent Lock	0=not support 1=support		13	0b		
Unused			15:14	11b		
Unused			31:16	FFh		FFh
Unused			6Fh:6Ch	31:00		FFh

Note 1: h/b is hexadecimal or binary.

Note 2: **(x-y-z)** means I/O mode nomenclature used to indicate the number of active pins used for the opcode (x), address (y), and data (z). At the present time, the only valid Read SFDP instruction modes are: (1-1-1), (2-2-2), and (4-4-4)

Note 3: **Wait States** is required dummy clock cycles after the address bits or optional mode bits.

Note 4: **Mode Bits** is optional control bits that follow the address bits. These bits are driven by the system controller if they are specified. (eg,read performance enhance toggling bits)

Note 5: 4KB=2⁰Ch,32KB=2⁰Fh,64KB=2¹0h

Note 6: All unused and undefined area data is blank FFh for SFDP Tables that are defined in Parameter Identification Header. All other areas beyond defined SFDP Table are reserved by Macronix.

7. ELECTRICAL SPECIFICATIONS

Table 6. DC Characteristics

Temperature = -40°C to 105°C/125°C; VCC = 2.65V- 3.6V

Symbol	Parameters	Notes	Min.	Typ.	Max. ⁽⁴⁾		Units	Test Conditions
					105°C	125°C		
ILI	Input Load Current	1			± 2		uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			± 2		uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		10	85	100	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			3	25	30	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1		2.5	7	10	mA	Normal Read(50MHz), SCLK=0.1VCC/0.9VCC, SO=Open
				10	22	25	mA	4 I/O Read(133MHz), SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		10	15		mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			10	15		mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		10	15		mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		10	15		mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5		0.8		V	
VIH	Input High Voltage		0.7VCC		VCC+0.4		V	
VOL	Output Low Voltage				0.4		V	IOL = 1.6mA
VOH	Output High Voltage		VCC-0.2				V	IOH = -100uA

Notes :

1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.
3. The value guaranteed by characterization, not 100% tested in production.
4. Under worst conditions from -40°C to 105°C/125°C and 2.65V.

Table 7. AC Characteristics

Temperature = -40°C to 105°C/125°C ; VCC = 2.65V - 3.6V

Symbol	Alt.	Parameters		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE32K, BE, CE, RES, WREN, WRDI, RDID, RDSR, WRSR		D.C.		133	MHz
fTCLK	fT	Clock Frequency for 2READ/DREAD instructions					MHz
	fQ	Clock Frequency for 4READ/QREAD instructions					MHz
f4PP		Clock Frequency for 4PP (Quad page program)					MHz
fRCLK	fR	Clock Frequency for READ instructions				50	MHz
tCH ⁽¹⁾	tCLH	Clock High Time	Others (fSCLK)	45% x (1/fSCLK)			ns
			Normal Read (fRCLK: 50MHz)	9			ns
tCL ⁽¹⁾	tCLL	Clock Low Time	Others (fSCLK)	45% x (1/fSCLK)			ns
			Normal Read (fRCLK)	9			ns
tCLCH ⁽²⁾		Clock Rise Time (peak to peak)		0.1			V/ns
tCHCL ⁽²⁾		Clock Fall Time (peak to peak)		0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)		4			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		4			ns
tDVCH	tDSU	Data In Setup Time		2			ns
tCHDX	tDH	Data In Hold Time		3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)		4			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)		4			ns
tSHSL	tCSH	CS# Deselect Time	From Read to next Read	15			ns
			From Write/Erase/Program to Read Status Register	50			ns
tSHQZ ⁽²⁾	tDIS	Output Disable Time	2.65V-3.6V			10	ns
			3.0V-3.6V			8	ns
tHLCH		HOLD# Setup Time (relative to SCLK)		5			ns
tCHHH		HOLD# Hold Time (relative to SCLK)		5			ns
tHHCH		HOLD Setup Time (relative to SCLK)		5			ns
tCHHL		HOLD Hold Time (relative to SCLK)		5			ns
tHHQX	tLZ	HOLD to Output Low-Z Loading=30pF	2.65V-3.6V			10	ns
			3.0V-3.6V			8	ns
tHLQZ	tHZ	HOLD# to Output High-Z Loading=30pF	2.65V-3.6V			10	ns
			3.0V-3.6V			8	ns
tCLQV	tV	Clock Low to Output Valid VCC=2.65V-3.6V	Loading: 15pF			6	ns
			Loading: 30pF			8	ns
tCLQX	tHO	Output Hold Time		1			ns
tWHSL ⁽³⁾		Write Protect Setup Time		20			ns
tSHWL ⁽³⁾		Write Protect Hold Time		100			ns
tESL ⁽⁴⁾		Erase Suspend Latency				20	us
tPSL ⁽⁴⁾		Program Suspend Latency				20	us
tPRS ⁽⁵⁾		Latency between Program Resume and next Suspend		0.3	100		us
tERS ⁽⁶⁾		Latency between Erase Resume and next Suspend		0.3	200		us

Symbol	Alt.	Parameters	Min.	Typ.	Max. ⁽⁷⁾		Unit
					105°C	125°C	
tRCR		Recovery Time from Read	20				us
tRCP		Recovery Time from Program	20				us
tRCE		Recovery Time from Erase	12				ms
tDP		CS# High to Deep Power-down Mode				10	us
tRES1		CS# High to Standby Mode without Electronic Signature Read				100	us
tRES2		CS# High to Standby Mode with Electronic Signature Read				100	us
tW		Write Status Register Cycle Time				40	ms
tBP		Byte-Program		10	60	70	us
tPP		Page Program Cycle Time		0.33	1.6	2.0	ms
tSE		Sector Erase Cycle Time (4KB)		25	240	260	ms
tBE32K		Block Erase Cycle Time (32KB)		0.14	0.7	0.8	s
tBE		Block Erase Cycle Time (64KB)		0.25	1.1	1.2	s
tCE		Chip Erase Cycle Time		10	33	35	s
tWSR		Write Security Register Time				1	ms
		Erase/Program cycles	100,000				cycles

Notes:

1. tCH + tCL must be greater than or equal to 1/ fC.
2. The value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
4. Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".
5. For tPRS, minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.
6. For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.
7. Under worst conditions from -40°C to 105°C/125°C and 2.65V.

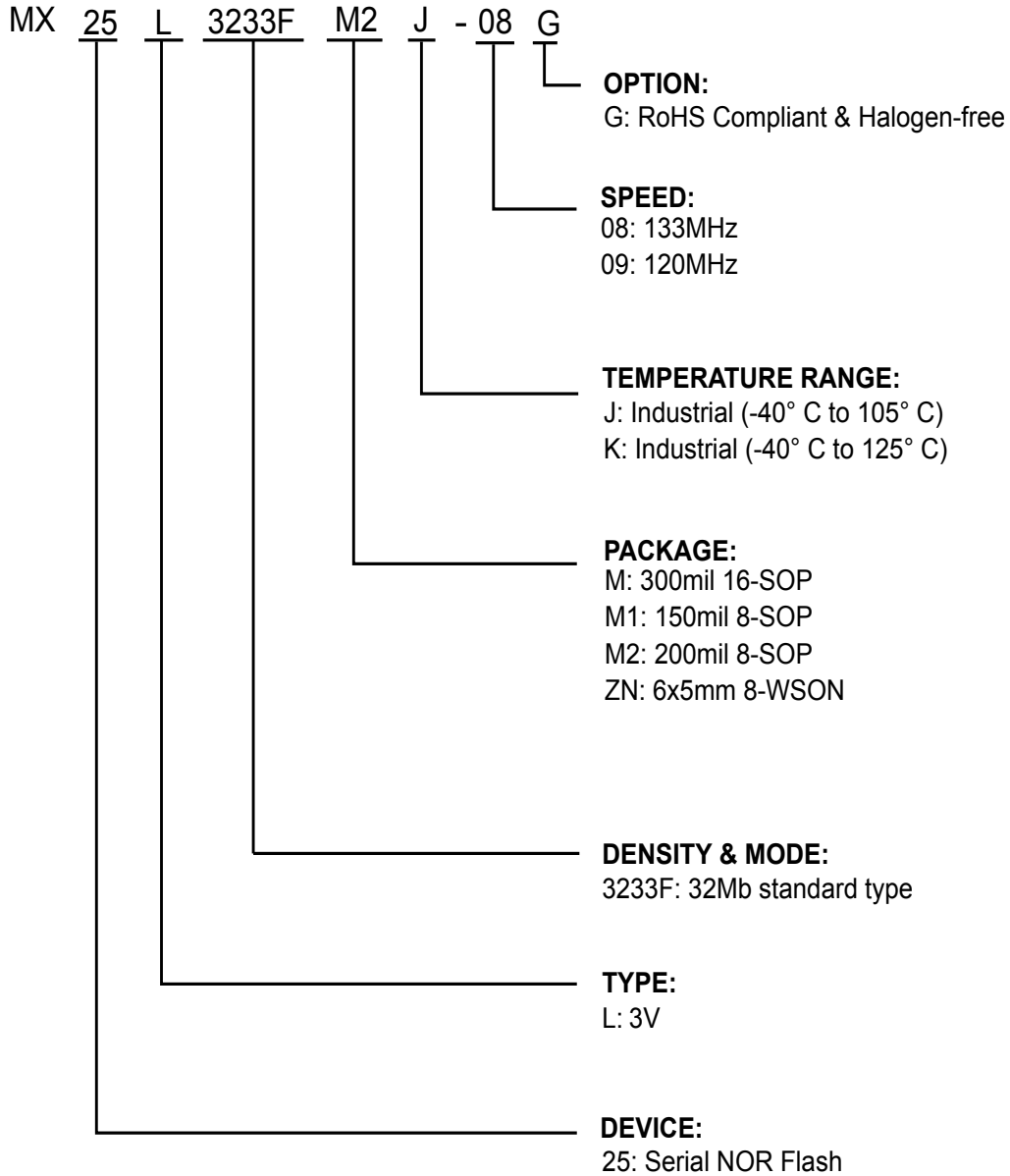


8. ORDERING INFORMATION

Please contact Macronix regional sales for the latest product selection and available form factors.

PART NO.	CLOCK (MHz)	TEMPERATURE	PACKAGE	Remark
MX25L3233FMJ-08G	133	-40°C to 105°C	300mil 16-SOP	
MX25L3233FM1J-08G	133	-40°C to 105°C	150mil 8-SOP	
MX25L3233FM2J-08G	133	-40°C to 105°C	200mil 8-SOP	
MX25L3233FM2K-09G	120	-40°C to 125°C	200mil 8-SOP	
MX25L3233FZNJ-08G	133	-40°C to 105°C	6x5mm 8-WSON	

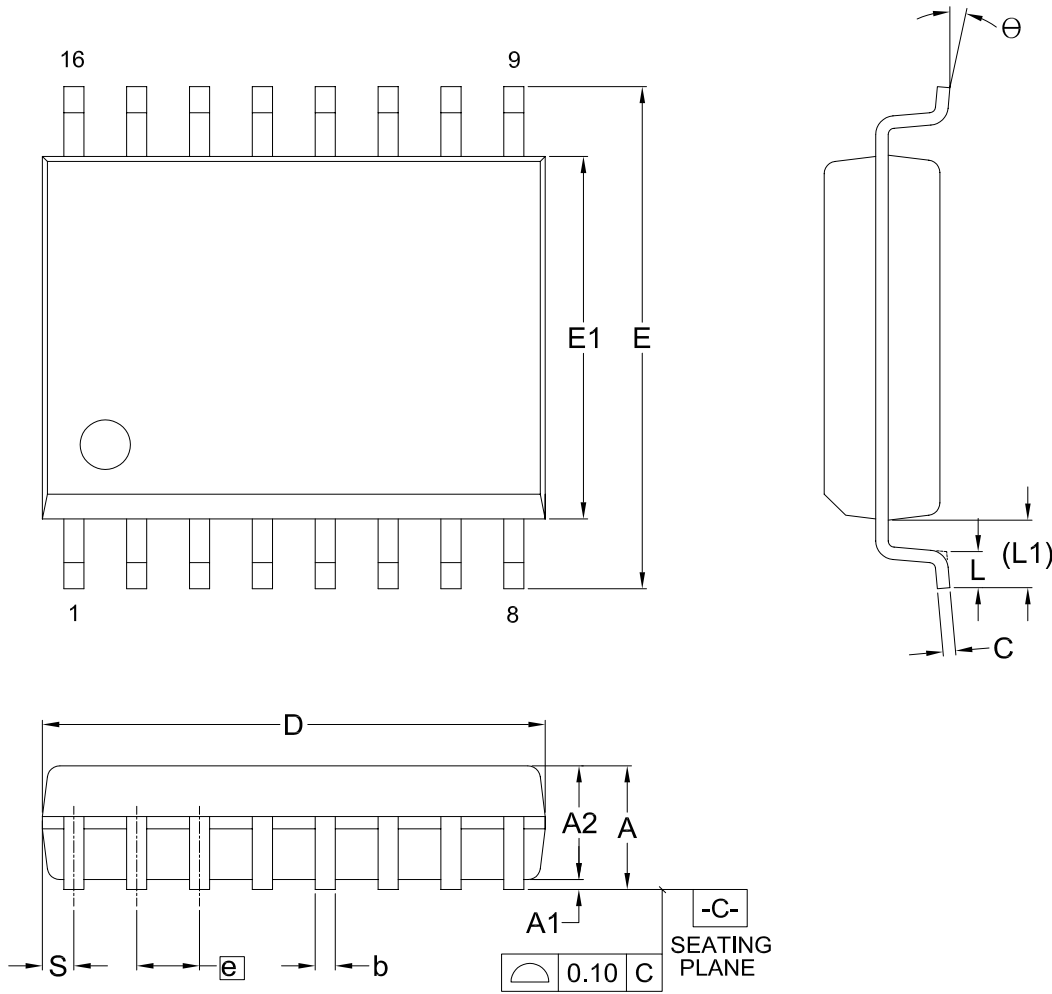
9. PART NAME DESCRIPTION



10. PACKAGE INFORMATION

9-1. 16-pin SOP (300mil)

Doc. Title: Package Outline for SOP 16L (300MIL)

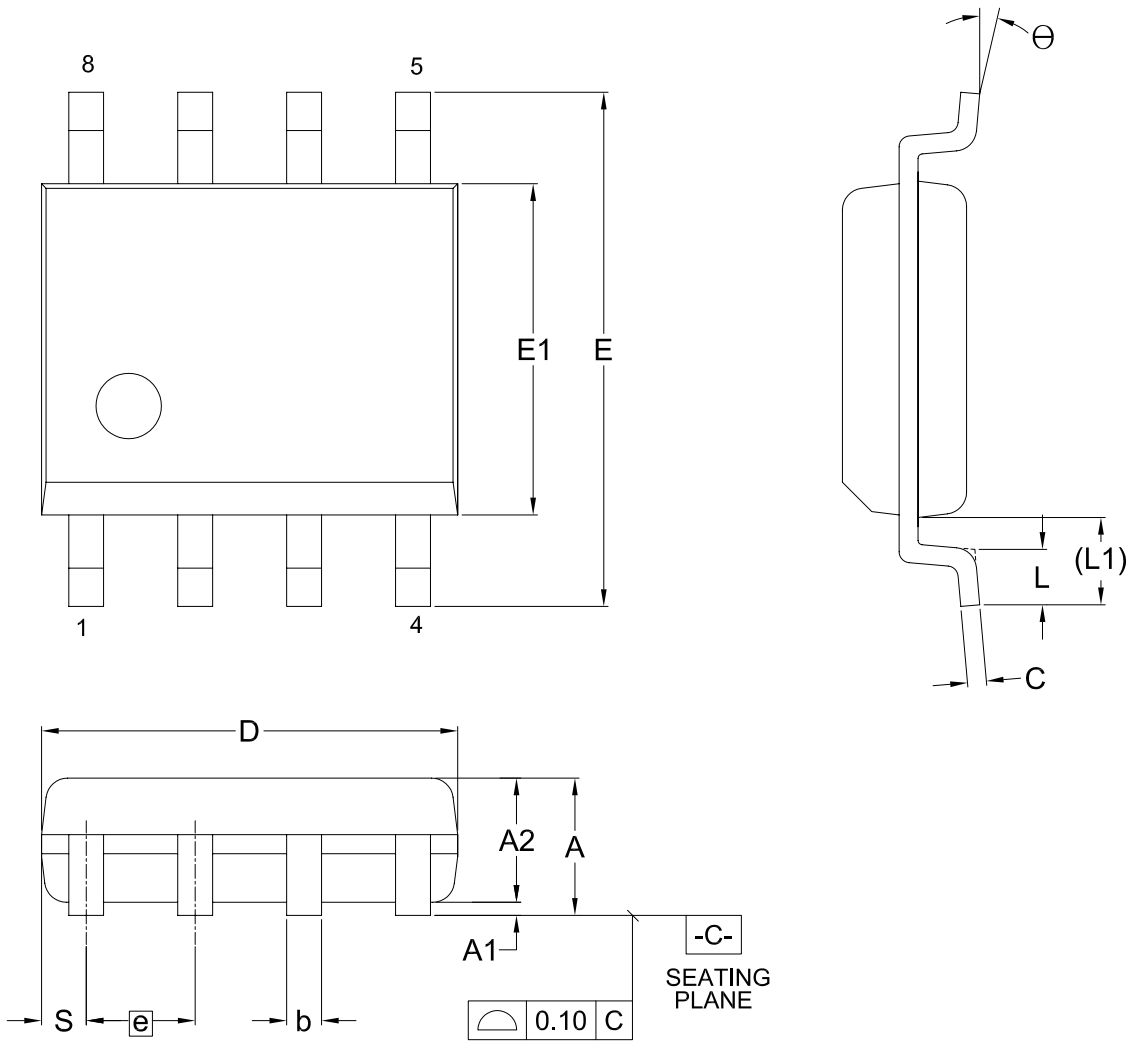


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
UNIT														
mm	Min.	—	0.10	2.25	0.31	0.20	10.10	10.10	7.42	—	0.40	1.31	0.51	0°
	Nom.	—	0.20	2.35	0.41	0.25	10.30	10.30	7.52	1.27	0.84	1.44	0.64	5°
	Max.	2.65	0.30	2.45	0.51	0.30	10.50	10.50	7.60	—	1.27	1.57	0.77	8°
Inch	Min.	—	0.004	0.089	0.012	0.008	0.397	0.397	0.292	—	0.016	0.052	0.020	0°
	Nom.	—	0.008	0.093	0.016	0.010	0.405	0.405	0.296	0.050	0.033	0.057	0.025	5°
	Max.	0.104	0.012	0.096	0.020	0.012	0.413	0.413	0.299	—	0.050	0.062	0.030	8°

10-1. 8-SOP (150mil)

Doe. Title: Package Outline for SOP 8L (150MIL)

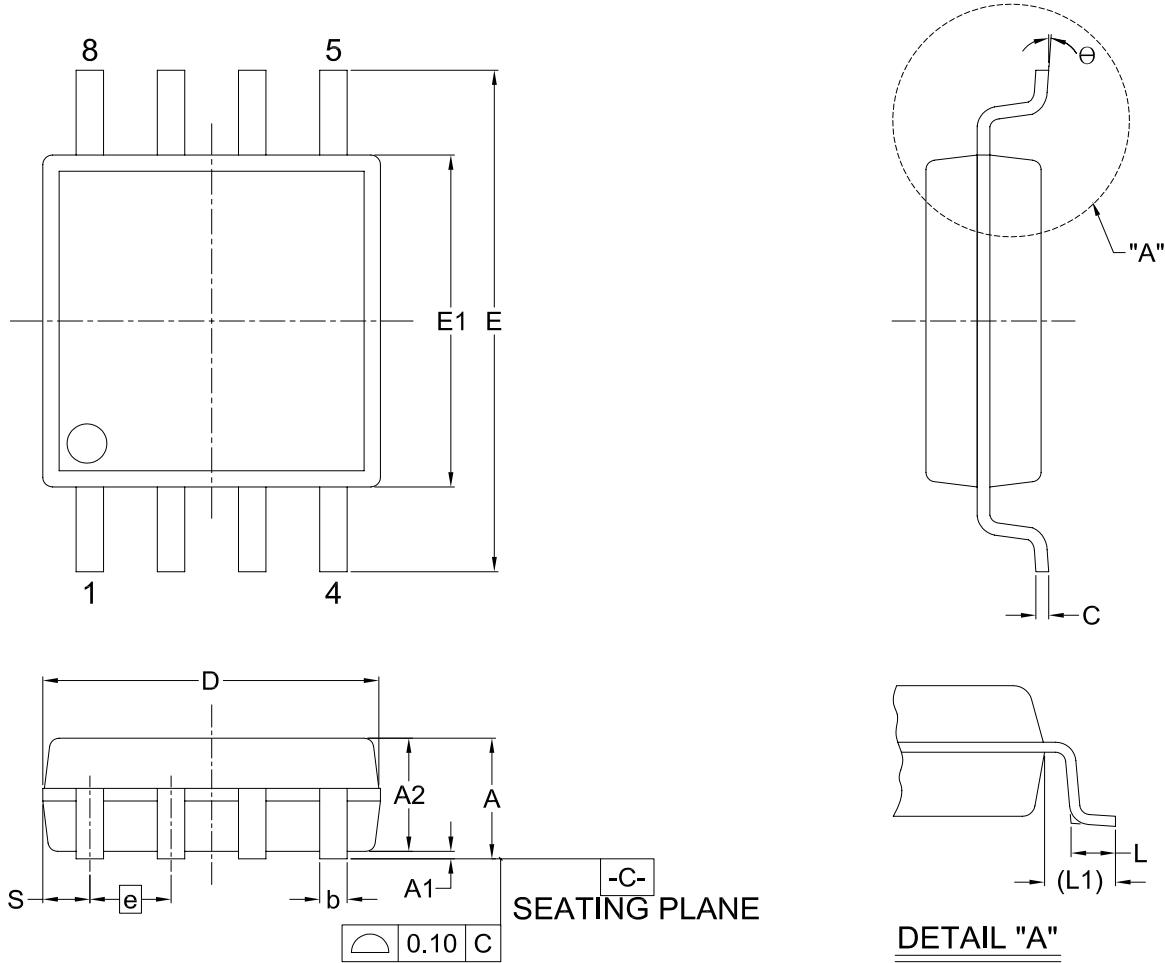


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	--	0.10	1.35	0.36	0.15	4.77	5.80	3.80	--	0.46	0.85	0.41	0°
	Nom.	--	0.15	1.45	0.41	0.20	4.90	5.99	3.90	1.27	0.66	1.05	0.54	5°
	Max.	1.75	0.20	1.55	0.51	0.25	5.03	6.20	4.00	--	0.86	1.25	0.67	8°
Inch	Min.	--	0.004	0.053	0.014	0.006	0.188	0.228	0.150	--	0.018	0.033	0.016	0°
	Nom.	--	0.006	0.057	0.016	0.008	0.193	0.236	0.154	0.050	0.026	0.041	0.021	5°
	Max.	0.069	0.008	0.061	0.020	0.010	0.198	0.244	0.158	--	0.034	0.049	0.026	8°

10-2. 8-SOP (200mil)

Doc. Title: Package Outline for SOP 8L 200MIL (official name - 209MIL)

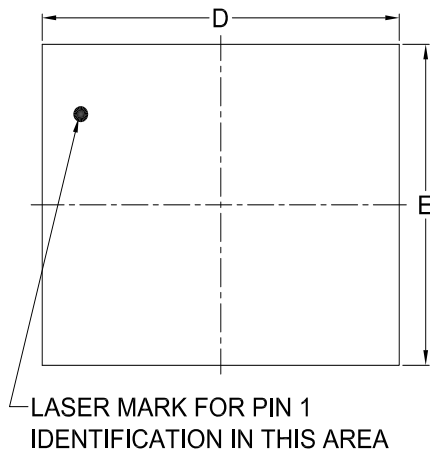


Dimensions (inch dimensions are derived from the original mm dimensions)

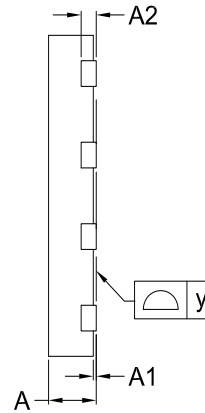
SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
UNIT														
mm	Min.	1.75	0.05	1.70	0.36	0.19	5.13	7.70	5.18	—	0.50	1.21	0.62	0°
	Nom.	1.95	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5°
	Max.	2.16	0.20	1.91	0.51	0.25	5.33	8.10	5.38	—	0.80	1.41	0.88	8°
Inch	Min.	0.069	0.002	0.067	0.014	0.007	0.202	0.303	0.204	—	0.020	0.048	0.024	0°
	Nom.	0.077	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5°
	Max.	0.085	0.008	0.075	0.020	0.010	0.210	0.319	0.212	—	0.031	0.056	0.035	8°

10-3. 8-land WSON (6x5mm)

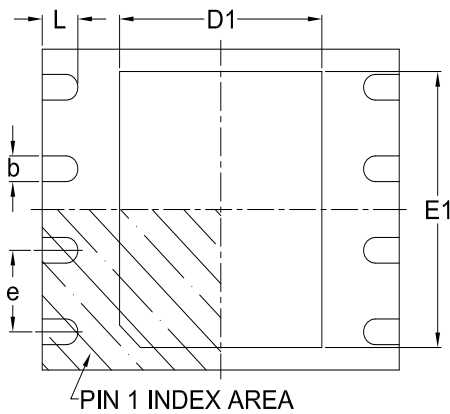
Doc. Title: Package Outline for WSON 8L (6x5x0.8MM, LEAD PITCH 1.27MM)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Note:

This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	D	D1	E	E1	L	e	y
UNIT												
mm	Min.	0.70	—	—	0.35	5.90	3.35	4.90	3.95	0.55	—	0.00
	Nom.	—	—	0.20	0.40	6.00	3.40	5.00	4.00	0.60	1.27	—
	Max.	0.80	0.05	—	0.48	6.10	3.45	5.10	4.05	0.65	—	0.05
Inch	Min.	0.028	—	—	0.014	0.232	0.132	0.193	0.156	0.022	—	0.00
	Nom.	—	—	0.008	0.016	0.236	0.134	0.197	0.157	0.024	0.05	—
	Max.	0.032	0.002	—	0.019	0.240	0.136	0.201	0.159	0.026	—	0.002

11. REVISION HISTORY

Revision	Descriptions	Page
April 06, 2016		
1.0	1. Initial Release.	All
September 19, 2017		
1.1	1. Added SFDP tables.	P7-12
	2. Updated " <i>10-3. 8-land WSON (6x5mm)</i> " in Min./Max. D1, E1 and L values.	P21
	3. Format modification.	P18-21
	4. Added the note for the internal pull up status of HOLD#/SIO3 and WP#/SIO2.	P5



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