Quad Comparator with Accurate Reference Output

Data Sheet

ADCMP396

FEATURES

- High accuracy reference output voltage: 1 V ± 0.9%
- Single-supply voltage operation: 2.3 V to 5.5 V
- Rail-to-rail, common-mode input voltage range
- Low input offset voltage across V_{CMR}: 1 mV typical
- Guarantees comparator output logic low from V_{CC} = 0.9 V to undervoltage lockout (UVLO)
- Operating temperature range: −40°C to +125°C
- 16-lead standard small outline package (SOIC)

APPLICATIONS

- Battery management/monitoring
- Power supply detection
- Window comparators
- Threshold detectors/discriminators
- Microprocessor systems

FUNCTIONAL BLOCK DIAGRAM

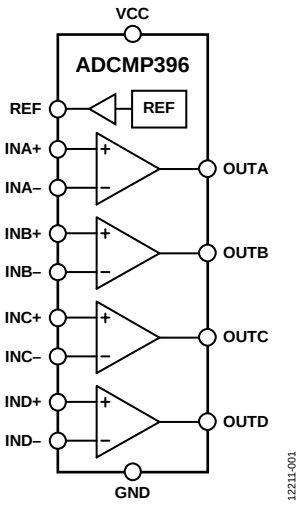

Figure 1.

GENERAL DESCRIPTION

The ADCMP396 is a quad, rail-to-rail input, low power comparator ideal for use in general-purpose applications. The device operates from a supply voltage of 2.3 V to 5.5 V and draws a minimal amount of current. The quad ADCMP396 consumes only 41.61 µA of supply current. The low voltage and low current operation of the ADCMP396 makes it ideal for battery-powered systems.

The ADCMP396 features a common-mode input voltage range of 200 mV beyond rails, an offset voltage of 1 mV typical across the full common-mode range, and a UVLO monitor. In addition, the design of the comparator allows a defined output state upon power-up. The comparator generates a logic low output while the supply voltage is less than the UVLO threshold.

The ADCMP396 incorporates a 1 V ± 0.9% buffered reference voltage. The reference voltage output can directly connect to the comparator input to serve as the trip value for precise monitoring and detection of positive voltage. It can also act as an offset when monitoring the negative voltage.

The ADCMP396 is available in a 16-lead narrow-body SOIC package, and it is specified to operate over the −40°C to +125°C extended temperature range.

Rev. 0 Document Feedback

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REVISION HISTORY

4/14—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2.3 V to 5.5 V, T_A = −40°C to +125°C, V_{CMR} = −200 mV to V_{CC} + 200 mV, unless otherwise noted. Typical values are at T_A = 25°C.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
Supply Voltage	V_{CC}	2.3		5.5	V	
		0.9		$UVLO_{RISE}$	V	Guarantees comparator output low
V_{CC} Quiescent Current	I_{CC}		41.61	59.4	µA	All outputs in high-Z state, V_{OD}[1] = 0.1 V
			41.32	56.45	µA	All outputs low, V_{OD}[1] = 0.1 V
UNDERVOLTAGE LOCKOUT						
V_{CC} Rising	$UVLO_{RISE}$	2.062	2.162	2.262	V	
Hysteresis	$UVLO_{HYS}$	5	25	50	mV	
REFERENCE OUTPUT						
Reference Output Voltage	V_{REF}	0.991	1	1.008	V	I_{REF} = ±1 mA, T_A = −40°C to +85°C
		0.991	1	1.008	V	I_{REF} = ±1 mA
COMPARATOR INPUT						
Common-Mode Input Range	V_{CMR}	−200		V_{CC} + 200	mV	
Input Offset Voltage	V_{OS}		0.5	2.5	mV	IN+ = IN− = 1 V
			0.5	2.5	mV	IN+ = IN− = 1 V, T_A = −40°C to +85°C
			1	5	mV	
			1	5	mV	T_A = −40°C to +85°C
Input Offset Current	I_{OS}			10	nA	V_{CMR} = −50 mV to V_{CC} + 50 mV
Input Bias Current	I_{BIAS}			±30	nA	IN+ = IN− = 1 V
				±80	nA	V_{CMR} = −50 mV to V_{CC} + 50 mV
				±10	nA	V_{CMR} = −50 mV to V_{CC} + 50 mV, T_A = −40°C to +85°C
Input Hysteresis	V_{HYST}		3	4	mV	V_{CM} = 1 V
			6	8	mV	
COMPARATOR OUTPUT						
Output Low Voltage	V_{OL}		0.1	0.3	V	V_{CC} = 2.3 V, I_{SINK} = 2.5 mA
			0.01	0.15	V	V_{CC} = 0.9 V, I_{SINK} = 100 µA
Output Leakage Current	I_{LEAK}			150	nA	V_{OUT} = 0 V to 5.5 V
COMPARATOR CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	60	80		dB	
Common-Mode Rejection Ratio	CMRR	50	74		dB	
Voltage Gain	A_V		132		dB	
Rise Time[2]	t_R		1.1		µs	V_{OUT} = 10% to 90% of V_{CC}
Fall Time[2]	t_F		0.15		µs	V_{OUT} = 90% to 10% of V_{CC}
Propagation Delay						
Input Rising[2]	t_{PROP_R}		4.72		µs	V_{CM} = 1 V, V_{CC} = 2.3 V, 10 mV overdrive
			4.94		µs	V_{CM} = 1 V, V_{CC} = 5 V, 10 mV overdrive
				2.78	µs	V_{CM} = 1 V, V_{CC} = 2.3 V, 100 mV overdrive
				3.23	µs	V_{CM} = 1 V, V_{CC} = 5 V, 100 mV overdrive
Input Falling[2]	t_{PROP_F}		4.46		µs	V_{CM} = 1 V, V_{CC} = 2.3 V, 10 mV overdrive
			9.5		µs	V_{CM} = 1 V, V_{CC} = 5 V, 10 mV overdrive
				2	µs	V_{CM} = 1 V, V_{CC} = 2.3 V, 100 mV overdrive
				4.21	µs	V_{CM} = 1 V, V_{CC} = 5 V, 100 mV overdrive

[1] V_{OD} = overdrive voltage.
[2] R_{PULLUP} = 10 kΩ, and C_L = 50 pF.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC Pin	−0.3 V to +6 V
All INx+ and INx− Pins	−0.3 V to +6 V
All OUTx Pins	−0.3 V to +6 V
Reference Load Current, I_{REF}	±1 mA
OUTx Pins Sink Current, I_{SINK}	10 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead Narrow-Body SOIC	80	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

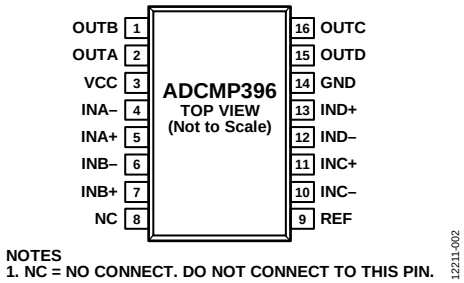


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUTB	Comparator B Output, Open Drain.
2	OUTA	Comparator A Output, Open Drain.
3	VCC	Device Supply Input.
4	INA–	Comparator A Inverting Input.
5	INA+	Comparator A Noninverting Input.
6	INB–	Comparator B Inverting Input.
7	INB+	Comparator B Noninverting Input.
8	NC	No Connect. Do not connect to this pin.
9	REF	Reference Output. This pin can be used to set up the comparator threshold.
10	INC–	Comparator C Inverting Input.
11	INC+	Comparator C Noninverting Input.
12	IND–	Comparator D Inverting Input.
13	IND+	Comparator D Noninverting Input.
14	GND	Device Ground.
15	OUTD	Comparator D Output, Open Drain.
16	OUTC	Comparator C Output, Open Drain.

TYPICAL PERFORMANCE CHARACTERISTICS

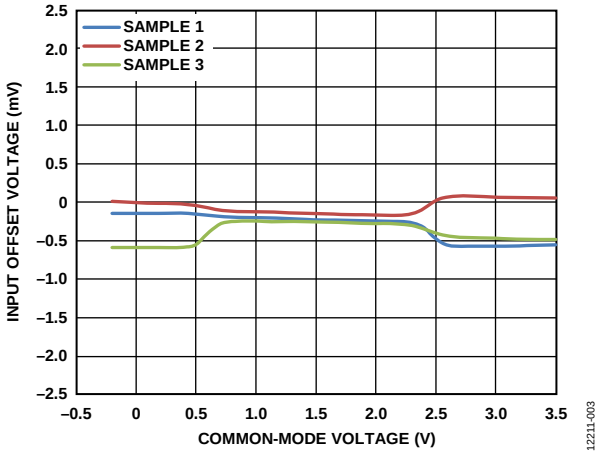


Figure 3. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{CC} = 3.3 V

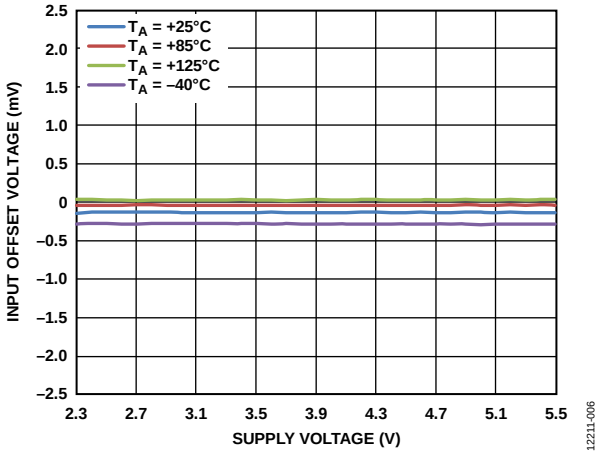


Figure 6. Input Offset Voltage (V_{OS}) vs. Supply Voltage (V_{CC}), V_{CM} = 1 V

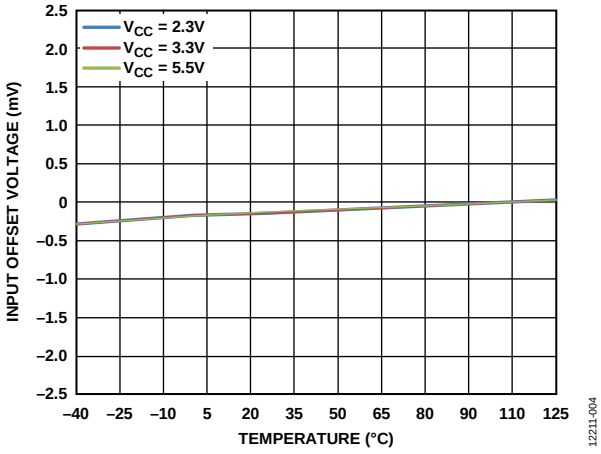


Figure 4. Input Offset Voltage (V_{OS}) vs. Temperature for Various Supply Voltages (V_{CC}), V_{CM} = 1 V

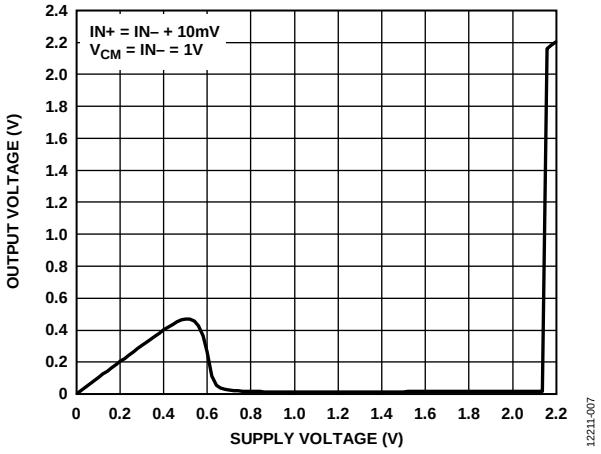


Figure 7. Output Voltage (V_{OUT}) vs. Supply Voltage (V_{CC}), R_{PULLUP} = 10 kΩ

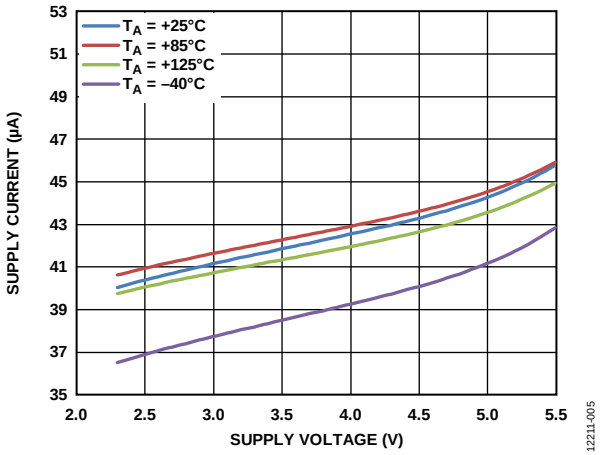


Figure 5. Supply Current (I_{CC}) vs. Supply Voltage (V_{CC}) at Output Low Voltage (V_{OL})

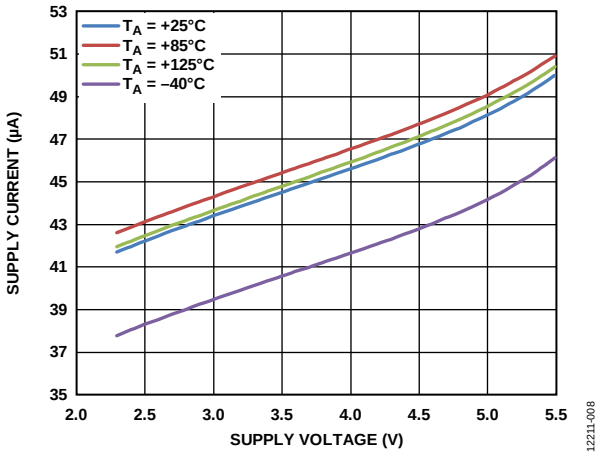


Figure 8. Supply Current (I_{CC}) vs. Supply Voltage (V_{CC}) at Output High Voltage (V_{OH})

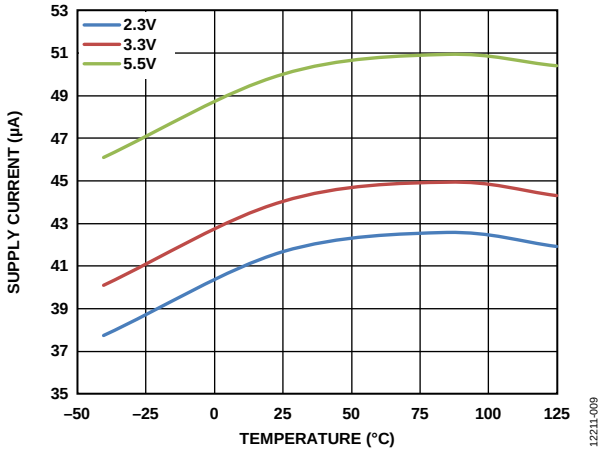


Figure 9. Supply Current (I_{CC}) vs. Temperature at Output High Voltage (V_{OH})

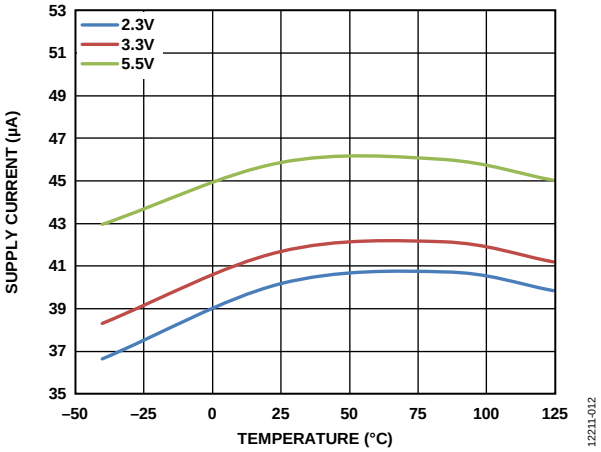


Figure 12. Supply Current (I_{CC}) vs. Temperature at Output Low Voltage (V_{OL})

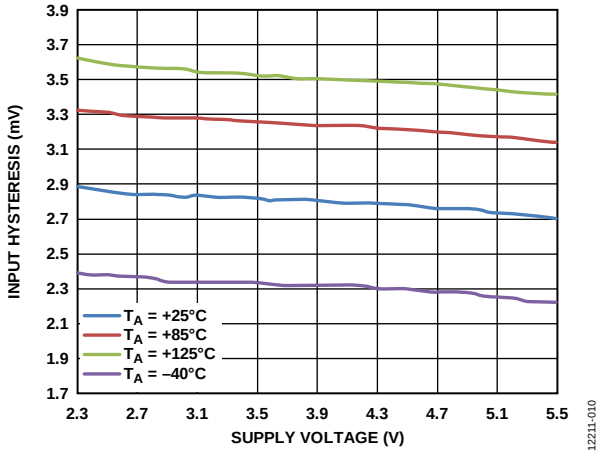


Figure 10. Input Hysteresis vs. Supply Voltage (V_{CC}), V_{CM} = 1 V

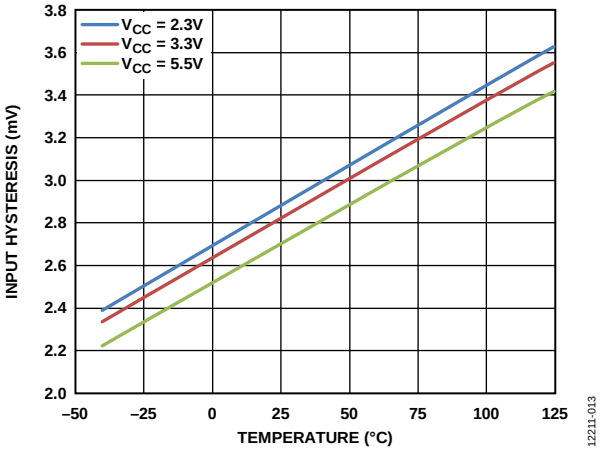


Figure 13. Input Hysteresis vs. Temperature, V_{CM} = 1 V

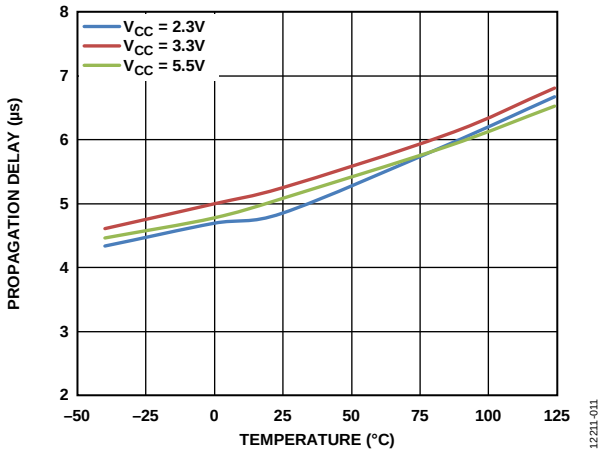


Figure 11. Propagation Delay vs. Temperature, Low to High, 10 mV Input Overdrive

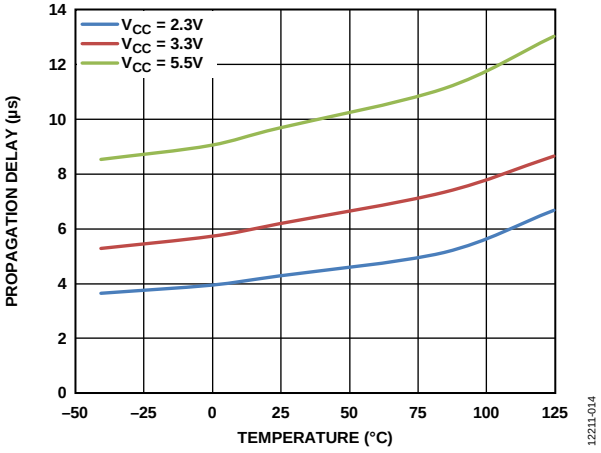


Figure 14. Propagation Delay vs. Temperature, High to Low, 10 mV Input Overdrive

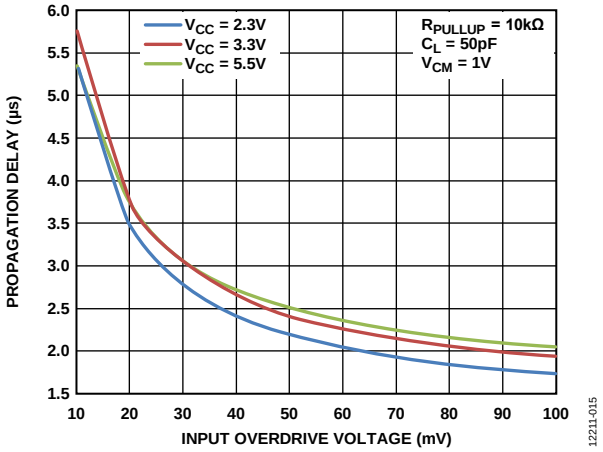


Figure 15. Propagation Delay vs. Input Overdrive Voltage, Low to High

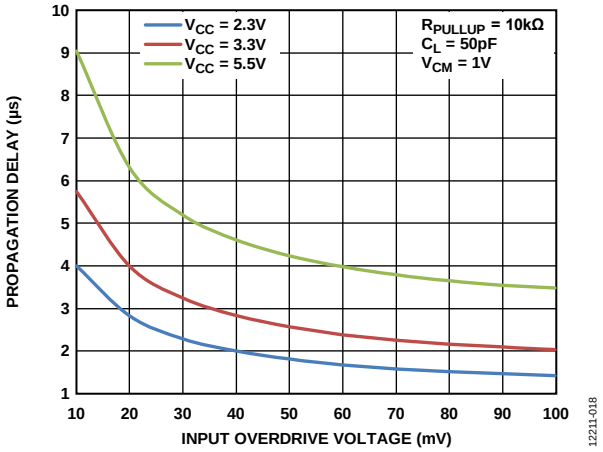


Figure 18. Propagation Delay vs. Input Overdrive Voltage, High to Low

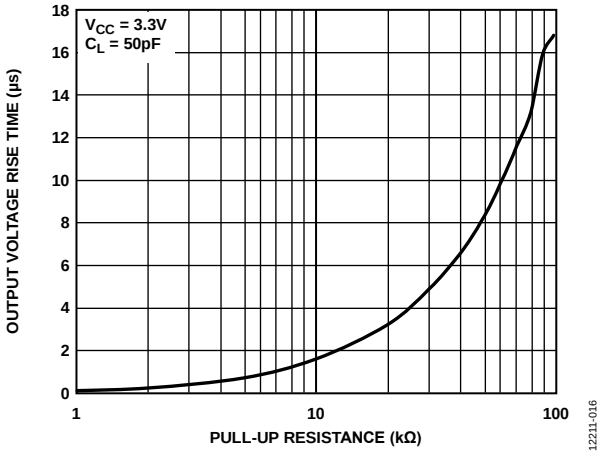


Figure 16. Output Voltage Rise Time (t_R) vs. Pull-Up Resistance (R_{PULLUP})

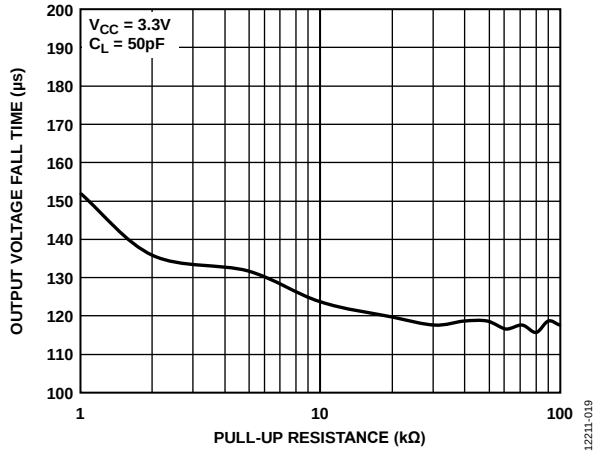


Figure 19. Output Voltage Fall Time (t_F) vs. Pull-Up Resistance (R_{PULLUP})

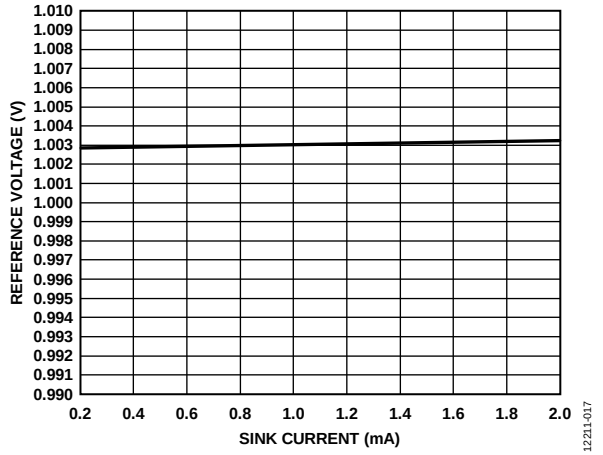


Figure 17. Reference Voltage (V_{REF}) vs. Sink Current (I_{SINK}) REF Pin, V_{CC} = 3.3 V

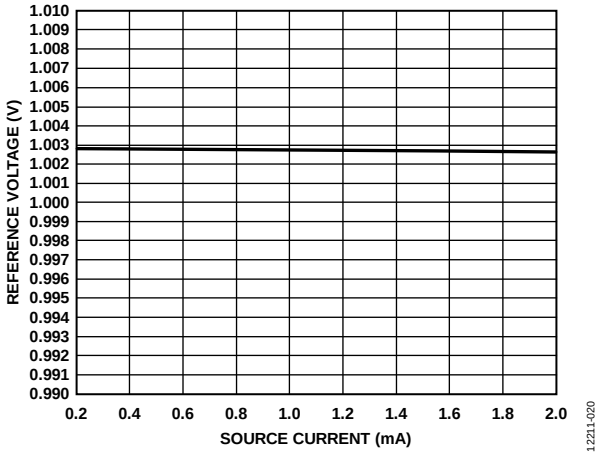


Figure 20. Reference Voltage (V_{REF}) vs. Source Current (I_{SOURCE}) REF Pin, V_{CC} = 3.3 V

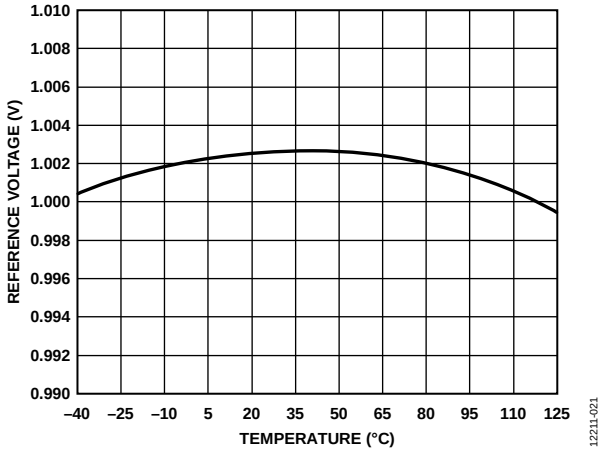


Figure 21. Reference Voltage (V_{REF}) vs. Temperature, V_{CC} = 3.3 V

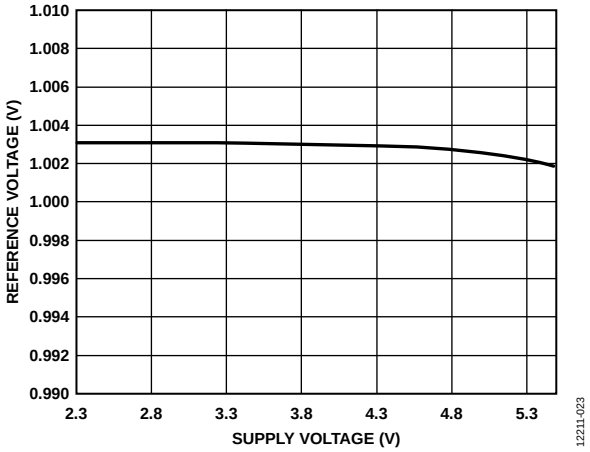


Figure 23. Reference Voltage (V_{REF}) vs. Supply Voltage (V_{CC})

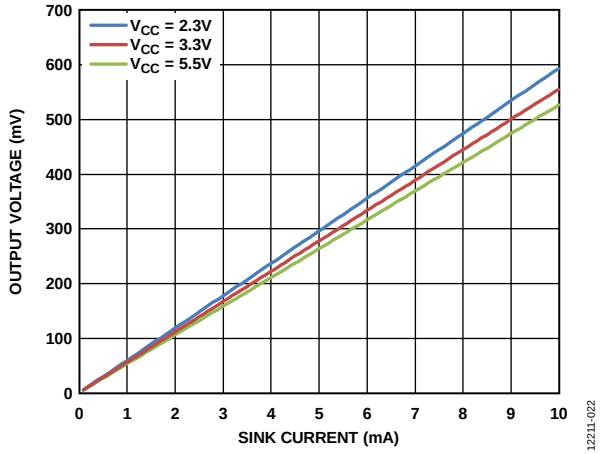


Figure 22. Output Voltage (V_{OUT}) Low vs. Sink Current (I_{SINK}) for Various Supply Voltages

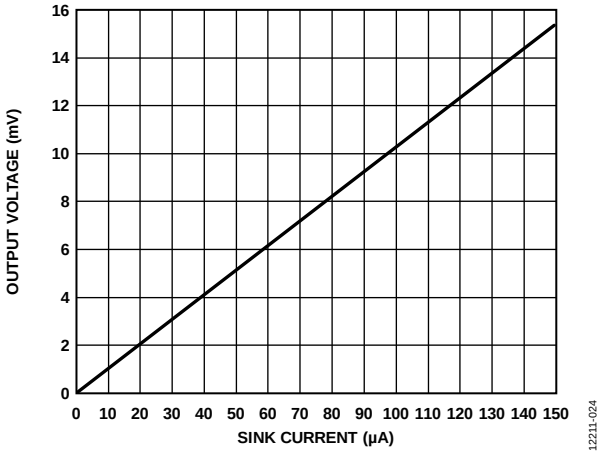


Figure 24. Output Voltage (V_{OUT}) Low vs. Sink Current (I_{SINK}), V_{CC} = 0.9 V

THEORY OF OPERATION

BASIC COMPARATOR

In its most basic configuration, a comparator can be used to convert an analog input signal to a digital output signal (see Figure 25). The analog signal on INx+ is compared to the voltage on INx−, and the voltage at OUTx is either high or low, depending on whether INx+ is at a higher or lower potential than INx−, respectively.

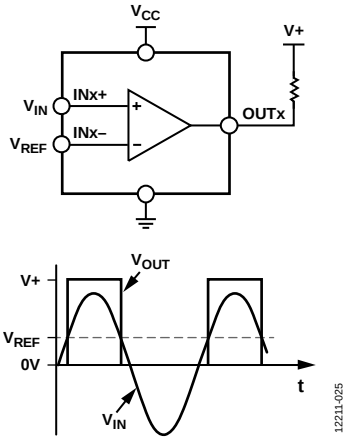


Figure 25. Basic Comparator and Input and Output Signals

RAIL-TO-RAIL INPUT (RRI)

Using a CMOS nonRRI stage (that is, a single differential pair) limits the input voltage to approximately one gate-to-source voltage (V_{GS}) away from one of the supply lines. Because V_{GS} for normal operation is commonly more than 1 V, a single differential pair input stage comparator greatly restricts the allowable input voltage. This restriction can be quite limiting with low supply voltage supplies. To resolve this issue, RRI stages allow the input signal range to extend up to the supply voltage range. In the case of the ADCMP396, the inputs continue to operate 200 mV beyond the supply rails.

OPEN-DRAIN OUTPUT

The ADCMP396 has an open-drain output stage that requires an external resistor to pull up to the logic high voltage level when the output transistor is switched off. The pull-up resistor must be large enough to avoid excessive power dissipation, but small enough to switch logic levels reasonably quickly when the comparator output is connected to other digital circuitry. The rise time of the open-drain output depends on the pull-up resistor and load capacitor used.

The rise time can be calculated by

$$t_R = 2.197\ R_{PULLUP}\ C_{LOAD} \quad (1)$$

POWER-UP BEHAVIOR

On power-up, when V_{CC} reaches 0.9 V, the ADCMP396 is guaranteed to assert an output low logic. When the voltage on the V_{CC} pin exceeds UVLO, the comparator inputs take control.

CROSSOVER BIAS POINT

Rail-to-rail inputs of this type of architecture, in both op amps and comparators, have a dual front-end design. PMOS devices are inactive near the V_{CC} rail, and NMOS devices are inactive near GND. At some predetermined point in the common-mode range, a crossover occurs. At this point, normally 0.8 V and V_{CC} − 0.8 V, there are changes in the measured offset voltages.

COMPARATOR HYSTERESIS

In noisy environments, or when the differential input amplitudes are relatively small or slow moving, adding hysteresis (V_{HYST}) to the comparator is often desirable. The transfer function for a comparator with hysteresis is shown in Figure 26. As the input voltage approaches the threshold (0 V in Figure 26) from below the threshold region in a positive direction, the comparator switches from low to high when the input crosses $+V_{HYST}/2$. The new switch threshold becomes $-V_{HYST}/2$. The comparator remains in the high state until the $-V_{HYST}/2$ threshold is crossed from below the threshold region in a negative direction. In this manner, noise or feedback output signals centered on the 0 V input cannot cause the comparator to switch states unless it exceeds the region bounded by $\pm V_{HYST}/2$.

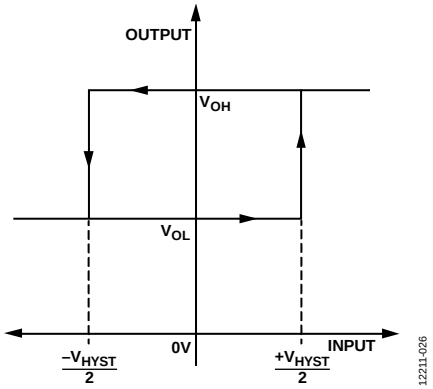


Figure 26. Comparator Hysteresis Transfer Function

TYPICAL APPLICATIONS

ADDING HYSTERESIS

To add hysteresis, see Figure 27; two resistors are used to create different switching thresholds, depending on whether the input signal is increasing or decreasing in magnitude. When the input voltage increases, the threshold is above V_{REF}, and when the input voltage decreases, the threshold is below V_{REF}.

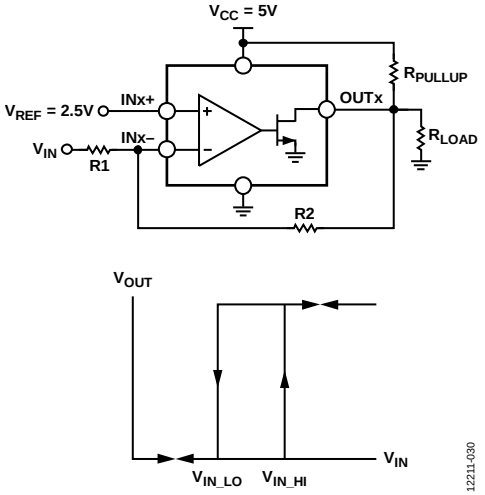


Figure 27. Noninverting Comparator Configuration with Hysteresis

The upper input threshold level is given by

$$V_{IN\_HI} = \frac{V_{REF}(R1+R2)}{R2} \quad (2)$$

Assuming R_{LOAD} >> R2, R_{PULLUP}.

The lower input threshold level is given by

$$V_{IN\_LO} = \frac{V_{REF}(R1+R2+R_{PULLUP}) - V_{CC}R1}{R2+R_{PULLUP}} \quad (3)$$

The hysteresis is the difference between these voltages levels.

$$\Delta V_{IN} = \frac{V_{CC}R1}{R2+R_{PULLUP}} \quad (4)$$

WINDOW COMPARATOR FOR POSITIVE VOLTAGE MONITORING

When monitoring a positive supply, the desired nominal operating voltage for monitoring is denoted by V_M, I_M is the nominal current through the resistor divider, V_{OV} is the overvoltage trip point, and V_{UV} is the undervoltage trip point.

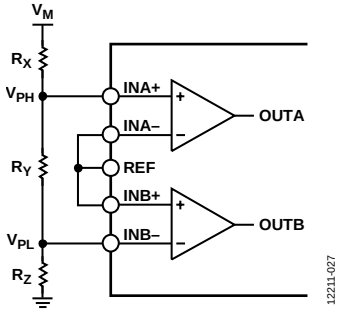


Figure 28. Positive Undervoltage/Overvoltage Monitoring Configuration

Figure 28 illustrates the positive voltage monitoring input connection. Three external resistors, R_X, R_Y, and R_Z, divide the positive voltage for monitoring, V_M, into the high-side voltage, V_{PH}, and the low-side voltage, V_{PL}. The high-side voltage is connected to the INA+ pin, and the low-side voltage is connected to the INB− pin.

To trigger an overvoltage condition, the low-side voltage (in this case, V_{PL}) must exceed the V_{REF} threshold on the INB+ pin. Calculate the low-side voltage, V_{PL}, by the following:

$$V_{PL} = V_{REF} = V_{OV}\left(\frac{R_Z}{R_X+R_Y+R_Z}\right) \quad (5)$$

In addition,

$$R_X + R_Y + R_Z = V_M/I_M \quad (6)$$

Therefore, R_Z, which sets the desired trip point for the overvoltage monitor, is calculated as

$$R_Z = \frac{(V_{REF})(V_M)}{(V_{OV})(I_M)} \quad (7)$$

To trigger the undervoltage condition, the high-side voltage, V_{PH}, must be less than the V_{REF} threshold on the INA− pin. The high-side voltage, V_{PH}, is calculated by

$$V_{PH} = V_{REF} = V_{UV}\left(\frac{R_Y+R_Z}{R_X+R_Y+R_Z}\right) \quad (8)$$

Because R_Z is already known, R_Y can be expressed as

$$R_Y = \frac{(V_{REF})(V_M)}{(V_{UV})(I_M)} - R_Z \quad (9)$$

When R_Y and R_Z are known, R_X can be calculated by

$$R_X = (V_M/I_M) - R_Y - R_Z \quad (10)$$

If V_M, I_M, V_{OV}, or V_{UV} changes, each step must be recalculated.

WINDOW COMPARATOR FOR NEGATIVE VOLTAGE MONITORING

Figure 29 shows the circuit configuration for negative supply voltage monitoring. To monitor a negative voltage, a reference voltage is required to connect to the end node of the voltage divider circuit, in this case, REF.

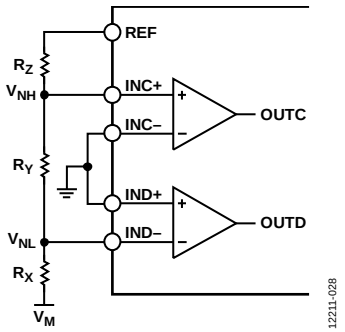


Figure 29. Negative Undervoltage/Overvoltage Monitoring Configuration

Equation 7, Equation 9, and Equation 10 need some minor modifications for use with negative voltage monitoring. The reference voltage, V_{REF}, is added to the overall voltage drop; therefore, it must be subtracted from V_M, V_{UV}, and V_{OV} before using each of them in Equation 7, Equation 9, and Equation 10.

To monitor a negative voltage level, the resistor divider circuit divides the voltage differential level between V_{REF} and the negative supply voltage into the high-side voltage, V_{NH}, and the low-side voltage, V_{NL}. The high-side voltage, V_{NH}, is connected to INC+, and the low-side voltage, V_{NL}, is connected to IND−.

To trigger an overvoltage condition, the monitored voltage must exceed the nominal voltage in terms of magnitude, and the high-side voltage (in this case, V_{NH}) on the INC+ pin must be more negative than ground. Calculate the high-side voltage, V_{NH}, by the following:

$$V_{NH} = GND = \left[\left(V_{REF} - V_{OV} \right) \left(\frac{R_X + R_Y}{R_X + R_Y + R_Z} \right) \right] + V_{OV} \quad (11)$$

In addition,

$$R_X + R_Y + R_Z = \frac{\left(V_M - V_{REF} \right)}{I_M} \quad (12)$$

Therefore, R_Z, which sets the desired trip point for the overvoltage monitor, is calculated by

$$R_Z = \frac{-V_{REF}\left(V_M - V_{REF} \right)}{I_M \left(V_{OV} - V_{REF} \right)} \quad (13)$$

To trigger an undervoltage condition, the monitored voltage must be less than the nominal voltage in terms of magnitude, and the low-side voltage (in this case, V_{NL}) on the IND− pin must be more positive than ground. Calculate the low-side voltage, V_{NL}, by the following:

$$V_{NL} = GND = \left[\left(V_{REF} - V_{UV} \right) \left(\frac{R_X}{R_X + R_Y + R_Z} \right) \right] + V_{UV} \quad (14)$$

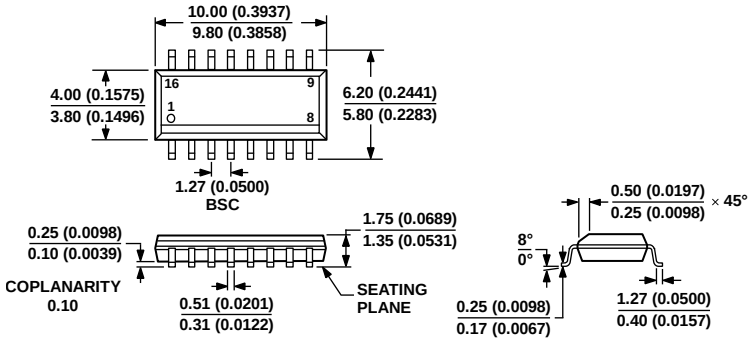
Because R_Z is already known, R_Y can be expressed as follows:

$$R_Y = \frac{-V_{REF}\left(V_M - V_{REF} \right)}{I_M \left(V_{UV} - V_{REF} \right)} - R_Z \quad (15)$$

When R_Y and R_Z are known, R_X is then calculated by

$$R_X = \frac{\left(V_M - V_{REF} \right)}{I_M} - R_Y - R_Z \quad (16)$$

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 30. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADCMP396ARZ	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADCMP396ARZ-RL7	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16

[1] Z = RoHS Compliant Part.

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