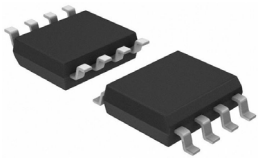
2.7V to 5.5V, 12Bit Single-Channel DAC

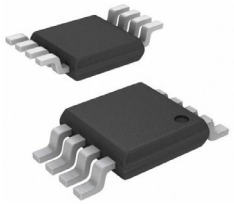
PRODUCT DESCRIPTION

The MS5221/5221M is a 12bit, single-channel output voltage DAC. The interface uses the three-wire serial port mode, and it can be compatible with TMS320, SPI, QSPI and Microwire serial port. The MS5221/5221M has 16bit control data, including control byte and 12bit DAC data. The power supply range is 2.7V to 5.5V. The output of integrated resistor string is connected to a class AB, rail-to-rail output amplifier with 6dB gain. The output buffer improves the stability and reduces the setup time.

The MS5221 is available in SOP8 package and The MS5221M is available in MSOP8 package.



SOP8



MSOP8

FEATURES

- 12bit Resolution
- Programmable Setup Time: 3μs or 9μs
- Compatible with TMS320, SPI and Microwire Interface
- Internal Power on Reset
- Integrated REF Buffer
- Output Range: Twice the Reference Voltage
- Not Sensitive to Temperature
- Software, Hardware Power down
- Power Supply :2.7V~5.5V

APPLICATIONS

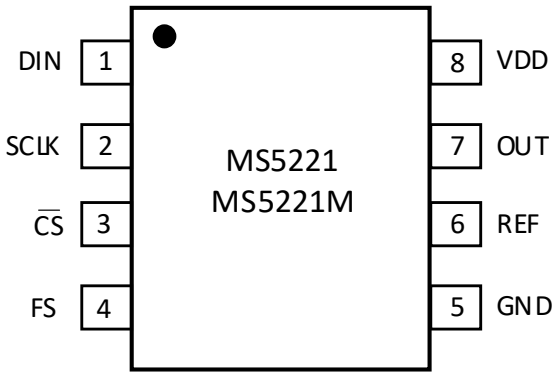
- Digital Servo System Control
- Digital Compensation and Gain Adjustment
- Industrial Process Control
- Mechanical and Mobile Control Equipment
- High-Capacity Storage Device

PRODUCT SPECIFICATION

Part Number	Package	Marking
*MS5221	SOP8	MS5221
MS5221M	MSOP8	MS5221M

* The package is not available temporarily. If necessary, please contact Hangzhou Ruimeng Sales Department Center.

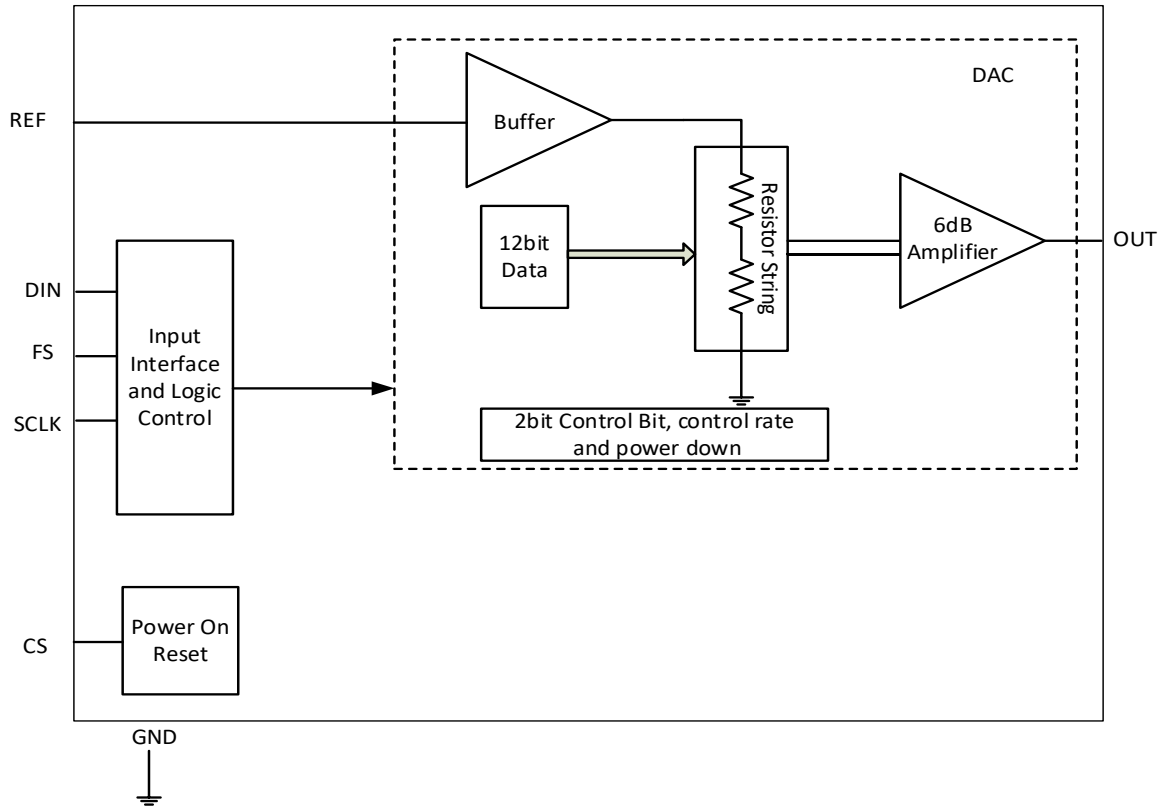
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	DIN	I	Serial Data Input
2	SCLK	I	Serial Digital Clock Input
3	$\overline{CS}$	I	Chip Select. Active Low
4	FS	I	Frame Synchronization Input Signal
5	GND	--	Ground
6	REF	I	Reference Input Voltage
7	OUT	O	Analog Output
8	VDD	-	Power Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply	VDD	-0.3 ~ +7	V
Input Digital Voltage	VIN	-0.3 ~ VDD+0.3	V
Reference Input Voltage	REF	-0.3 ~ VDD+0.3	V
Operating Temperature	TA	-40 ~ +105	°C
Storage Temperature	Tstg	-60 ~ +150	°C
Maximum Junction Temperature	Jt	150	°C
Lead Temperature (10s)		260	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Condition	Min	Typ	Max	Unit
Power Supply (VDD)	5V Supply	4.5	5	5.5	V
	3V Supply	2.7	3	3.3	
Digital Input High Level (VIH)	VDD=2.7V	2			V
	VDD=5.5V	2.4			
Digital Input Low Level (VIL)	VDD=2.7V			0.6	V
	VDD=5.5V			1	
Reference Voltage (REF)	5V Supply (See Note 1)	0	2.048	VDD-1.5	V
	3V Supply (See Note 1)	0	1.024	VDD-1.5	
Load Resistance		2	10		kΩ
Load Capacitance				100	pF
SCLK Rate				20	MHz

Note 1: The input voltage greater than VDD/2 would result in saturated output at large DAC input codes.

ELECTRICAL CHARACTERISTICS

Static DAC

Parameter		Condition	Min	Typ	Max	Unit
Resolution			12			Bits
Integral Non-linearity (INL)		See Note 1		±0.7	±3	LSB
Differential Non-linearity (DNL)		See Note 2		±0.7	±2	LSB
Zero-scale Offset		See Note 3			±12	mV
Zero-scale Offset Temperature Drift		See Note 4		10		ppm/°C
Gain Error		See Note 5			±0.6	%of FS Voltage
Gain Error Temperature Drift		See Note 6		10		ppm/°C
PSRR	Zero-scale	See Note 7 and 8		-80		dB
	Full-scale			-80		dB

Note:

1. Integrated non-linearity (INL) refers to linearity error, which is the maximum deviation of the output from the ideal output by eliminating zero-scale error and full-scale error.

2. Differential non-linearity (DNL), differential error, refers to the maximum amplitude change adjacent to the LSB.

3. Zero-scale offset refers to the analog output when digital input is zero.

4. Zero-scale temperature drift refers to temperature change of the analog output when digital input is zero.

5. Gain error refers to the deviation between the analog output and ideal output after zero-scale offset is removed.

6. Gain error temperature drift refers to the variation of the deviation between the analog output and ideal output with temperature after zero-scale offset is removed.

7. Zero-scale power supply rejection ratio is the change ratio of output caused by a change in VDD of 5±0.5V and 3±0.3V when the digital input is zero.

8. Full-scale power supply rejection ratio is the change ratio of output caused by a change in VDD of 5±0.5V and 3±0.3V when the digital input is high level.

DAC Output

Parameter	Condition	Min	Typ	Max	Unit
Output Voltage	RL=10kΩ	0		VDD-0.4	V
Output Load Regulation Accuracy	RL=2kΩ to 10kΩ		0.1	0.25	%of FS

Reference Input Voltage

Parameter	Condition	Min	Typ	Max	Unit
Input Voltage	See Note 9	0		VDD-1.5	V
Input Resistance			10		MΩ
Input Capacitance			5		pF

Parameter	Condition		Min	Typ	Max	Unit
Reference Feedthrough	REF= 1Vpp(1kHz) + 1.024V (See Note 10)			-75		dB
Reference Input Bandwidth	REF= 0.2Vpp+ 1.024V (Large Signal)	Slow		0.5		MHz
		Fast		1		

Note:

9. The reference input voltage greater than VDD/2 would result in output saturation distortion.

10. Reference feedthrough refers to the analog output rejection ratio when the output is zero and REF= 1Vpp (1kHz) +1.024V.

Digital Input

Parameter	Condition	Min	Typ	Max	Unit
Digital Input High-level Current	VI=VDD			±1	μA
Digital Input Low-level Current	VI=0V			±1	μA
Input Capacitance			3		pF

Power Dissipation

Parameter	Condition		Min	Typ	Max	Unit
Power Supply Current	5V supply, no load, add CLOCK, all inputs 0V or VDD	Slow		0.82	1.2	mA
		Fast		1.75	2	
	3V supply, no load, add CLOCK, all inputs 0V or VDD	Slow		0.38	0.5	mA
		Fast		1.12	1.5	
Power Down Current				10		nA

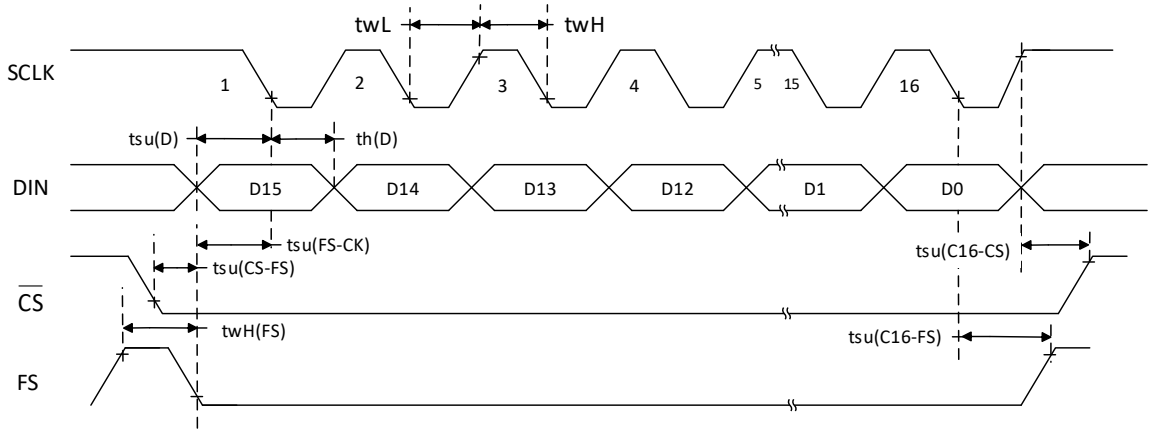
Analog Output Dynamic

Parameter	Condition		Min	Typ	Max	Unit
SR	CL=100pF,RL=10kΩ,Vo=10% to 90%， Vref=2.048,1.024	Fast		5		V/μs
		Slow		1		
Ts	To ±0.5LSB, CL＝100pF,RL=10kΩ	Fast		3	5.5	V/μs
		Slow		9	20	
Ts(c)	To ±0.5LSB, CL=100pF, RL=10kΩ	Fast		1		μs
		Slow		2		
Glitch Energy	From 7FF to 800			10		nV-sec
SNR	Vref=1.024 at 3V; Vref=2.048 at 5V, fs=400kSPS, fout=1.1kHz sine wave, CL=100pF, RL=10kΩ, BW=20kHz			74		dB
S/(N+D)				66		
THD				-68		
SFDR				70		

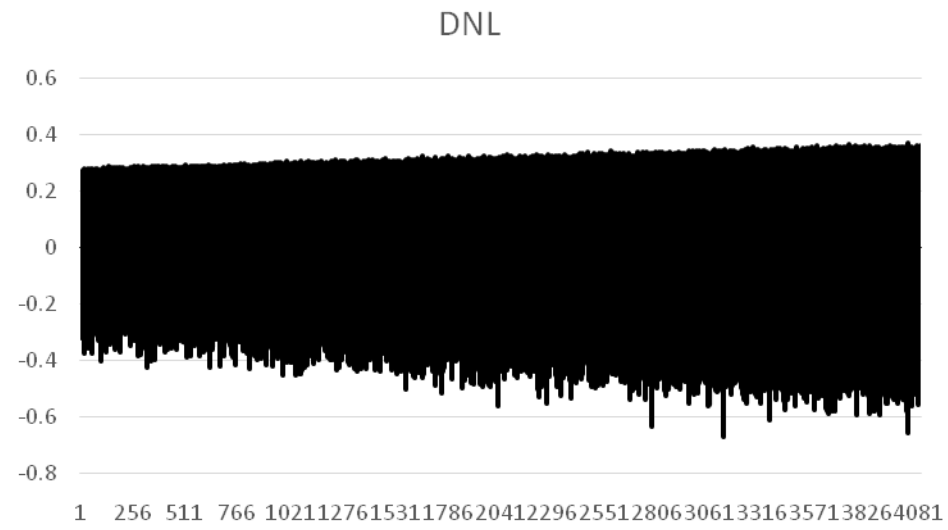
Digital Input Timing

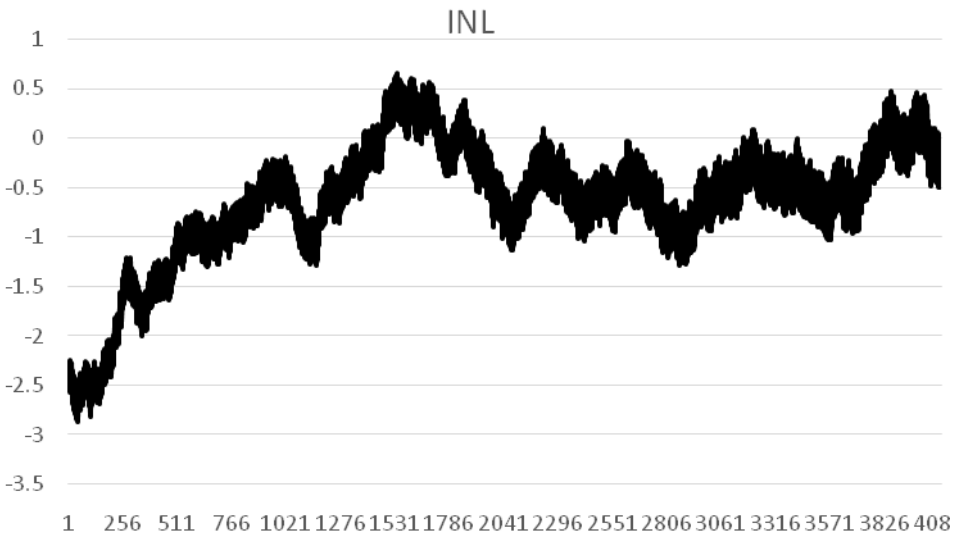
Parameter		Min	Typ	Max	Unit
tsu(CS–FS)	$\overline{CS}$ Low to the Falling Edge of FS	10			ns
tsu(FS–CK)	Setup Time, FS to the First Falling Edge of SCLK	8			ns
tsu(C16–FS) of FS	Setup Time, the Sixteenth Falling Edge of SCLK after FS low on which bit D0 is sampled before rising edge of FS	10			ns
tsu(C16–CS)	The First Falling Edge of SCLK after D0 is sampled before $\overline{CS}$ High	10			ns
twH	SCLK High Level Duration	25			ns
twL	SCLK Low Level Duration	25			ns
tsu(D)	Setup Time, Data Ready before Falling Edge of SCLK	8			ns
th(D)	Hold Time, Data Held Valid after Falling Edge of SCLK	5			ns
twH(FS)	FS High Level Duration	20			ns

Timing Diagram



TYPICAL CURVES





APPLICATION DESCRIPTION

The MS5221/5221M is a 12-bit, single-power digital-to-analog converter. Its architecture uses resistance string structure, which integrates serial interface, rate and power down logic control, reference input buffer, resistor string and output rail-to-rail amplifier.

The output voltage can be expressed as:

$$V(out)=2 \times (V_{REF} \times D/2^{12})$$

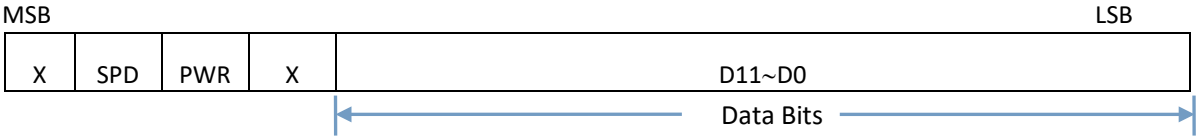
D represents digital input.

Serial Interface

The MS5221/5221M starts to input data bit-per-bit on the falling edge of FS (active high at first). After 16 bits have been transferred or when FS becomes high, the internal DAC updates the corresponding output level.

Data Format

The data word of the MS5221/5221M consists of two parts: control bits (D15~D12) and data bits(D11~D0).



SPD: Speed control, 1 for fast mode, 0 for slow mode.

PWR: Power dissipation control, 1 for off mode, 0 for normal mode.

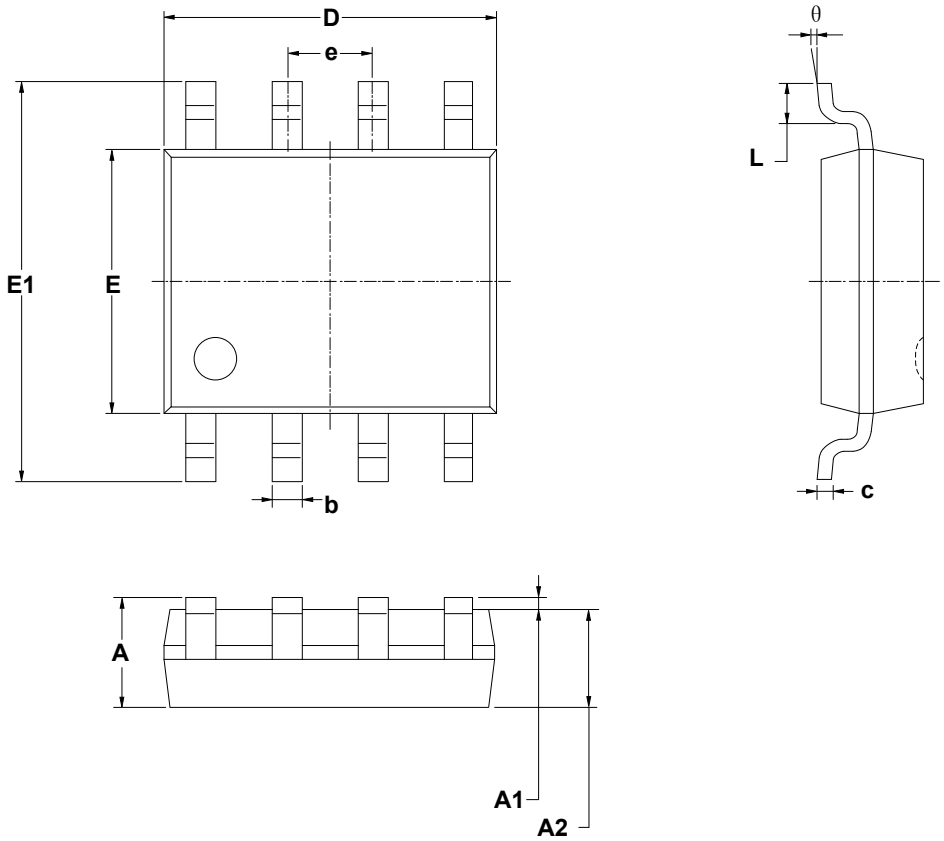
Power Supply Bypassing and Ground Management

In order to improve system performance, the analog and digital ground should be connected to different ground planes, which are linked together at low impedance node. It's better to connect DAC AGND to the system analog ground. Thus, the current of analog ground is managed well, and the voltage drop on the analog ground traces could be ignored.

The 0.1μF ceramic decoupling capacitance should be connected between ground and power supply. And it is placed as close to the chip as possible. If magnet ring is used, the analog and digital power supply could be further separated.

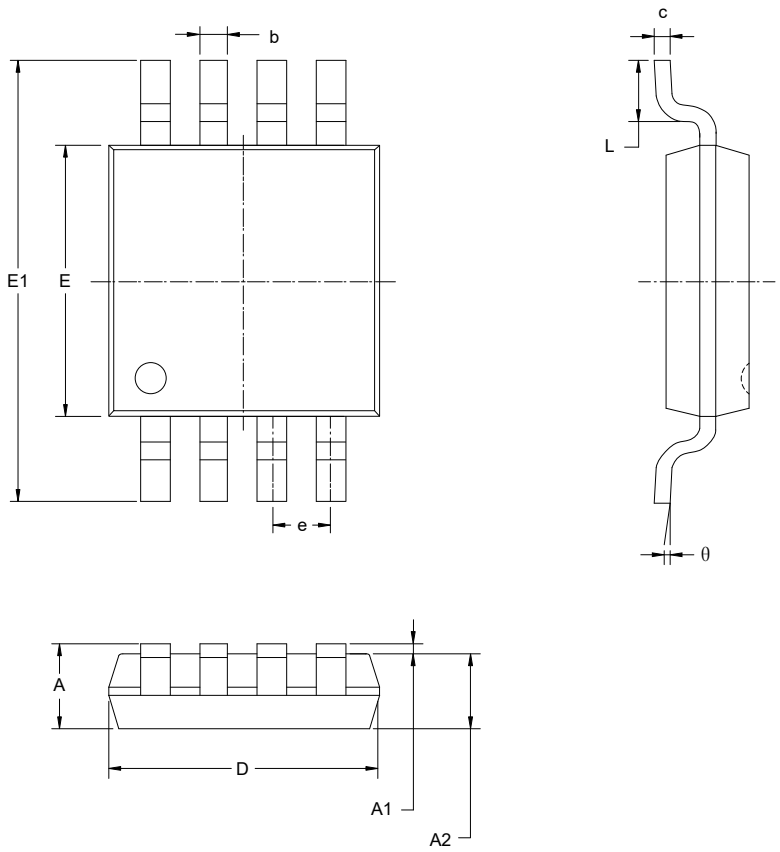
PACKAGE OUTLINE DIMENSIONS

SOP8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0 º	8 º	0 º	8 º

MSOP8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650BSC		0.026BSC	
L	0.400	0.800	0.016	0.031
θ	0º	6º	0º	6º

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name: MS5221, MS5221M

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS5221	SOP8	2500	1	2500	8	20000
MS5221M	MSOP8	3000	1	3000	8	24000

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9 Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

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