Application Notes: SY6345

40V, 300mA LDO Regulator

General Description

SY6345 is an efficient, precise LDO designed for high input voltage and ultra low quiescent current applications.

SY6345 provides adjustable output voltage with +/-2% accuracy and very low drop out (300mV at 300mA). Other features include the operation stability with low ESR ceramic or tantalum capacitors due to the optimized internal compensation, over current protection and thermal shutdown.

SY6345 is available in SOT23-5 package.

Features

- Wide input voltage range: 4V to 40V
- Low Dropout Voltage (300mV @ 300mA)
- Ultra-low quiescent current
- Extremely low shutdown current
- Stability with tantalum or ceramic capacitors
- Excellent load and line regulation
- +/-2% 0.6V reference accuracy
- 300mA maximum load current
- Enable control input
- Over current protection
- Thermal shutdown
- Compact SOT23-5 package

Ordering Information

SY6435 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6345AAC	SOT23-5	

Applications

- Battery powered Applications
- Automotive Applications
- Gateway Applications
- Remote Keyless Entry Systems
- SMPS post-regulator/ DC-DC modules

Typical Applications

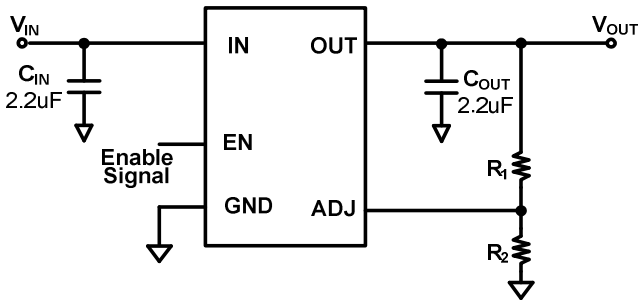


Figure 1. Schematic Diagram

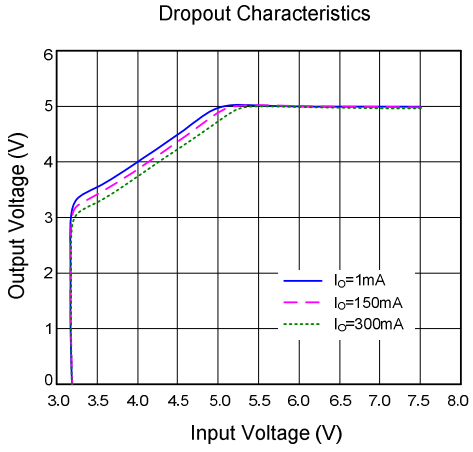
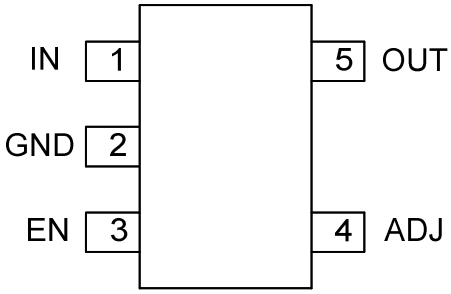


Figure 2. Dropout Characteristics

Pinout (top view)



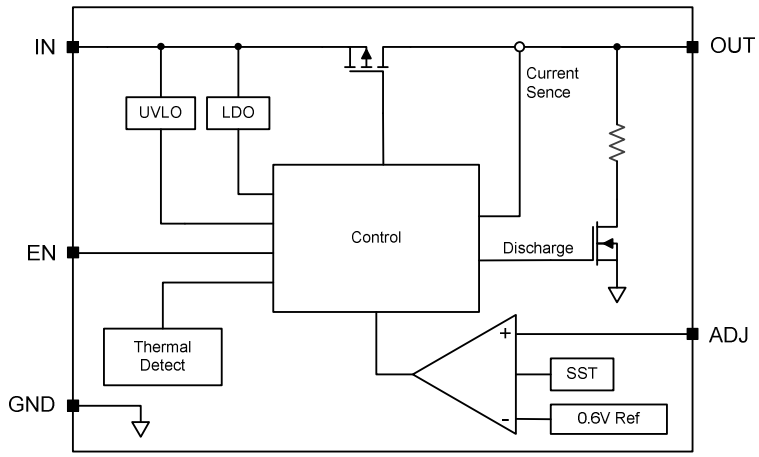
SOT23-5

Top mark: **YS*xyz*** for (Device code: YS, ***x=year code, y=week code, z= lot number code***)

Function Pin Description

Pin Name	Pin Number	Pin Description
IN	1	IC power supply input. Bypass this pin to Ground pin with a capacitor.
GND	2	Ground pin.
EN	3	Enable pin. Pull it low to shutdown or pull it high to enable, do not leave floating.
ADJ	4	Output voltage adjust pin. Feedback the output voltage through resistor voltage divider network. Vo=0.6×(1+R1/R2)
OUT	5	Output pin. Bypass this pin to Ground pin with a low ESR ceramic capacitor.

Function Block



Absolute Maximum Ratings (Note 1)

IN to GND ---------- -0.3V to 40V
OUT, EN, ADJ to GND ---------- -0.3V to 0.3V+Vin
Power Dissipation, PD @ T_A = 25°C SOT23-5 ---------- 0.6W
Package Thermal Resistance
θ_{JA} ----------170°C/W
θ_{JC} ----------130°C/W
Storage Temperature ---------- -65C to +150°C
Junction Temperature (T_J) ---------- +150°C
Lead Temperature (Soldering, 10sec.) ----------+260°C

Recommended Operating Conditions

Supply Input Voltage ---------- 4V to 40V
Junction Temperature (T_J) ---------- -40°C to +125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =12V,V_{EN}=V_{IN}, TA = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typical	Max	Unit
Input Voltage	V_{IN}	I_{OUT}=10mA	4		40	V
Reference Voltage	V_{REF}	V_{IN}=12V, Io=10mA	588	600	612	mV
Line Regulation	ΔV_{LNR}	V_{IN}=(V_{OUT}+0.3V) to 40V, I_O=10mA		1		mV/V
Load Regulation	ΔV_{LDR}	I_O=10mA to 300mA		0.25	1	%
Dropout Voltage	V_{IN}-V_{OUT}	I_O=10mA		10		mV
		I_O=150mA		150		mV
		I_O=300mA		300		mV
Quiescent Current	I_Q	No Load		7	10	μA
Shutdown Current	I_{SHDN}	V_{EN}=0V, V_{IN}=24V			1.25	μA
Output Current	I_O	V_{IN}=V_{OUT}+0.6V	0		300	mA
Output Current limit	I_{LIM}	V_{IN}= 6V,V_{OUT}=0.9xV_{OUT}(normal)	350		750	mA
Power-supply Rejection Ratio	PSRR	f=1kHz, C_{OUT}=10uF		60		dB
		f=150kHz, C_{OUT}=10uF		30		dB
Input UVLO Threshold	V_{UVLO}	V_{IN} rising			3.8	V
UVLO Hysteresis	V_{UVLO_th}			0.2		V
Shutdown Discharge Resistance	R_{DIS}			600		Ω
Enable Input Logic-High Voltage	V_{EN_H}	V_{IN}=5V to 40V	1.5			V
Enable Input Logic-Low Voltage	V_{EN_L}	V_{IN}=5V to 40V			0.4	V
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown hysteresis	T_{HYS}			20		°C

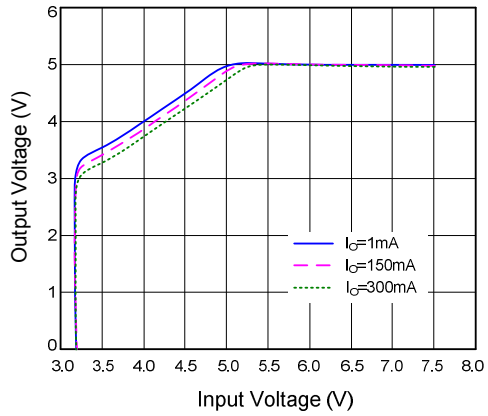
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at TA = 25°C on a low effective two-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

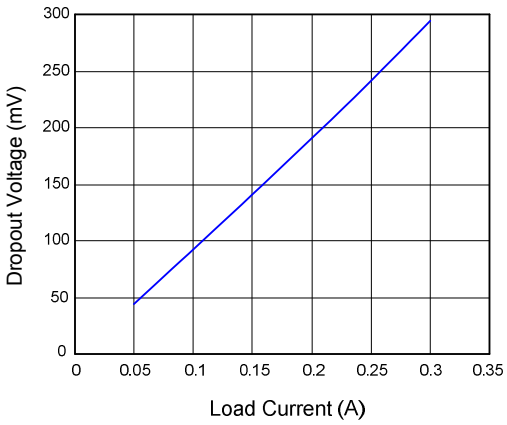
Note 3: The device is not guaranteed to function outside its operating conditions

Typical Performance Characteristics

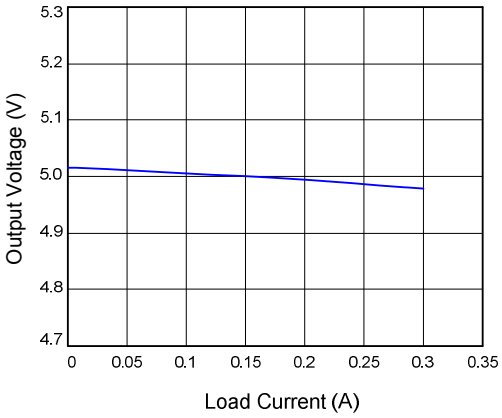
Dropout Characteristics



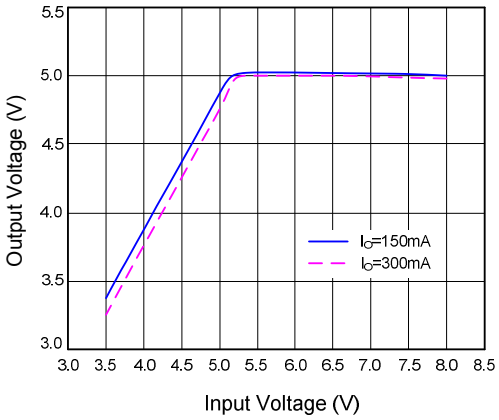
Dropout Voltage vs. Load Current



Load Regulation

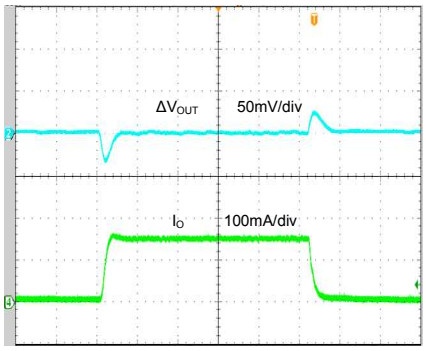


Line Regulation



Load Transient

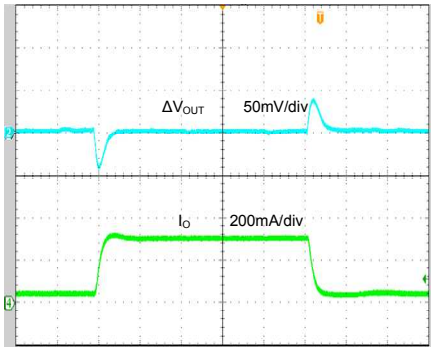
(V_{IN}=7.4V, V_{OUT}=5V, I_{OUT}=0~150mA)



Time (100μs/div)

Load Transient

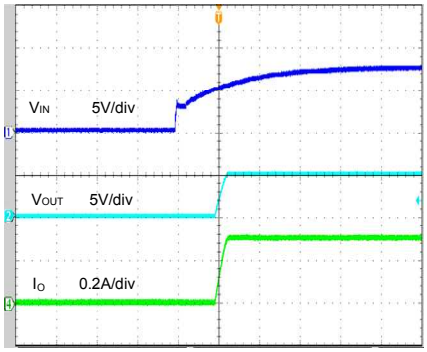
(V_{IN}=7.4V, V_{OUT}=5V, I_{OUT}=30~300mA)



Time (100μs/div)

Startup from V_{IN}

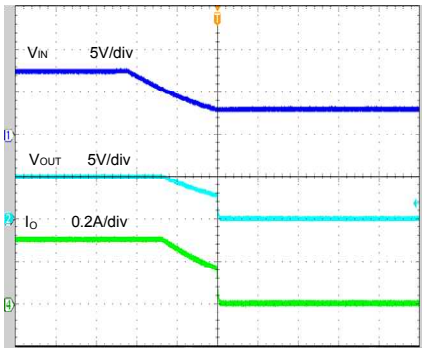
(V_{IN}=7.4V, V_{OUT}=5V, I_{OUT}=300mA)



Time (2ms/div)

Shutdown from V_{IN}

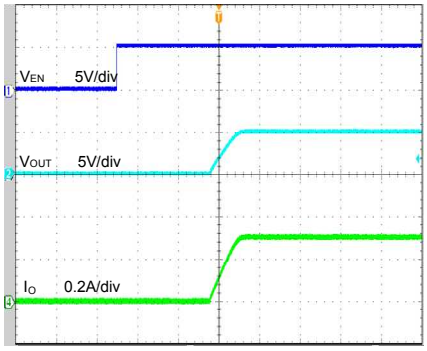
(V_{IN}=7.4V, V_{OUT}=5V, I_{OUT}=300mA)



Time (2ms/div)

Startup from Enable

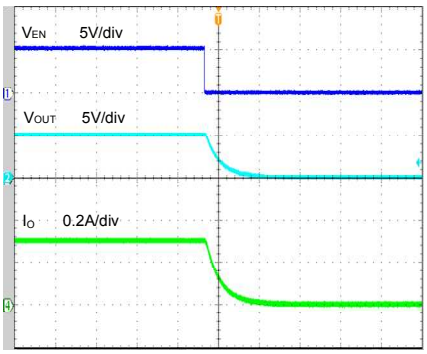
(V_{IN}=7.4V, V_{OUT}=5V, I_{OUT}=300mA)



Time (800μs/div)

Shutdown from Enable

(V_{IN}=7.4V, V_{OUT}=5V, I_{OUT}=300mA)



Time (100μs/div)

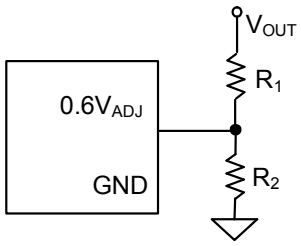
Application information

The SY6345 is a 300mA linear regulator with a low drop out voltage. Like any low-dropout regulator, SY6345 requires input and output decoupling capacitors.

Feedback resistor dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 3.3V, R_1=100k is chosen, then using following equation, R_2 can be calculated to be 22.1k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



Input capacitor C_{IN}:

An input capacitor about 2.2uF is required between the device input pin and ground pin. A typical X5R or better grade ceramic capacitor is recommended in this application. This input capacitor must be located close to the device to minimize the input noise.

Output capacitor C_{OUT}:

For transient stability, SY6345 is designed specifically to work with very small ceramic output capacitors. 2.2uF output capacitance can be used in this application. Higher capacitance values help to improve transient. The output capacitor's ESR is critical because it forms a zero to provide phase lead which is required for loop stability.

Dropout Voltage:

SY6345 has a very low dropout voltage due to its extra low $R_{DS(ON)}$ of the main PMOS determines the lowest usable supply .

$V_{DROPOUT}=V_{IN}-V_{OUT}=R_{DS(ON)}\times I_{OUT}$

Over Current and Short Circuit Protection:

The device includes over current and short circuit protection. The current limitation circuit regulates the output current to its limitation threshold to protect IC from damage. Under over current or short circuit condition, the power loss of the IC is relative high. And that may trigger the thermal protection.

Thermal Considerations:

The SY6345 can deliver a current of up to 300mA over the full operating junction temperature range. However, the maximum output current must be derated at higher ambient temperature to ensure the junction temperature does not exceed 125℃. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$P_D=(V_{IN}-V_{OUT})\times I_{OUT}+V_{IN}\times I_{GND}$

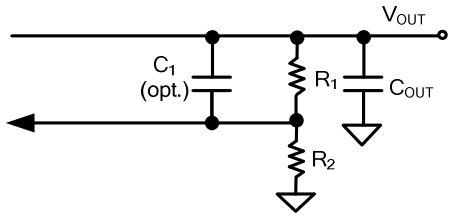
The final operating junction temperature for any set of condition can be estimated by the following thermal equation:

$P_{D(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA}$

Where $T_{J(MAX)}$ is the maximum junction temperature of die (125℃) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA}) footprint is 170℃/W for SOT23-5 package.

Load Transient Considerations:

The SY6345 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a small ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.



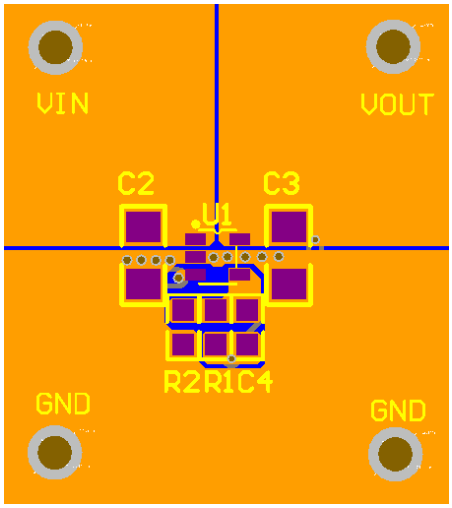
Layout Design:

Good board layout practices must be used or instability can be induced because of ground loops and voltage drops, and large PCB copper area can

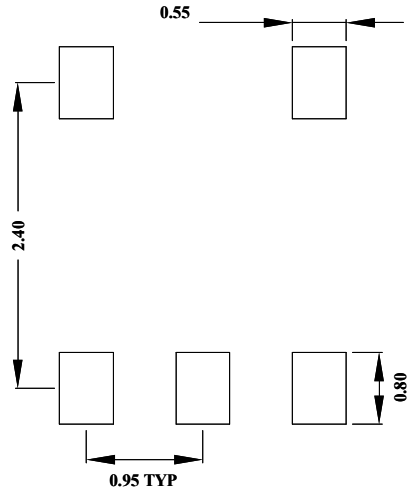
improve the thermal performance. The input and output capacitors MUST be directly connected to the input, output, and ground pins of the device using traces which have no other currents flowing through them.

The best way to do this is to layout C_{IN} and C_{OUT} near the device with short traces to the V_{IN}, V_{OUT}, and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a “single point ground”.

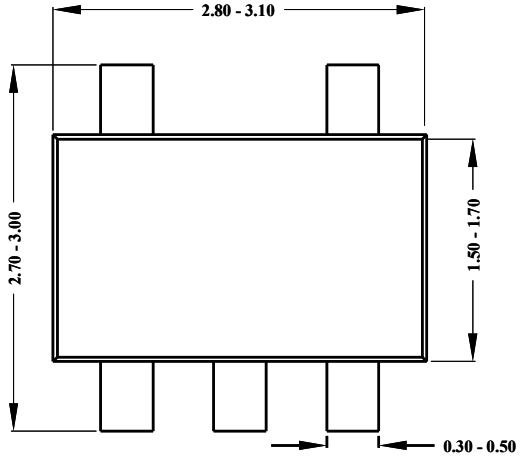
Below is the recommended PCB layout diagram:

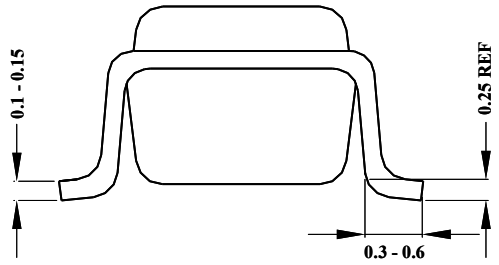


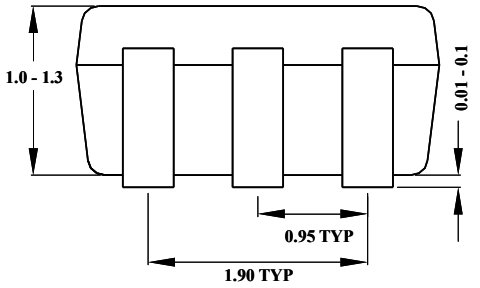
SOT23-5 Package outline & PCB layout design



Recommended Pad Layout





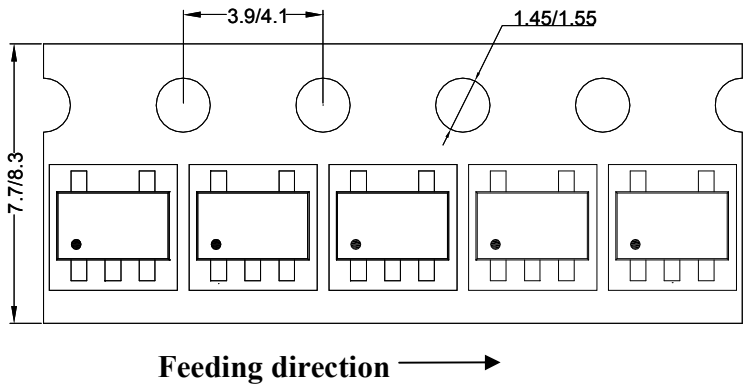


Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

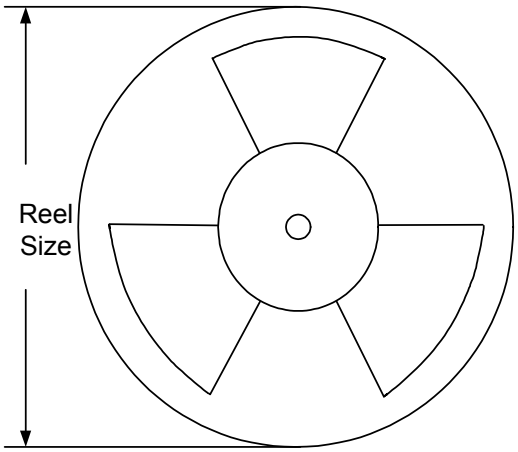
Taping & Reel Specification

1. Taping orientation

SOT23-5



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-5	8	4	7"	280	160	3000

3. Others: NA