High Side & Low Side Gate Drive IC

General description

The ID5S605 is a high voltage, high speed power MOSFET and IGBT driver based on P_SUB P_EPI process. The floating channel driver can be used to drive two N-channel power MOSFET or IGBT in a half-bridge configuration which operates up to 600 V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

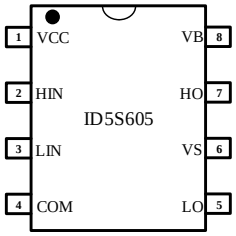
Application

- Small and medium- power motor driver
- Power MOSFET or IGBT driver
- Half-Bridge Power Converters
- Full-Bridge Power Converters
- Any Complementary Driver Converters

Features

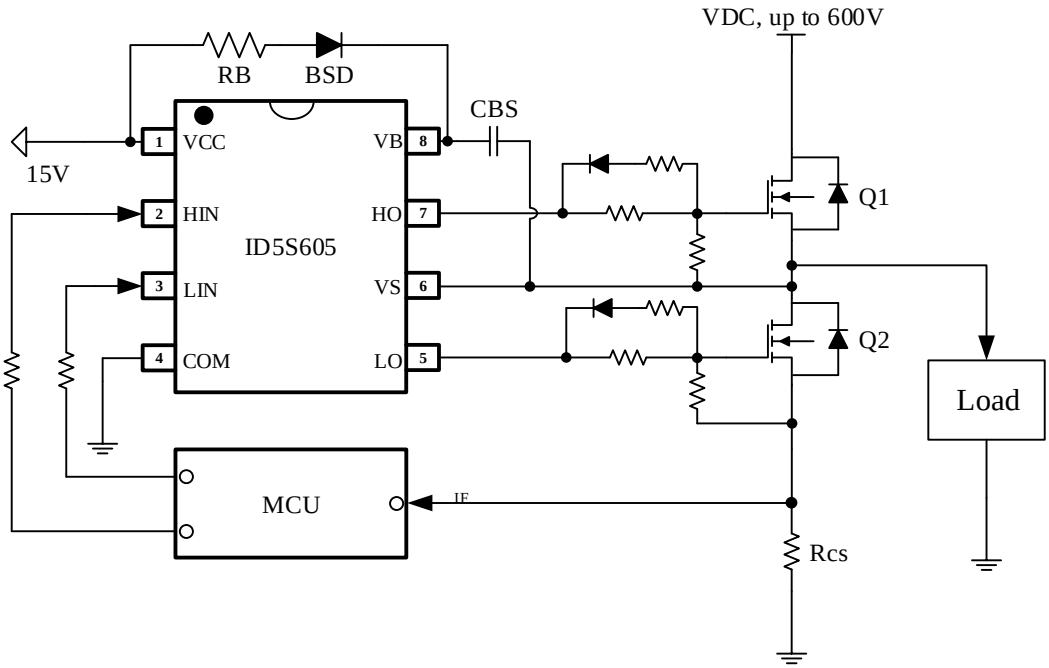
- Fully operational to +600 V
- 3.3 V logic compatible
- dV/dt Immunity ±50 V/nsec
- Floating channel designed for bootstrap operation
- Gate drive supply range from 10 V to 20 V
- UVLO for low side channel
- Output Source / Sink Current Capability 300 mA / 600mA
- Matched propagation delay for both channels

Package/Order Information



Order code	Package
ID5S605SEC-R1	SOP8

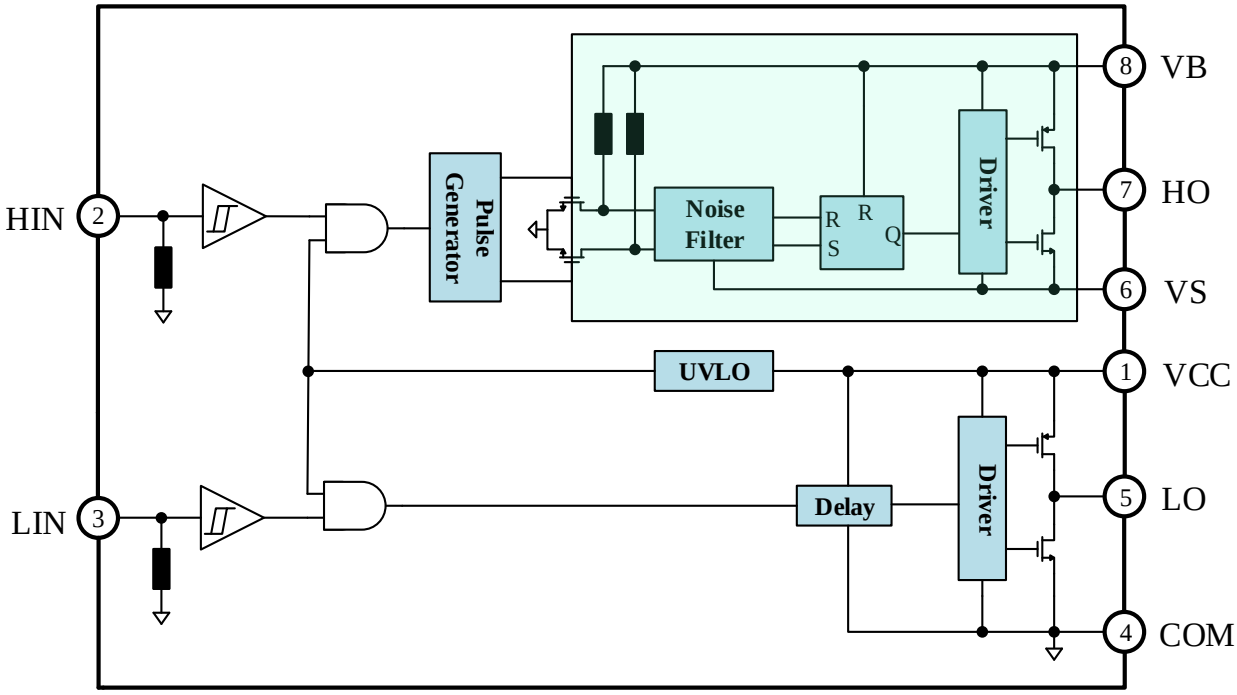
Typical Circuit



Pin Definitions

Pin Name	Pin Number	Pin Function Description
V_{CC}	1	Low side and main power supply
HIN	2	Logic input for high side gate driver output (HO)
LIN	3	Logic input for low side gate driver output (LO)
COM	4	Ground
LO	5	Low side gate drive output, out of phase with LIN
V_S	6	High side floating supply return or bootstrap return
HO	7	High side gate drive output, in phase with HIN
V_B	8	High side floating supply

Block Diagram



Absolute Maximum Ratings

Exceeding these ratings may damage the device.
The absolute maximum ratings are stress ratings only at T_A=25 ℃, unless otherwise specified.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	622[Note1]	V
V_S	High side floating supply return	V_B - 22	V_B + 0.3	
V_{HO}	High side gate drive output	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	22	
V_{LO}	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN &LIN	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	--	50	V/ns
ESD	HBM Model	2.5	--	kV
	CDM Model	200	--	V
P_D	Package Power Dissipation @ T_A ≤25°C (8 Lead SOP)	--	0.625	W
R_{thJA}	Thermal Resistance Junction to Ambient (8 Lead SOP)	--	200	℃ /W
T_J	Junction Temperature	--	150	℃
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	--	300	

Note 1: Max VB 622V is only for SOP8.

Recommended Operating Conditions

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply	V_S +10	V_S +20	V
V_S	High side floating supply return	--	600[Note2]	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	10	20	
V_{LO}	Low side gate drive output voltage	0	V_{CC}	
V_{IN}	Logic input voltage(HIN & LIN)	0	V_{CC}	
T_A	Ambient temperature	-40	125	℃

Note 2: Max VS 600V is only for SOP8.

Dynamic Electrical Characteristics

(V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25 ℃ unless otherwise specified.)

Symbol	Definition	TYP.	MAX.	Units
t_{ONH}	High side turn on propagation delay	160	220	ns
t_{OFFH}	High side turn off propagation delay	150	220	
t_{ONL}	Low side turn on propagation delay	160	220	
t_{OFFL}	Low side turn off propagation delay	150	220	
MT	Delay matching time (t_{ON}, t_{OFF})	20	50	
t_R	Turn on rising time	90	170	
t_F	Turn off falling time	40	90	

Static Electrical Characteristics

(V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25 ℃ unless otherwise specified.)

Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{UVCC+}	V_{CC} supply under-voltage positive going threshold	--	8.7	--	V
V_{UVCC-}	V_{CC} supply under-voltage negative going threshold	--	8	--	
I_{LK}	High-side floating supply leakage current	--	--	50	μA
I_{QBS}	Quiescent V_{BS} supply current	--	30	55	
I_{QCC}	Quiescent V_{CC} supply current	--	150	270	
V_{OH}	High level output voltage drop, V_{BIAS} - V_O	--	--	0.3	V
V_{OL}	Low level output voltage drop, V_O	--	--	0.3	
I_{O+}	Output high short circuit pulsed current	--	300	--	mA
I_{O-}	Output low short circuit pulsed current	--	600	--	
V_{IH}	Logic “1” (HIN& LIN) input voltage	2.5	--	--	V
V_{IL}	Logic “0” (HIN & LIN) input voltage	--	--	0.8	
I_{IN+}	Logic “1” input bias current	--	6	10	μA
I_{IN-}	Logic “0” input bias current	--	--	1	

Function Timing Diagram

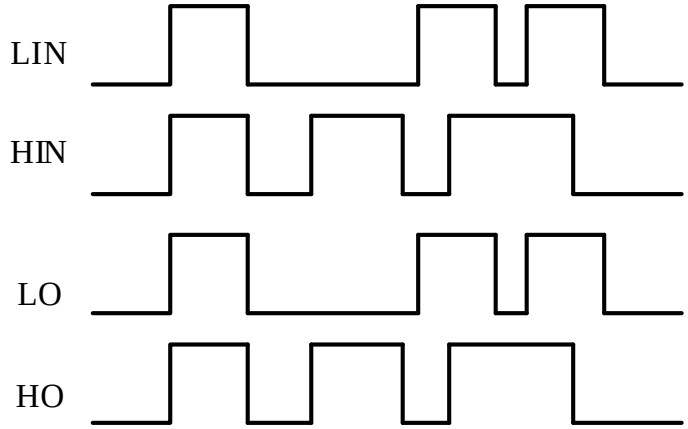


Fig.1 Input and output timing waveform

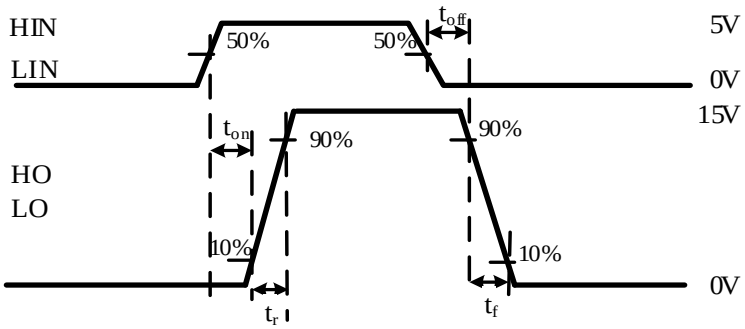


Fig.2 Propagation and Rise/Fall time definition

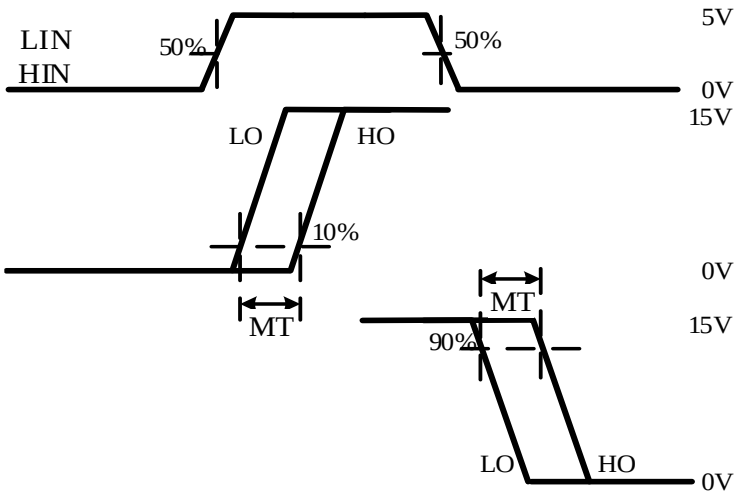


Fig.3 Delay matching definition

Characterization Curves

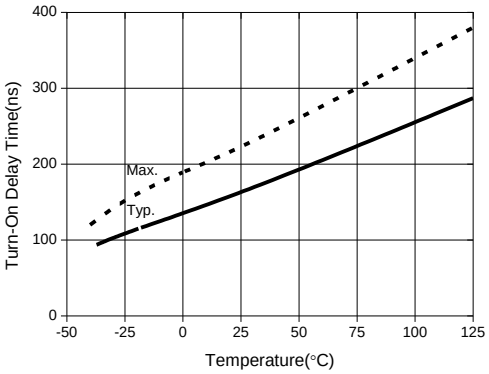


Fig.4 Turn-On Delay vs. Temperature

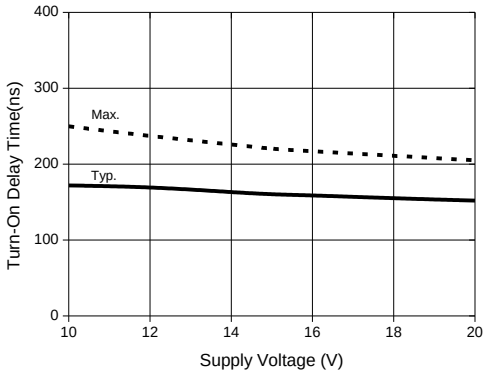


Fig.5 Turn-On Delay vs. Voltage

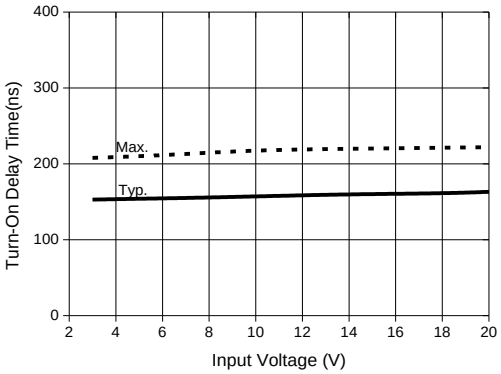


Fig.6 Turn-On Delay Time vs. Input Voltage

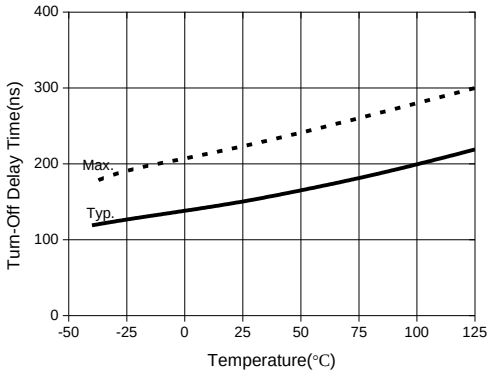


Fig.7 Turn-Off Delay Time vs. Temperature

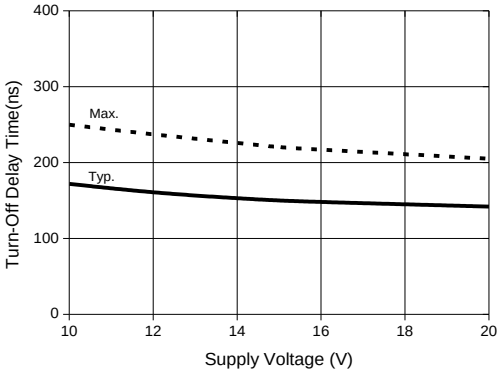


Fig.8Turn-Off Delay Time vs. Supply Voltage

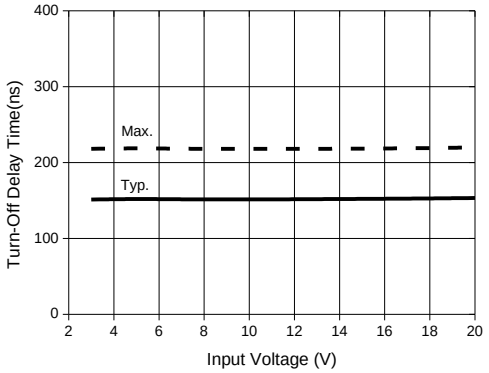


Fig.9 Turn-Off Delay Time vs. Input Voltage

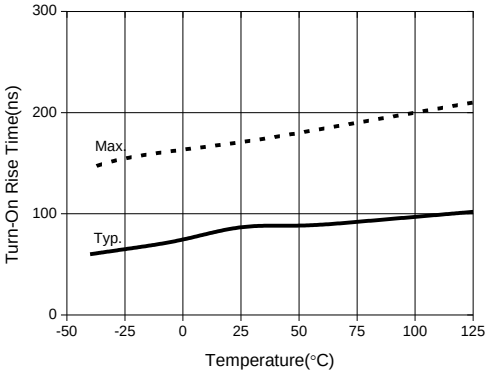


Fig.10 Turn-On Rise Time vs. Temperature

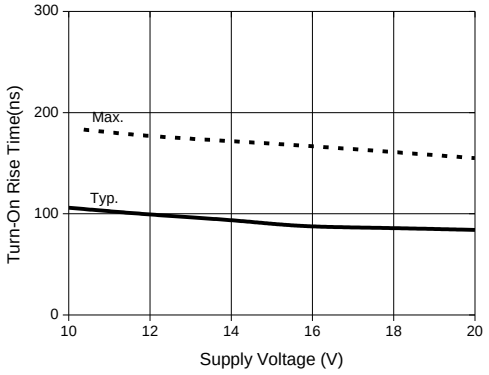


Fig.11 Turn-On Rise Time vs. Supply Voltage

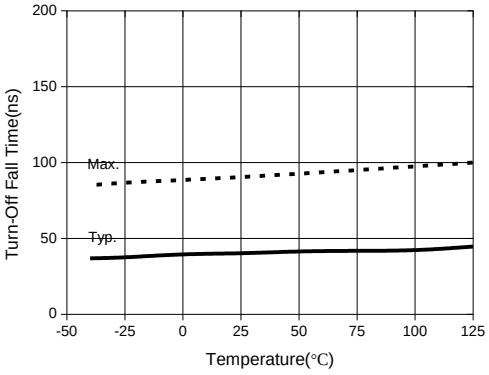


Fig.12 Turn-Off Fall Time vs. Temperature

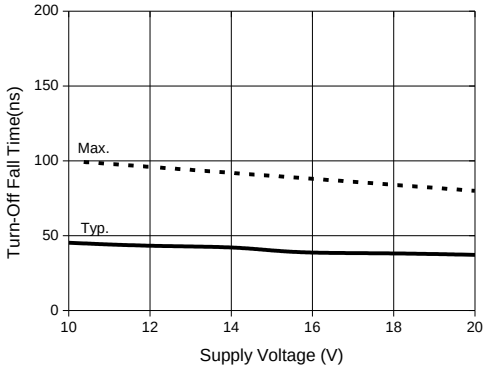


Fig.13 Turn-Off Fall Time vs. Supply Voltage

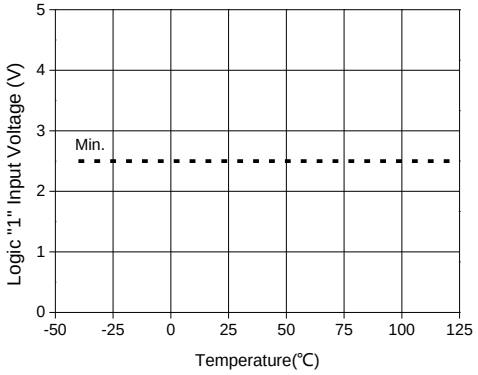


Fig.14 Logic "1" Input Voltage vs. Temperature

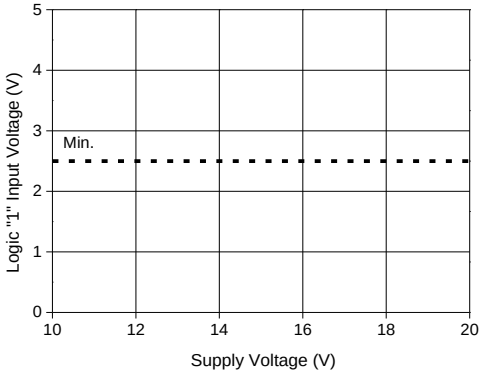


Fig.15 Logic "1" Input Voltage vs. Supply Voltage

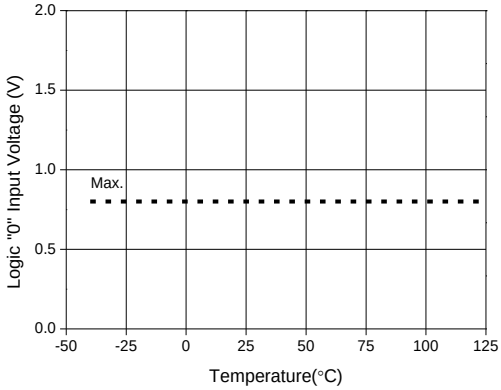


Fig.16 Logic "0" Input Voltage vs. Temperature

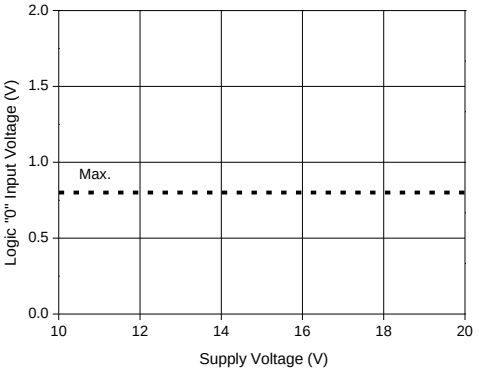


Fig.17 Logic "0" Input Voltage vs. Supply Voltage

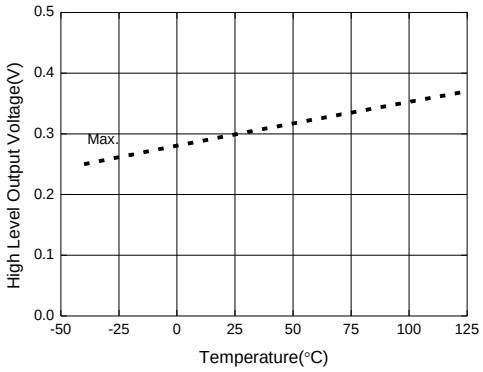


Fig.18 High Level Output vs. Temperature

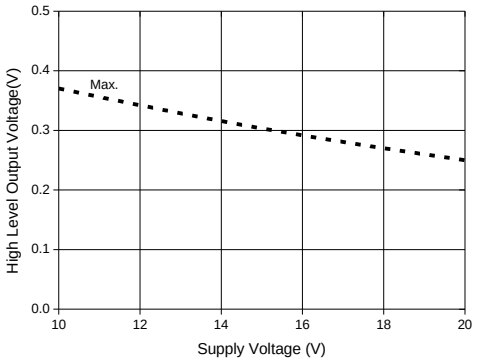


Fig.19 High Level Output vs. Supply Voltage

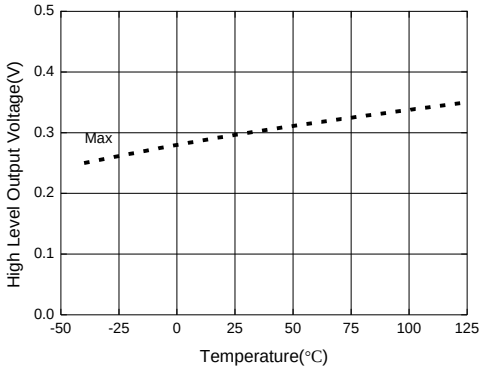


Fig.20 Low Level Output vs. Temperature

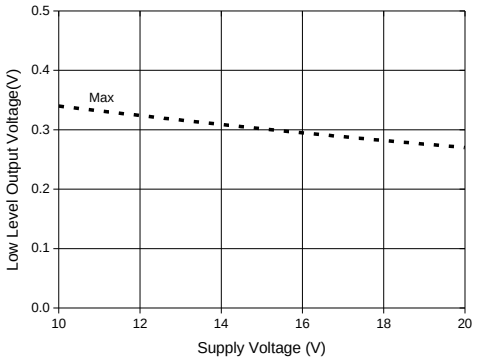


Fig.21 Low Level Output vs. Supply Voltage

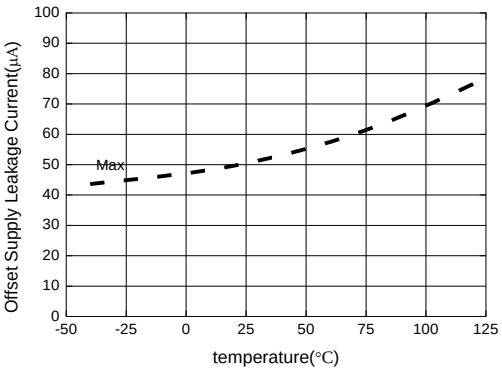


Fig.22 Offset Supply Current vs. Temperature

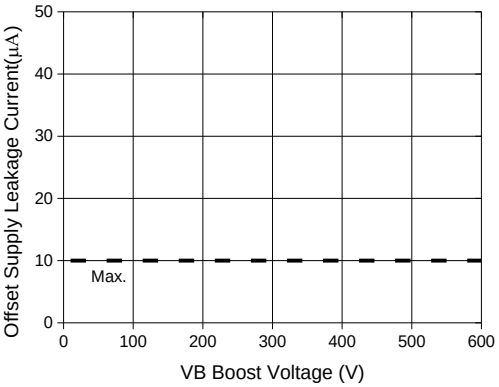


Fig.23 Offset Supply Current vs. Boost Voltage

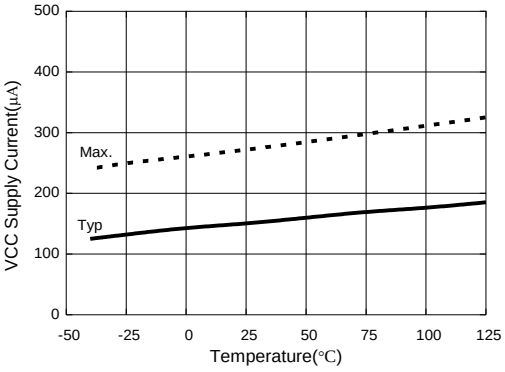


Fig.24 V_{CC} Supply Current vs. Temperature

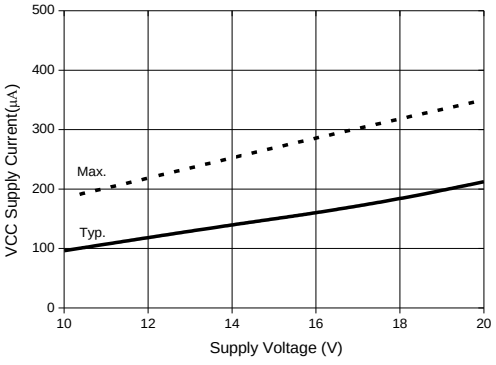


Fig.25 V_{CC} Supply Current vs. Supply Voltage

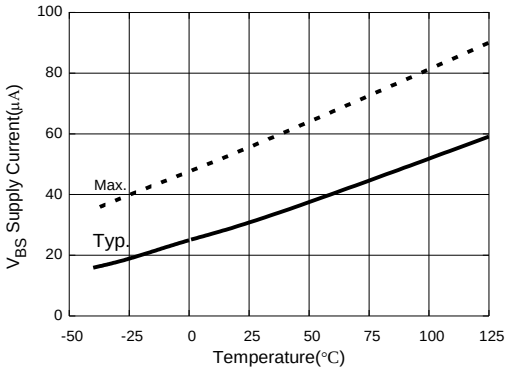


Fig.26 V_{BS} Supply Current vs. Temperature

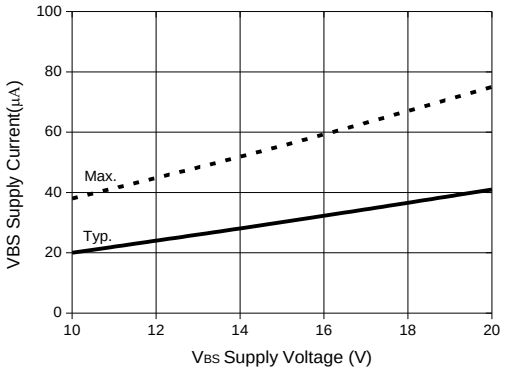


Fig.27 V_{BS} Supply Current vs. Supply Voltage

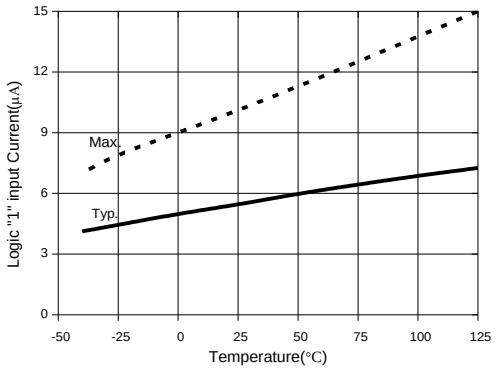


Fig.28 Logic "1" Input Current vs. Temperature

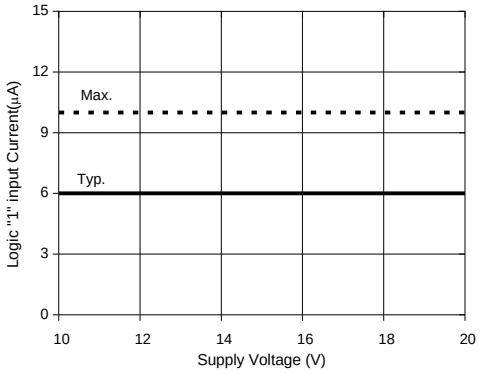


Fig.29 Logic "1" Input Current vs. Supply Voltage

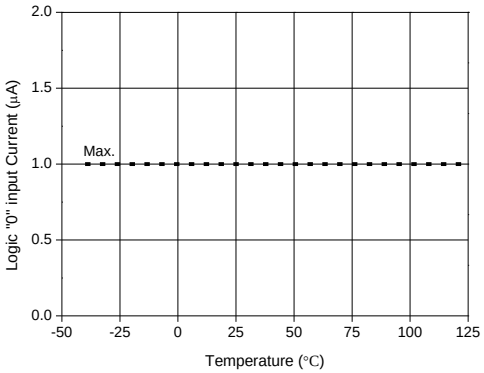


Fig.30 Logic "0" Input Current vs. Temperature

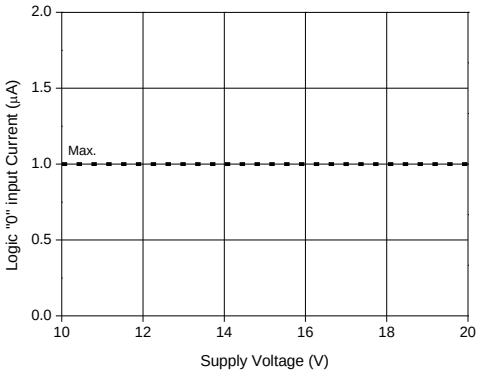


Fig.31 Logic "0" Input Current vs. Supply Voltage

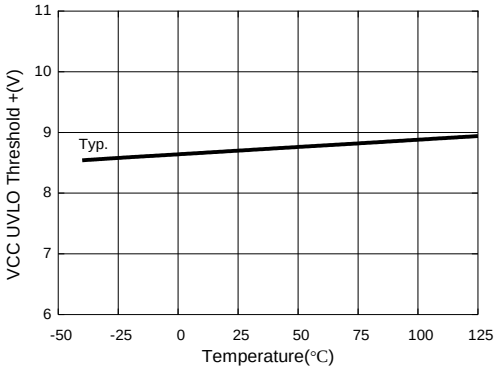


Fig.32 V_{CC} Under-voltage Threshold(+) vs Temperature

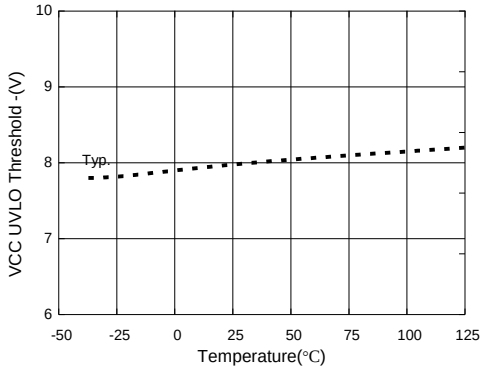


Fig.33 V_{CC} Under-voltage Threshold(-) vs Temperature

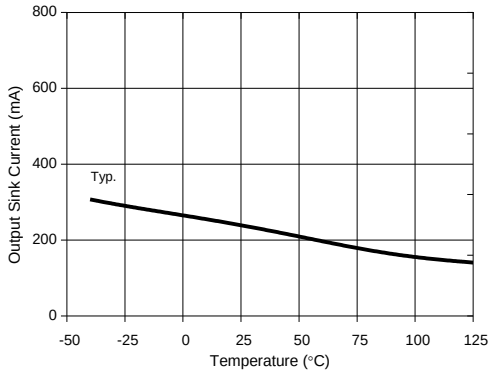


Fig.34 Output Source Current vs. Temperature

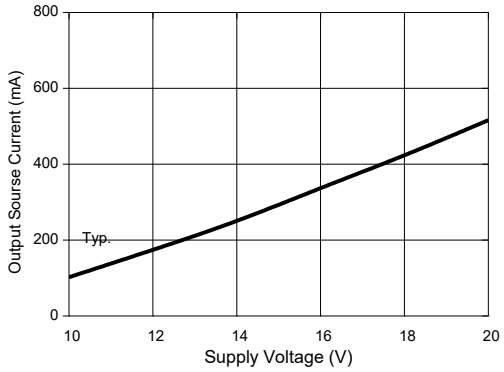


Fig.35 Output Source Current vs. Supply Voltage

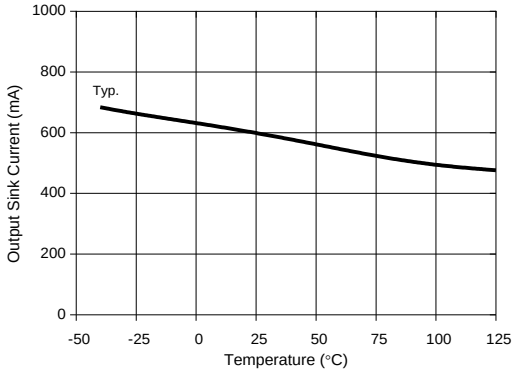


Fig.36 Output Sink Current vs. Temperature

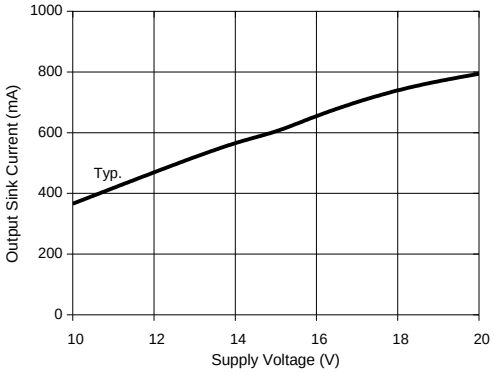


Fig.37 Output Sink Current vs. Supply Voltage

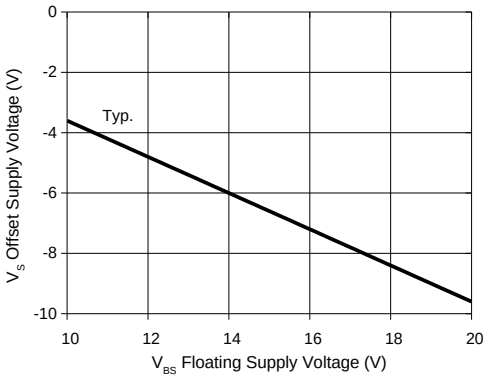
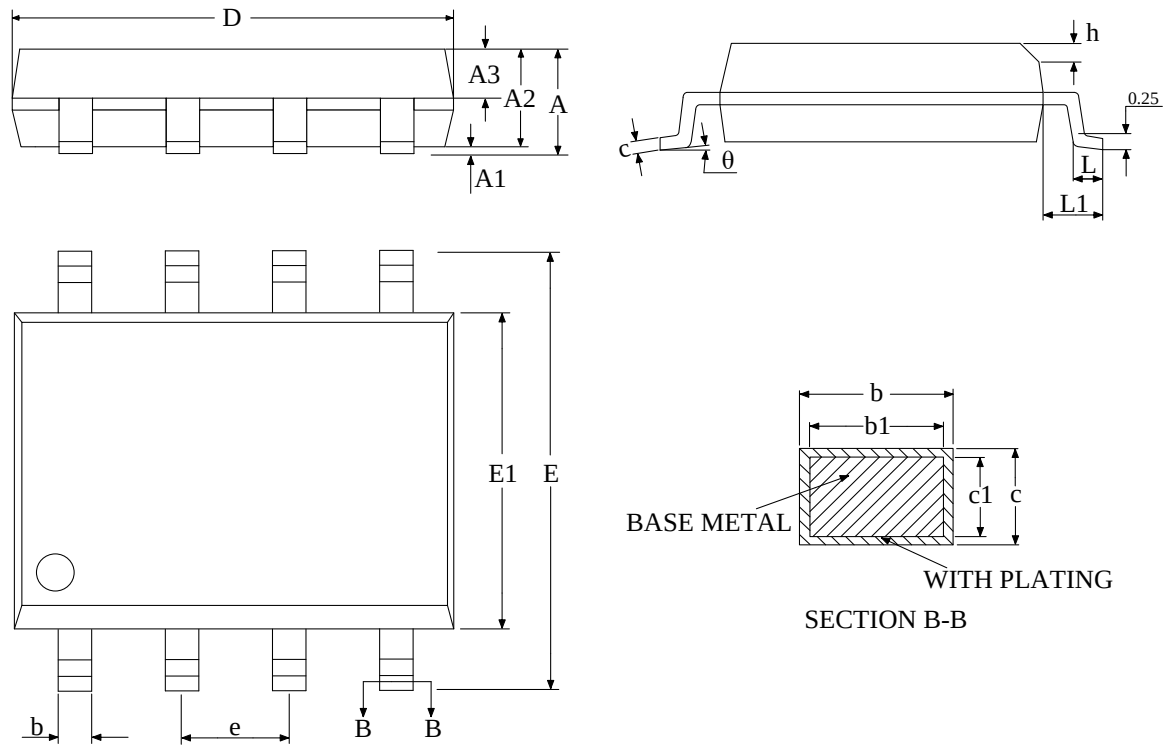


Fig.38 Maximum VS Negative Offset vs. Supply Voltag

Package Information

Package Information SOP8



Symbol \ Size	Min. (mm)	Typ. (mm)	Max. (mm)	Symbol \ Size	Min. (mm)	Typ. (mm)	Max. (mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50	-	0.80
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

Top mark	Package
iDR. ID5S605 YWWXXXXX	SOP8

Note：Y：Year Code；WW：Week Code；XXXXX：Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

Important Notice

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