High Performance Non-isolated PFM Converter

General Description

The PN8055 consists of an integrated Pulse Frequency Modulator (PFM) controller and Internal 800V avalanche-rugged smart power MOSFET, specifically designed for small power non-isolated switching power supply. PN8055 has internal high voltage start-up circuit and complete intelligent protections including adjustable Over Load Protection (OLP), Under Voltage Lockout (UVLO) and Over Temperature Protection (OTP). Excellent EMI performance could be achieved with Pulse Frequency Modulation.

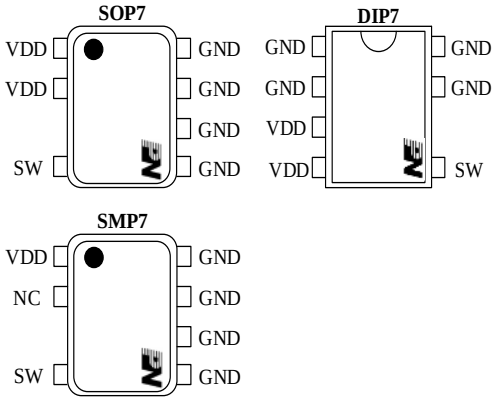
Features

- Internal 800V avalanche-rugged smart power MOSFET
- Internal HV Start-up Circuit
- Be optimized with 15V output non-isolated application
- Semi enclosed steady output power 3.0W@230VAC
- Frequency modulation for low EMI
- Excellent constant voltage regulation and high efficiency
- Excellent Protection Coverage:
  - ✧ Over Load Protection (OLP)
  - ✧ Over Temperature Protection (OTP)
  - ✧ Under Voltage Lockout (UVLO)

Applications

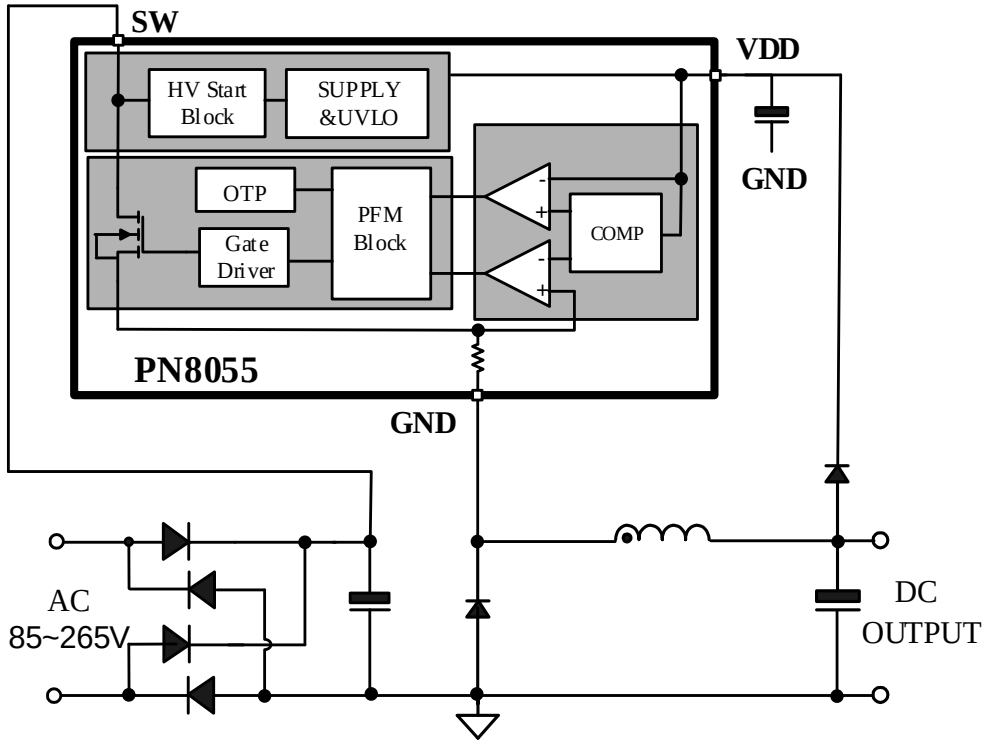
- non-isolated assistant power supply

Package/Order Information



Order Code	Package
PN8055SSC-R1	SOP7
PN8055NSC-T1	DIP7
PN8055SM-A1	SMP7

Typical Circuit



Pin Definitions

Pin Name	Pin Number			Pin Function Description
	SOP7	DIP7	SMP7	
VDD	1,2	3,4	1	Positive Supply voltage Input.
NC	-	-	2	NC
SW	3	5	3	HV MOSFET Drain pin.
GND	4,5,6,7	1,2,6,7	4,5,6,7	Ground

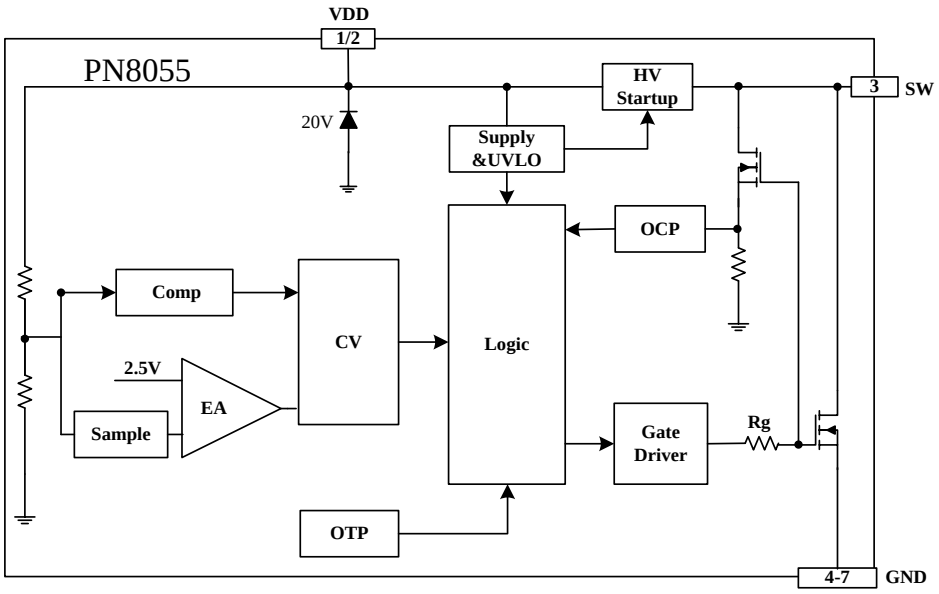
Typical Power

Part number	Input Voltage	Steady output power (1)	Peak Power (2)
PN8055	150-265V_{AC}	3W(15V200mA)	3.75W(15V250mA)
	85-265V_{AC}	2.25W(15V150mA)	3W(15V200mA)

Note:

1. Maximum output power in a semi enclosed design measured at 75℃ ambient temperature, Duration: 2 hours
2. Peak power in a semi enclosed design measured at 75℃ ambient temperature, Duration: 1 min

Block Diagram



Absolute Maximum Ratings

Supply voltage Pin VDD……-0.3~35V
High-Voltage Pin SW……-0.3~800V
Operating Junction Temperature……..…-40~150 ℃
Storage Temperature Range……..……-55~150 ℃
Lead Temperature (Soldering, 10Secs)……260 ℃
Package Thermal Resistance θ_{JC} (DIP7)……20 ℃ /W
Package Thermal Resistance θ_{JC} (SOP7)……40 ℃ /W
Package Thermal Resistance θ_{JC} (SMP7)……16 ℃ /W
HBM ESD Protection [1] (HBM)…… ±6kV
ESD voltage Protection [2] ……8kV
Pulse Drain Current (T_{pulse}=100us)……2A

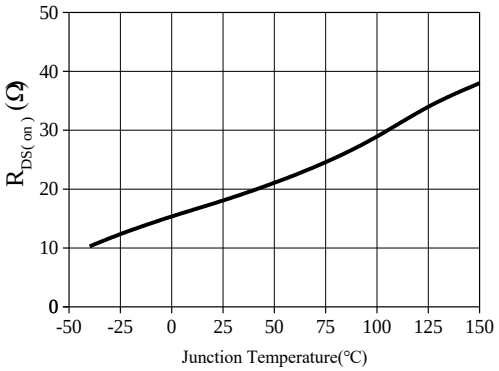
Note：
1. Test standard: ESDA/JEDEC JS-001-2017.
2. Air discharge to pins of PN8055 with ESD Generator, Enterprise internal standards, for reference only.

Electrical Characteristics

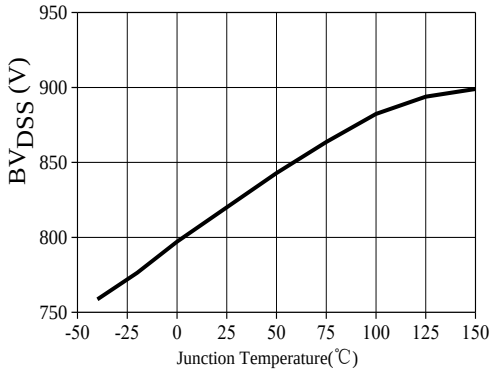
(T_A = 25 ℃, VDD = 14V, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Section						
Drain Break-down voltage	BV_{DSS}	I_{SW} =250uA, T_J =25 ℃	800	820		V
Off-state drain current	I_{OFF}	V_{SW} =650V, T_J =25 ℃	10	55	100	μA
Drain-source on state resistance	$R_{DS(on)}$	I_{SW} = 400mA, T_J =25 ℃		18		Ω
Start up threshold	V_{SW_START}	VDD=VDDon – 1V		30		V
Supply Voltage Section						
VDD start up threshold	VDD_{on}		11.0	12.0	13.0	V
VDD under voltage shutdown threshold	VDD_{off}		8.0	9.0	9.5	V
VDD voltage Hysteresis	VDD_{hys}			2.5		V
VDD clamp voltage	VDD_{clamp}		18	20	22	V
VDD feedback reference	VDD_{REF}			15.3		V
Supply Current Section						
VDD charge current	I_{DDch}	VDD=10V		-2		mA
Off-state current	I_{DD0}	VDD=6V	0.4	0.5	0.9	mA
Operating supply current	I_{DD1}	VDD =11V	0.9	1.2	1.5	mA
Current Sense Section						
Drain current limit	I_{limit}		450	500	550	mA
Leading edge blanking time	T_{LEB}			300		ns
Feedback Input Section						
Minimum turn OFF time	T_{offmin}		15	16.5	20	μs
Minimum turn ON time	T_{onmax}		10	13	16	μs
Thermal Shutdown Section						
OTP threshold	T_{SD}		135	150		℃
OTP Protect Hysteresis	T_{HYST}			30		℃
Restart Protection Section						
Restart time	$T_{RESTART}$	C_{VDD}=4.7μF		3		s

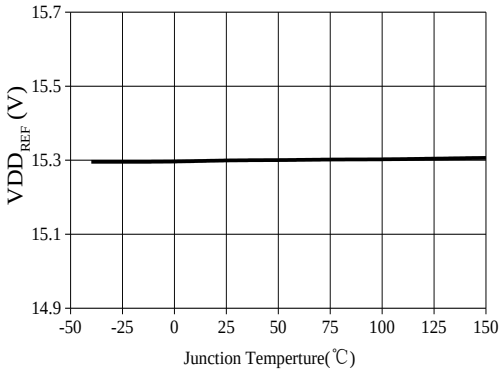
Typical Characteristics Plots



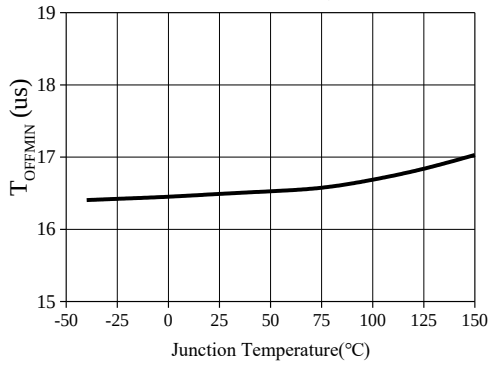
(a) $R_{DS(on)}$ vs T_j



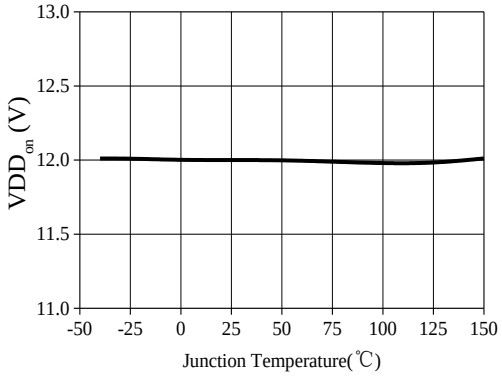
(b) BV_{DSS} vs T_j



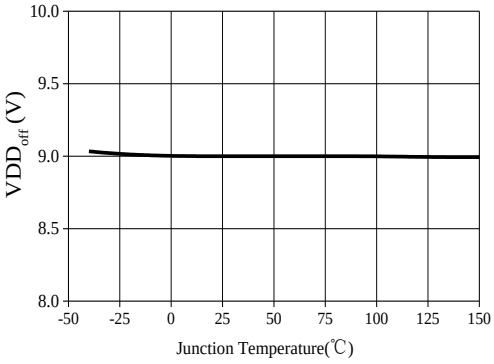
(c) VDD_{REF} vs T_j



(d) T_{offmin} vs T_j



(e) VDD_{on}vs T_j



(f) VDD_{off} vs T_j

Functional Description

The PN8055 consists of an integrated Pulse Frequency Modulator (PFM) controller and 800V power MOSFET, specifically designed for small power non-isolated switching power supply. PN8055 has internal 800V high voltage start-up circuit and complete intelligent protections including adjustable Over Load Protection (OLP), Under Voltage Lockout (UVLO) and Over Temperature Protection (OTP). Excellent EMI performance could be achieved with Pulse Frequency Modulation.

1. Start up

At start up, the internal high-voltage current source supplies 2mA current to charges the external VDD capacitor. When VDD rises to VDD_{on}, PN8055 starts switching and the internal high-voltage current source stops charging the capacitor. After start up, the VDD voltage is supplied from output.

2. CV Operation Mode

In CV operation, PN8055 samples the feedback signal through VDD pin. While the feedback voltage remains below VDD_{RF} the IC turns on the integrated MOSFET. When the current of the inductor reaches the peak current limit (Ipeak), the integrated MOSFET is turned off. Fig1-1 and Fig 1-2 shows the operating waveform of key nodes in continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Meanwhile, the IC integrates load compensation function to improve load regulation and CV accuracy.

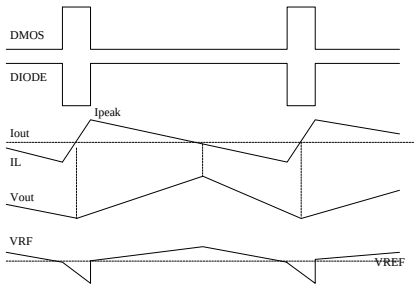


Fig1-1 Waveform if CCM mode

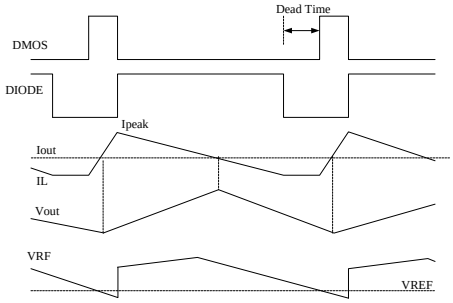


Fig1-2 Waveform of DCM mode

In actual applications, VDD sampling voltage is affected by isolation diode. So chip VDD_{REF} is set as 15.3V(TYP), to counteract the voltage drop on the isolation diode.

3. PFM modulation

The IC operates in PFM mode, and Ipeak is set to decrease with the decrease of the IC operating frequency (F_{SW}).when the IC switching cycle increase 1us,Ipeak will decrease 3mA. As a result of the internal current sampling and the maximum current limit (I_{limit}), inductance is the only parameter of the frequency modulation when output voltage and output current are fixed. The recommended inductance is 0.8~1.6mH, if the inductance is too small ,the carrying capacity of the system will be small, if too high, it is easy to cause inductance saturation, affecting reliability.

4. Soft-Start up

In order to regulate peak current in deep CCM mode, PN8055 build in soft-start function, reduce the switching frequency of the startup phase by limiting T_{offmin}. Meanwhile, the leading edge blanking (LEB) is 300ns (Typ.), in order to regulate peak current.

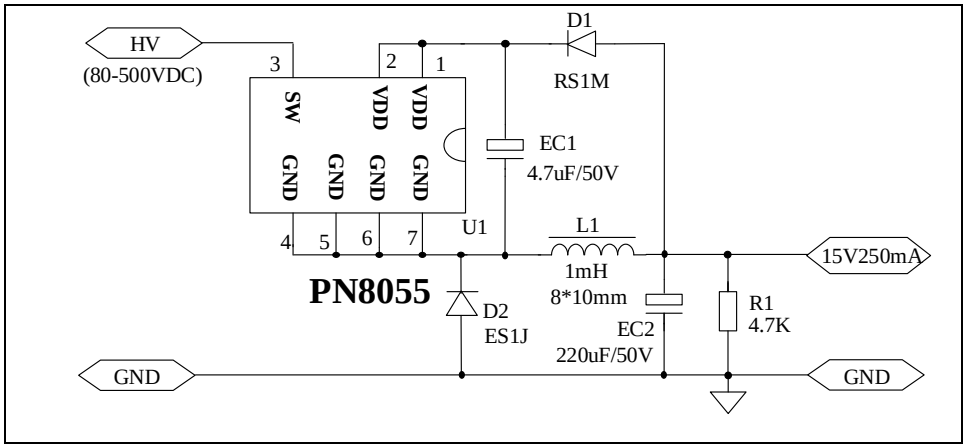
5. Smart Protection Control

PN8055 has several smart self-protection functions, such as Over Temperature Protection (OTP), VDD Under-Voltage Lockout (UVLO).And all these protections have self-recovery mode.

OTP----If the inner junction temperature exceeds 150℃, the IC will shut down switching, until the junction temperature falls to 120℃.

UVLO----If VDD pin Voltage drops below VDD_{off} , the IC will restart. Otherwise, self-restart time can be changed by VDD capacitor. The larger the capacitor, the longer the self-restart time is.

Typical Application

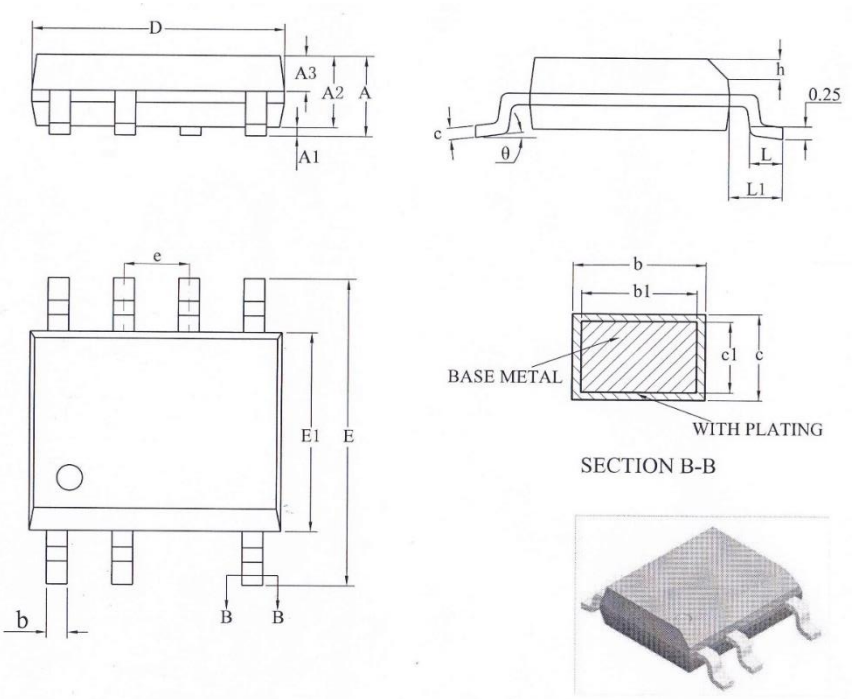


Component Parameter and Layout Considerations:

1. VDD capacitor EC1 should be placed at the nearest place from the VDD pin and the GND pin.

Package Information

Package Information SOP7



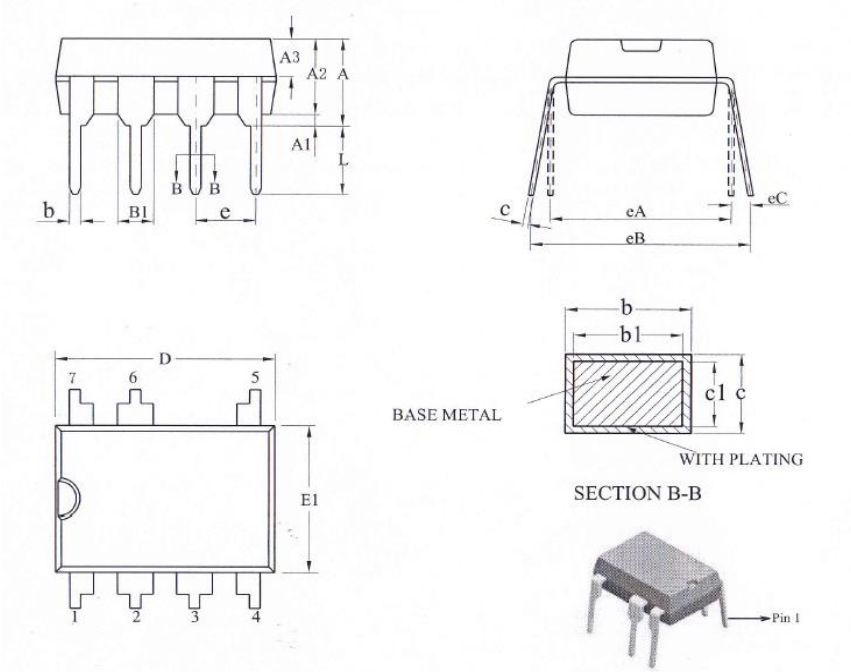
Size / Symbol	Min.(mm)	Typ.(mm)	Max.(mm)	Size / Symbol	Min.(mm)	Typ.(mm)	Max.(mm)
A	—	—	1.75	D	4.80	4.90	5.00
A1	0.10	—	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.80	3.90	4.00
A3	0.60	0.65	0.70	c	1.27BSC		
b	0.39	—	0.47	h	0.25	—	0.50
b1	0.38	0.41	0.44	L	0.50	—	0.80
c	0.20	—	0.24	L1	1.05REF		
c1	0.19	0.20	0.21	θ	0 °	—	8 °

Top mark	Package
PN PN8055 YWWXXXXX	SOP7

Note: Y: Year Code; WW: Week Code; XXXXX: Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

Package Information DIP7



Size / Symbol	Min.(mm)	Typ.(mm)	Max.(mm)	Size / Symbol	Min.(mm)	Typ.(mm)	Max.(mm)
A	3.60	3.80	4.00	c 1	0.24	0.25	0.26
A1	0.51	—	—	D	9.15	9.25	9.35
A2	3.20	3.30	3.40	E1	6.25	6.35	6.45
A3	1.55	1.60	1.65	e	2.54BSC		
b	0.44	—	0.52	eA	7.62REF		
b 1	0.43	0.46	0.49	eB	7.62	—	9.30
B1	1.52REF			eC	0	—	0.84
c	0.25	—	0.29	L	3.00	—	—

Top mark	Package
PN PN8055 YWWXXXXX	DIP7

Note: Y: Year Code; WW: Week Code; XXXXX: Internal Code

Notes:
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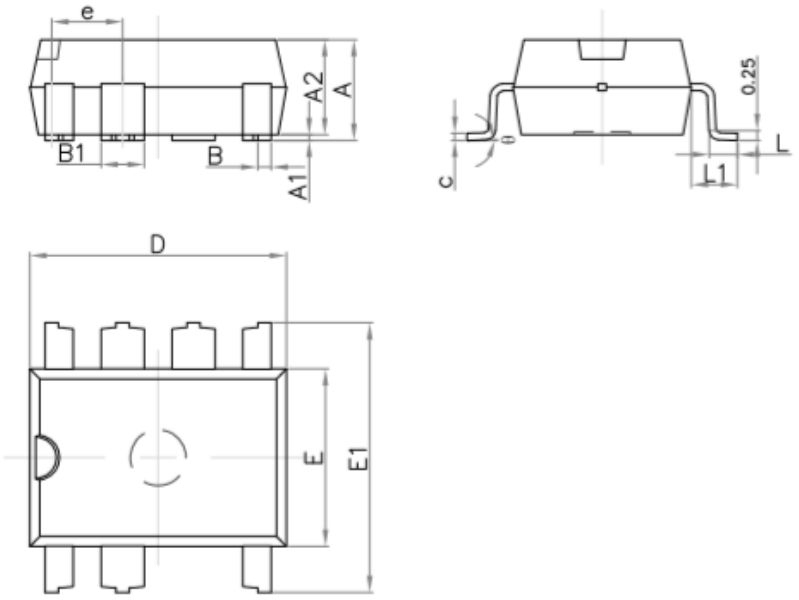
Package Information SMP7



Size / Symbol	Min. (mm)	Max. (mm)	Size / Symbol	Min. (mm)	Max. (mm)
A	3.424	3.776	E	6.250	6.450
A1	0.100	0.300	E1	9.450	9.850
A2	3.324	3.476	e	0.540BSC	
B	0.440	0.520	L	0.920	1.120
B1	1.484	1.564	L1	0.065REF	
c	0.204	0.304	θ	0 °	8 °
D	9.100	9.300			

Top mark	Package
PN PN8055 YWWXXXXX	SMP7

Note: Y: Year Code; WW: Week Code; XXXXX: Internal Code

Notes:
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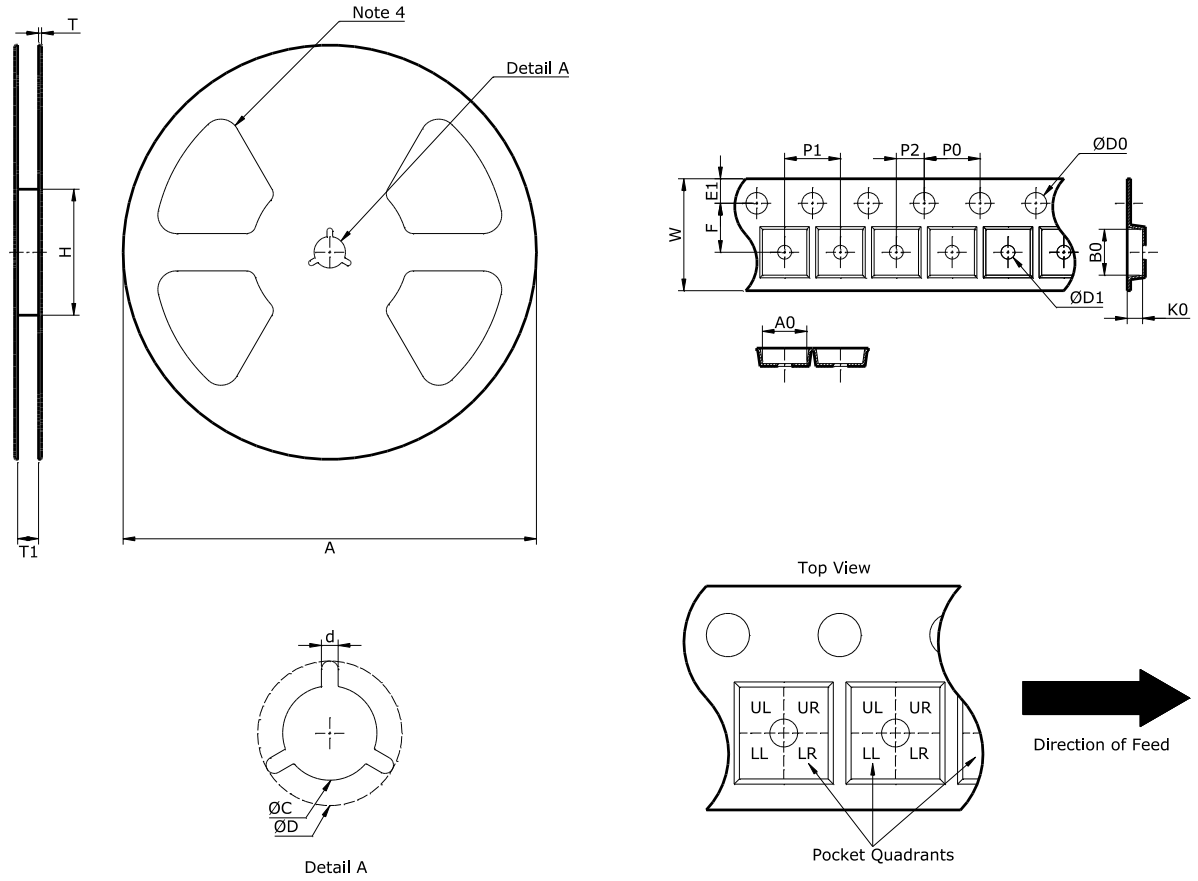
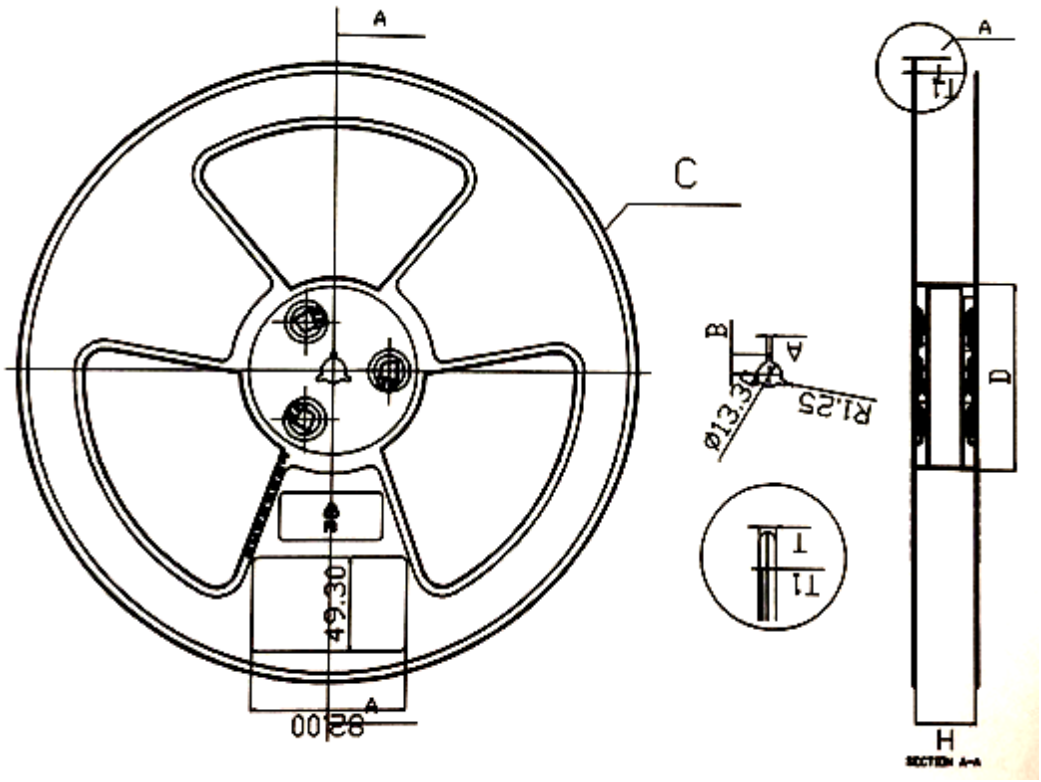
Tape and Reel Information



SOP7 Package									
A (mm)	**T (mm)**	**T1 (mm)**	**H (mm)**	**ØC (mm)**	**ØD (mm)**	**d (mm)**	**A0 (mm)**	**B0 (mm)**	**K0 (mm)**
330 ±1.0	3 +1/-0	12.4 +1/-0	100 ±0.5	12.00 +0.5/-0.2	17.70 ±0.40	2 +0.5/-0.2	6.60 ±0.1	5.3 ±0.1	1.9 ±0.1
W (mm)	**F (mm)**	**E1 (mm)**	**P0 (mm)**	**P1 (mm)**	**P2 (mm)**	**ØD0 (mm)**	**ØD1 (mm)**	**Pin 1 Quadrant**	
12.00 ±0.1	5.50 ±0.1	1.75 ±0.10	4.00 ±0.10	8.0 ±0.1	2.0 ±0.1	1.5 +0.1/-0	1.55 ±0.05	UL	

Notes:
1. This drawing is subjected to change without notice.
2. All dimensions are nominal and in mm.
3. This drawing is not in scale and for reference only. Customer can contact Chipown sales representative for further details.
4. The number of flange openings depends on the reel size and assembly site. This drawing shows an example only.

Tape and Reel Information



				Unit: MM
Material: PS		Unspecified tolerance: ±0.2		
H	12	16	24	32
C ±0.2	330	330	330	330
T1 ±0.2	1.45	1.45	1.45	1.45
B ±0.2	10.7	10.7	10.7	10.7
A ±0.2	2.5	2.5	2.5	2.5
T ±0.2	1.85	1.85	1.85	1.85
D ±0.2	100	100	100	100

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