CD4099B Types

CMOS
8-Bit Addressable Latch

High-Voltage Types (20-Volt Rating)

■ CD4099B 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.
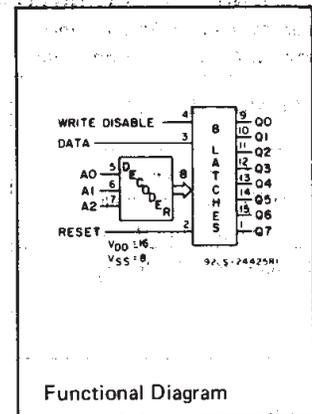
The CD4099B types are supplied in 16-lead hermetic ceramic dual-in-line packages (F3A suffix), 16-lead plastic dual-in-line packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

■ Serial data input   ■ Active parallel output
■ Storage register capability   ■ Master clear
■ Can function as demultiplexer
■ Standardized, symmetrical output characteristics
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 μA at 18 V (full package-temperature range), 100 nA at 18 V and 25°C
■ Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

■ Multi-line decoders
■ A/D converters

Functional Diagram

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  Voltages referenced to V_{SS} Terminal) .... –0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... –0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
  For T_A = –55°C to +100°C 500mW
  For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE–TEMPERATURE RANGE (All Package Types) 100mW
OPERATING–TEMPERATURE RANGE (T_A) .... –55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... –65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

Fig. 1 — Logic diagram of CD4099B and detail of 1 of 8 latches.

92CM-2767R1

TERMINAL ASSIGNMENT
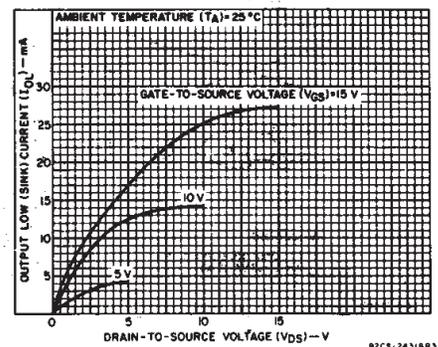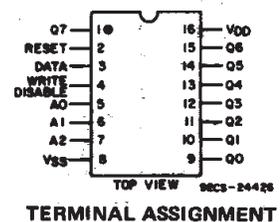
Fig. 2 — Typical output low (sink) current characteristics.

CD4099B Types

RECOMMENDED OPERATING CONDITIONS *at $T_A = 25°C$ (Unless otherwise specified)*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	SEE FIG. 15*	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply Voltage Range: (At T_A = Full Package Temperature Range)			3	18	V
Minimum Pulse Width, t_W Data	4	5	200	—	
		10	100	—	
		15	80		
Address	8	5	400	—	ns
		10	200	—	
		15	125		
Reset	5	5	150	—	
		10	75	—	
		15	50	—	
Setup Time, t_S Data to WRITE DISABLE	6	5	100	—	
		10	50	—	
		15	35	—	ns
Hold Time, t_H Data to WRITE DISABLE	7	5	150	—	
		10	75	—	ns
		15	50	—	

* Circled numbers refer to times indicated on master timing diagram.

Note: In addition to the above characteristics, a WRITE DISABLE ON time (the time that WRITE DISABLE is at a high level) must be observed during an address change for the total time that the external address lines A0, A1, and A2 are settling to a stable level, to prevent a wrong cell from being addressed (see Fig. 3).
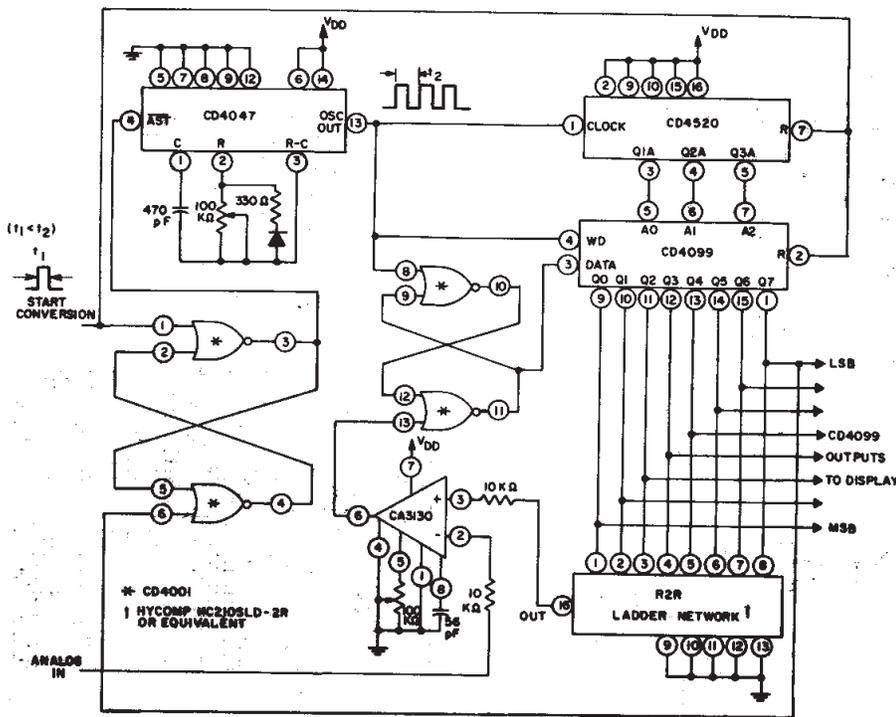
MODE SELECTION

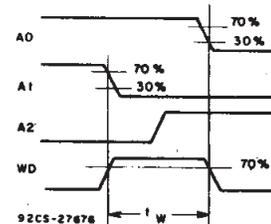| WD	R	ADDRESSED LATCH	UNADDRESSED LATCH
0	0	Follows Data	Holds Previous State
0	1	Follows Data (Active High 8-Channel Demultiplexer)	Reset to "0"
1	0	Holds Previous State	
1	1	Reset to "0"	Reset to "0"

WD = WRITE DISABLE   R = RESET
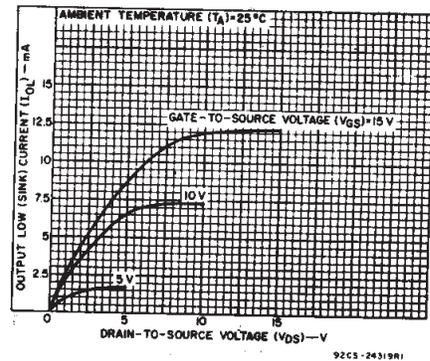

Fig. 3 — Definition of WRITE DISABLE ON time.

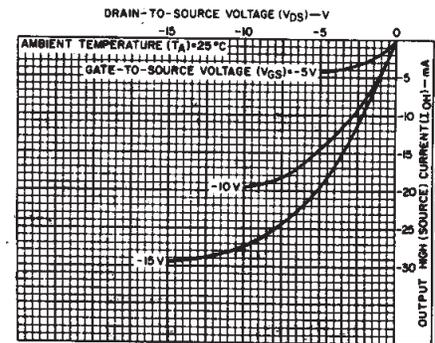Fig. 4 — Minimum output low (sink) current characteristics.
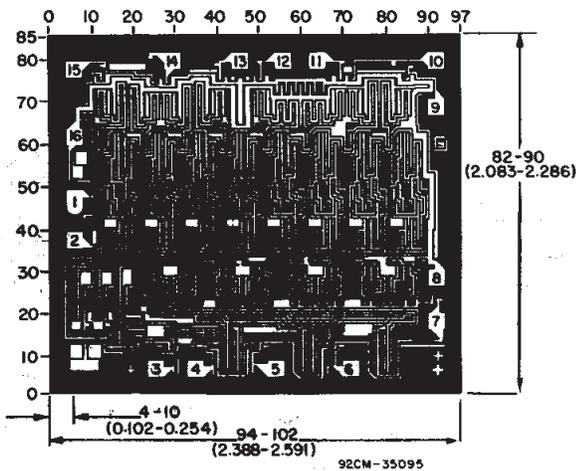

Fig. 5 — A/D converter

Fig. 6 — Typical output high (source) current characteristics.

3-232

CD4099B Types

STATIC ELECTRICAL CHARACTERISTICS

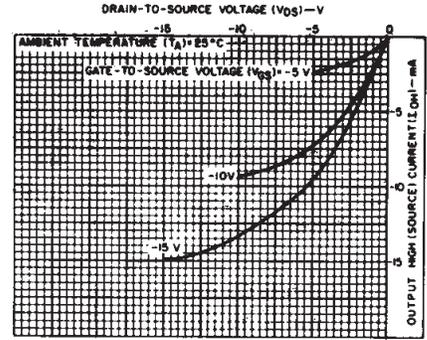| CHARACTER-ISTIC	CONDITIONS VQ (V)	VIN (V)	VDD (V)	LIMITS AT INDICATED TEMPERATURES (°C) −55	−40	+85	+125	+25 Min.	Typ.	Max.	UNITS
Quiescent Device Current, IDD Max.	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current IOL Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, IOH Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	mA
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, VOL Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, VOH Min.	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, VIL Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, VIH Min.	0.5, 4.5	–	5	3.5				3.5	–	–	V
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current IIN Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA

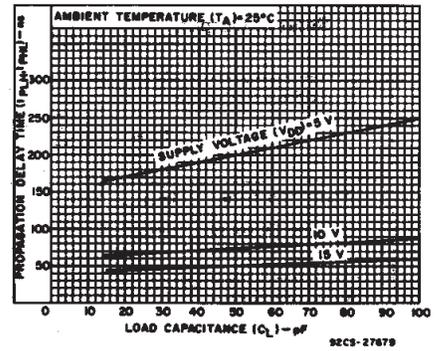Fig.7 — Minimum output high (source) current characteristics.

Fig. 8 — Typical propagation delay time (data to Qn) vs. load capacitance.

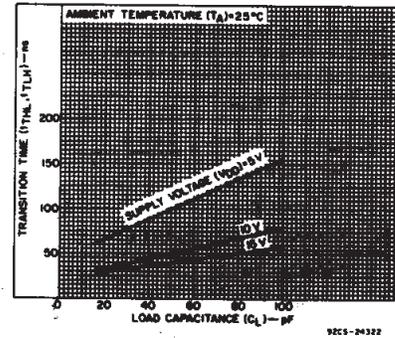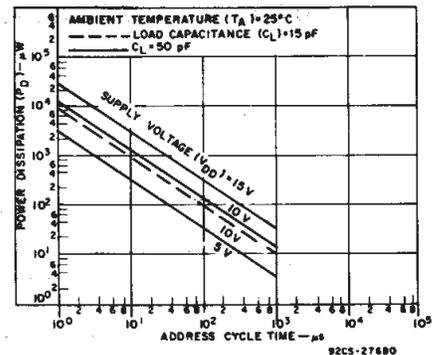Fig. 9 — Typical transition time vs. load capacitance.

Fig.10 — Typical dynamic power dissipation vs. address cycle time.

CD4099BH
DIMENSIONS AND PAD LAYOUT

82-90
(2.083-2.286)

4-10
(0.102-0.254)

94-102
(2.388-2.591)

92CM-35095

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

3

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $C_L = 50\,pF$,
Input t_r, $t_f = 20\,ns$, $R_L = 200\,K\Omega$

CHARACTERISTIC	CONDITIONS		LIMITS ALL PACKAGE TYPES		UNITS
	SEE FIG.15*	V_{DD} (V)	TYP.	MAX.	
Propagation Delay: t_{PLH}, t_{PHL} Data to Output,	①	5	200	400	
		10	75	150	
		15	50	100	
WRITE DISABLE to Output, t_{PLH}, t_{PHL}	②	5	200	400	ns
		10	80	160	
		15	60	120	
Reset to Output, t_{PHL}	③	5	175	350	
		10	80	160	
		15	65	130	
Address to Output, t_{PLH}, t_{PHL}	⑨	5	225	450	
		10	100	200	
		15	75	150	
Transition Time, t_{THL}, (Any Output) t_{TLH}		5	100	200	
		10	50	100	ns
		15	40	80	
Minimum Pulse Width, t_W Data	④	5	100	200	
		10	50	100	ns
		15	40	80	
Address	⑧	5	200	400	
		10	100	200	ns
		15	65	125	
Reset	⑤	5	75	150	
		10	40	75	ns
		15	25	50	
Minimum Setup Time, t_S Data to WRITE DISABLE	⑥	5	50	100	
		10	25	50	ns
		15	20	35	
Minimum Hold Time, t_H Data to WRITE DISABLE	⑦	5	75	150	
		10	40	75	ns
		15	25	50	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

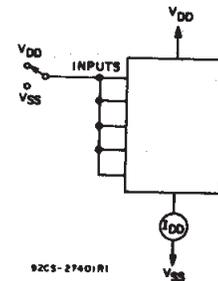*Circled numbers refer to times indicated on master timing diagram.
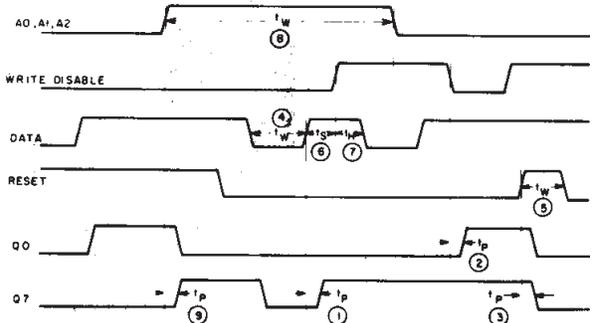
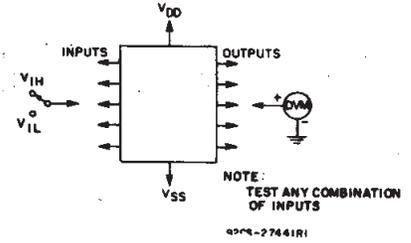Fig. 11 — Quiescent device current test circuit.

Fig. 12 — Input voltage test circuit.
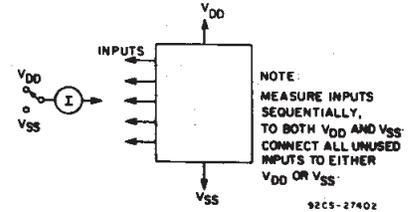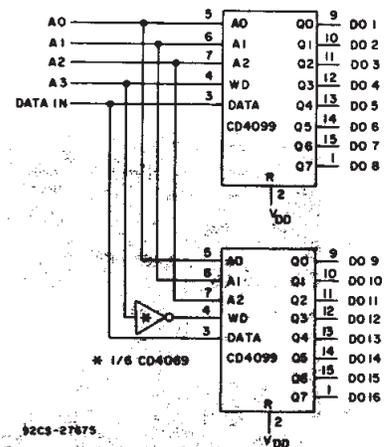

Fig. 13 — Input current test circuit.

Fig. 14 — 1 of 16 decoder/demultiplexer.
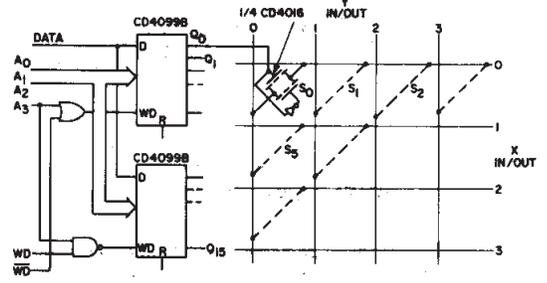

Fig. 15 — Master timing diagram.

Fig. 16 — Multiple selection decoding — 4 x 4 crosspoint switch.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4099BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4099BE	Samples
CD4099BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4099BE	Samples
CD4099BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4099BF	Samples
CD4099BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4099BF3A	Samples
CD4099BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4099BM	Samples
CD4099BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4099BM	Samples
CD4099BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4099BM	Samples
CD4099BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4099B	Samples
CD4099BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM099B	Samples
JM38510/17601BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 17601BEA	Samples
M38510/17601BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 17601BEA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4099B, CD4099B-MIL :

● Catalog: CD4099B

● Military: CD4099B-MIL

NOTE: Qualified Version Definitions:

      ● Catalog - TI's standard catalog product

      ● Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
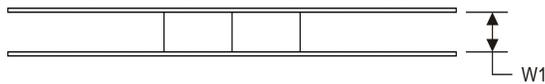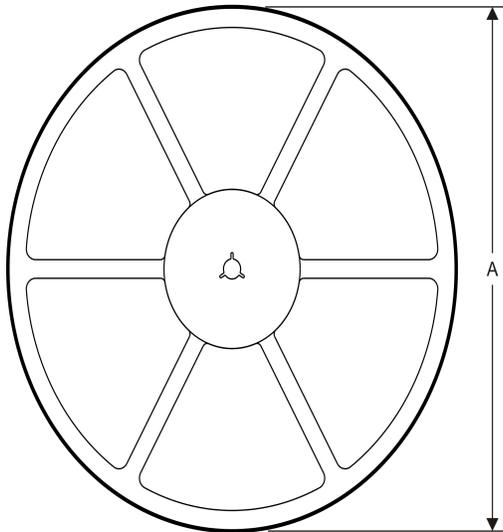
TAPE DIMENSIONS
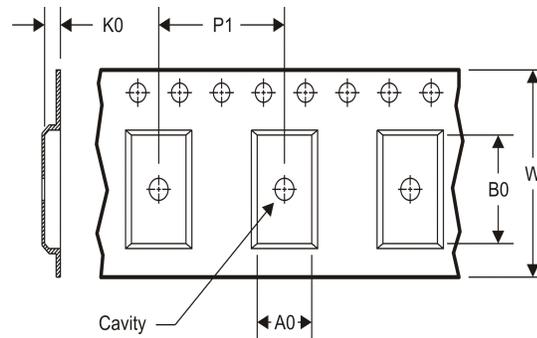
A0	Dimension designed to accommodate the component width	
B0	Dimension designed to accommodate the component length	
K0	Dimension designed to accommodate the component thickness	
W	Overall width of the carrier tape	
P1	Pitch between successive cavity centers	

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4099BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4099BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4099BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4099BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4099BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD4099BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R−PDSO−G16) PLASTIC SMALL OUTLINE
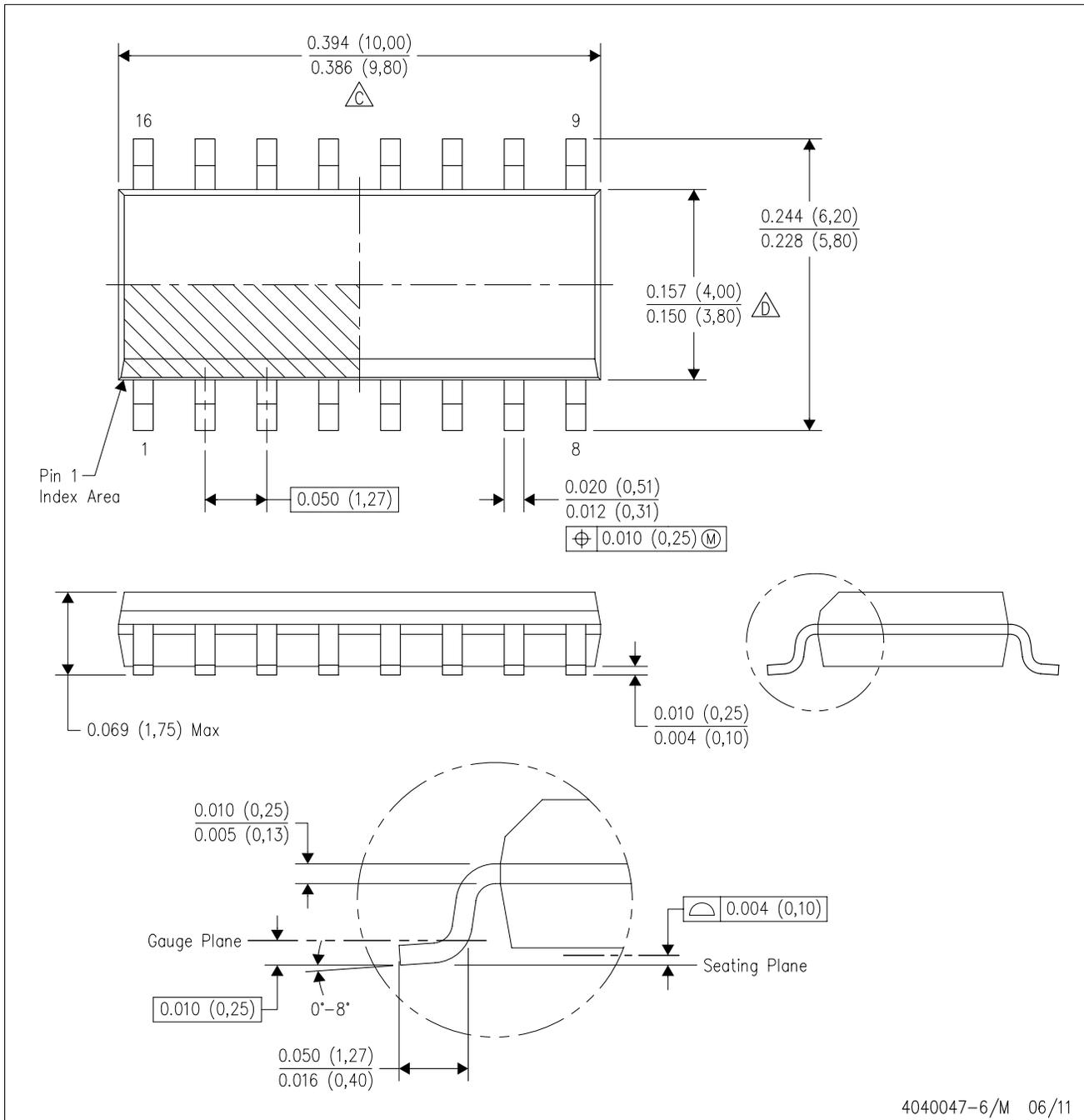
0.394 (10,00)
0.386 (9,80)
⚠C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⚠D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

◎ 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040047-6/M 06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
     ⚠C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
          not exceed 0.006 (0,15) each side.
     ⚠D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS–012 variation AC.
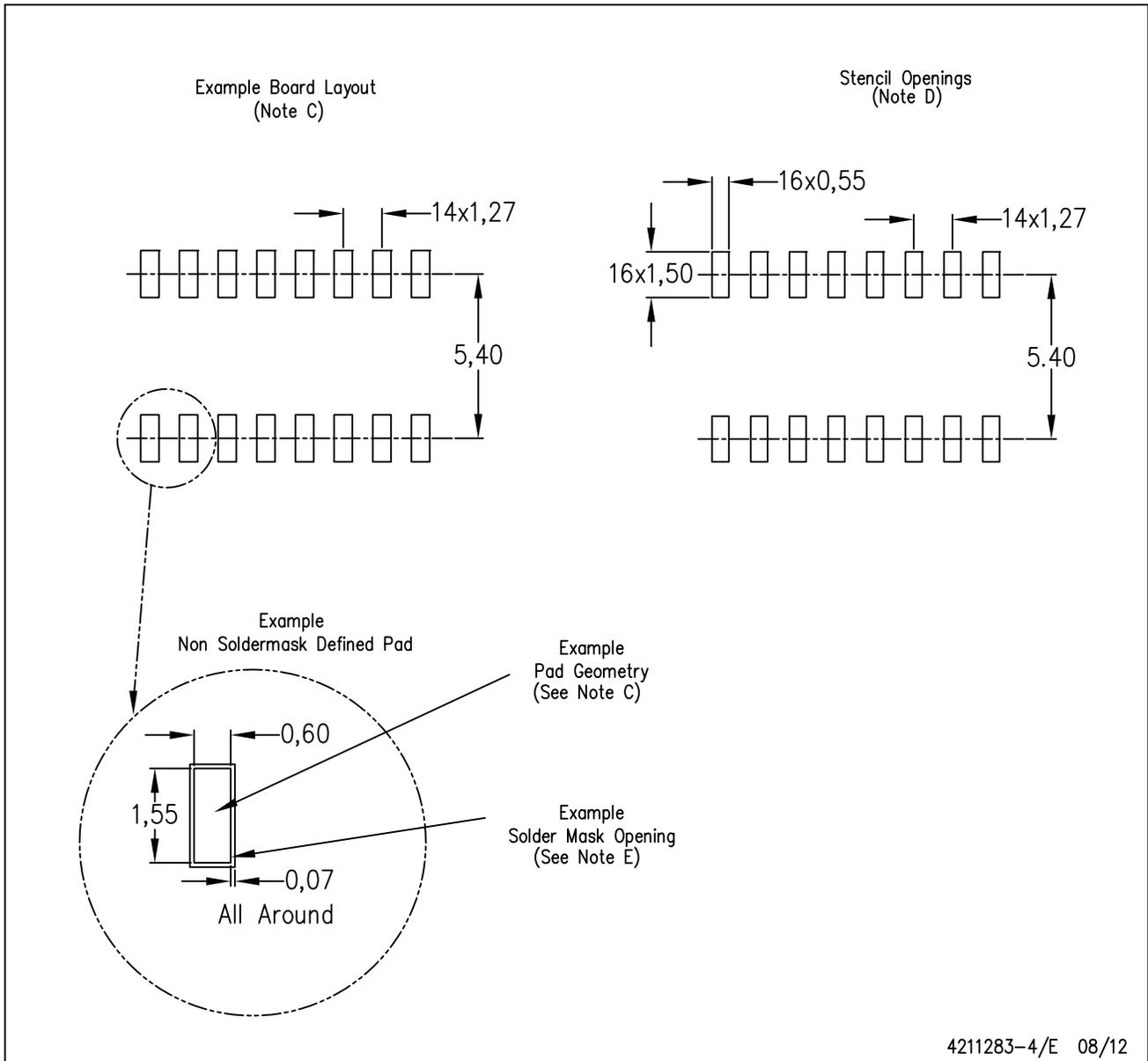
**TEXAS
INSTRUMENTS**
www.ti.com

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x1,27

16x0,55

14x1,27

16x1,50

5,40

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

Example
Solder Mask Opening
(See Note E)

1,55

0,07

All Around

4211283−4/E 08/12

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Publication IPC−7351 is recommended for alternate designs.
          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
INSTRUMENTS
www.ti.com

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN
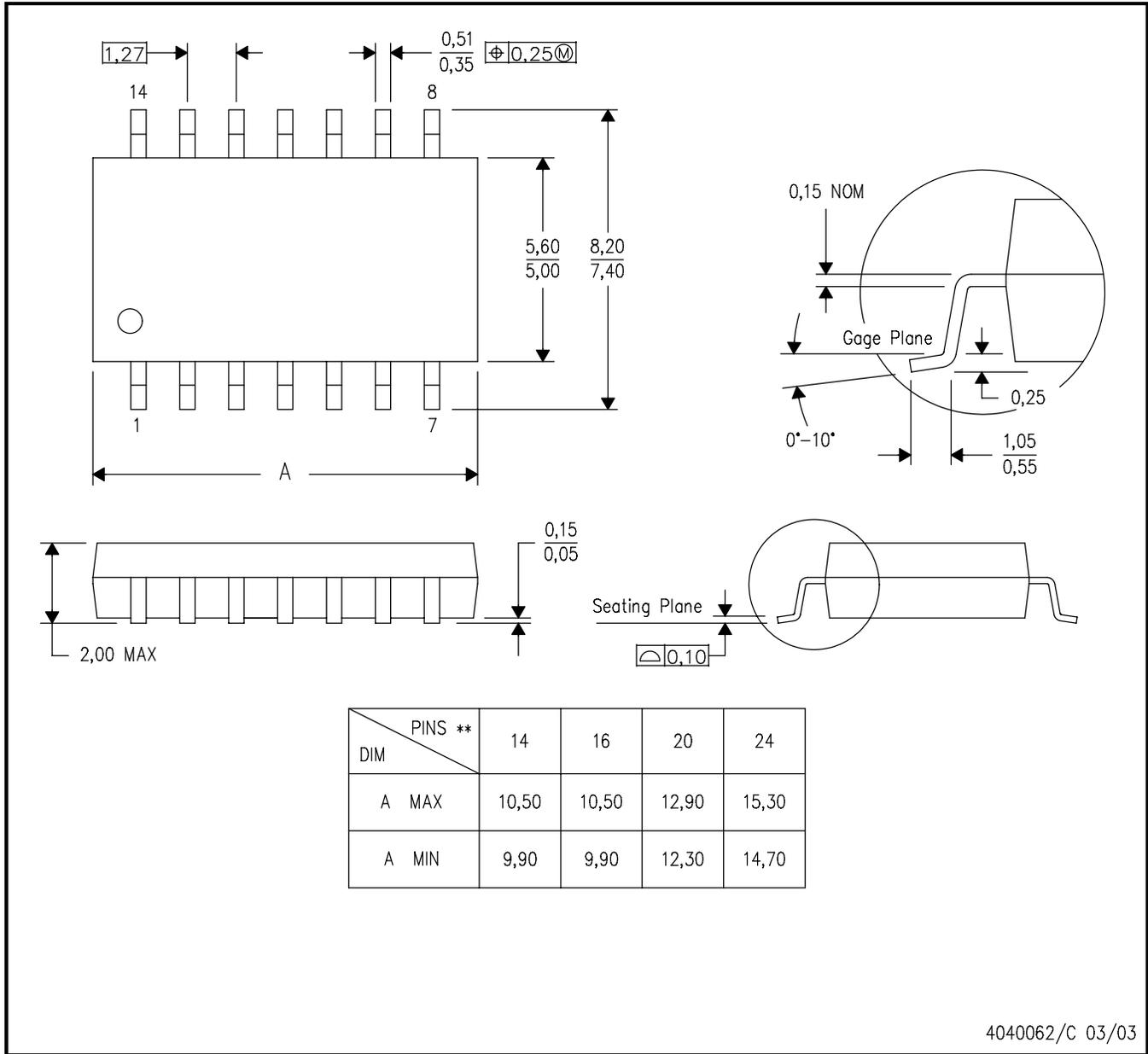
	PINS **	14	16	20	24
DIM					
A	MAX	10,50	10,50	12,90	15,30
A	MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R—GDIP—T**)   CERAMIC DUAL IN—LINE PACKAGE
14 LEADS SHOWN
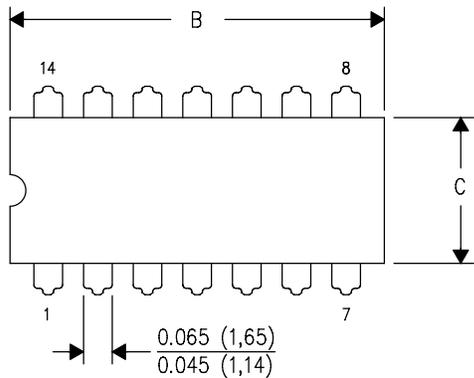
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°—15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

16   9

△D 4,50
    4,30

6,60
6,20

1   8

5,10
4,90

△C

0,15 NOM

Gage Plane

0,25

0°−8°

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ 0,10

4040064−4/G 02/11
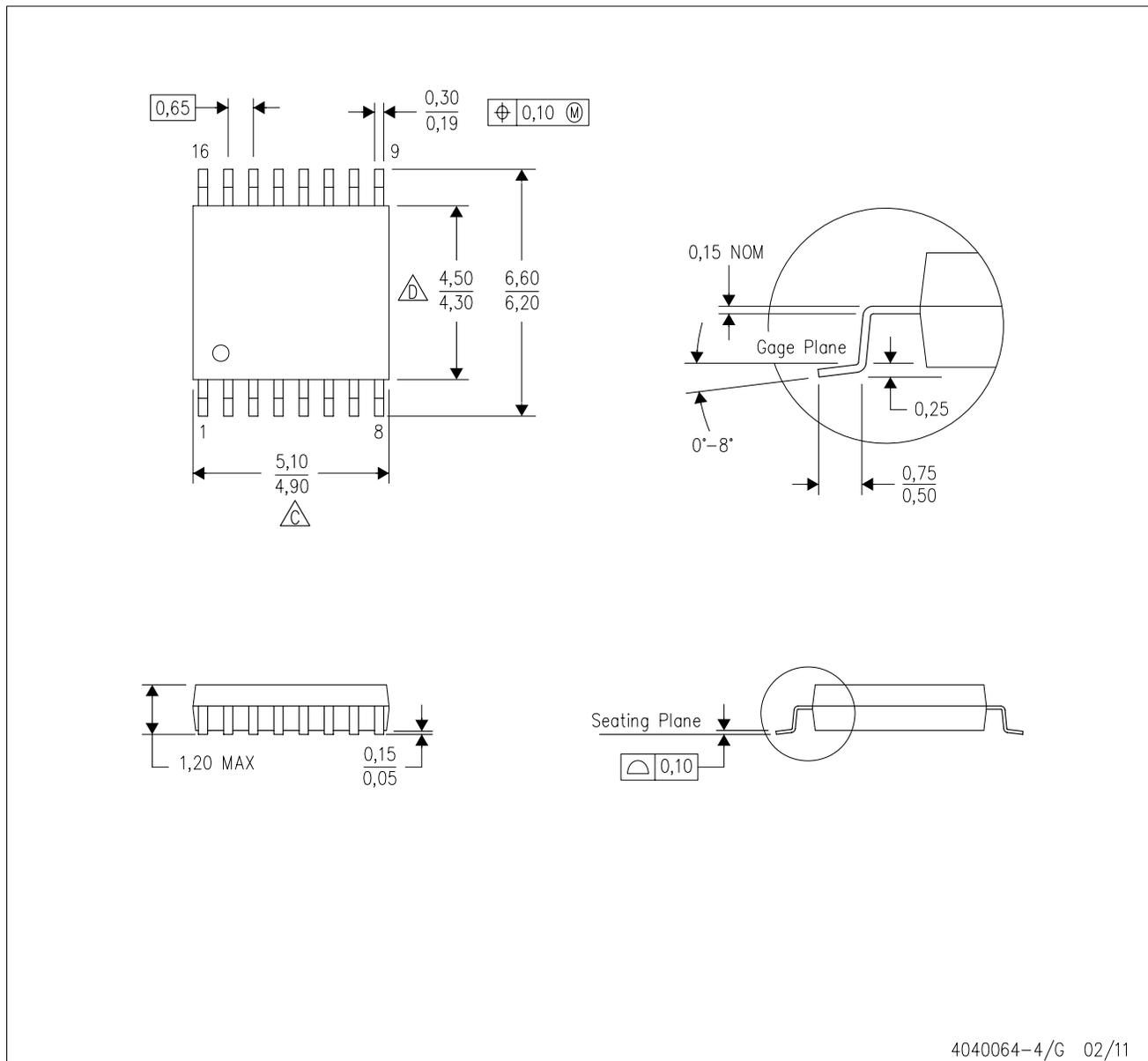
NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
        △C   Body length does not include mold flash, protrusions, or gate burrs.   Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
        △D   Body width does not include interlead flash.   Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

PW (R—PDSO—G16)   PLASTIC SMALL OUTLINE
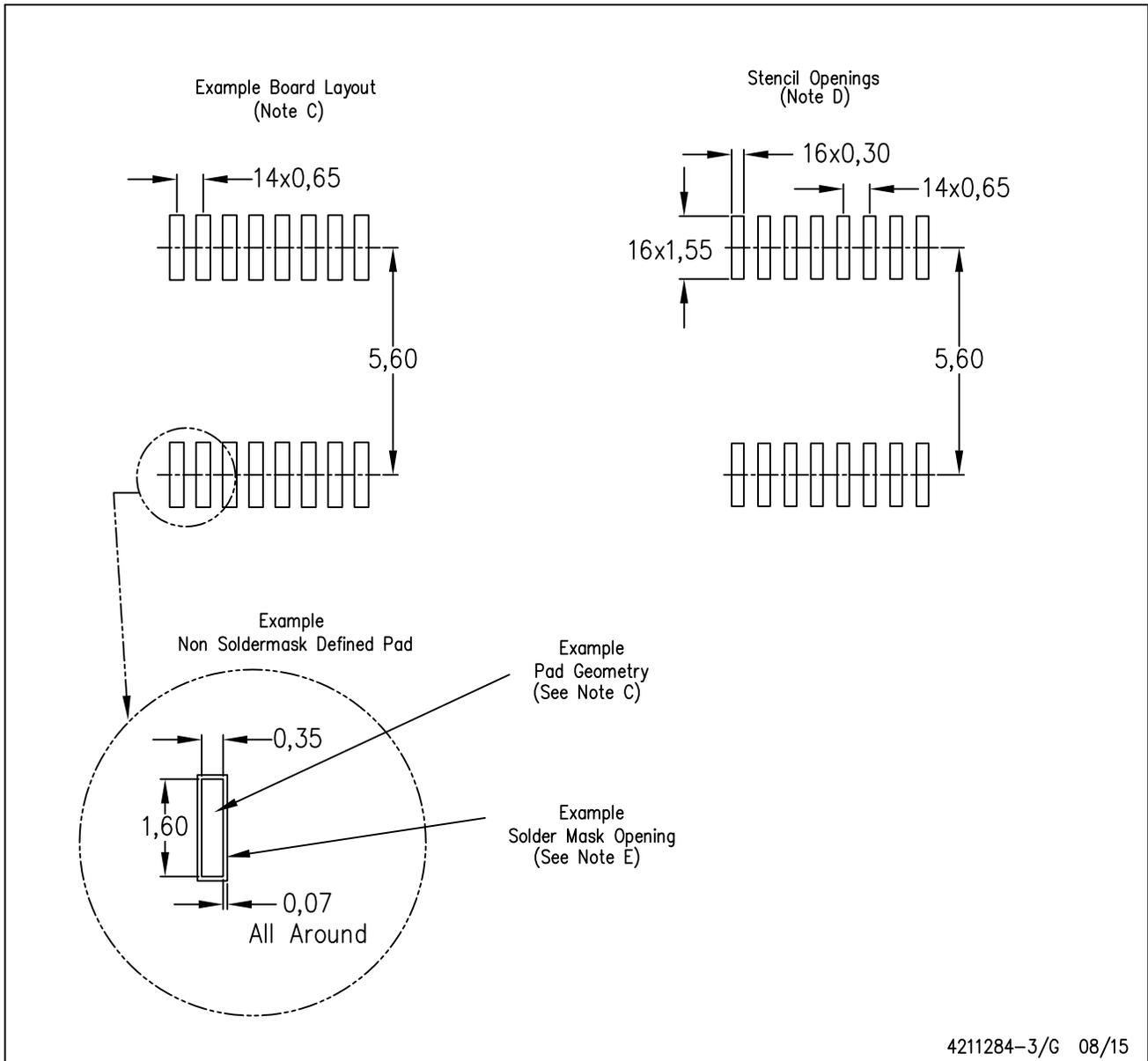
Example Board Layout
(Note C)

⊢—14x0,65

5,60

Stencil Openings
(Note D)

⊢— 16x0,30

⊢—14x0,65

16x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

⊢—0,35

1,60

Example
Solder Mask Opening
(See Note E)

⊢— 0,07
All Around

4211284–3/G   08/15

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate designs.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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N (R−PDIP−T**)

PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

	PINS **	14	16	18	20
DIM					
A MAX		0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN		0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
⚠C MS−001 VARIATION		AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) ⚠D

0.045 (1,14) / 0.030 (0,76) ⚠D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option ⚠D

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
     ⚠C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
     ⚠D The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE