NIKO-SEM

P-Channel Logic Level Enhancement Mode Field Effect Transistor

P2504EDG

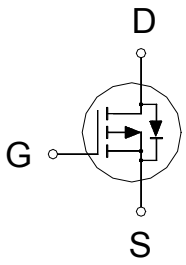
TO-252

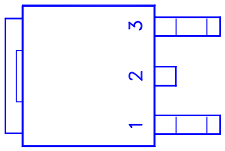
Halogen-Free & Lead- Free

RoHS Compliant

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-40V	25.8mΩ	-18A





1. GATE
2. DRAIN
3. SOURCE

100% UIS tested
100% Rg tested

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	-18	A
	T_C = 70 °C		-13.5	
Pulsed Drain Current[1]		I_{DM}	-40	
Power Dissipation	T_C = 25 °C	P_D	42	W
	T_C = 70 °C		27	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		3	°C / W
Junction-to-Ambient	$R_{\theta JA}$		75	°C / W

[1]Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

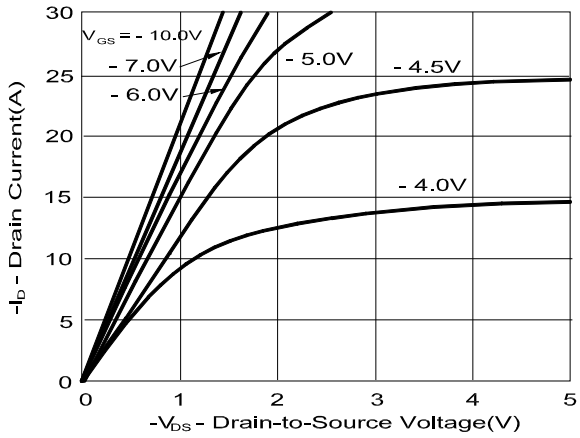
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.5	-2.2	-3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±250	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -32V, V_{GS} = 0V			1	μA
		V_{DS} = -30V, V_{GS} = 0V, T_J = 125 °C			10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-40			A

Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -7V, I_D = -10A		30	40	mΩ
		V_{GS} = -10V, I_D = -18A		22	25.8	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -18A		20		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		1570		pF
Output Capacitance	C_{oss}			320		
Reverse Transfer Capacitance	C_{rss}			210		
Total Gate Charge[2]	Q_g	V_{DS} = 0.5$V_{(BR)DSS}$, V_{GS} = -10V, I_D = -18A		29		nC
Gate-Source Charge[2]	Q_{gs}			6		
Gate-Drain Charge[2]	Q_{gd}			7		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = -20V, R_L = 1Ω, $I_D \cong$ -1A, V_{GS} = -10V, R_{GS} = 6Ω		12		nS
Rise Time[2]	t_r			29		
Turn-Off Delay Time[2]	$t_{d(off)}$			42		
Fall Time[2]	t_f			33		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I_S				-18	A
Forward Voltage[1]	V_{SD}	I_F = -18A , V_{GS} = 0V			-1.3	V
Reverse Recovery Time	t_{rr}	I_F = -18 A, dI_F/dt = 100A / μS		29		nS
Reverse Recovery Charge	Q_{rr}			21		nC

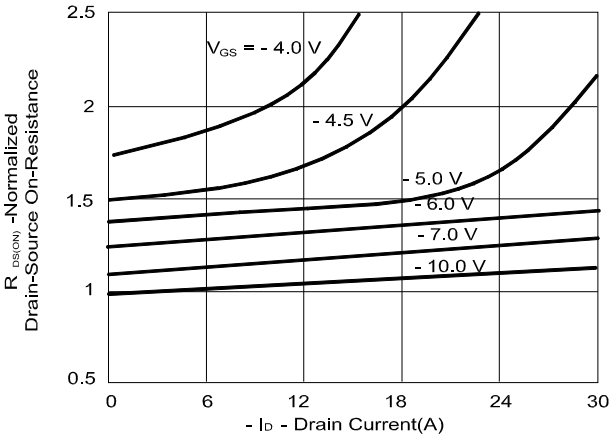
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

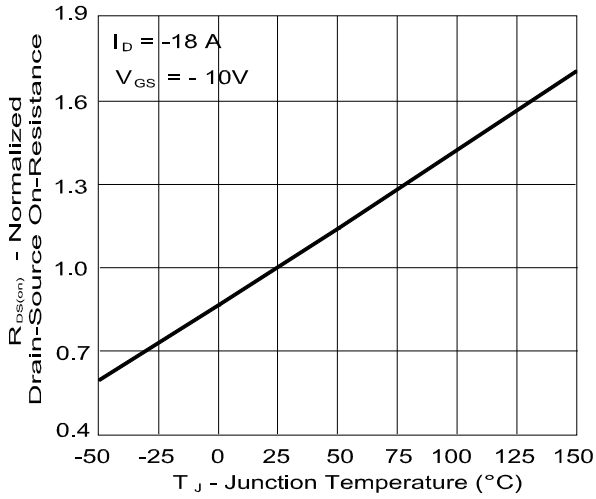
On-Region Characteristics



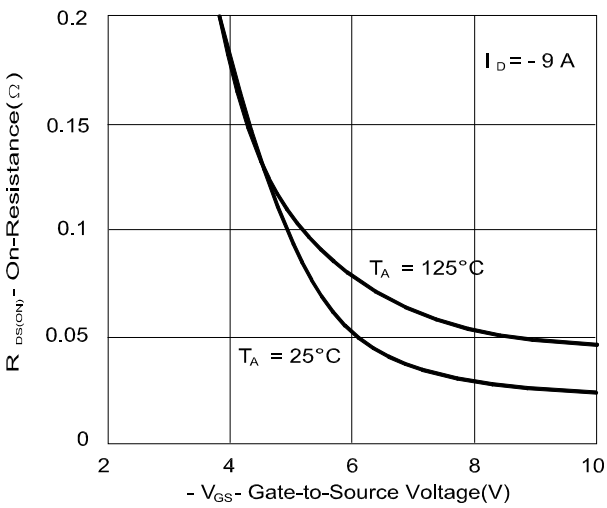
On-Resistance Variation with Drain Current and Gate Voltage



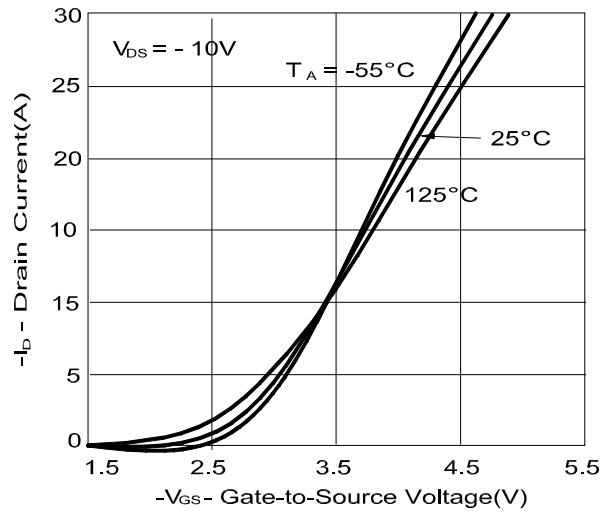
On-Resistance Variation with Temperature



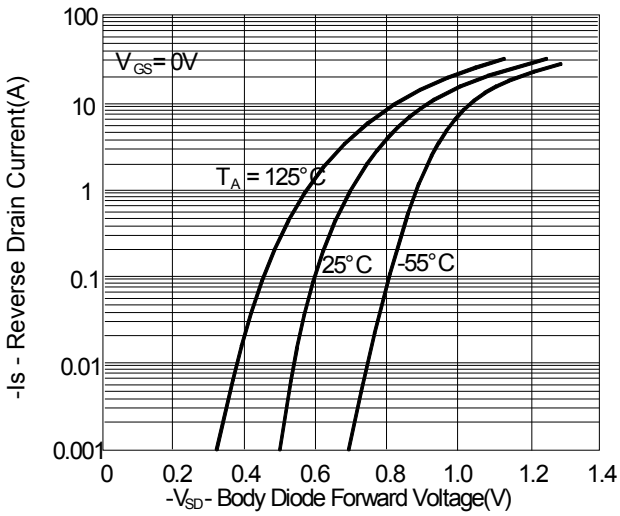
On-Resistance Variation with Gate-to-Source Voltage



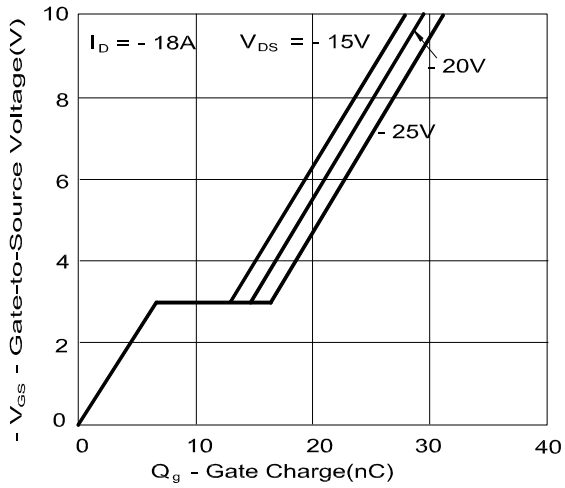
Transfer Characteristics



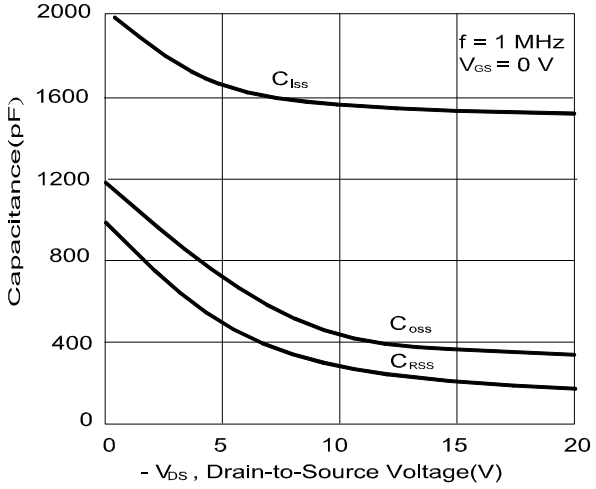
Body Diode Forward Voltage Variation with Source Current and Temperature



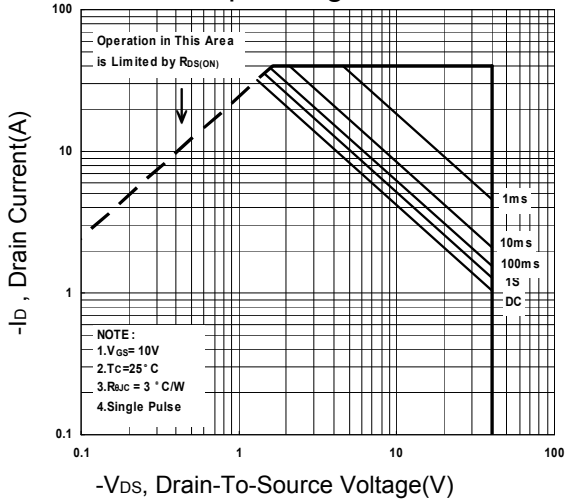
Gate Charge Characteristics



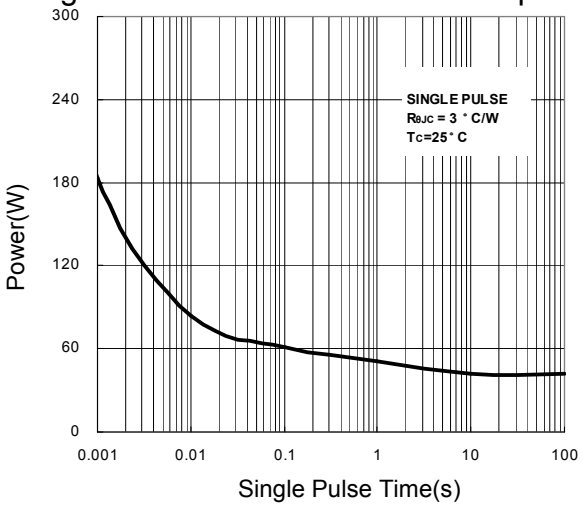
Capacitance Characteristics



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

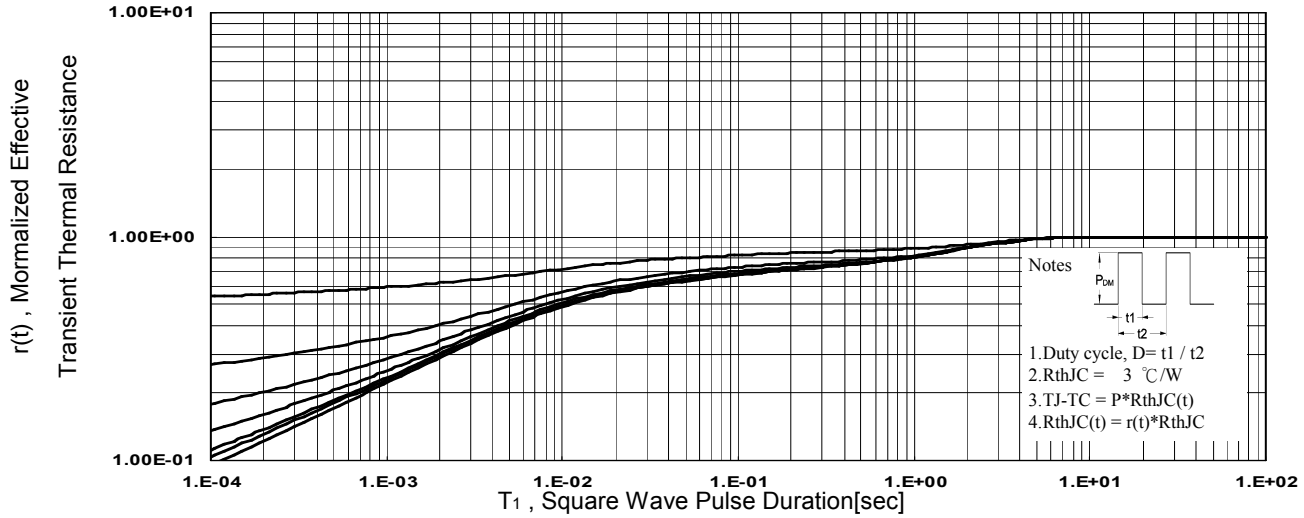


Figure 1
Gate Charge Test Circuit

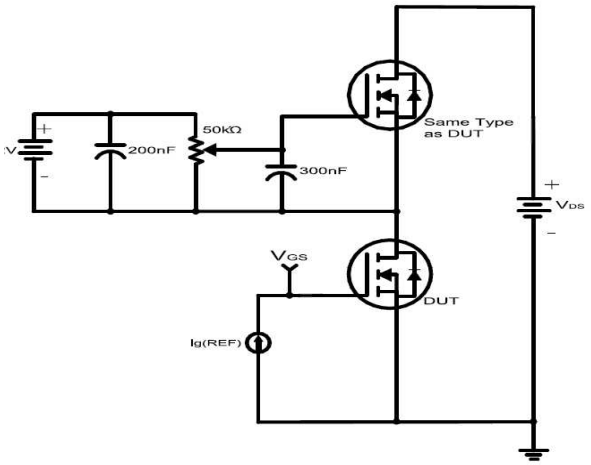


Figure 2
Gate Charge Waveforms

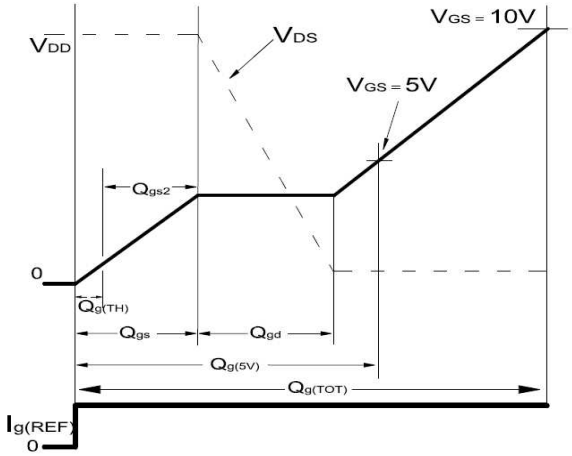


Figure 3
Switching Time Test Circuit

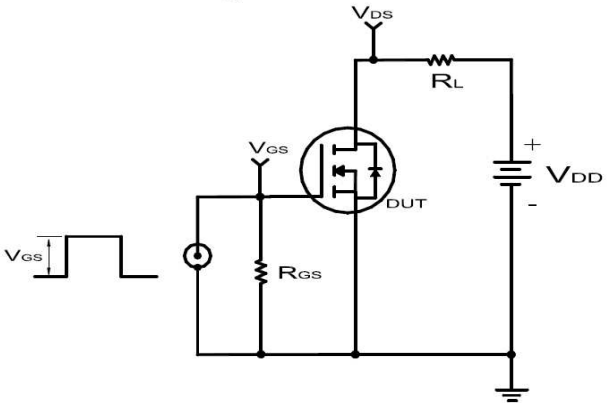


Figure 4
Switching Time Waveforms

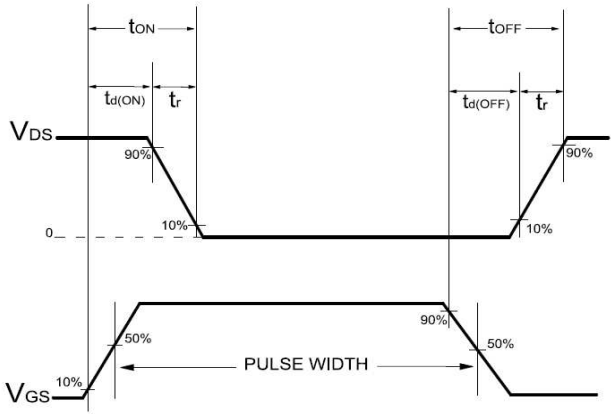


Figure 5
Unclamped Energy Test Circuit

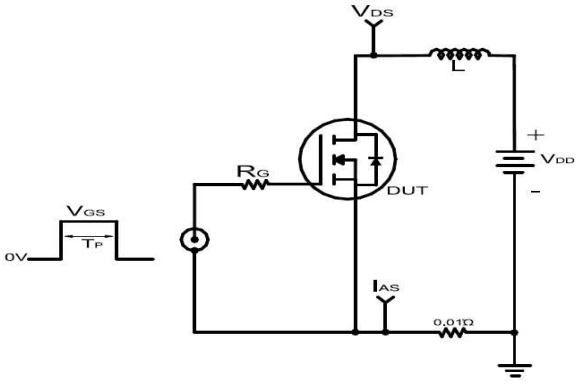


Figure 6
Unclamped Energy Waveforms

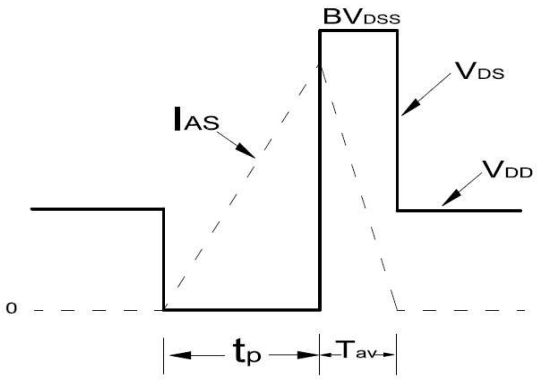


Figure 7

Diode Recovery Test Circuit

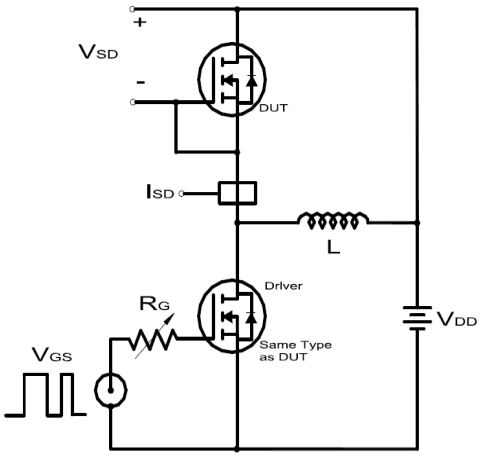


Figure 8

Diode Recovery Test Waveforms