1 Overview

STC8H series of microcontrollers do not require an external crystal oscillator and external reset circuit. They are 8051 microcontrollers with the properties of strong anti-interference/ultra low price/high speed/low power consumption. Under the same operating frequency, STC8H series of microcontrollers are about 12 times faster (11.2 ~ 13.2 times) than traditional 8051. To execute all 111 instructions in sequence, the STC8H series microcontroller only needs 147 clocks, while the traditional 8051 requires 1944 clocks. STC8H series of microcontrollers are single clock/machine cycle (1T) microcontrollers produced by STC. They are new generation 8051 microcontrollers with wide voltage/high speed / high reliability / low power consumption / strong antistatic / strong anti-interference, and is super encrypted. The instruction codes are fully compatible with traditional 8051.

High precision of ±0.3% @+25℃ RC clock is integrated in MCU with −1.38% to +1.42% temperature drift under the temperature range of -40℃ to +85℃, and 0.88% to +1.05% temperature drift under temperature range from -20℃ to +65℃. The frequency of RC clock can be set from 4MHz to 35MHz when programming a MCU using ISP. Note: The maximum frequency must be controlled below 35MHz when the temperature range is -40℃ to + 85℃. Moreover, high reliable reset circuit is integrated in MCU with 4 levels optional reset threshold voltages, which can be selected when user programming using ISP. So, external expensive crystal and the external reset circuit can be eliminated completely.

There are three optional clock sources inside the MCU, internal high precision IRC which can be adjusted appropriately, internal 32KHz low speed IRC, external 4MHz~33MHz oscillator or external clock signal. The clock source can be freely chosen in user codes. After the clock source is selected, it may be 8-bit divided and then be supplied to the CPU and the peripherals, such as timers, UARTs, SPI, and so on.

Two low power modes are provided in MCU, the IDLE mode and the STOP mode. In IDLE mode, MCU stops clocking CPU, CPU stops executing instructions without clock, while all peripherals are still working. At this moment, the power consumption is about 1.0mA at 6MHz working frequency. The STOP mode is the power off or power-down mode. At this momont, the main clock stops, CPU and all peripherals stop working, and the power consumption can be reduced to about 0.6uA when VCC is 5.0V, 0.4uA when VCC is 3.3V.

The Power-down mode can be woke-up by one of the following interrupts: INT0(P3.2), INT1(P3.3), INT2(P3.6), INT3(P3.7), INT4(P3.0), T0(P3.4), T1(P3.5), T2(P1.2), T3(P0.4), T4(P0.6), RXD(P3.0/P3.6/P1.6/P4.3), RXD2(P1.0/P4.6), RXD3(P0.0/P5.0), RXD4(P0.2/P5.2), I2C_SDA(P1.4/P2.4/P3.3), Comparator, LVD, Power-down wake-up timer.

Rich digital peripherals and analog peripherals are provided in MCU, including UARTs, timers, enhanced PWMs and I2C, SPI, USB, ultra-high speed ADC and comparator, which can meet the requirements of users when designing a product.

The enhanced dual data pointers are integrated in the STC8H series of microcontrollers. Using user codes, the function of automatic increasing or decreasing of data pointer and automatic switching of two sets of data pointers can be realized.

Products Line	I/O	UART	Timers	ADC	Enhanced PWM	CMP	SPI	I2C	USB	MDU16	LED DRV	Touch Key	RTC	I/O Int.	Color LCM	LCD DRV	DMA
STC8H1K08 family	17	2	3	$9_{CH}*10_{B}$	●	●	●	●									
STC8H1K28 family	29	2	5	$12_{CH}*10_{B}$	●	●	●	●									
STC8H3K64S4 family	45	4	5	$12_{CH}*12_{B}$	●	●	●	●		●				●			
STC8H3K64S2 family	45	2	5	$12_{CH}*12_{B}$	●	●	●	●		●				●			
STC8H8K64U family Version A	60	4	5	$15_{CH}*12_{B}$	●	●	●	●	●	●							
STC8H8K64U familyVersion B	60	4	5	$15_{CH}*12_{B}$	●	●	●	●	●	●			●	●	●		●
STC8H2K64T family	44	4	5	$15_{CH}*12_{B}$	●	●	●	●		●	●	●	●	●			
STC8H4K64TLR family	44	4	5	$15_{CH}*12_{B}$	●	●	●	●		●	●	●	●	●	●		●
STC8H4K64TLCD family	60	4	5	$15_{CH}*12_{B}$	●	●	●	●		●		●	●	●	●	●	●
STC8H4K64LCD family	61	4	5	$15_{CH}*12_{B}$	●	●	●	●		●			●	●	●	●	●
STC8H1K08TR family	16	2	3	$15_{CH}*12_{B}$	●	●	●	●		●		●	●	●	●		●

2 Features

2.1 STC8H1K08-36I-TSSOP20/QFN20 family

2.1.1Features and Price

➢ **Selection and price (No external crystal and external reset required with 9 channels 10-bit ADC)**

MCU	Operating voltage (V)	Flash Code Memory (100 thousand times) (Byte)	Idata, Internal DATA RAM(Byte)	Xdata, Internal extended SRAM (Byte)	Enhanced Dual DPTR(increasing or decreasing)	EEPROM 100 thousand times) (Byte)	Maximum I/O Lines	Traditional I/O interrupt(INT0/INT1/INT2/INT3/INT4) (can wake-up CPU)	UARTs which can wake-up CPU	SPI	I²C which can wake-up CPU	Timers/Counters (T0-T2 Pin can wake-up CPU)	16-bit advanced PWM timers with Complementary symmetrical dead-time	Power-down Wake-up timer	9-channels high speed ADC (8 PWMs can be used as 8 DACs)	Comparator (May be used as ADC to detect external power-down)	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4 level optional reset threshold	Internal high precision Clock (adjustabal under 35MHz)	Clock output and Reset	Program encrypted transmission (Anti-blocking)	Password can be set for next update	Support RS485 download	Support software USB download directly	Online debugging	Price & Package: TSSOP20 <6.5mm*6.5mm>	Price & Package: QFN20 <3mm*3mm>	Main product supply information
STC8H1K08	1.9-5.5	8K	256B	1K	2	4K	17	Y	2	Y	Y	3	8	Y	10bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		√	Available
STC8H1K17	1.9-5.5	17K	256B	1K	2	IAP	17	Y	2	Y	Y	3	8	Y	10bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	√	√	
~~STC8H1K12~~	~~1.9-5.5~~	~~12K~~	~~256B~~	~~1K~~	~~2~~	~~IAP~~	~~17~~	~~¥~~	~~2~~	~~¥~~	~~¥~~	~~3~~	~~8~~	~~¥~~	~~10bit~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	Not available		

➢ **Core**
- ✓ Ultra-high speed 8051 Core with single clock per machine cycle, which is called 1T, and the speed is about 12 times faster than traditional 8051
- ✓ Fully compatible instruction set with traditional 8051
- ✓ 17interrupt sources and 4 interrupt priority levels
- ✓ Online debugging is supported

➢ **Operating voltage**
- ✓ 1.9V～5.5V

➢ **Operating temperature**
- ✓ -40℃~85℃(The chip is produced in -40℃～125℃ process. Please refer to the description of the electrical characteristics chapter for applications beyond the temperature range)

➢ **Flash memory**
- ✓ Up to 17Kbytes of Flash memory to be used for storing user code
- ✓ Configurable size EEPROM, 512bytes single page for being erased, which can be repeatedly erased more than 100 thousand times.
- ✓ In-System-Programming, ISP in short, can be used to update the application code. No dedicated programmer is needed.
- ✓ Online debugging with single chip is supported, and no dedicated emulator is needed. The number of breakpoints is unlimited theoratically.

➢ **SRAM**
- ✓ 128 bytes internal direct access RAM (DATA, use keyword *data* to declare in C language program)

- ✓ 128 bytes internal indirect access RAM (IDATA, use keyword *idata* to declare in C language program)
- ✓ 1024 bytes internal extended RAM (internal XDATA, use keyword *xdata* to declare in C language program)

➢ **Clock**
- ✓ Internal high precise RC clock(IRC for short, ranges from 4MHz to 36MHz), adjustable while ISP and can be divided to lower frequency by user software, 100KHz for instance.
  - ✓ Error:±0.3% (at the temperature 25℃)
  - ✓ -1.35%～+1.30% temperature drift (at the temperature range of -40℃ to +85℃)
  - ✓ -0.76%～+0.98% temperature drift (at the temperature range of -20℃ to 65℃)
- ✓ Internal 32KHz low speed IRC with large error
- ✓ External 4MHz~33MHz oscillator or external clock

The three clock sources above can be selected freely by user code.

➢ **Reset**
- ✓ Hardware reset
  - ✓ Power-on reset. (**Effective when the chip does not enable the low voltage reset function**)
  - ✓ Reset by reset pin. The default function of P5.4 is the I/O port. P5.4 pin can be set as the reset pin while ISP download. (**Note: When the P5.4 pin is set as the reset pin, the reset level is low**.)
  - ✓ Watch dog timer reset
  - ✓ Low voltage detection reset. 4 low voltage detection levels are provided, 2.0V, 2.4V, 2.7V, 3.0V.
- ✓ Software reset
  - ✓ Writing the reset trigger register using software

➢ **Interrupts**
- ✓ 17 interrupt sources: INT0(Supports rising edge and falling edge interrupt), INT1(Supports rising edge and falling edge interrupt), INT2(Supports falling edge interrupt only), INT3(Supports falling edge interrupt only), INT4(Supports falling edge interrupt only), timer 0, timer 1, timer 2, UART 1, UART 2, ADC, LVD, SPI, I^2C, comparator, PWMA, PWMB
- ✓ 4 interrupt priority levels
- ✓ Interrupts that can wake up the CPU in clock stop mode: INT0(P3.2), INT1(P3.3), INT2(P3.6), INT3(P3.7), INT4(P3.0), T0(P3.4), T1(P3.5), T2(P1.2), RXD(P3.0/P3.6/P1.6), RXD2(P1.0), I2C_SDA(P1.4/P3.3), Comparator interrupt, LVD interrupt, Power-down wake-up timer.

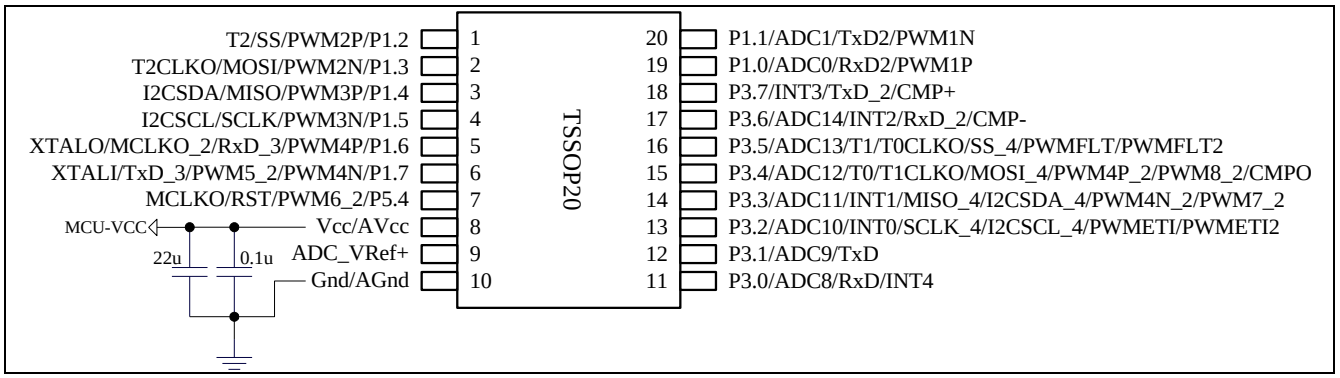
➢ **Digital peripherals**
- ✓ 3 16-bit timers: timer0, timer1, timer2, where the mode 3 of timer 0 has the Non-Maskable Interrupt (NMI in short) function. Mode 0 of timer 0 and timer 1 is 16-bit Auto-reload mode.
- ✓ 2 high speed UARTs: UART1, UART2, whose maximum baudrate clock may be FOSC/4
- ✓ 8 channels/2 groups of enhanced PWMs, which can realize control signals with dead time, and support external fault detection function. In addition, it also supports 16-bit timers, 8 external interrupts, 8 channels of external capture and pulse width measurement functions.
- ✓ SPI: Master mode, slave mode or master/slave automatic switch mode are supported.
- ✓ I^2C: Master mode or slave mode are supported.

➢ **Analog peripherals**
- ✓ 9 channels (channel 0 to channel 1, channel 8 to channel 14) ultra high speed ADC which supports 10-bit precision. The maximum speed can be 500K(Half a million ADC conversions per second)
- ✓ Channel 15 of ADC is used to test the internal reference voltage. (The default internal reference voltage is 1.19V when the chip is shipped)
- ✓ A set of comparator (the CMP+ port and all ADC input ports can be selected as the positive terminal of the comparator, so the comparator can be used as a multi-channel comparator for time division multiplexing)
- ✓ DAC: 8 channels advanced PWMs timers can be used as 8 channels DAC

➢ **GPIO**
- ✓ Up to 17 GPIOs: P1.0~P1.7, P3.0~P3.7, P5.4
- ✓ 4 modes for all GPIOs: quasi_bidirectional mode, push-pull outputmode, open drain mode, high-impedance input mode
- ✓ Except for P3.0 and P3.1, all other I/O ports are in a high-impedance state after power-on. User must configure the I/O ports mode before using them. In addition, the internal 4K pull-up resistor of every I/O can be enabled independently.

➢ **Package**
- ✓ TSSOP20 <6.5mm*6.5mm>, QFN20 <3mm*3mm>

2.1.2 Pinouts



Note:
1. ADC's external reference power supply pin ADC_VRef+ must not be floating. It must be connected to an external reference power supply or directly connected to Vcc.
2. If USB download is not required, P3.0/P3.1/P3.2 cannot be at low level at the same time when the chip is reset.

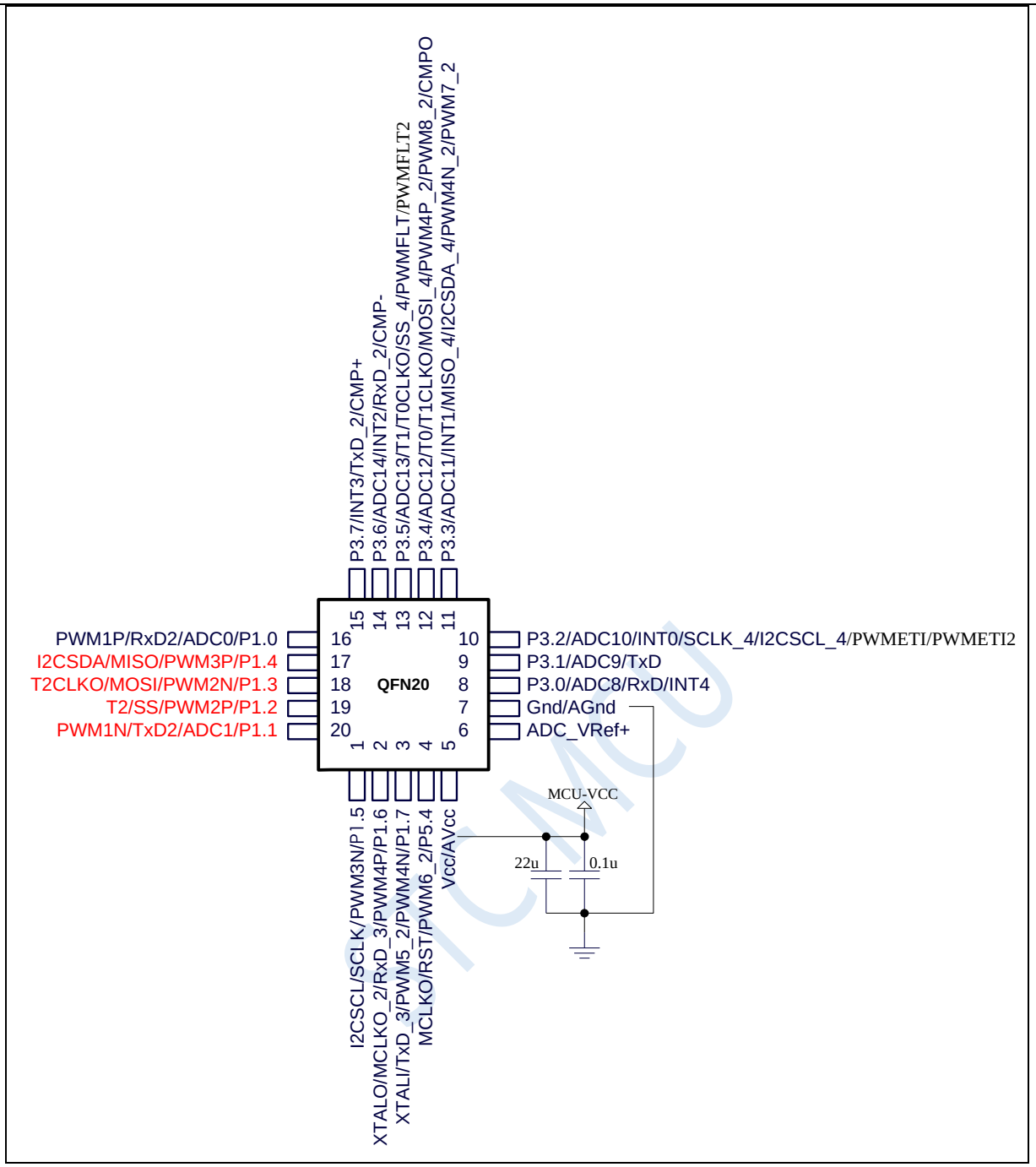
universal USB to UART tool

ISP download steps:

1. **Connect the universal USB to UART tool to the target chip according to the connection method shown in the figure above.**
2. **Press the power button to confirm that the target chip is in a power-off state (the power-on LED is off).**
   Note: When the tool is powered on for the first time, there is no external power supply, so if it is the first time to use this tool, you can skip this step.
3. **Click the "Download/Program" button in the STC-ISP download software.**
4. **Press the power button again to power on the target chip (the power-on LED is on).**
5. **Start ISP download.**
   Note: It has been found that when using the USB cable for ISP download, if the USB cable is too thin and the voltage drop on the USB cable is too large, this will result in insufficient power supply during the ISP download. Therefore, please be sure to use the booster USB cable for ISP download.

Note:

1. **Except for P3.0 and P3.1, all other I/O ports are in high-impedance input state after power-on. User must set the I/O port mode firstly when using I/O.**
2. **All I/O ports can be set to quasi-bidirectional port mode, push-pull output mode, open-drain output mode or high-impedance input mode. In addition, each I/O can enable the internal 4K pull-up resistor independently.**
3. **When P5.4 is enabled as the reset pin, the reset level is low.**


P3.7/INT3/TxD_2/CMP+
P3.6/ADC14/INT2/RxD_2/CMP-
P3.5/ADC13/T1/T0CLKO/SS_4/PWMFLT/PWMFLT2
P3.4/ADC12/T0/T1CLKO/MOSI_4/PWM4P_2/PWM8_2/CMPO
P3.3/ADC11/INT1/MISO_4/I2CSDA_4/PWM4N_2/PWM7_2
15
14
13
12
11
PWM1P/RxD2/ADC0/P1.0
16
I2CSDA/MISO/PWM3P/P1.4
17
T2CLKO/MOSI/PWM2N/P1.3
18
T2/SS/PWM2P/P1.2
19
PWM1N/TxD2/ADC1/P1.1
20
QFN20
10
P3.2/ADC10/INT0/SCLK_4/I2CSCL_4/PWMETI/PWMETI2
9
P3.1/ADC9/TxD
8
P3.0/ADC8/RxD/INT4
7
Gnd/AGnd
6
ADC_VRef+
1
2
3
4
5
I2CSCL/SCLK/PWM3N/P1.5
XTALO/MCLKO_2/RxD_3/PWM4P/P1.6
XTALI/TxD_3/PWM5_2/PWM4N/P1.7
MCLKO/RST/PWM6_2/P5.4
Vcc/AVcc
MCU-VCC
22u
0.1u

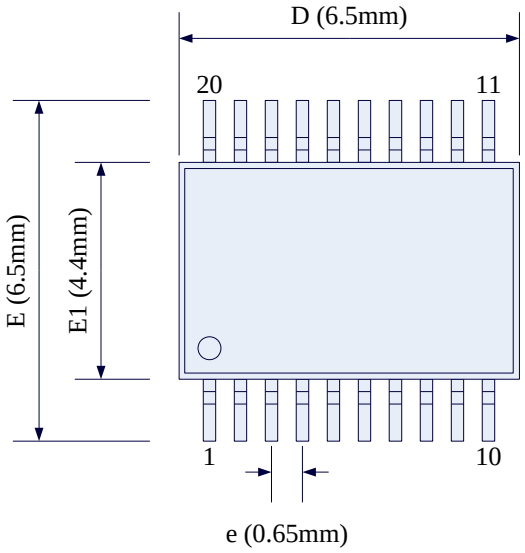
2.1.3 Pin descriptions

Pin number		name	type	description
TSSOP20	QFN20			
1	19	P1.2	I/O	Standard IO port
		SS	I/O	Slave selection of SPI
		T2	I	Timer2 external input
		PWM2P	I/O	Capture of external signal/Positive of PWMB pulse output
2	18	P1.3	I/O	Standard IO port
		MOSI	I/O	Master Output/Slave Input of SPI
		T2CLKO	O	Clock out of timer 2
		PWM2N	I/O	Capture of external signal/Negative of PWMB pulse output
3	17	P1.4	I/O	Standard IO port
		MISO	I/O	Master Iutput/Slave Onput of SPI
		SDA	I/O	Serial data line of I2C
		PWM3P	I/O	Capture of external signal/ Positive of PWM3 pulse output
4	1	P1.5	I/O	Standard IO port
		SCLK	I/O	Serial Clock of SPI
		SCL	I/O	Serial Clock line of I2C
		PWM3N	I/O	Capture of external signal/ Negative of PWM3 pulse output
5	2	P1.6	I/O	Standard IO port
		RxD_3	I	Serial input of UART1
		PWM4P	I/O	Capture of external signal/ Positive of PWM4 pulse output
		MCLKO_2	O	Master clock output
		XTALO	O	Connect to external oscillator
6	3	P1.7	I/O	Standard IO port
		TxD_3	O	Serial Transmit pin of UART 1
		PWM4N	I/O	Capture of external signal/ Negative of PWM4 pulse output
		PWM5_2	I/O	Capture of external signal/ Positive of PWM5 pulse output
		XTALI	I	Connect to external oscillator
7	4	P5.4	I/O	Standard IO port
		NRST	I	Reset pin
		MCLKO	O	Main clock output
		PWM6_2	I/O	Capture of external signal/ Positive of PWM6 pulse output
8	5	Vcc	Vcc	Power Supply
		AVcc	Vcc	Power Supply for ADC
9	6	VREF+	I	Reference voltage pin of ADC
10	7	Gnd	Gnd	Ground
		AGnd	Gnd	ADC Ground
11	8	P3.0	I/O	Standard IO port
		ADC8	I	ADC analog input 8
		RxD	I	Serial input of UART1
		INT4	I	External interrupt 4
12	9	P3.1	I/O	Standard IO port
		ADC9	I	ADC analog input 9
		TxD	O	Serial Transmit pin of UART 1

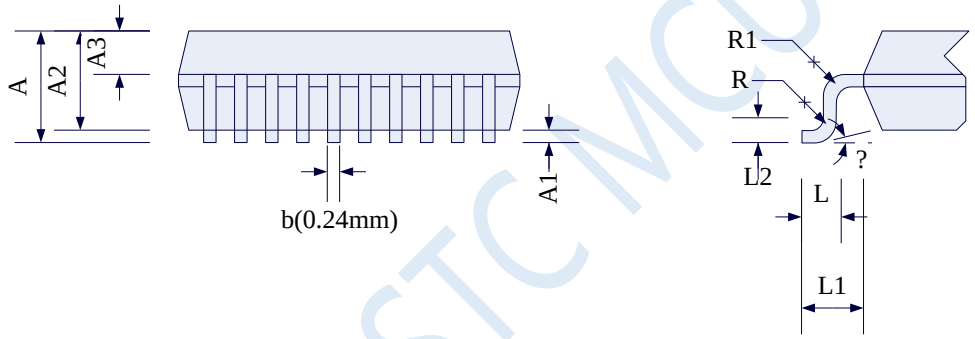
Pin number		name	type	
TSSOP20	QFN20			
13	10	P3.2	I/O	Standard IO port
		ADC10	I	ADC analog input 10
		INT0	I	External interrupt 0
		SCLK_4	I/O	Serial Clock of SPI
		SCL_4	I/O	Serial Clock line of I2C
		PWMETI	I	PWM External trigger input pin
		PWMETI2	I	PWM External trigger input pin 2
14	11	P3.3	I/O	Standard IO port
		ADC11	I	ADC analog input 11
		INT1	I	External interrupt 1
		MISO_4	I/O	Master Iutput/Slave Onput of SPI
		SDA_4	I/O	Serial data line of I2C
		PWM4N_4	I/O	Capture of external signal/ Negative of PWM4 pulse output
		PWM7_2	I/O	Capture of external signal/ Positive of PWM7 pulse output
15	12	P3.4	I/O	Standard IO port
		ADC12	I	ADC analog input 12
		T0	I	Timer0 external input
		T1CLKO	O	Clock out of timer 1
		MOSI_4	I/O	Master Output/Slave Input of SPI
		PWM4P_4	I/O	Capture of external signal/ Positive of PWM4 pulse output
		PWM8_2	I/O	Capture of external signal/ Positive of PWM8 pulse output
		CMPO	O	Comparator output
16	13	P3.5	I/O	Standard IO port
		ADC13	I	ADC analog input 13
		T1	I	Timer1 external input
		T0CLKO	O	Clock out of timer 0
		SS_4	I/O	Slave selection of SPI
		PWMFLT	I	PWMA external anomaly detection pin
		PWMFLT2	I	PWMB external anomaly detection pin
17	14	P3.6	I/O	Standard IO port
		ADC14	I	ADC analog input 14
		INT2	I	External interrupt 2
		RxD_2	I	Serial input of UART1
		CMP-	I	Comparator negative input
18	15	P3.7	I/O	Standard IO port
		INT3	I	External interrupt 3
		TxD_2	O	Serial Transmit pin of UART 1
		CMP+	I	Comparator positive input
19	16	P1.0	I/O	Standard IO port
		ADC0	I	ADC analog input 0
		RxD2	I	Serial input of UART2
		PWM1P	I/O	Capture of external signal/ Positive of PWMA pulse output
20	20	P1.1	I/O	Standard IO port
		ADC1	I	ADC analog input 1
		TxD2	O	Serial Transmit pin of UART 2
		PWM1N	I/O	Capture of external signal/ Negative of PWMA pulse output

3 Package Dimensions

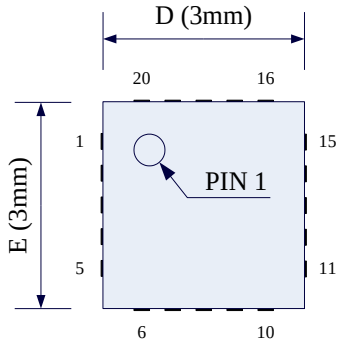
3.1 TSSOP20 Package mechanical data

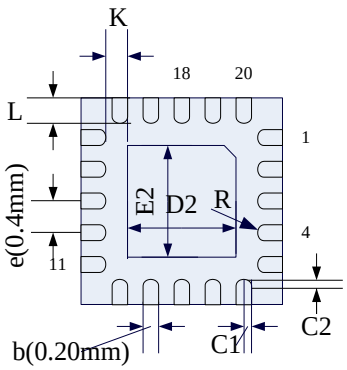


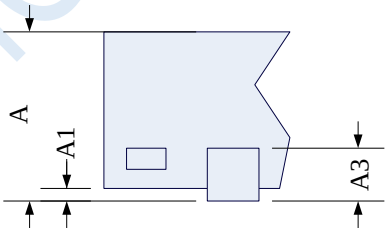
General size			
			mm
SYMBOL	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	0.24	0.28
D	6.40	6.50	6.60
E	6.20	6.50	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.09	-	-
R2	0.09	-	-



3.2 QFN20 Package mechanical data（3mm*3mm）







General size			
			mm
SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3	-	0.20REF	-
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	1.40	1.50	1.60
e	0.30	0.40	0.50
L	0.35	0.40	0.45
K	0.35REF		
R	0.085	-	-
C1	-	0.07	-
C2	-	0.07	-

The back metal sheet (substrate) of STC's existing DFN8 packaged chip is not grounded inside the chip. It can be grounded or ungrounded on the user's PCB board, which will not affect the performance of the chip.

3.3 Naming rules of STC8 family