

WINSTAR Display

OLED SPECIFICATION

Model No:

WEX013232ALPP3N00000

OLED Specification

Contents

www.winstar.com.tw

Module Classification Information

General Description



WINSTAR Display
華凌光電股份有限公司

Absolute Maximum Ratings

Block Diagram

Counter Drawing

Interface Pin Function

Optics & Electrical Characteristics

Reliability

Inspection specification

Technology - Innovation - Value

Eco Friendly - Revolution

WIN YOUR LIFE, STAR YOUR EYES

SPECIFICATION **Ver:A**

CUSTOMER :
MODULE NO. : WEX013232ALPP3N00000

APPROVED BY: (FOR CUSTOMER USE ONLY)	PCB VERSION:	DATA:
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SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
ISSUED DATE:			

MODLE NO :

RECORDS OF REVISION

DOC. FIRST ISSUE

VERSION

DATE

REVISED
PAGE
NO.

SUMMARY

0

2012.07.06

A

2012.10.26

16

First issue

Modify Brightness

2. General Description

Item	Dimension	Unit
Number of Characters	132 Dots x 32 Dots	-
Module dimension	84.0 × 44.0 × 9.7 (Max) (mm)	mm
Active Area	60.0 × 18.0 (mm)	mm
Pixel Pitch	0.39 × 0.45 (mm)	mm
Pixel Size	0.42 × 0.48 (mm)	mm
Display Mode	Passive Matrix	
Display Color	Monochrome (Yellow)	
Drive Duty	1/32 Duty	

3. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	VDD	-0.3	3.5	V	1,2
Supply Voltage for Display	VCC	8	16	V	1,2
Operating Temperature	TOP	-40	80	°C	—
Storage Temperature	TSTG	-40	80	°C	—

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

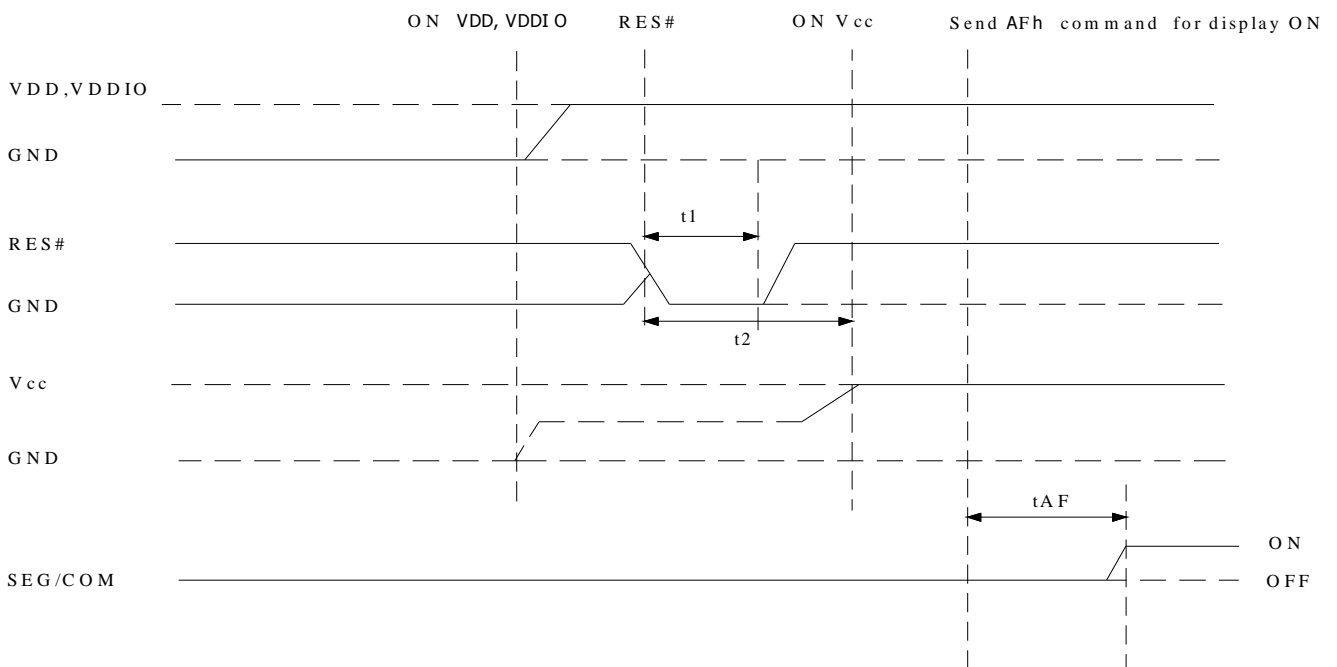
4. Block Diagram

4.1. POWER ON/OFF SEQUENCE & APPLICATION CIRCUIT

3.1.1 POWER ON/OFF SEQUENCE

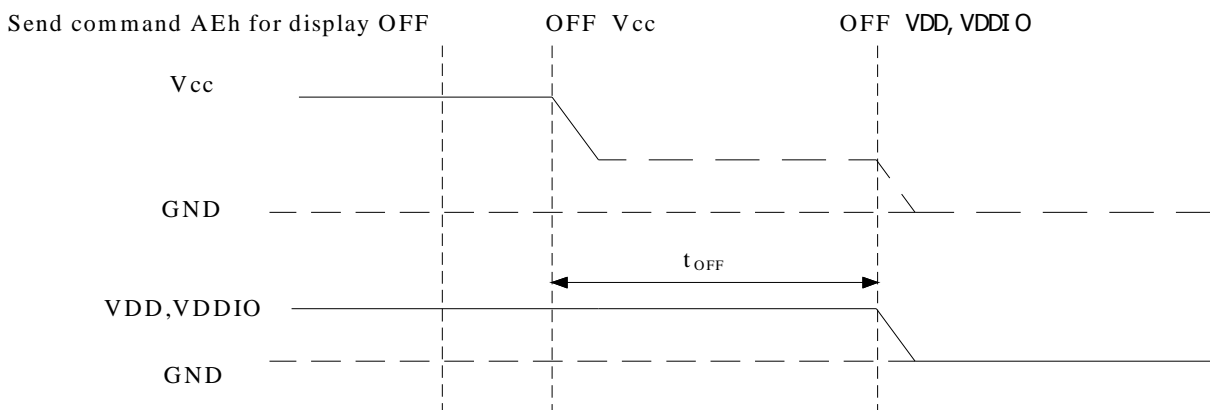
Power ON sequence

1. Power ON VDD ,VDDIO
2. After VDD ,VDDIO become stable , set RES# pin LOW (logic low) for at least 3us(t1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low),wait for at least 3us(t2). Then Power ON Vcc. (1)
4. After Vcc. become stable , send command AFh for display ON. DEG/COM will be ON after 100ms(tAF).



Power OFF sequence

1. Send command AEh for display OFF.
2. Power OFF Vcc.(1),(2)
3. Wait for t_{OFF} . Power OFF VDD ,VDDIO. (where Minimum $t_{OFF}=80ms$,Typical $t_{OFF}=100ms$)

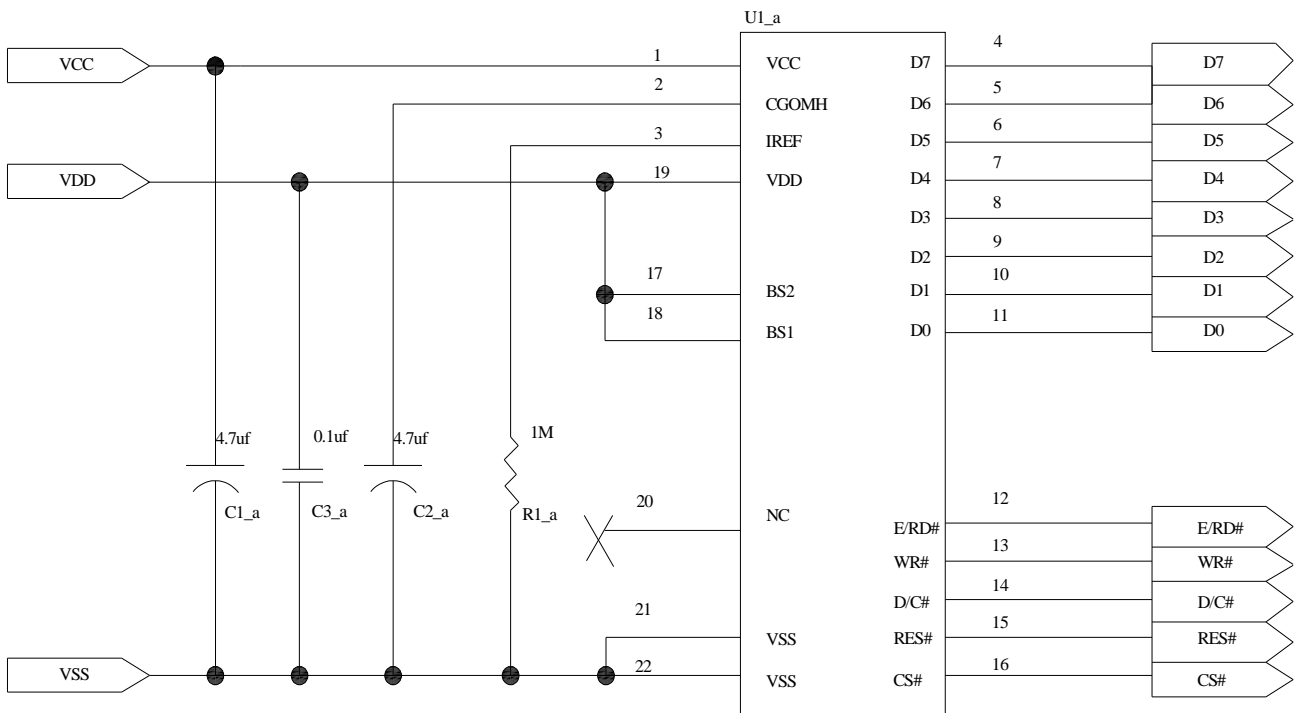


Note:

- (1) Since an ESD protection circuit is connected between VDD ,VDDIO and Vcc, Vcc

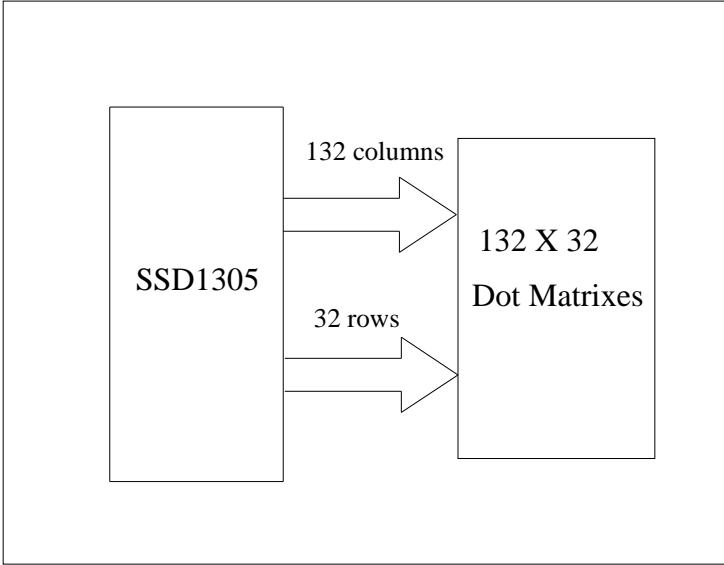
becomes lower than VDD and VDD , VDDIO is ON and Vcc is OFF as shown in the dotted line of Vcc in above figures.
 (2) Vcc should be disabled when it is OFF.

4.2 APPLICATION CIRCUIT

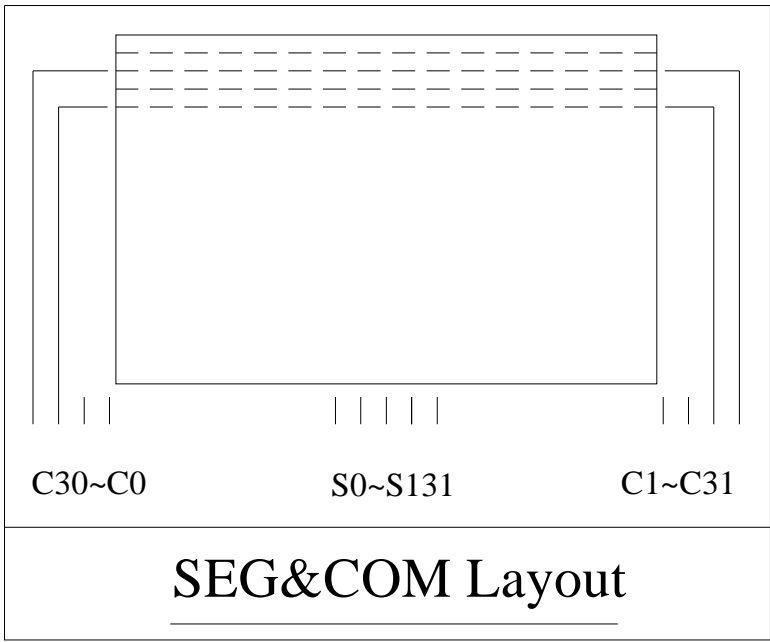


4.3 INTERFACE

4.3.1 FUNCTION BLOCK DIAGRAM



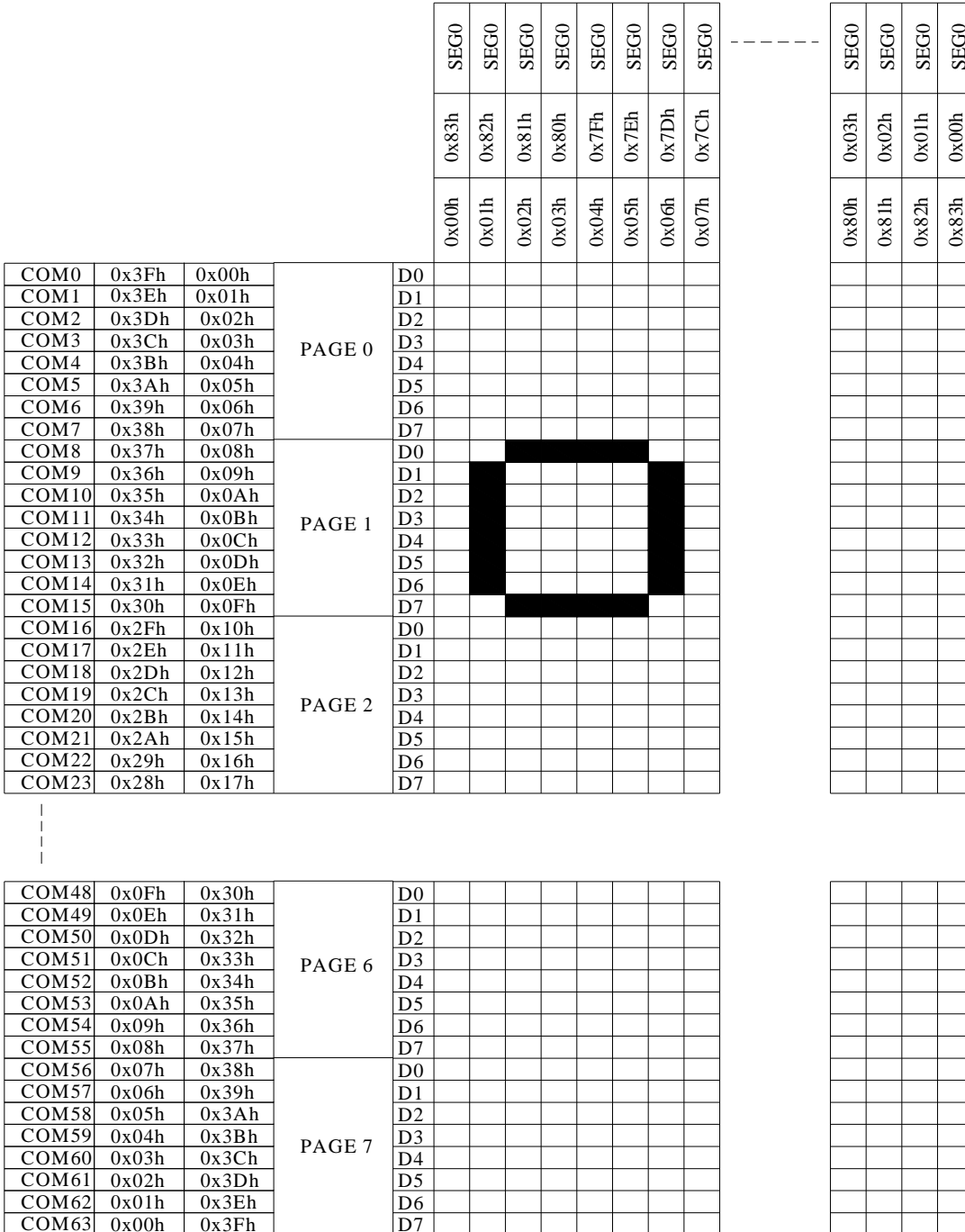
4.4 PANEL LAYOUT DIAGRAM



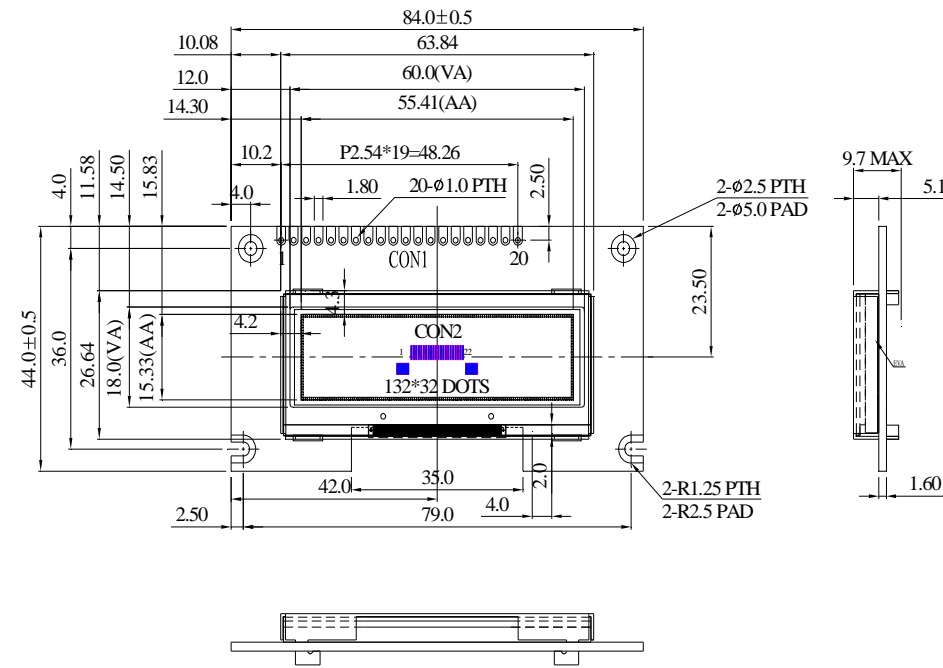
4.5 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132x64=8448bits

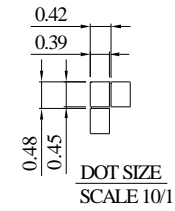
For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.



5. Contour Drawing



CON2		CON1	
PIN NO.	SYMBOL	PIN NO.	SYMBOL
1	VCC	1	VSS
2	VCOMH	2	VDD
3	IREF	3	NC
4	D7	4	A0
5	D6	5	/CSB
6	D5	6	NC
7	D4	7	NC
8	D3	8	E
9	D2	9	R/W
10	D1	10	DB0
11	D0	11	DB1
12	E/RD#	12	DB2
13	R/W#	13	DB3
14	D/C#	14	DB4
15	RES#	15	DB5
16	CS#	16	DB6
17	BS2	17	DB7
18	BS1	18	/RES
19	VDD	19	DISP
20	NC	20	NC
21	VSS		
22	VSS		



The non-specified tolerance of dimension is ± 0.3 mm.

6. Interface Pin Function

No.	Symbol	Function			
1	VCC	Power supply for analog circuit.			
2	VCOMH	Com Voltage Output. A capacitor should be connected between this pin and VSS.			
3	IREF	Reference current input pin. A resistor should be connected between this pin and VSS.			
4~11	D7~D0	Data bus.			
12	E/RD#	Data read operation is initiated when it's pull low.			
13	R/W#	Data write operation is initiated when it's pull low.			
14	D/C#	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.			
15	RES#	Reset signal input. When it's low, initialization of SSD1305 is executed.			
16	CS#	Chip select input.			
17	BS2	Communicating Protocol Select These pins are MCU interface selection input. See the following table:			
18	BS1		68XX-paralle l	80XX-paralle l	Serial
		BS1	0	1	0
		BS2	1	1	0
19	VDD	Power supply for logic circuit.			
20	NC	No connection			
21	VSS	Ground.			
22	VSS	Ground.			

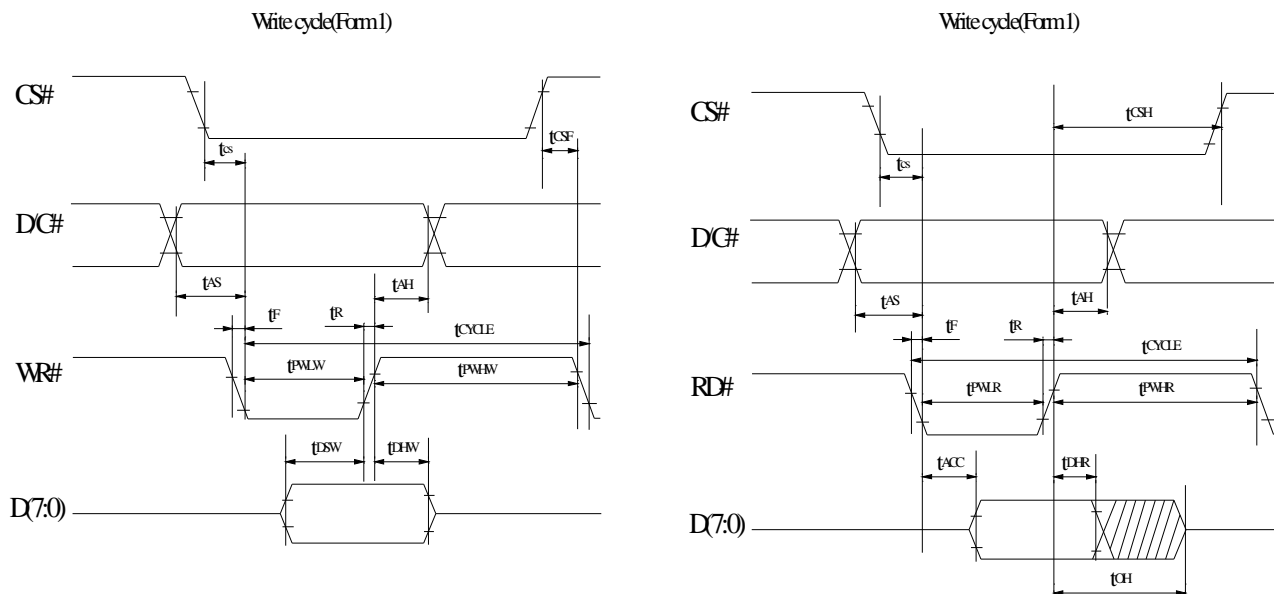
7. Optics & Electrical Characteristics

7.1 INTERFACE TIMING CHART

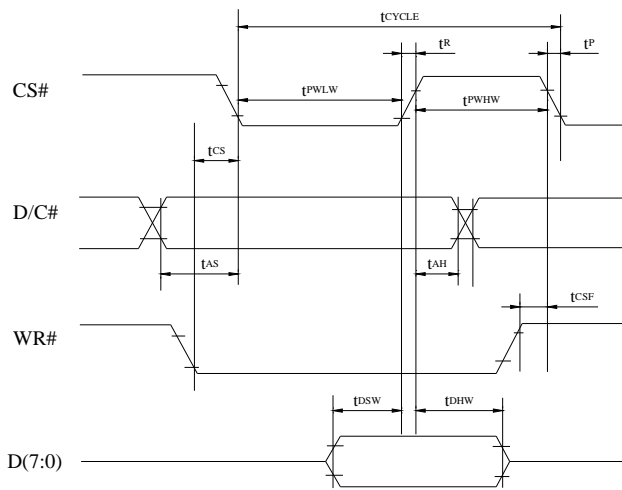
8080-Series MCU Parallel Interface Timing Characteristics
(VDD-VSS=2.4V to 3.5V, VDDIO=VDD, TA=25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t _{cycle}	Clock Cycle Time	300	-	-	ns
t _{AS}	Address Setup Time	10	-	-	ns
t _{AH}	Address Hold Time	0	-	-	ns
t _{DSW}	Write Data Setup Time	40	-	-	ns
t _{DHW}	Write Data Hold Time	7	-	-	ns
t _{DHR}	Read Data Hold Time	20	-	-	ns
t _{OH}	Output Disable Time	-	-	70	ns
t _{ACC}	Access Time	-	-	140	ns
t _{PWLR}	Read Low Time	120	-	-	ns
t _{PWLW}	Write Low Time	60	-	-	ns
t _{PWHR}	Read High Time	60	-	-	ns
t _{PWHW}	Write High Time	60	-	-	ns
t _R	Rise Time	-	-	15	ns
t _F	Fall Time	-	-	15	ns
t _{CS}	Chip select setup time	0	-	-	ns
t _{CSH}	Chip select setup hold time to read signal	0	-	-	ns
t _{CSF}	Chip select setup hold time	20	-	-	ns

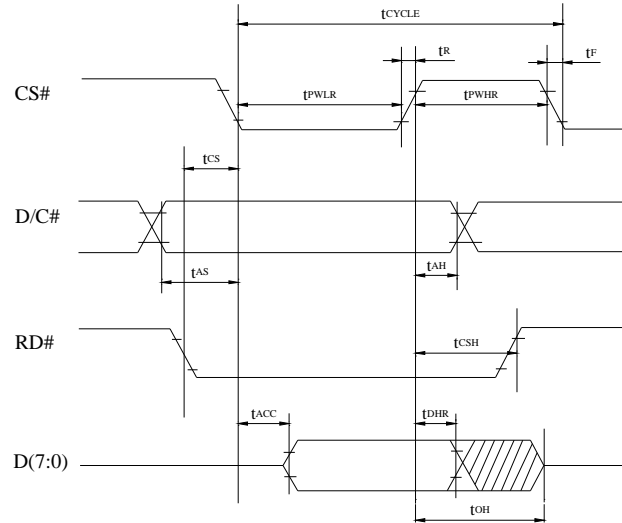
8080-series parallel interface characteristics (Form 1)



Write cycle(Form 2)



Write cycle(Form 2)



7.2 Optics Characteristics

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness	Lbr	With Polarizer (Note 3)	130	150	—	cd/m ²
C.I.E. (Yellow)	(x)	Without Polarizer	0.44	0.48	0.52	
	(y)		0.46	0.50	0.54	
Dark Room Contrast	CR		—	>2000:1	—	—
View Angle			>160	—	—	

* Optical measurement taken at VDD = 3.0V, VCC = 13V.

7.3 DC Characteristics

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Logic	VDD	—	2.8	3	3.3	V
Supply Voltage for Display	VCC	—	10	11	12	V
High Level Input	VIH	Iout = 100μA, 3.3MHz	0.8×VDD	—	VDD	V
Low Level Input	VIL	Iout = 100μA, 3.3MHz	0	—	0.2×VDD	V
High Level Output	VOH	Iout = 100μA, 3.3MHz	0.9×VDD	—	VDD	V
Low Level Output	VOL	Iout = 100μA, 3.3MHz	0	—	0.1×VDD	V
Operating Current for VDD	IDD	Note 4	—	250	400	μA
		Note 5	—	250	400	μA
Operating Current for VCC	ICC	Note 4	—	35	40	mA
		Note 5	—	45	50	mA
Sleep Mode Current for VDD	IDD, SLEEP			—	10	μA
Sleep Mode Current for VCC	ICC, SLEEP		—	—	10	μA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 4: $V_{DD} = 3.0V$, $V_{CC} = 13V$, 50% Display Area Turn on.

Note 5: $V_{DD} = 3.0V$, $V_{CC} = 13V$, 100% Display Area Turn on.

* Software configuration follows Section 4.4 Initialization.

8. Reliability

8.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation Low Temperature Operation	80°C,240hrs -40°C,240hrs	The operational functions work.
High Temperature Storage Low Temperature Storage	80°C,240hrs -40°C,240hrs	
High Temperature/Humidity Operation/ Thermal Shock	60°C,90%RH,120hrs , -40°C 80°C , 24cycles 1 hr dwell	

* The samples used for the above tests do not include polarizer.

* No moisture condensation is observed during tests.

8.2 Lifetime

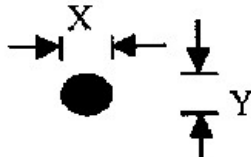
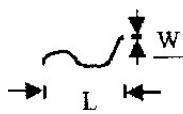
Parameter	Min	Typ	Max	Unit	Condition	Notes
Operating Life Time		50,000	—	Hrs	150 cd/m ² , 50% Checkerboard	6

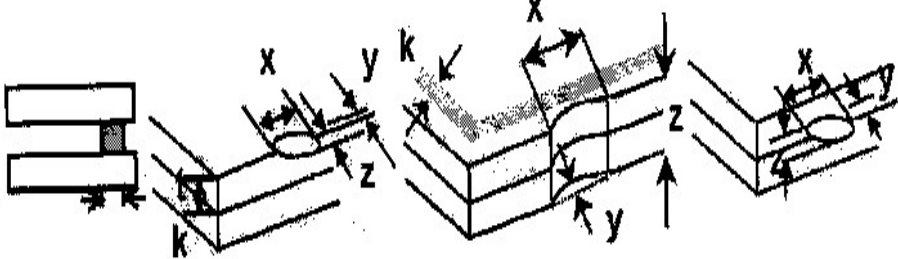
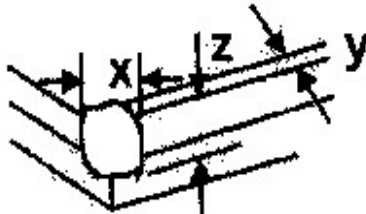
Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

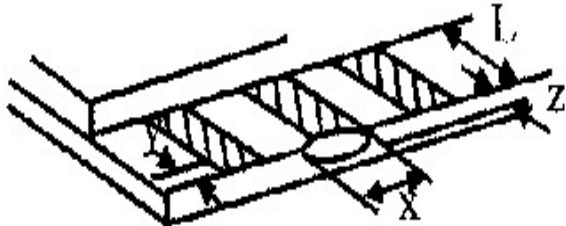
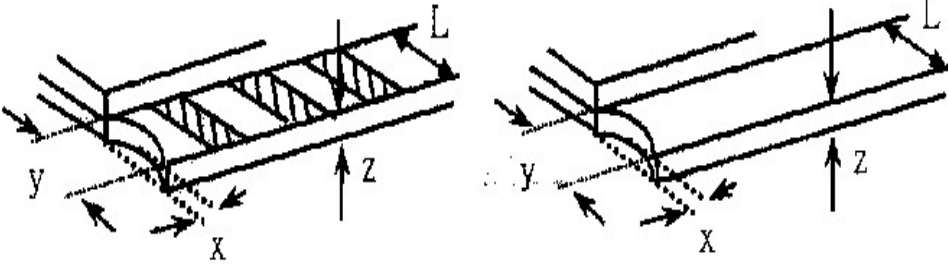
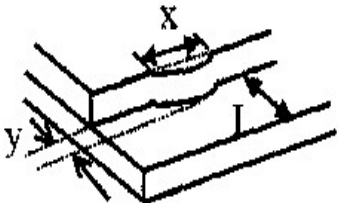
8.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

9. Inspection specification

NO	Item	Criterion	AQL												
01	Electrical Testing	1.1 Missing vertical, horizontal segment, segment contrast defect. 1.2 Missing character, dot or icon. 1.3 Display malfunction. 1.4 No function or no display. 1.5 Current consumption exceeds product specifications. 1.6 Viewing angle defect. 1.7 Mixed product types. 1.8 Contrast defect.	0.65												
02	Black or white spots (display only)	2.1 White and black spots on display $\leq 0.25\text{mm}$, no more than three white or black spots present. 2.2 Densely spaced: No more than two spots or lines within 3mm	2.5												
03	Black spots, white spots, contamination (non-display)	3.1 Round type : As following drawing $\Phi = (x + y) / 2$  <table border="1" data-bbox="742 869 1268 1146"> <thead> <tr> <th>SIZE</th> <th>Acceptable QTY</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.10$</td> <td>Accept no dense</td> </tr> <tr> <td>$0.10 < \Phi \leq 0.20$</td> <td>2</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.25$</td> <td>1</td> </tr> <tr> <td>$0.25 < \Phi$</td> <td>0</td> </tr> </tbody> </table>	SIZE	Acceptable QTY	$\Phi \leq 0.10$	Accept no dense	$0.10 < \Phi \leq 0.20$	2	$0.20 < \Phi \leq 0.25$	1	$0.25 < \Phi$	0	2.5		
		SIZE	Acceptable QTY												
$\Phi \leq 0.10$	Accept no dense														
$0.10 < \Phi \leq 0.20$	2														
$0.20 < \Phi \leq 0.25$	1														
$0.25 < \Phi$	0														
3.2 Line type : (As following drawing)  <table border="1" data-bbox="622 1191 1268 1473"> <thead> <tr> <th>Length</th> <th>Width</th> <th>Acceptable QTY</th> </tr> </thead> <tbody> <tr> <td>---</td> <td>$W \leq 0.02$</td> <td>Accept no dense</td> </tr> <tr> <td>$L \leq 3.0$</td> <td>$0.02 < W \leq 0.03$</td> <td rowspan="2">2</td> </tr> <tr> <td>$L \leq 2.5$</td> <td>$0.03 < W \leq 0.05$</td> </tr> <tr> <td>---</td> <td>$0.05 < W$</td> <td>As round type</td> </tr> </tbody> </table>	Length	Width	Acceptable QTY	---	$W \leq 0.02$	Accept no dense	$L \leq 3.0$	$0.02 < W \leq 0.03$	2	$L \leq 2.5$	$0.03 < W \leq 0.05$	---	$0.05 < W$	As round type	
Length	Width	Acceptable QTY													
---	$W \leq 0.02$	Accept no dense													
$L \leq 3.0$	$0.02 < W \leq 0.03$	2													
$L \leq 2.5$	$0.03 < W \leq 0.05$														
---	$0.05 < W$	As round type													
04	Polarizer bubbles	If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction. <table border="1" data-bbox="758 1512 1268 1825"> <thead> <tr> <th>Size Φ</th> <th>Acceptable QTY</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.20$</td> <td>Accept no dense</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.50$</td> <td>3</td> </tr> <tr> <td>$0.50 < \Phi \leq 1.00$</td> <td>2</td> </tr> <tr> <td>$1.00 < \Phi$</td> <td>0</td> </tr> <tr> <td>Total QTY</td> <td>3</td> </tr> </tbody> </table>	Size Φ	Acceptable QTY	$\Phi \leq 0.20$	Accept no dense	$0.20 < \Phi \leq 0.50$	3	$0.50 < \Phi \leq 1.00$	2	$1.00 < \Phi$	0	Total QTY	3	2.5
Size Φ	Acceptable QTY														
$\Phi \leq 0.20$	Accept no dense														
$0.20 < \Phi \leq 0.50$	3														
$0.50 < \Phi \leq 1.00$	2														
$1.00 < \Phi$	0														
Total QTY	3														


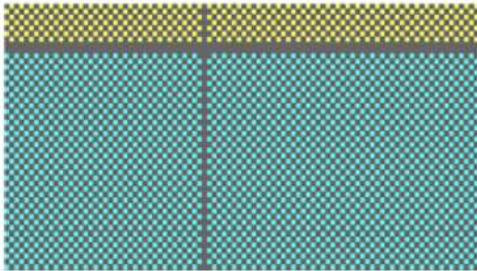
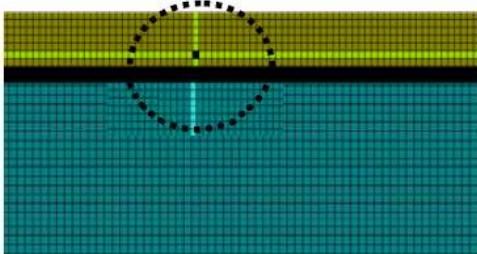
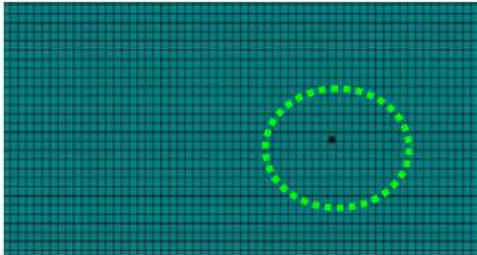
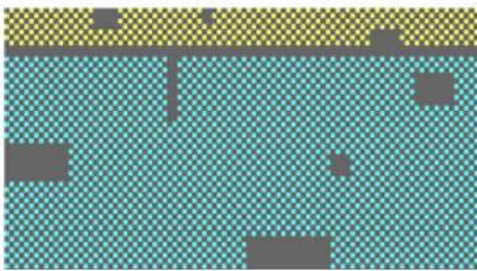
NO	Item	Criterion	AQL																		
05	Scratches	Follow NO.3 Black spots, white spots, contamination																			
06	Chipped glass	<p>Symbols Define: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: Side length L: Electrode pad length:</p> <p>6.1 General glass chip : 6.1.1 Chip on panel surface and crack between panels:</p>  <table border="1" data-bbox="422 734 1332 891"> <thead> <tr> <th>z: Chip thickness</th> <th>y: Chip width</th> <th>x: Chip length</th> </tr> </thead> <tbody> <tr> <td>$Z \leq 1/2t$</td> <td>Not over viewing area</td> <td>$x \leq 1/8a$</td> </tr> <tr> <td>$1/2t < z \leq 2t$</td> <td>Not exceed 1/3k</td> <td>$x \leq 1/8a$</td> </tr> </tbody> </table> <p>⊙ If there are 2 or more chips, x is total length of each chip.</p> <p>6.1.2 Corner crack:</p>  <table border="1" data-bbox="422 1272 1332 1429"> <thead> <tr> <th>z: Chip thickness</th> <th>y: Chip width</th> <th>x: Chip length</th> </tr> </thead> <tbody> <tr> <td>$Z \leq 1/2t$</td> <td>Not over viewing area</td> <td>$x \leq 1/8a$</td> </tr> <tr> <td>$1/2t < z \leq 2t$</td> <td>Not exceed 1/3k</td> <td>$x \leq 1/8a$</td> </tr> </tbody> </table> <p>⊙ If there are 2 or more chips, x is the total length of each chip.</p>	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$	2.5
z: Chip thickness	y: Chip width	x: Chip length																			
$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$																			
$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$																			
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$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$																			

NO	Item	Criterion	AQL																
06	Glass crack	<p>Symbols : x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: Side length L: Electrode pad length</p> <p>6.2 Protrusion over terminal : 6.2.1 Chip on electrode pad :</p>  <table border="1" data-bbox="339 595 1251 674"> <tr> <td>y: Chip width</td> <td>x: Chip length</td> <td>z: Chip thickness</td> </tr> <tr> <td>$y \leq 0.5\text{mm}$</td> <td>$x \leq 1/8a$</td> <td>$0 < z \leq t$</td> </tr> </table> <p>6.2.2 Non-conductive portion:</p>  <table border="1" data-bbox="411 1003 1251 1122"> <tr> <td>y: Chip width</td> <td>x: Chip length</td> <td>z: Chip thickness</td> </tr> <tr> <td>$y \leq L$</td> <td>$x \leq 1/8a$</td> <td>$0 < z \leq t$</td> </tr> </table> <p>⊙ If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications. ⊙ If the product will be heat sealed by the customer, the alignment mark not be damaged.</p> <p>6.2.3 Substrate protuberance and internal crack.</p>  <table border="1" data-bbox="746 1368 1257 1447"> <tr> <td>y: width</td> <td>x: length</td> </tr> <tr> <td>$y \leq 1/3L$</td> <td>$x \leq a$</td> </tr> </table>	y: Chip width	x: Chip length	z: Chip thickness	$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$	y: Chip width	x: Chip length	z: Chip thickness	$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$	y: width	x: length	$y \leq 1/3L$	$x \leq a$	2.5
y: Chip width	x: Chip length	z: Chip thickness																	
$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$																	
y: Chip width	x: Chip length	z: Chip thickness																	
$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$																	
y: width	x: length																		
$y \leq 1/3L$	$x \leq a$																		

NO	Item	Criterion	AQL
07	Cracked glass	With extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using Spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB · COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down.	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP.	2.5
		12.2 No cracks on interface pin (OLB) of TCP.	0.65
		12.3 No contamination, solder residue or solder balls on product.	2.5
		12.4 The IC on the TCP may not be damaged, circuits.	2.5
		12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever.	2.5
		12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color.	2.5
		12.7 Sealant on top of the ITO circuit has not hardened.	0.65
		12.8 Pin type must match type in specification sheet.	0.65
		12.9 Pin loose or missing pins.	
		12.10 Product packaging must the same as specified on packaging specification sheet.	0.65
		12.11 Product dimension and structure must conform to product specification sheet.	

Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	