LP38798 800-mA Ultra-Low-Noise, High-PSRR LDO

1 Features

- Wide Operating Input Voltage Range: 3 V to 20 V
- Ultra-Low Output Noise: 5 μV_{RMS} (10 Hz to 100 kHz)
- High PSRR: 90 dB at 10 kHz, 60 dB at 100 kHz
- ±1% Output Voltage Initial Accuracy (T_J = 25°C)
- Very Low Dropout: 200 mV (Typical) at 800 mA
- Stable with Ceramic or Tantalum Output Capacitors
- Excellent Line and Load Transient Response
- Current Limit and Overtemperature Protection
- Create a Custom Design Using the LP38798 With the WEBENCH® Power Designer

2 Applications

- RF Power Supplies: PLLs, VCOs, Mixers, LNAs
- Telecom Infrastructure
- Wireless Infrastructure
- Very Low-Noise Instrumentation
- Precision Power Supplies
- High-Speed, High-Precision Data Converters

3 Description

The LP38798-ADJ is a high-performance, low-noise LDO that can supply up to 800 mA output current. Designed to meet the requirements of sensitive RF/Analog circuitry, the LP38798-ADJ implements a novel linear topology on an advanced CMOS process to deliver ultra-low output noise and high PSRR at switching power supply frequencies. The LP38798SD-ADJ is stable with both ceramic and tantalum output capacitors and requires a minimum output capacitance of only 1 µF for stability.

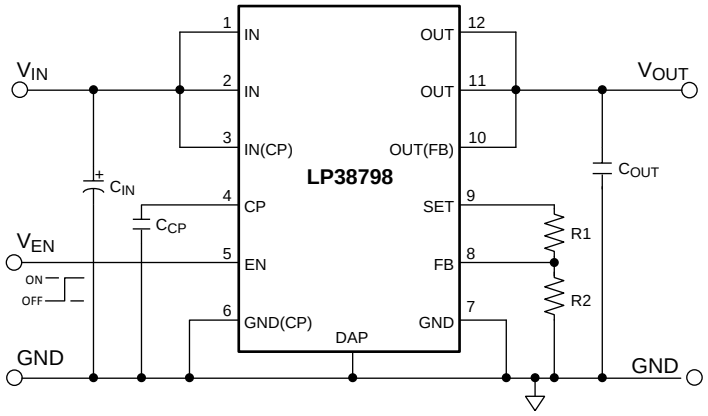
The LP38798-ADJ can operate over a wide input voltage range (3 V to 20 V) making it well suited for many post-regulation applications.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP38798	WSON (12)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision E (August 2016) to Revision F — **Page**

- Created Rev F toonly add WEBENCH links to data sheet ... 1

Changes from Revision D (June 2016) to Revision E — **Page**

- Changed title of data sheet and updated list of *Applications* ... 1
- Changed first wording of first sentence of *Description* ... 1

Changes from Revision C (June2016) to Revision D — **Page**

- Added 1.2 V row to Table 1 ... 16
- Changed "Value for R2 = 12.9 kΩ and 100 kΩ" to "R2 = 12.9 kΩ minimum to 100 kΩ maximum" ... 19
- Changed "value of 13.3 kΩ" to "value of 15 kΩ for R2" ... 19
- Changed "for R1 is" to "needed for R1 to provide an output voltage of 5 V is" ... 19

Changes from Revision B (December 2014) to Revision C — **Page**

- Changed "linear regulator" to "LDO" on page 1; add top nav icon for reference design ... 1
- Changed *Handling Ratings* table to *ESD Ratings* table; move storage temperature to *Abs Max* table ... 4
- Added links for *Community Resources* ... 21

Changes from Revision A (May 2013) to Revision B — **Page**

- Added *Device Information* and *Handling Rating* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; updated *Thermal Information*; moved some curves to *Application Curves* section ... 1

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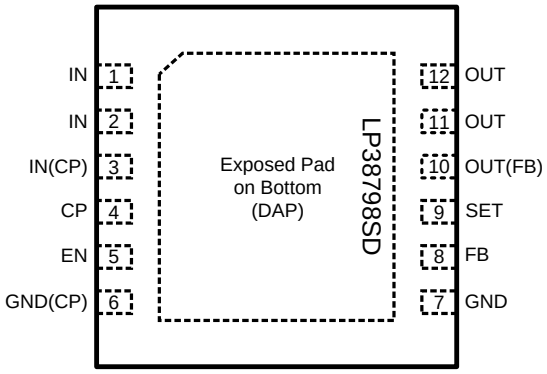
5 Pin Configuration and Functions

DNT Package
12-Pin WSON
Top View



Connect WSON DAP to GND at Pins 6 and 7.

Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1, 2	IN	I	Device unregulated input voltage pins. Connect pins together at the package.
3	IN(CP)	I	Charge pump input voltage pin. Connect directly to pins 1 and 2 at the package.
4	CP	O	Charge pump output. See *Charge Pump* section in *Application and Implementation* for more information.
5	EN	I	Enable pin. This pin has an internal pullup to turn the LDO output on by default. A logic low level turns the LDO output Off, and reduce the operating current of the device. See *Enable Input Operation* section in *Application and Implementation* for more information.
6	GND(CP)	—	Device charge pump ground pin.
7	GND	—	Device analog ground pin.
8	FB	i	Feedback pin for programming the output voltage.
9	SET	I/O	Reference voltage output, and noise filter input. A feedback resistor divider network from this pin to FB and GND will set the output voltage of the device.
10	OUT(FB)	I	OUT buffer feedback input pin. Connect directly to pins 11 and 12 at the package.
11, 12	OUT	O	Device regulated output voltage pins. Connect pins together at the package.
Exposed Pad	DAP	—	The exposed die attach pad on the bottom of the package must be connected to a copper thermal pad on the PCB at ground potential. Connect to ground potential or leave floating. Do not connect to any potential other than the same ground potential seen at device pins 6 (GND(CP)) and 7 (GND). See *Thermal Considerations* section in *Layout* for more information.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN}, $V_{IN(CP)}$	–0.3	22	V
V_{OUT}, $V_{OUT(FB)}$	–0.3	V_{IN} + 0.3	V
V_{SET}	–0.3	V_{IN} + 0.3	V
V_{FB}	–0.3	V_{IN} + 0.3	V
V_{EN}	–0.3	6	V
Power dissipation(2)		Internally Limited	
I_{OUT} (Survival)		Internally Limited	
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The value of $R_{\theta JA}$ for the WSON package is dependent on PCB copper area, copper thickness, the number of copper layers in the PCB, and the number of thermal vias under the exposed thermal pad (DAP). Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator may go into thermal shutdown. See *Thermal Considerations*.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Input voltage, V_{IN}	3	20	V
Output voltage, V_{OUT}	1.2	(V_{IN} – V_{DO})	V
Enable voltage, V_{EN}	0	5	V
Junction temperature, T_J	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LP38798 DNT (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

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6.5 Electrical Characteristics

Unless otherwise stated the following conditions apply: V_{IN} = 5.5 V, V_{SET} = 5 V, C_{CP} = 10 nF X7R, C_{IN} = 10 µF, 50-mΩ tantalum, C_{OUT} = 10 µF X7R MLCC, I_{OUT} = 10 mA, and T_J = –40°C to +125°C.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{FB}	Feedback voltage	V_{IN} = 5.5 V T_J = 25°C	1.188	1.2	1.212	V
		5.5 V ≤ V_{IN} ≤ 20 V	1.176	1.2	1.224	
V_{OS}	V_{OUT} – V_{SET}		0	3.5	16	mV
I_{FB}	Feedback pin current	V_{FB} = 1.2 V		0	1	µA
I_{SET}	SET pin internal current sink	V_{IN} = 3 V, V_{SET} = 2.5 V		46		µA
		V_{IN} = 5.5 V, V_{SET} = 5 V	25.2	52	67.8	
		V_{IN} = 12.5 V, V_{SET} = 12 V		71		
ΔV_{OUT} / ΔV_{IN}	Line regulation(3)	5.5 V ≤ V_{IN} ≤ 20 V I_{OUT} = 10 mA		0.005		%/V
ΔV_{OUT} / ΔI_{OUT}	Load regulation(4)	V_{IN} = 5.5 V 10 mA ≤ I_{OUT} ≤ 800 mA		–0.2		%/A
V_{DO}	Dropout voltage(5)	I_{OUT} = 800 mA		200	420	mV
UVLO	Undervoltage lock-out	V_{IN} Rising until output is On	2.47	2.65	2.83	V
ΔUVLO	UVLO hysteresis	V_{IN} Falling from > UVLO threshold until output is Off		180		mV
I_{GND}	Ground pin current(6)	I_{OUT} = 800 mA		1.4	2.25	mA
		V_{IN} = 20 V, I_{OUT} = 800 mA		1.6	2.51	
I_Q	Ground pin current, quiescent(6)	I_{OUT} = 0 mA		1.4	2.1	mA
		V_{IN} = 20 V, I_{OUT} = 0 mA		1.5	2.2	
I_{SD}	Ground pin current, shutdown(6)	V_{EN} = 0 V		9	20	µA
		V_{IN} = 20 V, V_{EN} = 0 V		12	40	
I_{SC}	Short-circuit current	R_{LOAD} = 0 Ω	850	1200	1600	mA
ΔV_{CP}	V_{CP} – V_{IN}			2.8		V
		V_{IN} = 20 V		2.3		
t_{START}	Start-up time	From V_{EN} > $V_{EN(ON)}$ to V_{OUT} ≥ 98% of $V_{OUT(NOM)}$		155	300	µs
PSRR	Power Supply Rejection Ratio	V_{OUT} = 1.2 V, f = 10 kHz		110		dB
		V_{OUT} = 5 V, f = 10 kHz		90		
		V_{OUT} = 1.2 V, f = 100 kHz		90		
		V_{OUT} = 5 V, f = 100 kHz		60		
		V_{OUT} = 1.2 V, f = 1 MHz		70		
		V_{OUT} = 5 V, f = 1 MHz		60		

(1) Minimum and maximum limits are ensured through test, design, or statistical correlation over the operating junction temperature (T_J) range of –40°C to 125°C, unless otherwise stated.
(2) Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.
(3) Line Regulation: % change in $V_{OUT(NOM)}$ for every 1V change in V_{IN}= ((ΔV_{OUT} / $V_{OUT(NOM)}$) / ΔV_{IN}) × 100%
(4) Load Regulation: % change in $V_{OUT(NOM)}$ for every 1A change in I_{OUT} = ((ΔV_{OUT} / $V_{OUT(NOM)}$) / ΔI_{OUT}) × 100%
(5) Dropout voltage (V_{DO}) is defined as the differential voltage measured between V_{OUT} and V_{IN} when V_{IN}, falling from V_{IN} = V_{OUT} + 1 V, causes V_{OUT} to drop 2% below the value measured with V_{IN} = V_{OUT} + 1 V. Dropout voltage specification does not apply when the programmed output voltage is below the Minimum Operating Input Voltage.
(6) Ground pin current is the sum of the current in both GND pins (pin 4 and pin 5) only, and does not include current from the SET pin.

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Electrical Characteristics (continued)

Unless otherwise stated the following conditions apply: V_{IN} = 5.5 V, V_{SET} = 5 V, C_{CP} = 10 nF X7R, C_{IN} = 10 µF, 50-mΩ tantalum, C_{OUT} = 10 µF X7R MLCC, I_{OUT} = 10 mA, and T_J = –40°C to +125°C.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
e_N	Output noise voltage (RMS)	V_{IN} = 3 V, V_{OUT} = 1.2 V C_{OUT} = 1 µF X7R BW = 10 Hz to 100 kHz		4.96		$\mu V_{(RMS)}$
		V_{IN} = 3 V, V_{OUT} = 1.2 V BW = 10 Hz to 100 kHz		5.21		
		V_{IN} = 3 V, V_{OUT} = 1.2 V BW = 10 Hz to 10 MHz		11.53		
		V_{IN} = 6 V, V_{OUT} = 5 V C_{OUT} = 1 µF X7R BW = 10 Hz to 100 kHz		5.38		
		V_{IN} = 6 V, V_{OUT} = 5 V BW = 10 Hz to 100 kHz		5.43		
		V_{IN} = 6 V, V_{OUT} = 5 V BW = 10 Hz to 10 MHz		11.58		
ENABLE INPUT						
$V_{EN(ON)}$	Enable ON threshold voltage	V_{EN} rising from 500 mV until Output is ON	1.14	1.24	1.34	V
ΔV_{EN}	Enable threshold voltage hysteresis	V_{EN} falling from $V_{EN(ON)}$		110		mV
$I_{EN(IL)}$	EN pin pullup current	V_{EN} = 500 mV		2	3	µA
$I_{EN(IH)}$	EN pin pullup current	V_{EN} = 2 V		2	3	
$V_{EN(CLAMP)}$	Enable pin clamp voltage	EN pin = Open		5		V
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown	Junction temperature (T_J) rising		170		°C
ΔT_{SD}	Thermal shutdown hysteresis	Junction temperature (T_J) falling from T_{SD}		12		

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6.6 Typical Characteristics

Unless otherwise specified: V_{IN} = 5.5 V, V_{OUT} = 5 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16 V X7R, and T_J = 25°C.

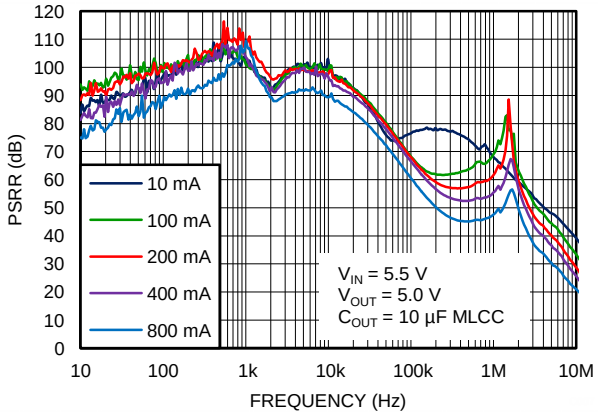

Figure 1. PSRR

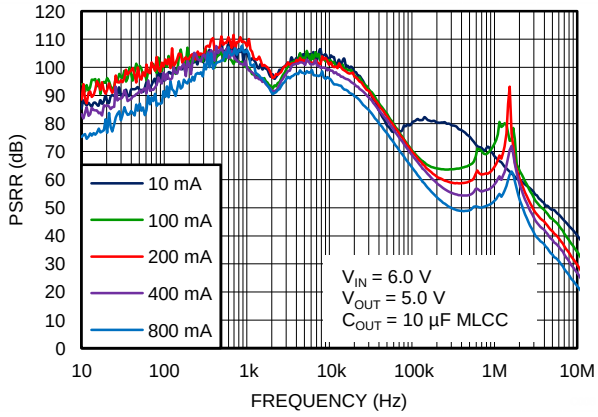

Figure 2. PSRR

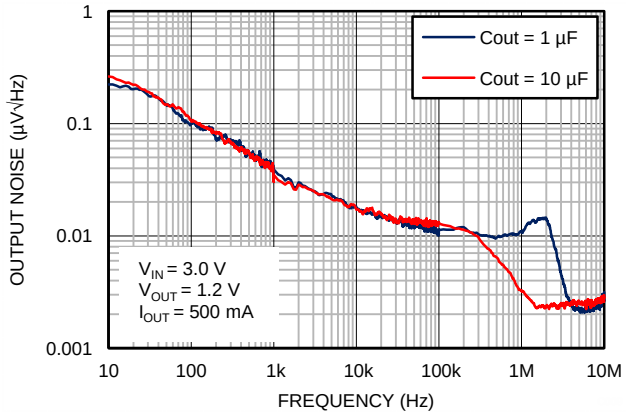

Figure 3. Noise Density

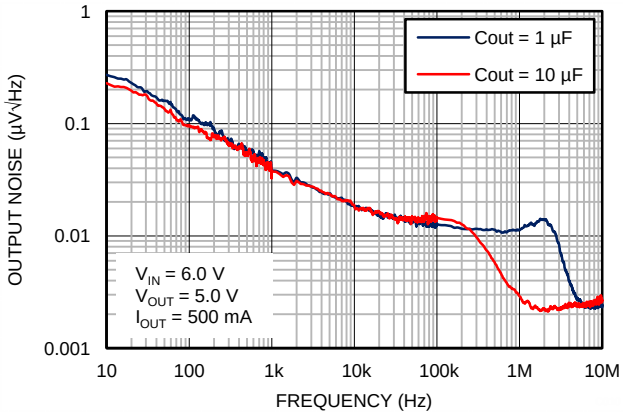

Figure 4. Noise Density

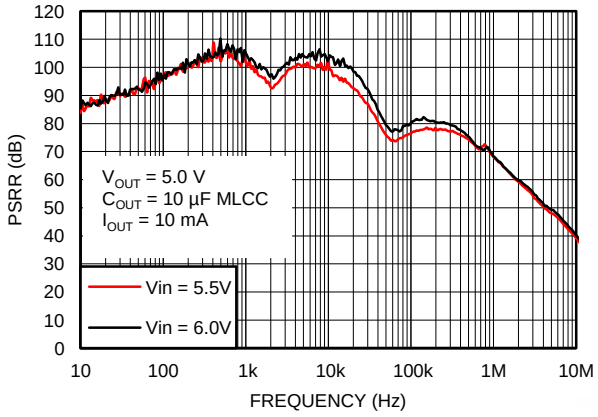

Figure 5. PSRR

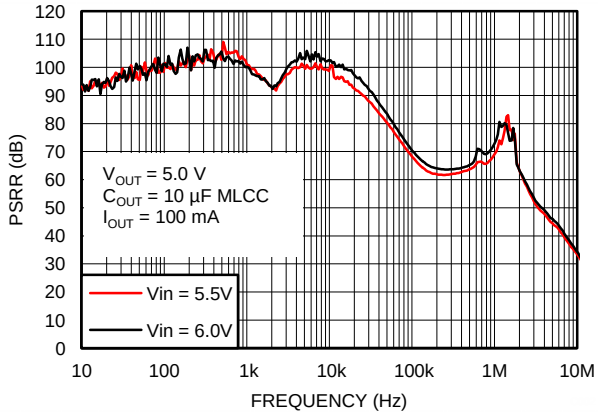

Figure 6. PSRR

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Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5.5 V, V_{OUT} = 5 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16 V X7R, and T_J = 25°C.

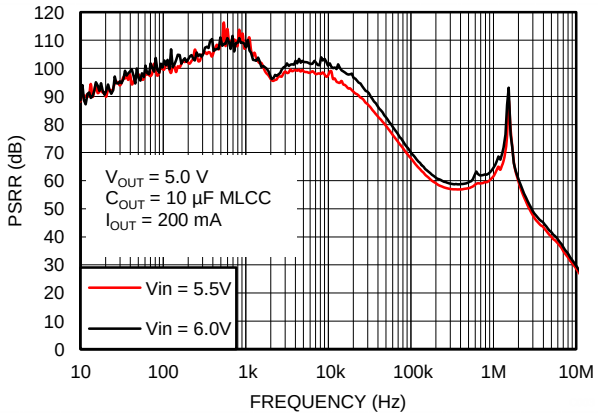

Figure 7. PSRR

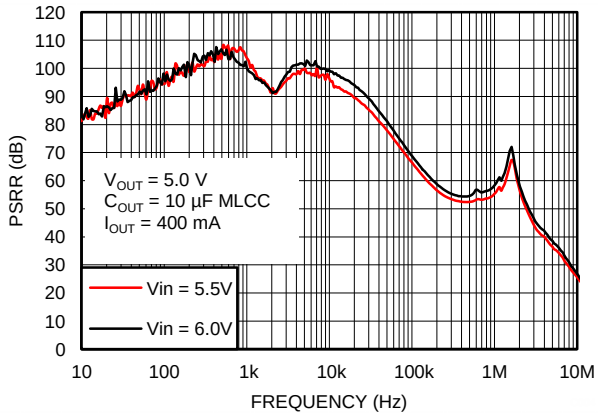

Figure 8. PSRR

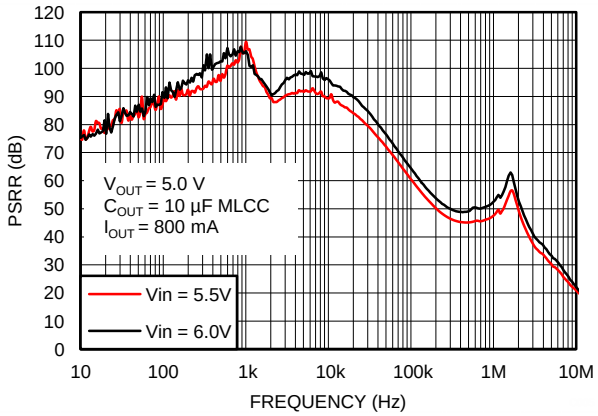

Figure 9. PSRR

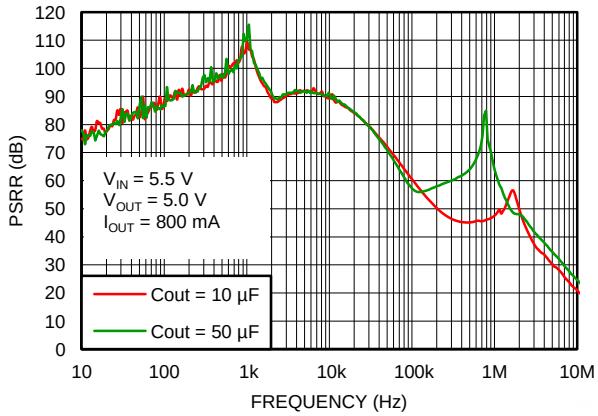

Figure 10. PSRR

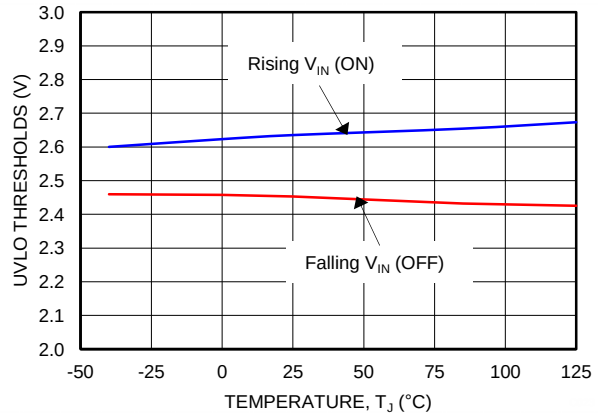

Figure 11. UVLO Thresholds vs T_J

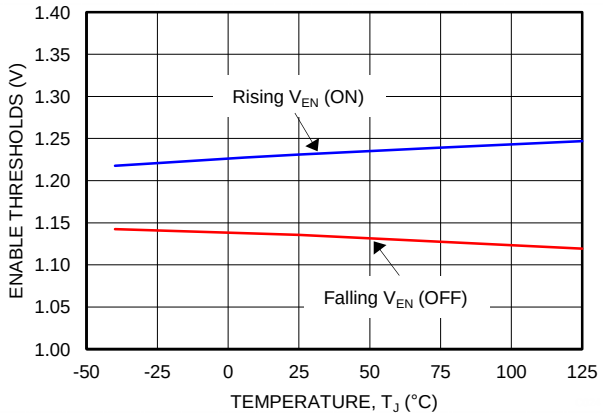

Figure 12. Enable Thresholds vs T_J

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Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5.5 V, V_{OUT} = 5 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16 V X7R, and T_J = 25°C.

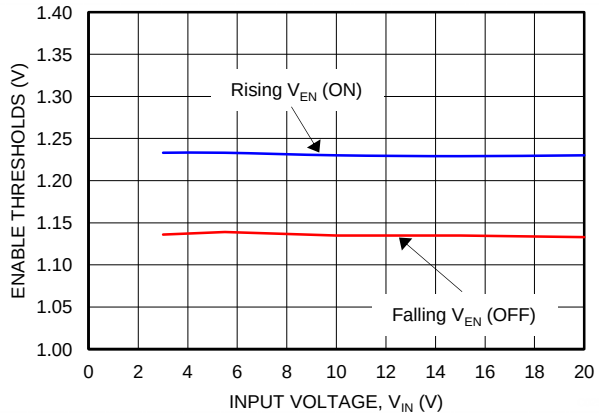

Figure 13. Enable Thresholds vs V_{IN}

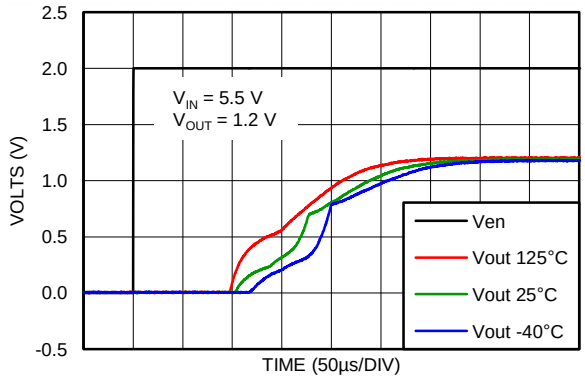

Figure 14. Start-Up Time

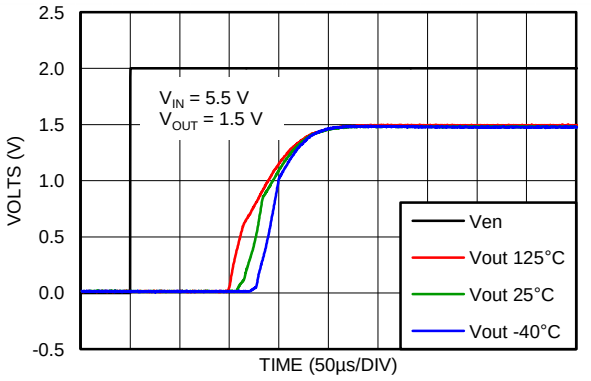

Figure 15. Start-Up Time

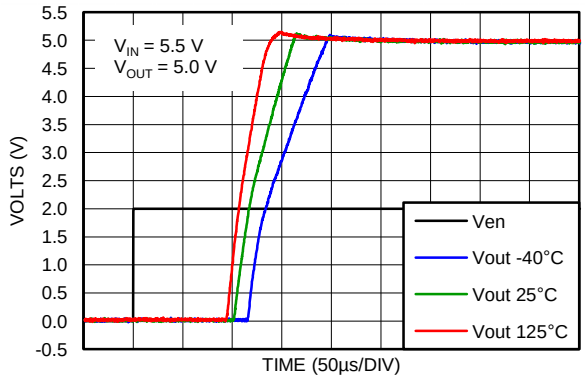

Figure 16. Start-Up Time

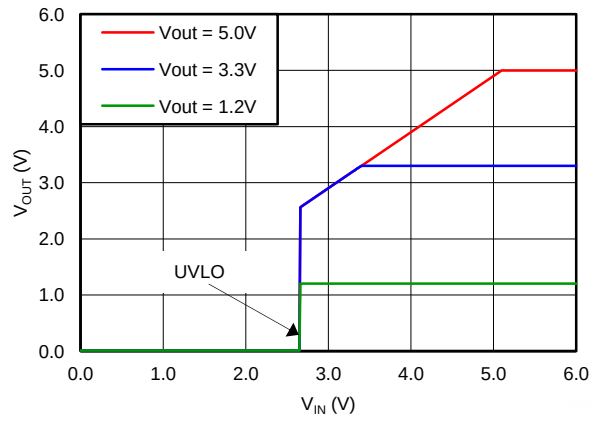

Figure 17. V_{OUT} vs Rising V_{IN}

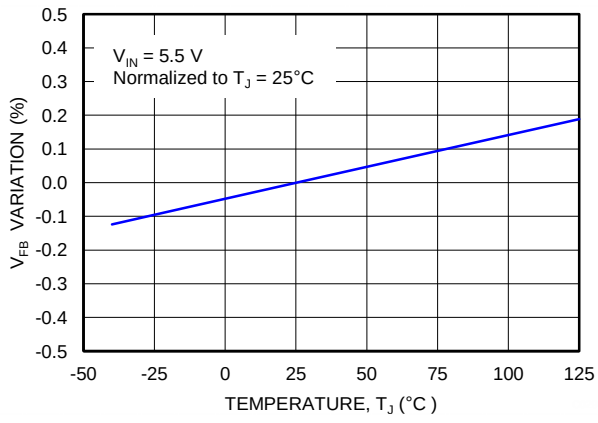

Figure 18. V_{FB} Variation vs T_J

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Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5.5 V, V_{OUT} = 5 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16 V X7R, and T_J = 25°C.

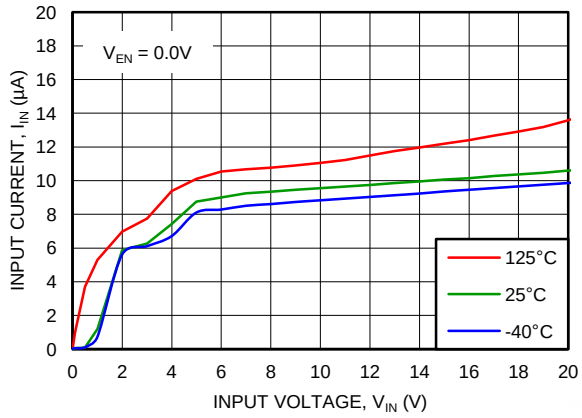

Figure 19. IN Pin Current vs V_{IN}

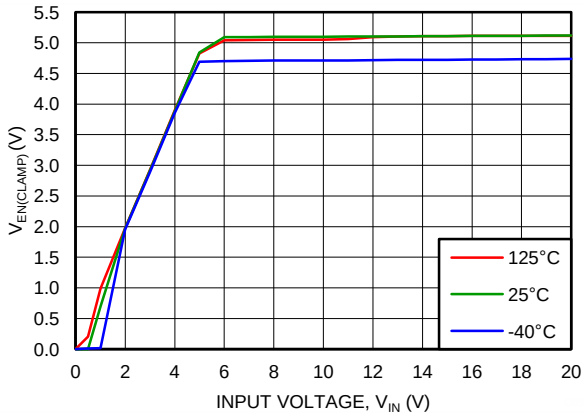

Figure 20. $V_{EN(CLAMP)}$ vs V_{IN}

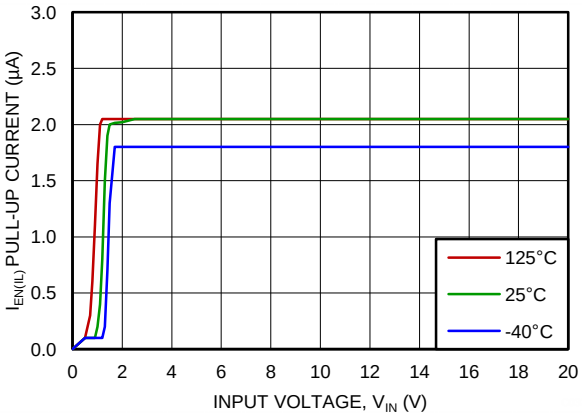

Figure 21. Enable Pin Pull-Up Current vs V_{IN}

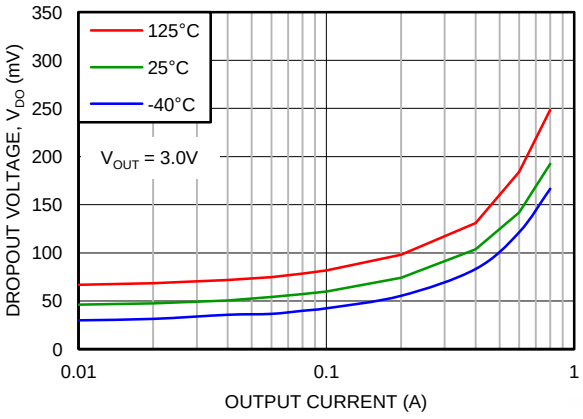

Figure 22. Dropout Voltage vs Output Current

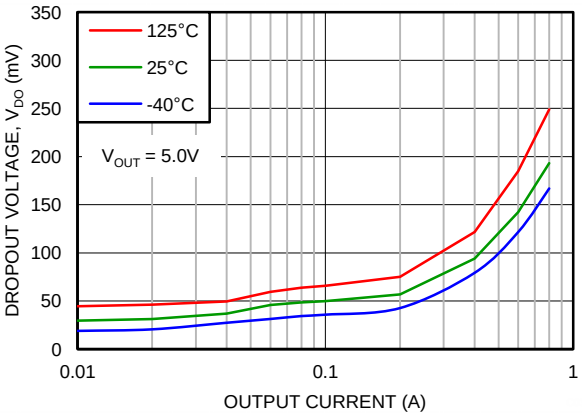

Figure 23. Dropout Voltage vs Output Current

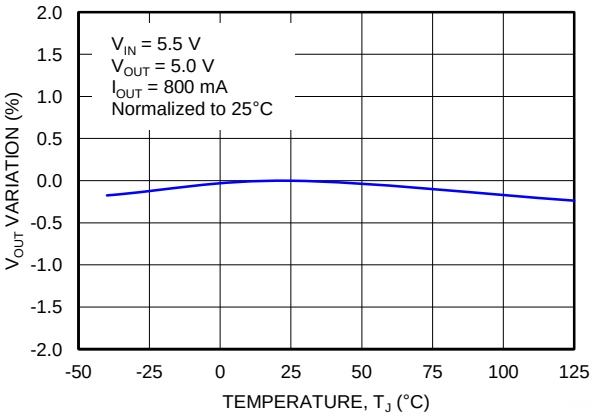

Figure 24. V_{OUT} Variation vs T_J

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Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5.5 V, V_{OUT} = 5 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16 V X7R, and T_J = 25°C.

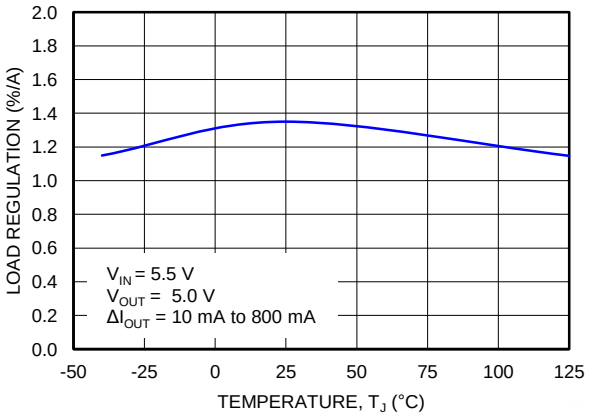

Figure 25. Load Regulation vs T_J

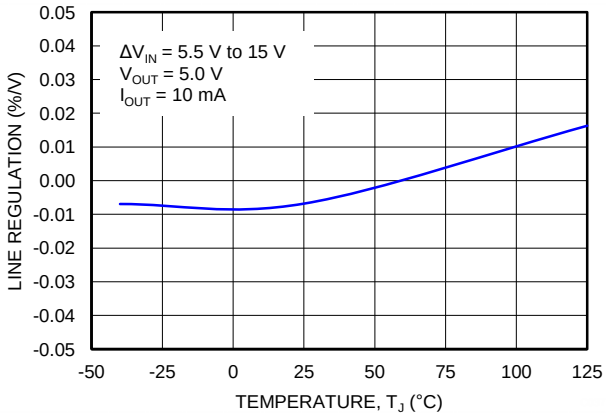

Figure 26. Line Regulation vs T_J

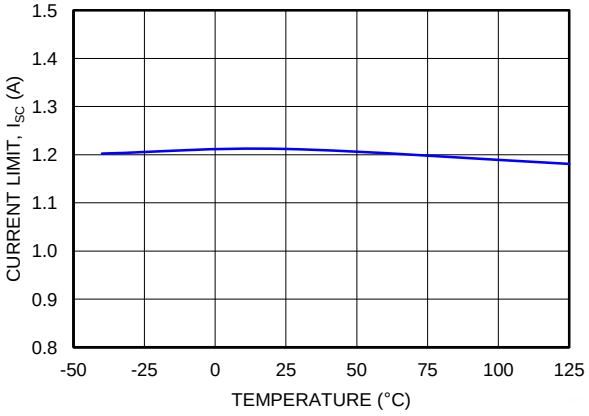

Figure 27. Current Limit, I_{SC} vs T_J

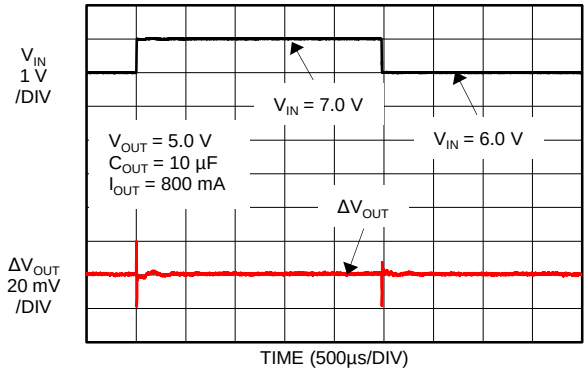

Figure 28. Line Transient

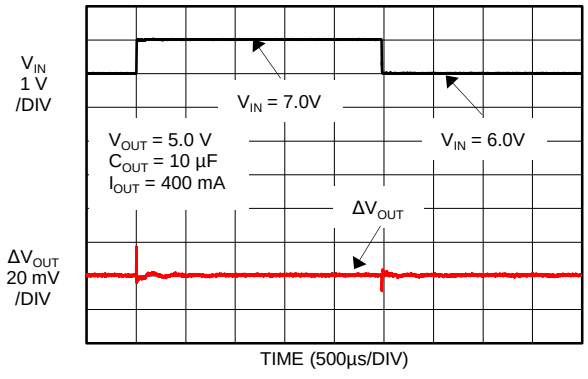

Figure 29. Line Transient

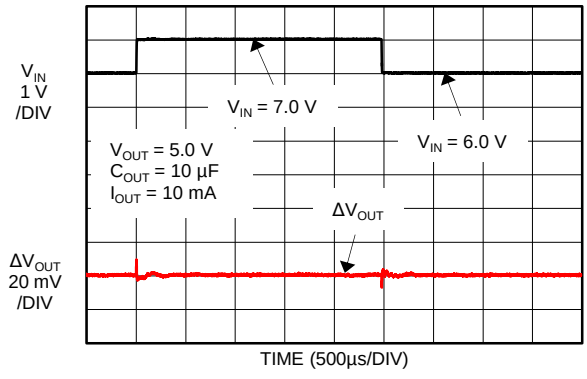

Figure 30. Line Transient

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Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5.5 V, V_{OUT} = 5 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16 V X7R, and T_J = 25°C.

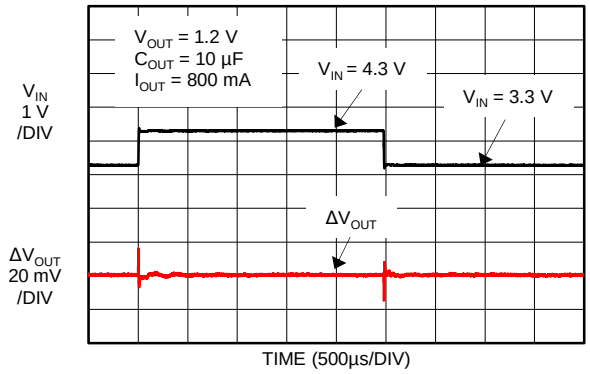

Figure 31. Line Transient

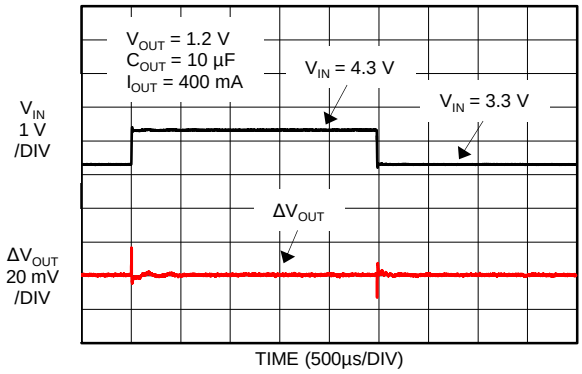

Figure 32. Line Transient

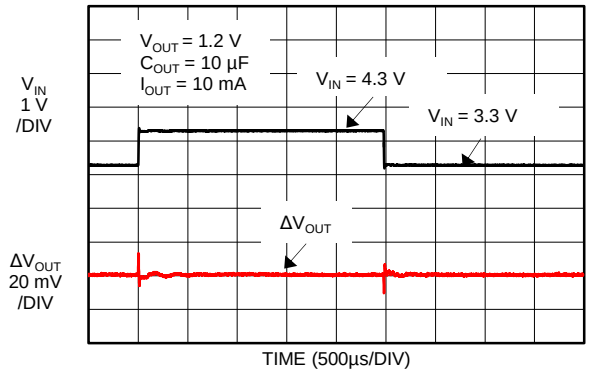

Figure 33. Line Transient

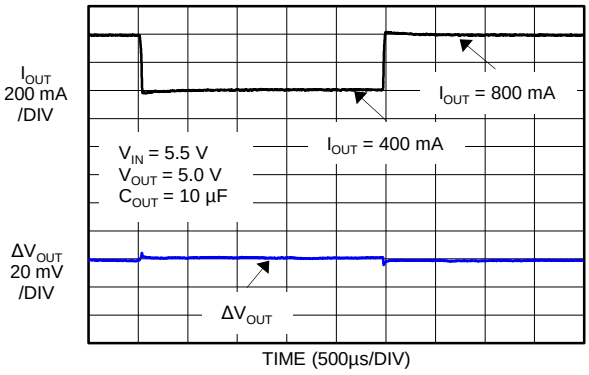

Figure 34. Load Transient

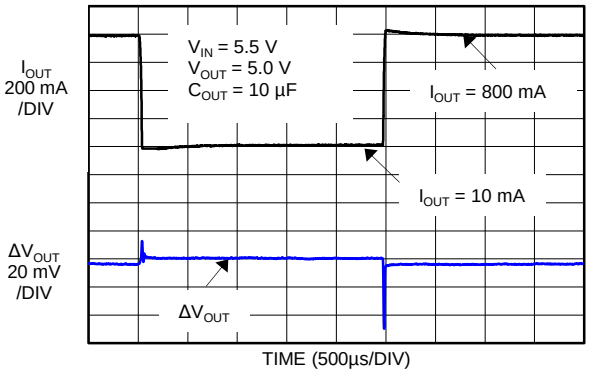

Figure 35. Load Transient

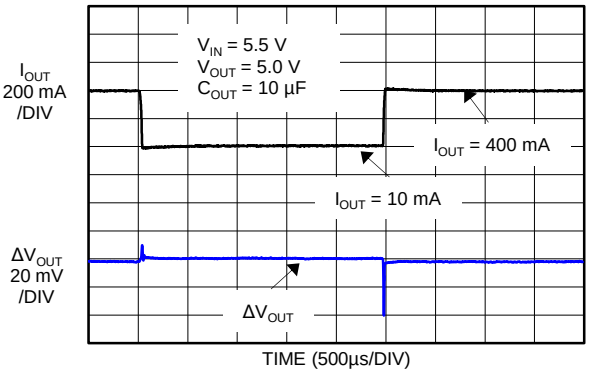

Figure 36. Load Transient

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Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5.5 V, V_{OUT} = 5 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16 V X7R, and T_J = 25°C.

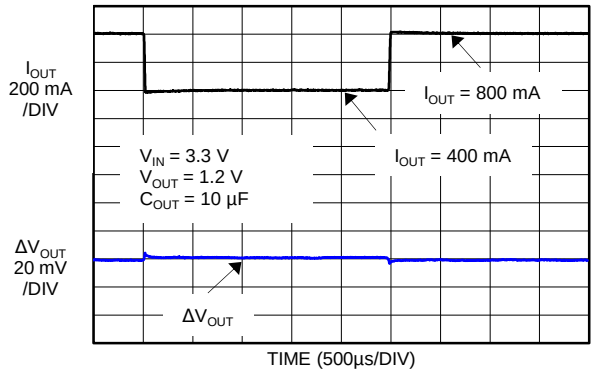


Figure 37. Load Transient

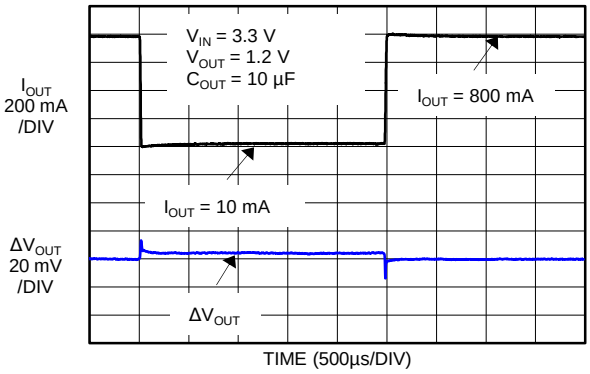


Figure 38. Load Transient

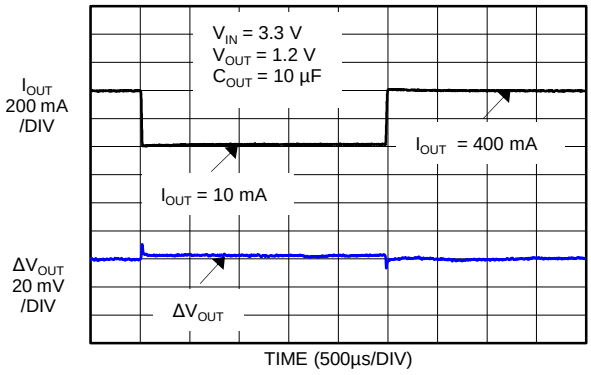


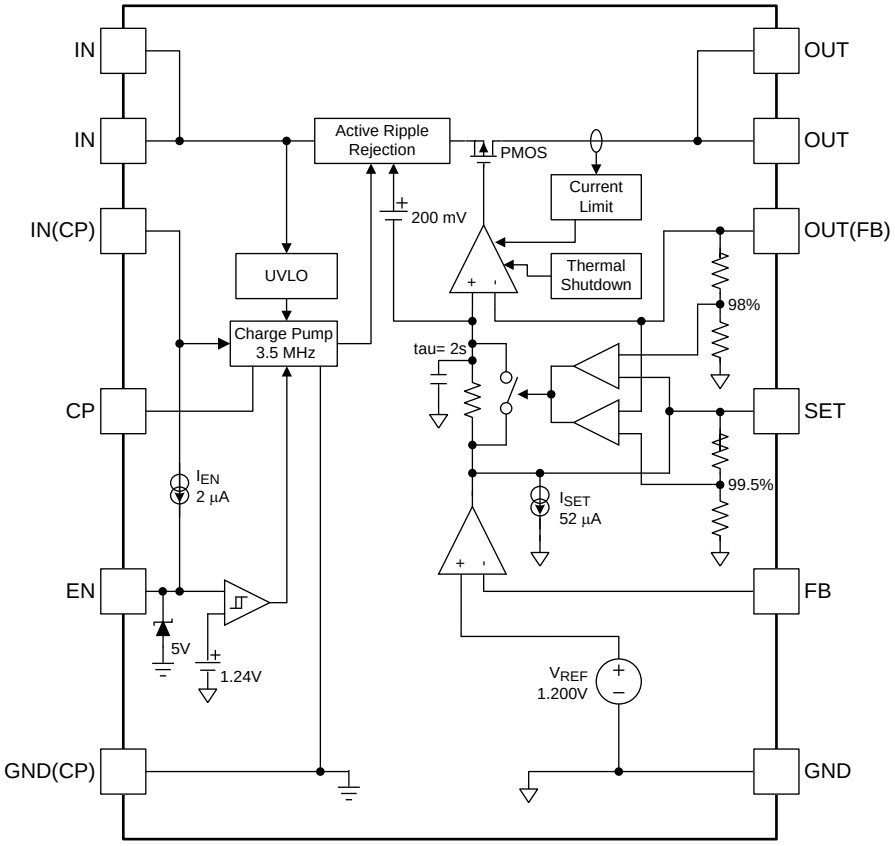
Figure 39. Load Transient

7 Detailed Description

7.1 Overview

The LP38798 is a positive voltage (20 V), ultra-low-noise (5 μV_{RMS}), low-dropout (LDO) regulator capable of supplying a well-regulated, low-noise voltage to an 800-mA load. The LP38798 uses an advanced design with a CMOS process to deliver ultra low output noise and high PSRR at switching power supply (SMPS) frequencies.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Noise Filter

Any noise at LP38798 SET pin is reduced by an internal passive, first order low-pass RC filter before it is passed to the output buffer stage. The low-pass filter has a –3-dB cut-off frequency of approximately 0.08 Hz.

To keep the low-pass filter from interfering with the output voltage rise time at start-up, a voltage comparator keeps the filter in a fast-charge mode while the output voltage (V_{OUT}) is less than 99.5% of the SET pin voltage (V_{SET}) . When the rising V_{OUT} is within 0.5% of V_{SET} the fast-charge mode ends, and V_{OUT} will rise the final 0.5% based on the RC time constant (τ = 2s) of the filter.

Should V_{OUT} be more than 2% above the V_{SET} voltage, a voltage comparator will put the filter into the fast-charge mode to allow the filter to discharge and V_{OUT} to fall a value closer to V_{SET}. When the falling V_{OUT} is within 2% of V_{SET} the fast-charge mode ends, and V_{OUT} will fall the final 2% based on the RC time constant (τ = 2s) of the filter.

If the input voltage has an extended rise time, the output voltage may exhibit a stair-case waveform as the fast-charge mode is activated and de-activated as V_{SET} rises with V_{IN}, and V_{OUT} follows. Once the V_{IN} has risen above the programmed V_{SET} voltage, and V_{OUT} is within 0.5% of V_{SET}, the stair-case behavior will end.

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Feature Description (continued)

7.3.2 Enable Input Operation

The Enable pin (EN) is pulled high internally by a 2 μA (typical) current source from the IN pin, and internally clamped at 5 V (typical) by a zener. Pulling the EN pin low, by sinking the I_{EN} current to ground, will turn the output off.

If the EN function is not needed the EN pin should be left open (floating). Do not connect the EN pin directly to V_{IN} if there is any possibility that V_{IN} might exceed 5.5 V (that is, EN pin AbsMax). If external pullup is required, the external current into the EN pin should be limited to no more than 10 μA.

$$R_{PULL\text{-}UP} > (V_{PULL\text{-}UP} – 5\ V) / 10\ \mu A\ ) \quad (1)$$

7.3.3 Undervoltage Lockout (UVLO)

The LP38798 incorporates UVLO. The UVLO circuit monitors the input voltage and keeps the LP38798 disabled while a rising V_{IN} is less than 2.65 V (typical). The rising UVLO threshold is approximately 350 mV below the recommended minimum operating V_{IN} of 3 V.

7.3.4 Output Current Limiting

The LP38798 incorporates active output current limiting. The threshold for the output current limiting is set well above the ensured output operating current such that it does not interfere with normal operation.

Note that output current limiting is provided as a safety feature and is outside the recommended operating conditions. Operation at the current limit is not recommended as the device junction temperature (T_J) will rise rapidly and operation will likely cross into thermal shutdown behavior .

7.3.5 Thermal Shutdown

The LP38798 includes thermal protection that will shut-off the output current when activated by excessive device dissipation. Thermal shutdown (T_{SD}) will occur when the junction temperature has risen to 170°C. The junction temperature must fall typically 12°C from the shutdown temperature for the output current to be restored. Junction temperature is calculated from the formula in Equation 2:

$$T_J = (T_A + (P_D \times R_{\theta JA})) \quad (2)$$

Where the power being dissipated, P_D, is defined as:

$$P_D = ((V_{IN} – V_{OUT}) \times I_{OUT}) \quad (3)$$

NOTE

Thermal shutdown is provided as a safety feature and is outside the specified Operating Ratings temperature range. Operation with a junction temperature (T_J) above 125°C is not recommended as the device behavior is not specified.

7.4 Device Functional Modes

The LP38798 has two functional modes:

1. Enabled: When the EN pin voltage is above the $V_{EN(ON)}$ threshold, and V_{IN} is above the UVLO threshold, the device is enabled.
2. Disabled: When the EN pin voltage is below the ($V_{EN(ON)}$ + ΔV_{EN}) threshold, or V_{IN} is below the UVLO threshold, the device is disabled.

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7.5 Programming

7.5.1 Programming the Output Voltage

Current sourced from the SET pin, through R1 and R2, must be kept to less than 100 µA. The minimum allowed value for R2 is 12.9 kΩ.

$$I_{SET} = V_{FB} / R2 \quad (4)$$

$$R2_{MIN} = V_{FB(MAX)} / 100\ \mu A \quad (5)$$

$$R2_{MIN} = 12.9\ k\Omega; \quad (6)$$

The values for R1 and R2 may be adjusted as needed to achieve the desired output voltage as long as the value for R2 is no less than 12.9 kΩ. The maximum recommended value for R2 is 100 kΩ.

Equation 7 is used to determine the output voltage:

$$V_{OUT} = (V_{FB} \times (1 + (R1 / R2\ ))) + V_{OS} \quad (7)$$

Alternately, Equation 8 can be used to determine the appropriate R1 value for a given R2 value:

$$R1 = R2 \times (((V_{OUT}) / V_{FB}) - 1) \quad (8)$$

Table 1 suggests some ±1% values for R1 and R2 for a range of output voltages using the typical V_{FB} value of 1.200V. This is not a definitive list, as other combinations exist that will provide similar, possibly better, performance.

Table 1. Typical R1 and R2 Values for Assorted Output Voltages

TARGET V_{OUT}	R1	R2	TYPICAL V_{OUT}
1.2 V	0 Ω	15 kΩ	1.2 V
1.5 V	4.22 kΩ	16.9 kΩ	1.5 V
1.8 V	10.5 kΩ	21 kΩ	1.8 V
2 V	10 kΩ	15 kΩ	2 V
2.5 V	16.2 kΩ	15.0 kΩ	2.496 V
3 V	21 kΩ	14 kΩ	3 V
3.3 V	23.2 kΩ	13.3 kΩ	3.293 V
5 V	47.5 kΩ	15 kΩ	5 V

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP38798 is a high-performance linear regulator capable of supplying a well-regulated, low-noise voltage into an 800-mA load. The LP38798 can operate over a wide input voltage range (3 V to 20 V) making it well suited for many post-regulation applications.

8.2 Typical Application: V_{OUT} = 5 V

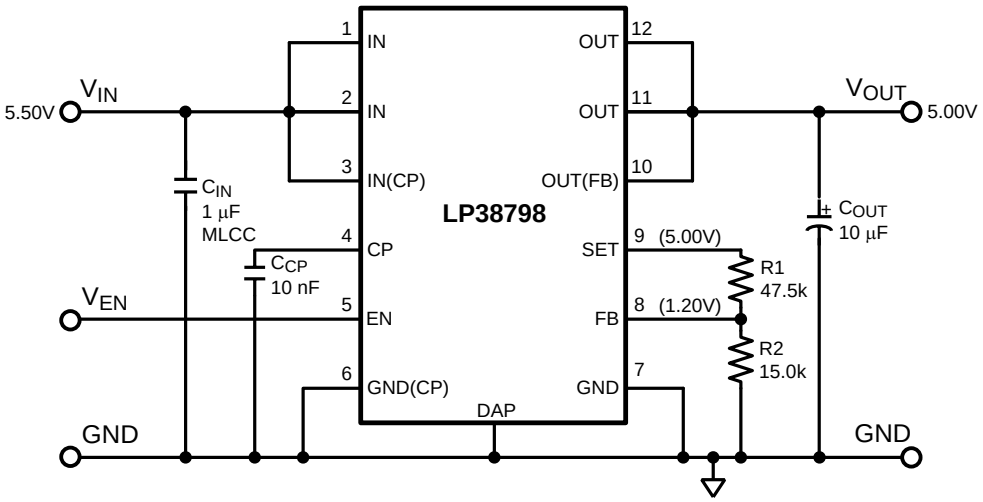

Figure 40. Typical Application, V_{OUT} = 5 V

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	5.5 V, ±10%
Output voltage	5. V, ±3.5%
Output current	500 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LP39798 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance

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- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Input Capacitor Recommendations

The LP38798 is designed and characterized for operation with a ceramic capacitor of 1 µF, or greater, at the input. Note especially that the input capacitances must be located as near as practical to the IN pins

The minimum recommended input capacitance is 1 µF, ceramic or tantalum. However, if the LP38798 is operating in conditions where input ripple, fast changes in the input voltage, or large changes in the load current demand are expected, a minimum input capacitance of 10 µF is strongly recommended

Ceramic capacitor tolerance and variations due temperature and applied voltage must be considered when selecting a capacitor to assure the minimum input capacitance requirement is met over the intended operating range.

The input capacitor must be located as close as physically possible to the input pin and returned to a clean analog ground. Any good quality tantalum capacitor may be used, while a ceramic capacitor should be X5R or X7R rated with appropriate adjustments due to the loss of capacitance value from the applied DC voltage.

Attention must be given to the input capacitance value to minimize transient input voltage droop during load current steps at the OUT pin. Larger input capacitor values are necessary for good transient load response, and have no detrimental influence on the stability of the device. Note, however, that using large value ceramic input capacitances can also cause unwanted ringing at the output if the input capacitor, in combination with the trace inductance, creates a high-Q peaking effect during transients. Short, well-designed interconnect leads to the up-stream supply minimize this effect without adding damping. Damping of unwanted ringing can be accomplished by using a tantalum capacitor, with a few hundred milli-ohms of ESR, in parallel with the ceramic input capacitor.

8.2.2.3 Output Capacitor Recommendations

The LP38798 requires an output capacitance of at least 1 µF, ceramic or tantalum; however, a minimum output capacitance of 10 µF is strongly recommended if fast load transient conditions are expected. While the LP38798 is designed to work with Ceramic output capacitors, the output capacitor can be Ceramic, Tantalum, or a combination. The total output capacitance must be sized appropriately to handle any fast load current steps. Capacitance type, tolerance, ESR, as well as temperature and voltage characteristics, must be considered when selecting an output capacitor for the application.

Note especially that the output capacitances must be located as near as practical to the OUT pins.

Even though the LP38798 is stable with an output capacitance of 1 µF to 10 µF, a single output capacitor will generally not be able to provide the best PSRR performance across a wide frequency range. Multiple parallel capacitors, each with a different self-resonance frequency will provide better performance over a wider frequency range.

The LP38798 is characterized with a ceramic capacitor of 10 µF, or greater, at the output. Noise performance is characterized using a single output capacitor of 10 µF ±10%, 16V, X7R, 1206.

8.2.2.4 Charge Pump

The charge pump is running when both the input voltage is above the UVLO threshold (2.65 V typical) and the EN pin voltage is above the $V_{EN(ON)}$ threshold (1.24 V typical). The typical charge pump operating frequency is 3.5 MHz.

A low leakage 10 nF X7R storage capacitor is required between the CP pin and ground to store the energy required for gate drive of the internal NMOS pass device. Larger values of capacitance may slow start-up times, while smaller capacitance values may result in degraded dynamic performance.

Do not make any other connection to the CP pin. Loading this pin in any manner degrades regulator performance. No external biasing may be applied to, or derived from, this pin, as permanent damage to the internal charge pump circuitry may occur.

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8.2.2.5 Setting the Output Voltage

The output voltage is buffered from the SET pin. The output voltage is defined as:

$V_{OUT} = V_{SET} = (V_{FB} \times (1 + (R1 / R2))$

where

- V_{FB} = 1.2 V (typical)
- R2 = 12.9 kΩ minimum to 100 kΩ maximum (9)

Selecting a standard 1% resistor value of 15 kΩ for R2, the resistor value needed for R1 to provide an output voltage of 5V is calculated from:

$R1 = R2 \times ((V_{OUT} / V_{FB}) – 1)$ (10)

$R1 = 15\ k\Omega \times ((5\ V / 1.2\ V) – 1)$ (11)

$R1 = 47.5\ k\Omega$ (12)

8.2.2.6 Device Dissipation

Device power dissipation is defined as:

$P_D = ((V_{IN} – V_{OUT}) \times I_{OUT})$ (13)

$P_D = ((5.5\ V - 5\ V) \times 0.5\ A)$ (14)

$P_D = 250\ mW$ (15)

Given 250 mW of device power dissipation, a maximum operating junction temperature (T_J) of 125°C, and presuming a $R_{\theta JA}$ of 35.4°C/W, the maximum ambient temperature (T_A) is defined as:

$T_{A(MAX)} = T_{J(MAX)} – (P_D \times R_{\theta JA})$ (16)

$T_{A(MAX)} = (125°C – (0.25\ W \times 35.4°C/W))$ (17)

$T_{A(MAX)} = 116°C$ (18)

8.2.3 Application Curve

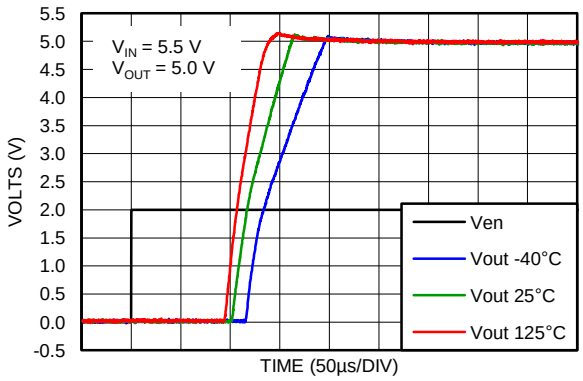


Figure 41. Start-Up Time

9 Power Supply Recommendations

The LP38798 device is designed to operate from an input voltage supply range of 3 V to 20 V. The input supply must be able to supply enough current to keep the input voltage from drooping during load transients and high load current. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP38798 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP38798.

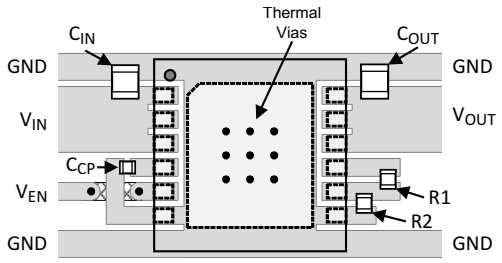
Best performance is achieved by placing all of the components on the same side of the PCB as the LP38798, and as close as is practical to the LP38798 package. All component ground connections must be back to the LP38798 analog ground connection using as wide and short of a copper trace as is practical. The connection from the FB pin to the V_{SET} resistors must be as short as possible as the FB pin is a high impedance input. Any trace length on the FB pin acts as an antenna.

Connections using long trace lengths, narrow trace widths; avoid connections through vias, which add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

A ground plane, either on the opposite side of a two-layer PCB, or embedded in a multi-layer PCB, is strongly recommended. This Ground Plane serves two purposes :

1. Provides a circuit reference plane to assure accuracy, and
2. Provides a thermal plane to remove heat from the LP38798 through thermal vias under the package DAP.

10.2 Layout Example



10.3 Thermal Considerations

The value of $R_{\theta JA}$ for the 12-lead WSON package is specifically dependent on PCB copper area, copper thickness, the number of layers, and thermal vias under the exposed thermal pad (DAP). Refer to *A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* for general guidelines for mounting packages with exposed thermal pads.

Exceeding the maximum allowable power dissipation defined by the final $R_{\theta JA}$ will cause excessive die temperature, and the regulator may go into thermal shutdown.

10.4 Estimating the Junction Temperature

The EIA/JEDEC standard (JESD51-2) provides methodologies to estimate the junction temperature from external measurements (Ψ_{JB} references the temperature at the PCB, and Ψ_{JT} references the temperature at the top surface of the package) when operating under steady-state power dissipation conditions. These methodologies have been determined to be relatively independent of the copper thermal spreading area that may be attached to the package DAP when compared to the more typical $R_{\theta JA}$. Refer to *Semiconductor and IC Package Thermal Metrics*, for specifics.

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Suppport

11.1.1.1 Custom Design With WEBENCH® Tools

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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401)
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* (SNVA183)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38798SD-ADJ/NOPB	ACTIVE	WSON	DNT	12	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00075B	Samples
LP38798SDE-ADJ/NOPB	ACTIVE	WSON	DNT	12	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00075B	Samples
LP38798SDX-ADJ/NOPB	ACTIVE	WSON	DNT	12	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00075B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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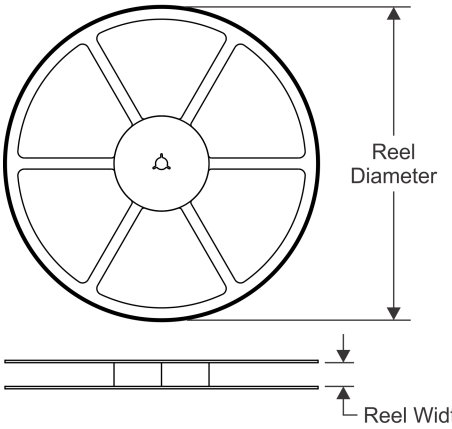
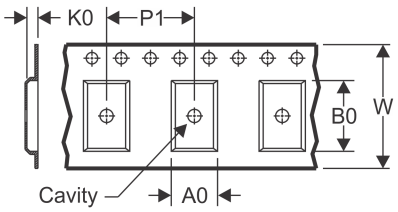
TAPE AND REEL INFORMATION

REEL DIMENSIONS

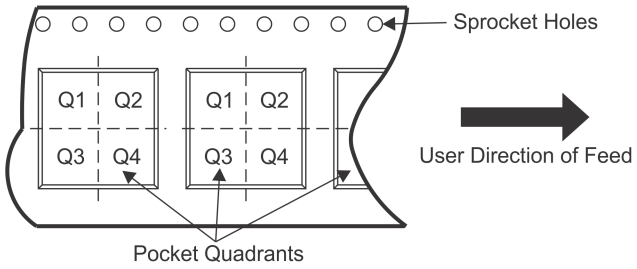


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

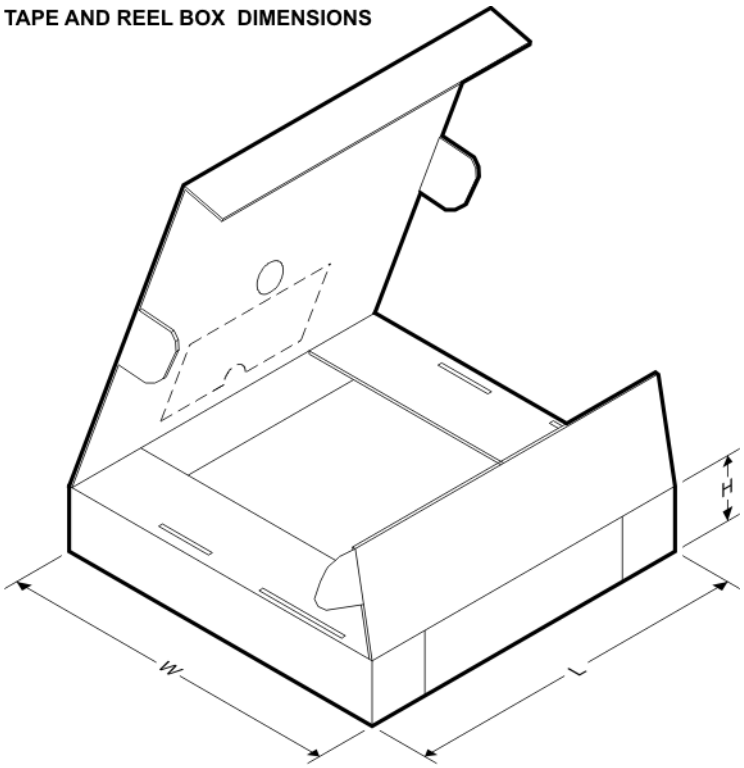
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38798SD-ADJ/NOPB	WSON	DNT	12	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP38798SDE-ADJ/NOPB	WSON	DNT	12	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP38798SDX-ADJ/NOPB	WSON	DNT	12	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



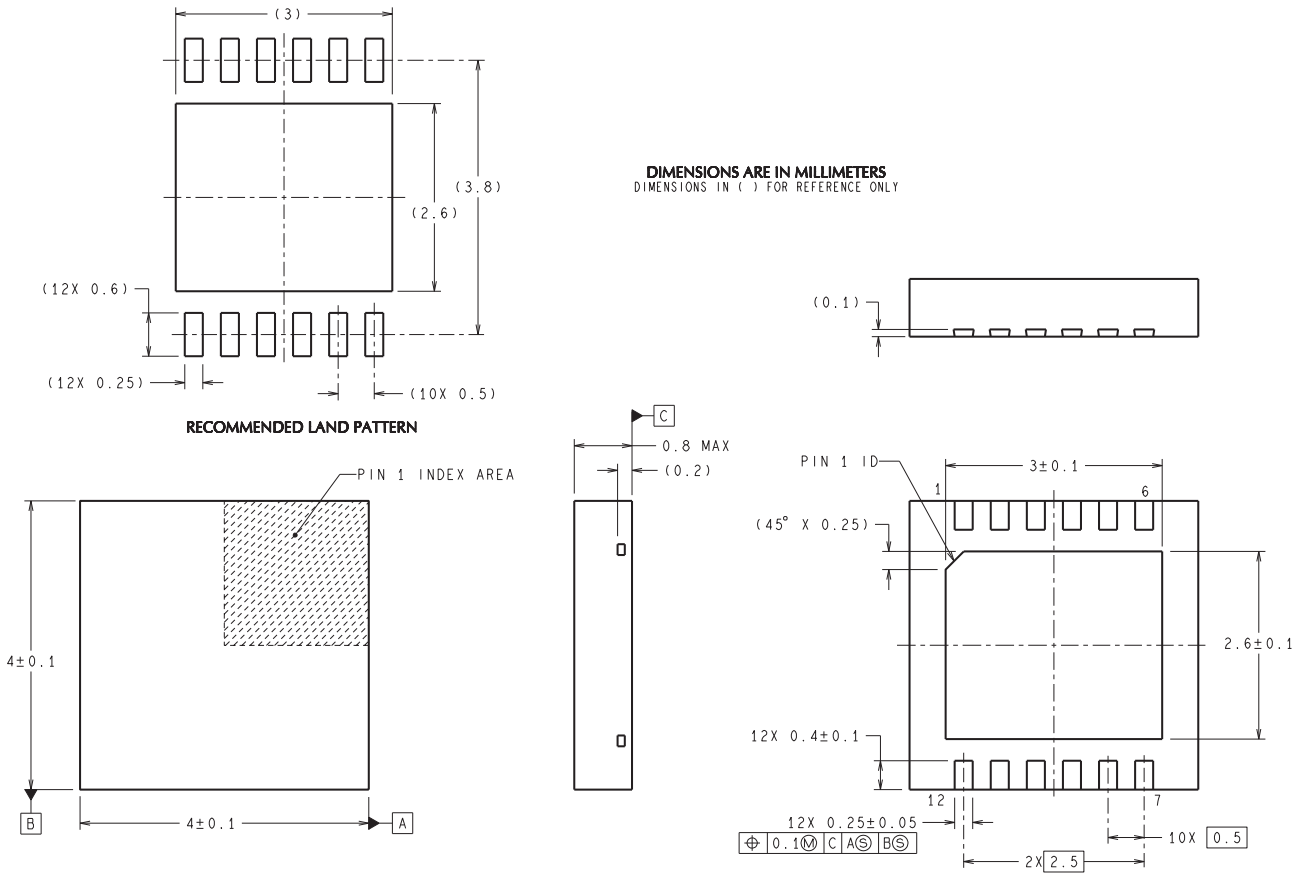
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38798SD-ADJ/NOPB	WSON	DNT	12	1000	210.0	185.0	35.0
LP38798SDE-ADJ/NOPB	WSON	DNT	12	250	210.0	185.0	35.0
LP38798SDX-ADJ/NOPB	WSON	DNT	12	4500	367.0	367.0	35.0

DNT0012B

WSON - 0.8mm max height

SON (PLASTIC SMALL OUTLINE - NO LEAD)



NOTES:
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is designed to be soldered to a thermal pad on the board for thermal and mechanical performance. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

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