

L, S-band Medium Power SPDT Switch

AEC Q100 Qualified

DESCRIPTION

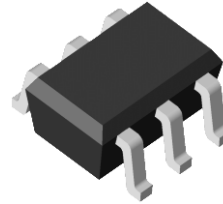
- The CG2179M2-Q is a pHEMT GaAs SPDT_ (Single Pole Double Throw) switch. This device can operate from 0.05 GHz to 3.0GHz, having low insertion loss and high isolation.

FEATURES

- Control voltage :
VC(H) = 1.8 to 5.3 V (3.0 V TYP.)
VC(L) = -0.2 to 0.2 V (0 V TYP.)
- Low insertion loss :
L_{ins1} = 0.30 dB TYP. @ f = 0.05 to 0.5 GHz
L_{ins2} = 0.30 dB TYP. @ f = 0.5 to 1.0 GHz
L_{ins3} = 0.40 dB TYP. @ f = 1.0 to 2.0 GHz
L_{ins4} = 0.45 dB TYP. @ f = 2.0 to 2.5 GHz
L_{ins5} = 0.45 dB TYP. @ f = 2.5 to 3.0 GHz
- High isolation :
ISL1 = 39 dB TYP. @ f = 0.05 to 0.5 GHz
ISL2 = 33 dB TYP. @ f = 0.5 to 1.0 GHz
ISL3 = 27 dB TYP. @ f = 1.0 to 2.0 GHz
ISL4 = 26 dB TYP. @ f = 2.0 to 2.5 GHz
ISL5 = 23 dB TYP. @ f = 2.5 to 3.0 GHz
- Power handling :
P_{in(0.5dB)} = +32 dBm TYP. @ f = 3.0 GHz,
VC(H) = 3.0 V, VC(L) = 0 V

PACKAGE

- 6-pin mini mold Package
(2.0mm x 1.25mm x 0.9mm)



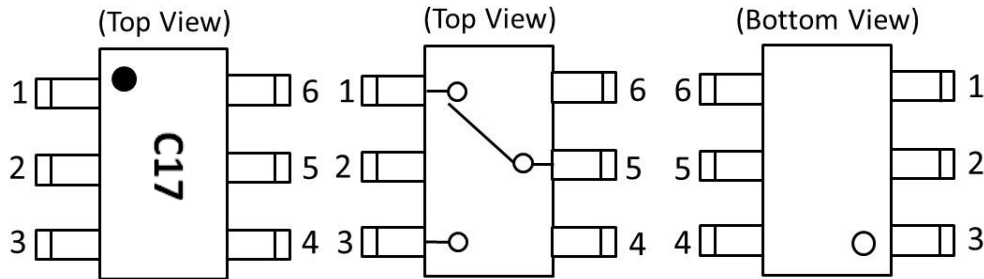
APPLICATIONS

- Wireless LAN (IEEE 802.11 b/g/n/ac)
- Wireless Automotive Systems

ORDERING INFORMATION

Part Number	Order Number	Package	Marking	Description
CG2179M2-Q	CG2179M2-C4-Q	6-pin mini mold package (Pb-Free)	C17	<ul style="list-style-type: none"> Embossed tape 8 mm wide Pin 4, 5, 6 face the perforation side of the tape MOQ 10 kpcs/reel
CG2179M2-EVAL	CG2179M2-EVAL			<ul style="list-style-type: none"> Evaluation Board with DC block capacitors, power supply bypass capacitors, and RF and DC connectors MOQ 1

PIN CONFIGURATION AND INTERNAL BLOCK DIAGRAM



Pin No.	Pin Name
1	RF1
2	GND
3	RF2
4	VC2
5	RFC
6	VC1

TRUTH TABLE

VC1	VC2	RFC-RF1	RFC-RF2
Low	High	ON	OFF
High	Low	OFF	ON

ABSOLUTE MAXIMUM RATINGS

(TA = +25°C, unless otherwise specified)

Parameter	Symbol	Rating	Unit
Control Voltage	VC	6.0 ^{Note 1}	V
Input Power	P _{in1}	+33 ^{Note 2}	dBm
	P _{in2}	+29 ^{Note 3}	dBm
Operating Ambient Temperature	T _A	-45 ~ +105	°C
Storage Temperature	T _{stg}	-55 ~ +150	°C

- Note**
1. $|VC1 - VC2| \leq 6.0V$
 2. $3.0V \leq |VC1 - VC2| \leq 5.0V, 0.4GHz \leq f$
 3. $3.0V \leq |VC1 - VC2| \leq 5.0V, 0.05GHz \leq f \leq 0.4GHz$

RECOMMENDED OPERATING RANGE

(TA = +25°C, unless otherwise specified)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Operating Frequency	f	0.05	-	3.0	GHz
Switch Control Voltage (H)	VC(H)	+1.8	+3.0	+5.3	V
Switch Control Voltage (L)	VC(L)	-0.2	0	+0.2	V

ELECTRICAL CHARACTERISTICS 1

(TA = +25°C, VC(H) = 3.0V, VC(L) = 0V, Zo = 50Ω, DC Block Capacitance = 56pF, unless otherwise specified)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Insertion Loss	L _{INS1}	f=0.05 to 0.5GHz ^{Note 1}	-	0.30	0.50	dB
	L _{INS2}	f=0.5 to 1.0GHz	-	0.30	0.50	dB
	L _{INS3}	f=1.0 to 2.0GHz	-	0.40	0.60	dB
	L _{INS4}	f=2.0 to 2.5GHz	-	0.45	0.65	dB
	L _{INS5}	f=2.5 to 3.0GHz	-	0.45	0.65	dB
Isolation	ISL1	f=0.05 to 0.5GHz ^{Note 1}	36	39	-	dB
	ISL2	f=0.5 to 1.0GHz	30	33	-	dB
	ISL3	f=1.0 to 2.0GHz	23	27	-	dB
	ISL4	f=2.0 to 2.5GHz	22	26	-	dB
	ISL5	f=2.5 to 3.0GHz	21	24	-	dB
Return Loss	RL	f=0.05 to 3.0GHz ^{Note 1}	15	20	-	dB
0.1dB Loss Compression Input Power Note 2	P _{in(0.1dB)}	f=0.05~0.5GHz ^{Note 1}	-	+26	-	dBm
		f=0.5~3.0GHz	-	+30	-	dBm
0.5dB Loss Compression Input Power Note 3	P _{in(0.5dB)}	f=0.05~0.5GHz ^{Note 1}	-	+28.5	-	dBm
		f=0.5~3.0GHz	-	+32	-	dBm
2nd Harmonics	2f ₀	f=3.0GHz, P _{in} =+20dBm	-	-85	-	dBc
3rd Harmonics	3f ₀	f=3.0GHz, P _{in} =+20dBm	-	-85	-	dBc
3rd Order Input Intercept Point	IIP ₃	f=2.5GHz, 2-tone 1MHz Spacing	-	+58	-	dBm
Error Vector Magnitude	EVM	802.11g, 64QAM, 54Mbps P _{in} ≤ +25dBm	-	2.5	-	%
Switch Control Current	I _{CONT}	RF none	-	1	10	uA
Switching Speed	t _{SW}	50% CTL to 90/10% RF	-	50	-	ns

Note 1. DC block capacitance = 1000pF at f=0.05 to 0.5GHz

2. P_{in(0.1dB)} is the measured input power level when the insertion loss increases 0.1dB more than that of the linear range.

3. P_{in(0.5dB)} is the measured input power level when the insertion loss increases 0.5dB more than that of the linear range

ELECTRICAL CHARACTERISTICS 2

(TA = +25°C, VC(H) = 1.8V, VC(L) = 0V, Zo = 50Ω, DC Block Capacitance = 56pF, unless otherwise specified)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Insertion Loss	L _{INS1}	f=0.05 to 0.5GHz ^{Note 1}	-	0.30	0.50	dB
	L _{INS2}	f=0.5 to 1.0GHz	-	0.30	0.50	dB
	L _{INS3}	f=1.0 to 2.0GHz	-	0.40	0.60	dB
	L _{INS4}	f=2.0 to 2.5GHz	-	0.45	0.65	dB
	L _{INS5}	f=2.5 to 3.0GHz	-	0.45	0.65	dB
Isolation	ISL1	f=0.05 to 0.5GHz ^{Note 1}	36	39	-	dB
	ISL2	f=0.5 to 1.0GHz	30	33	-	dB
	ISL3	f=1.0 to 2.0GHz	23	27	-	dB
	ISL4	f=2.0 to 2.5GHz	22	26	-	dB
	ISL5	f=2.5 to 3.0GHz	21	24	-	dB
Return Loss	RL	f=0.05 to 3.0GHz ^{Note 1}	15	20	-	dB
0.1dB Loss Compression Input Power Note 2	P _{in(0.1dB)}	f=0.05~0.5GHz ^{Note 1}	-	+19	-	dBm
		f=0.5~3.0GHz	-	+23	-	dBm
0.5dB Loss Compression Input Power Note 3	P _{in(0.5dB)}	f=0.05~0.5GHz ^{Note 1}	-	+22	-	dBm
		f=0.5~3.0GHz	-	+26	-	dBm
Switch Control Current	I _{CONT}	RF none	-	1	10	uA
Switching Speed	t _{SW}	50% CTL to 90/10% RF	-	50	-	ns

Note 1. DC block capacitance = 1000pF at f=0.05 to 0.5GHz

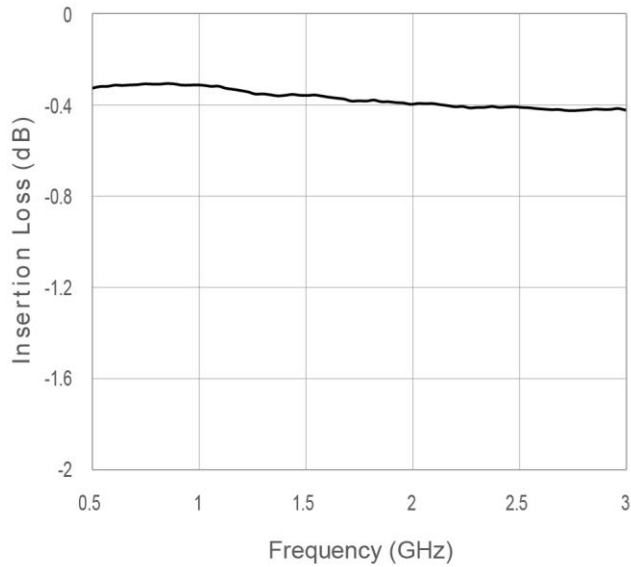
2. P_{in(0.1dB)} is the measured input power level when the insertion loss increases 0.1dB more than that of the linear range.

3. P_{in(0.5dB)} is the measured input power level when the insertion loss increases 0.5dB more than that of the linear range

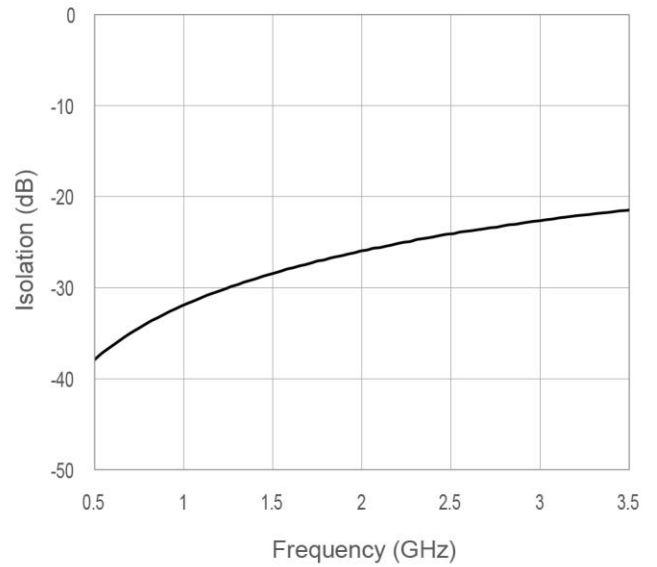
TYPICAL CHARACTERISTICS

(Vc(H)=3V, Vc(L)=0V, TA= +25°C, DC Block Capacitance=56pF, through board loss is subtracted in insertion loss data)

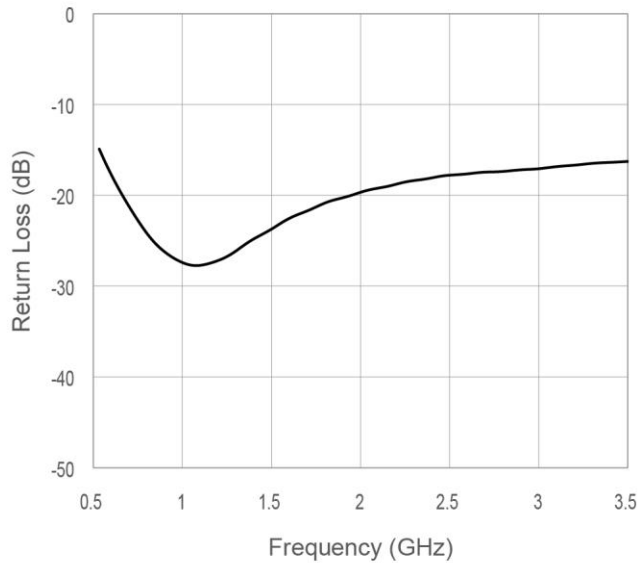
Typical Insertion Loss vs. Frequency



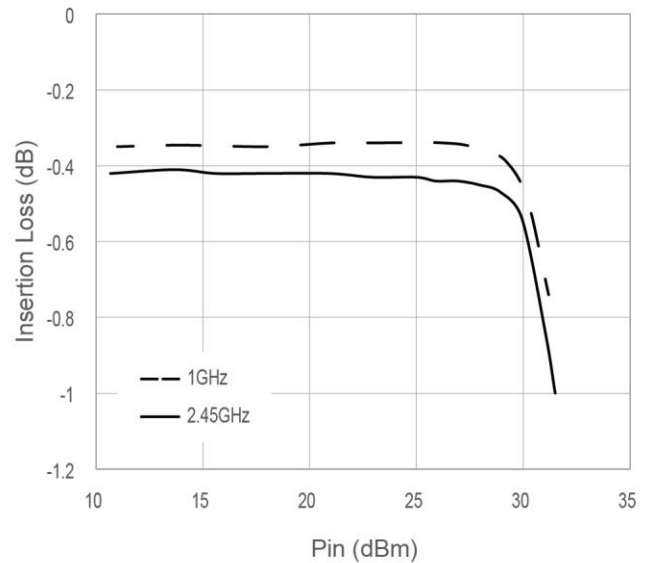
Typical Isolation vs. Frequency



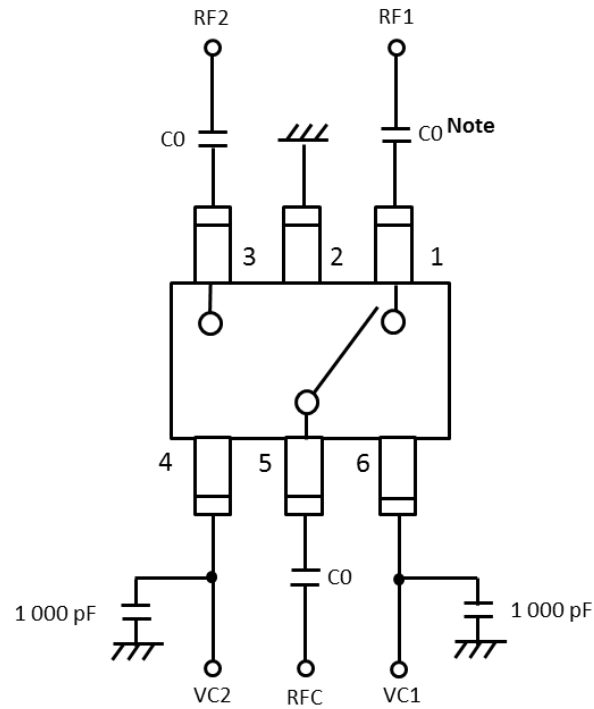
Typical Return Loss vs. Frequency



Typical Insertion Loss vs. Input Power



EVALUATION CIRCUIT

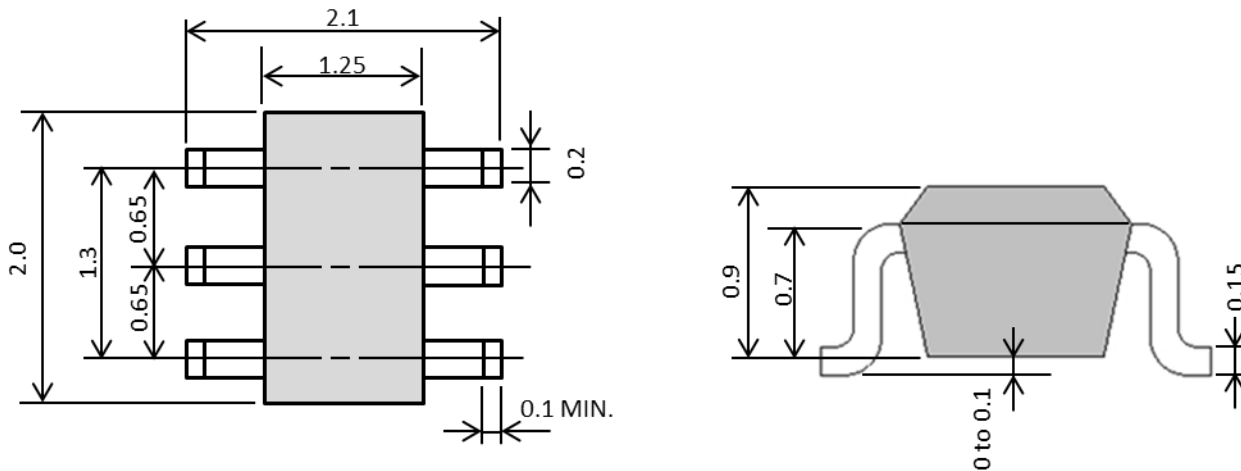


Note C0 : 0.05 to 0.5 GHz 1000pF
: 0.4 to 3.0 GHz 56pF

The application circuits and their parameters are for reference only and are not intended for use in actual designs. DC Blocking Capacitors are required at all RF ports.

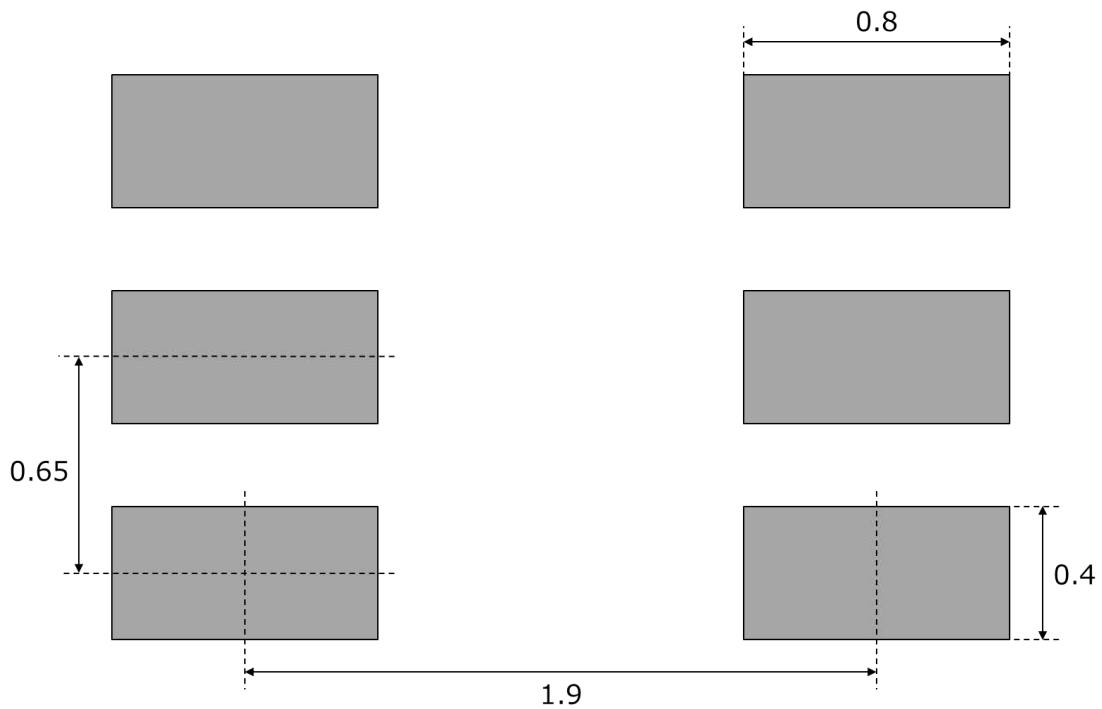
PACKAGE DIMENSIONS

6-pin mini mold package (Unit: mm)



PCB LAYOUT FOOTPRINT

6-pin mini mold (Unit: mm)



The PCB Layout Footprint in this document is for reference only

RECOMMENDED SOLDERING CONDITIONS

Recommended Soldering Conditions are available on CEL's [Part Summary page](#) under Associated Documents

REVISION HISTORY

Version	Change to current version	Page(s)
CDS-0008-06-Q (Issue A) Sept 2018	Preliminary initial datasheet	N/A
CDS-0008-06-Q (Issue B) April 1, 2019	Removed "Preliminary" from page 1	1
CDS-0008-07-Q (Issue C) April 12, 2019	Updated Order Number and Marking Information Added PCB Layout Footprint	1, 2 7

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