

Product Overview

The NSi823x devices are high reliability triple-channel digital isolators. The NSi823x device is safety certified by UL1577 support 5kV_{rms} insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi823x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/us. The NSi823x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi823x device supports to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use. AEC-Q100 (Grade 1) option is provided for all devices.

Key Features

- Up to 5000V_{rms} Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- AEC-Q100 Grade 1 available for all devices
- High CMTI: 250kV/us
- Chip level ESD: HBM: ±8kV
- Robust Electromagnetic Compatibility (EMC)
 - System-Level ESD, EFT, and Surge Immunity
 - Low Emissions
- Default output high level or low level option
- Isolation barrier life: >60 years
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -55°C~125°C
- RoHS-compliant packages:
 - SOP16(300mil)
 - SOP16(600mil)

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

Part Number	Package	Body Size
NSI823x-DSWR	SOP16(300mil)	10.30mm × 7.50mm
NSI823x-DSWWR	SOP16(600mil)	10.30mm × 14.0mm

Functional Block Diagrams

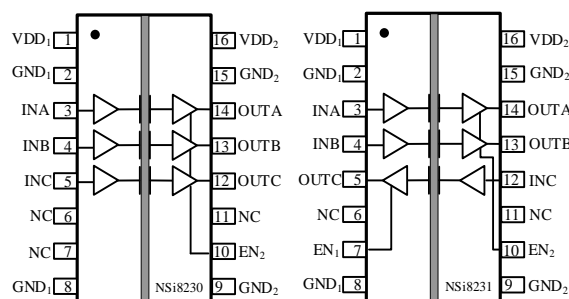


Figure 1. NSi823x Block Diagram

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1. Pin Configuration and Functions

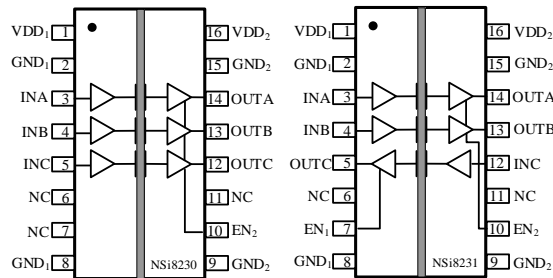


Figure 1.1 NSi8230W Package Figure 1.2 NSi8231W Package

Table 1.1 NSi8230W/ NSi8231W Pin Configuration and Description

NSi8230W PIN NO.	NSi8231W PIN NO.	SYMBOL	FUNCTION
1	1	VDD ₁	Power Supply for Isolator Side 1
2	2	GND ₁	Ground 1, the ground reference for Isolator Side 1
3	3	INA	Logic Input A
4	4	INB	Logic Input B
5	12	INC	Logic Input C
6	6	NC	No Connection.
7	7	NC/ EN ₁	No Connection. or Output Enable 1. Active high logic input. When EN ₁ is high or NC, the output of Side 1 is enabled. When EN ₁ is low, the output of Side 1 is disabled to high impedance state.
8	8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	9	GND ₂	Ground 2, the ground reference for Isolator Side 2
10	10	EN ₂	Output Enable 2. Active high logic input. When EN ₂ is high or NC, the output of Side 2 is enabled. When EN ₂ is low, the output of Side 2 is disabled to high impedance state.
11	11	NC	No Connection.
12	5	OUTC	Logic Output C
13	13	OUTB	Logic Output B
14	14	OUTA	Logic Output A
15	15	GND ₂	Ground 2, the ground reference for Isolator Side 2
16	16	VDD ₂	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB, VINC	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	VOUTA, VOUTB, VOUTC	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	VINA, VINB, VINC, VOUTA, VOUTB, VOUTC	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	I _o	-15		15	mA	
Maximum Surge Isolation Voltage	V _{IOSM}			6.25	kV	
Operating Temperature	T _{opr}	-55		125	°C	
Storage Temperature	T _{stg}	-55		150	°C	
Electrostatic discharge	HBM			±8000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	T _{opr}	-55		125	°C
High Level Input Voltage	V _{IH}	2			V
Low Level Input Voltage	V _{IL}			0.8	V
Data rate	DR			150	Mbps

4. Thermal Information

Parameters	Symbol	SOP16(300mil)	SOP16(600mil)	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	78.9	78.9	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC (top)}$	41.6	41.1	°C/W
Junction-to-board thermal resistance	θ_{JB}	43.6	49.5	°C/W

5. Specifications

5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD _{POR}		2.2		V	POR threshold as during power-up
	VDD _{HYS}		0.1		V	POR threshold Hysteresis
Input Threshold	V _{IT}		1.6		V	Input Threshold at rising edge
	V _{IT_HYS}		0.4		V	Input Threshold Hysteresis
High Level Input Voltage	V _{IH}	2			V	
Low Level Input Voltage	V _{IL}			0.8	V	
High Level Output Voltage	V _{OH}	VDD-0.4			V	I _{OH} = - 4mA
Low Level Output Voltage	V _{OL}			0.4	V	I _{OL} = 4mA
Output Impedance	R _{out}		50		ohm	
Input Pull high or low Current	I _{pull}		8	15	uA	
Start Up Time after POR	t _{rs}		10		us	
Common Mode Transient Immunity	CMTI	±200	±250		kV/us	See Figure 5.11 , C _L = 15pF

5.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ.	Max	Unit	Comments
Supply current	NSi8230					
	I _{DD1} (Q0)		1.24	2.04	mA	All Input 0V for NSi8230x0 Or All Input at supply for NSi8230x1
	I _{DD2} (Q0)		2.94	4.84	mA	
	I _{DD1} (Q1)		4.25	7.02	mA	All Input at supply for NSi8230x0 Or All Input 0V for NSi8230x1
	I _{DD2} (Q1)		3.00	4.95	mA	
	I _{DD1} (1M)		2.43	4.00	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		2.45	4.27	mA	
	I _{DD1} (10M)		2.92	4.82	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		3.06	5.99	mA	
	I _{DD1} (100M)		3.97	7.93	mA	All Input with 100Mbps, C _L =15pF
	I _{DD2} (100M)		12.47	29.28	mA	
	NSi8231					
	I _{DD1} (Q0)		1.66	2.74	mA	All Input 0V for NSi8231x0 Or All Input at supply for NSi8231x1
	I _{DD2} (Q0)		2.51	4.14	mA	
	I _{DD1} (Q1)		3.69	6.09	mA	All Input at supply for NSi8231x0 Or All Input 0V for NSi8231x1
	I _{DD2} (Q1)		3.56	5.87	mA	
	I _{DD1} (1M)		2.31	3.81	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		2.40	4.17	mA	
	I _{DD1} (10M)		2.75	4.53	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		3.40	5.61	mA	
I _{DD1} (100M)		6.69	13.38	mA	All Input with 100Mbps, C _L = 15pF	
I _{DD2} (100M)		12.47	24.94	mA		

5.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C)

Parameters	Symbol	Min	Typ.	Max	Unit	Comments
Supply current	NSi8230					
	I _{DD1} (Q0)		1.19	1.96	mA	All Input 0V for NSi8230x0 Or All Input at supply for NSi8230x1
	I _{DD2} (Q0)		2.87	4.74	mA	
	I _{DD1} (Q1)		4.20	6.93	mA	All Input at supply for NSi8230x0 Or All Input 0V for NSi8230x1
	I _{DD2} (Q1)		2.93	4.83	mA	
	I _{DD1} (1M)		2.38	3.92	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		2.37	4.14	mA	
	I _{DD1} (10M)		2.81	4.64	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.66	5.27	mA	
	I _{DD1} (100M)		3.30	6.59	mA	All Input with 100Mbps, C _L =15pF
	I _{DD2} (100M)		10.01	20.01	mA	
	NSi8231					
	I _{DD1} (Q0)		1.61	2.66	mA	All Input 0V for NSi8231x0 Or All Input at supply for NSi8231x1
	I _{DD2} (Q0)		2.45	4.04	mA	
	I _{DD1} (Q1)		3.64	6.00	mA	All Input at supply for NSi8231x0 Or All Input 0V for NSi8231x1
	I _{DD2} (Q1)		3.49	5.76	mA	
	I _{DD1} (1M)		2.25	3.71	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		2.34	4.06	mA	
	I _{DD1} (10M)		2.53	4.18	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		3.00	4.94	mA	
I _{DD1} (100M)		5.42	10.84	mA	All Input with 100Mbps, C _L = 15pF	
I _{DD2} (100M)		10.01	20.01	mA		

5.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C)

Parameters	Symbol	Min	Typ.	Max	Unit	Comments
Supply current	NSi8230					
	I _{DD1} (Q0)		1.17	1.92	mA	All Input 0V for NSi8230x0 Or All Input at supply for NSi8230x1
	I _{DD2} (Q0)		2.83	4.66	mA	
	I _{DD1} (Q1)		4.14	6.83	mA	All Input at supply for NSi8230x0 Or All Input 0V for NSi8230x1
	I _{DD2} (Q1)		2.87	4.74	mA	
	I _{DD1} (1M)		2.30	3.80	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		2.31	4.05	mA	
	I _{DD1} (10M)		2.70	4.46	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.46	4.90	mA	
	I _{DD1} (100M)		2.85	5.70	mA	All Input with 100Mbps, C _L =15pF
	I _{DD2} (100M)		8.22	16.44	mA	
	NSi8231					
	I _{DD1} (Q0)		1.58	2.61	mA	All Input 0V for NSi8231x0 Or All Input at supply for NSi8231x1
	I _{DD2} (Q0)		2.41	3.98	mA	
	I _{DD1} (Q1)		3.58	5.90	mA	All Input at supply for NSi8231x0 Or All Input 0V for NSi8231x1
	I _{DD2} (Q1)		3.43	5.67	mA	
	I _{DD1} (1M)		2.18	3.60	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		2.29	3.95	mA	
	I _{DD1} (10M)		2.39	3.95	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.80	4.61	mA	
I _{DD1} (100M)		4.53	9.05	mA	All Input with 100Mbps, C _L = 15pF	
I _{DD2} (100M)		8.22	16.44	mA		

5.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ.	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t _{PLH}	2.5	6.54	15	ns	See Figure 5.9 , C _L = 15pF
	t _{PHL}	2.5	8.30	15	ns	See Figure 5.9 , C _L = 15pF
Pulse Width Distortion t _{PHL} - t _{PLH}	PWD			5.0	ns	See Figure 5.9 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 5.9 , C _L = 15pF
Falling Time	t _f			5.0	ns	See Figure 5.9 , C _L = 15pF
Peak Eye Diagram Jitter	t _{JIT(PK)}		350		ps	
Channel-to-Channel Delay Skew	t _{SK(c2c)}			2.5	ns	
Part-to-Part Delay Skew	t _{SK(p2p)}			5.0	ns	
Disable high to Tri-State	t _{PHZ}		10.0	30	ns	See Figure 5.10 , C _L = 15pF, R _L =1k
Enable to Data high Valid	t _{PZH}		8.3	30	ns	See Figure 5.10 , C _L = 15pF, R _L =1k
Disable low to Tri-State	t _{PLZ}		10.2	30	ns	See Figure 5.10 , C _L = 15pF, R _L =1k
Enable to Data high Valid	t _{PZL}		8.6	30	ns	See Figure 5.10 , C _L = 15pF, R _L =1k

5.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t _{PLH}	2.5	7.5	15	ns	See Figure 5.9 , C _L = 15pF
	t _{PHL}	2.5	8.7	15	ns	See Figure 5.9 , C _L = 15pF
Pulse Width Distortion t _{PHL} - t _{PLH}	PWD			5.0	ns	See Figure 5.9 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 5.9 , C _L = 15pF

Falling Time	t_f			5.0	ns	See Figure 5.9 , $C_L = 15\text{pF}$
Peak Eye Diagram Jitter	$t_{\text{JIT}}(\text{PK})$		350		ps	
Channel-to-Channel Delay Skew	$t_{\text{sk}}(\text{c2c})$			2.5	ns	
Part-to-Part Delay Skew	$t_{\text{sk}}(\text{p2p})$			5.0	ns	
Disable high to Tri-State	t_{PHZ}		11.6	30	ns	See Figure 5.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$
Enable to Data high Valid	t_{PZH}		11.7	30	ns	See Figure 5.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$
Disable low to Tri-State	t_{PLZ}		14.5	30	ns	See Figure 5.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$
Enable to Data high Valid	t_{PZL}		11.8	30	ns	See Figure 5.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$

5.7. Switching Characteristics - 2.5V Supply

($V_{\text{DD1}}=2.5\text{V}\pm 10\%$, $V_{\text{DD2}}=2.5\text{V}\pm 10\%$, $T_a=-55^\circ\text{C}$ to 125°C . Unless otherwise noted, Typical values are at $V_{\text{DD1}} = 2.5\text{V}$, $V_{\text{DD2}} = 2.5\text{V}$, $T_a = 25^\circ\text{C}$)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	9.0	15	ns	See Figure 5.9 , $C_L = 15\text{pF}$
	t_{PHL}	2.5	9.3	15	ns	See Figure 5.9 , $C_L = 15\text{pF}$
Pulse Width Distortion $ t_{\text{PHL}} - t_{\text{PLH}} $	PWD			5.0	ns	See Figure 5.9 , $C_L = 15\text{pF}$
Rising Time	t_r			5.0	ns	See Figure 5.9 , $C_L = 15\text{pF}$
Falling Time	t_f			5.0	ns	See Figure 5.9 , $C_L = 15\text{pF}$
Peak Eye Diagram Jitter	$t_{\text{JIT}}(\text{PK})$		350		ps	
Channel-to-Channel Delay Skew	$t_{\text{sk}}(\text{c2c})$			2.5	ns	
Part-to-Part Delay Skew	$t_{\text{sk}}(\text{p2p})$			5.0	ns	
Disable high to Tri-State	t_{PHZ}		12.2	30	ns	See Figure 5.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$
Enable to Data high Valid	t_{PZH}		17.0	30	ns	See Figure 5.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$
Disable low to Tri-State	t_{PLZ}		17.2	30	ns	See Figure 5.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$
Enable to Data high Valid	t_{PZL}		17.8	30	ns	See Figure 5.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$

5.8. Typical Performance Characteristics

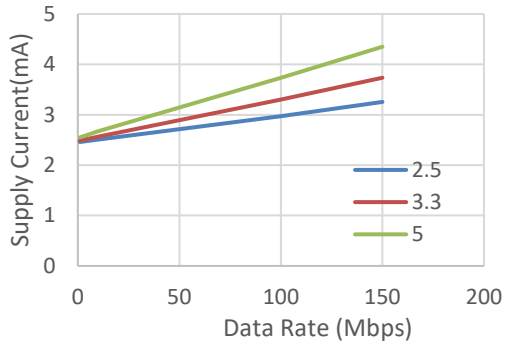


Figure 5.1 NSi8130 VDD1 Supply Current vs Data Rate

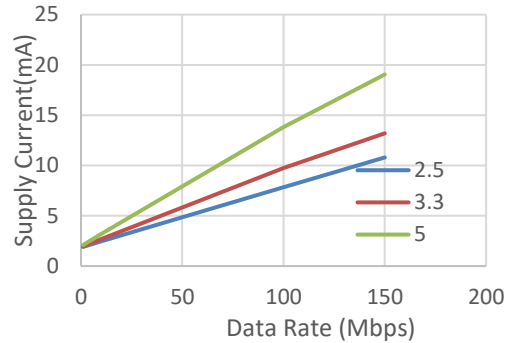


Figure 5.2 NSi8130 VDD2 Supply Current vs Data Rate

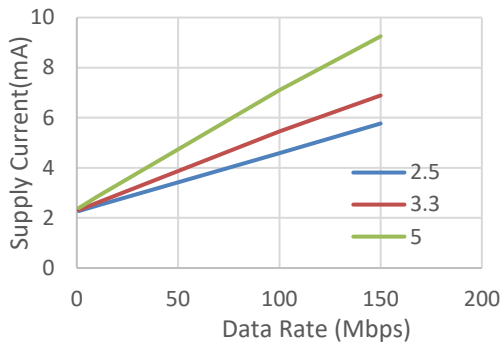


Figure 5.3 NSi8131 VDD1 Supply Current vs Data Rate

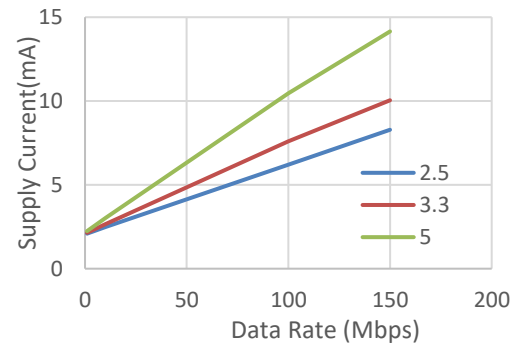


Figure 5.4 NSi8131 VDD2 Supply Current vs Data Rate

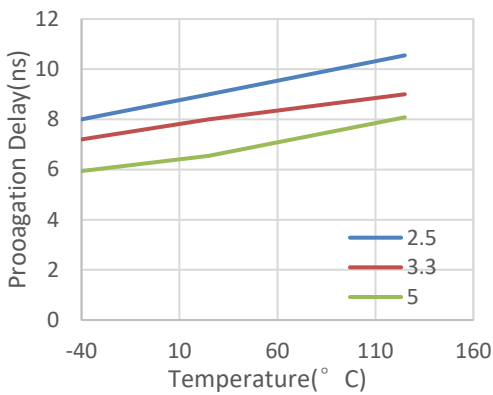


Figure 5.5 Rising Edge Propagation Delay Vs Temp

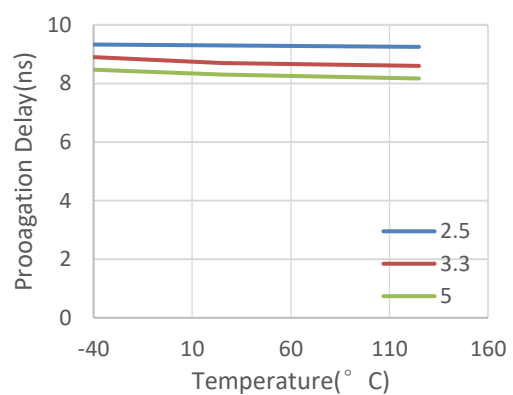


Figure 5.6 Falling Edge Propagation Delay Vs Temp

5.9. Parameter Measurement Information

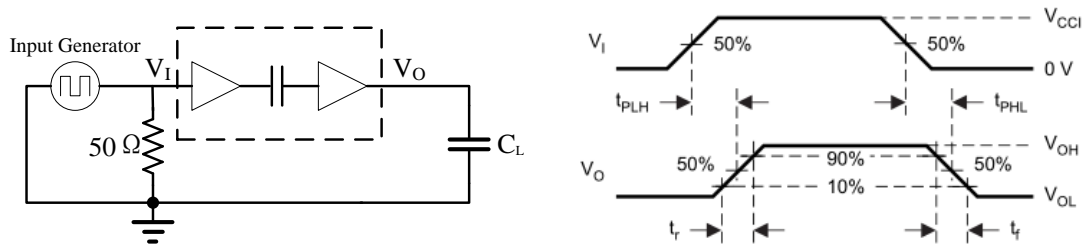


Figure 5.9 Switching Characteristics Test Circuit and Waveform

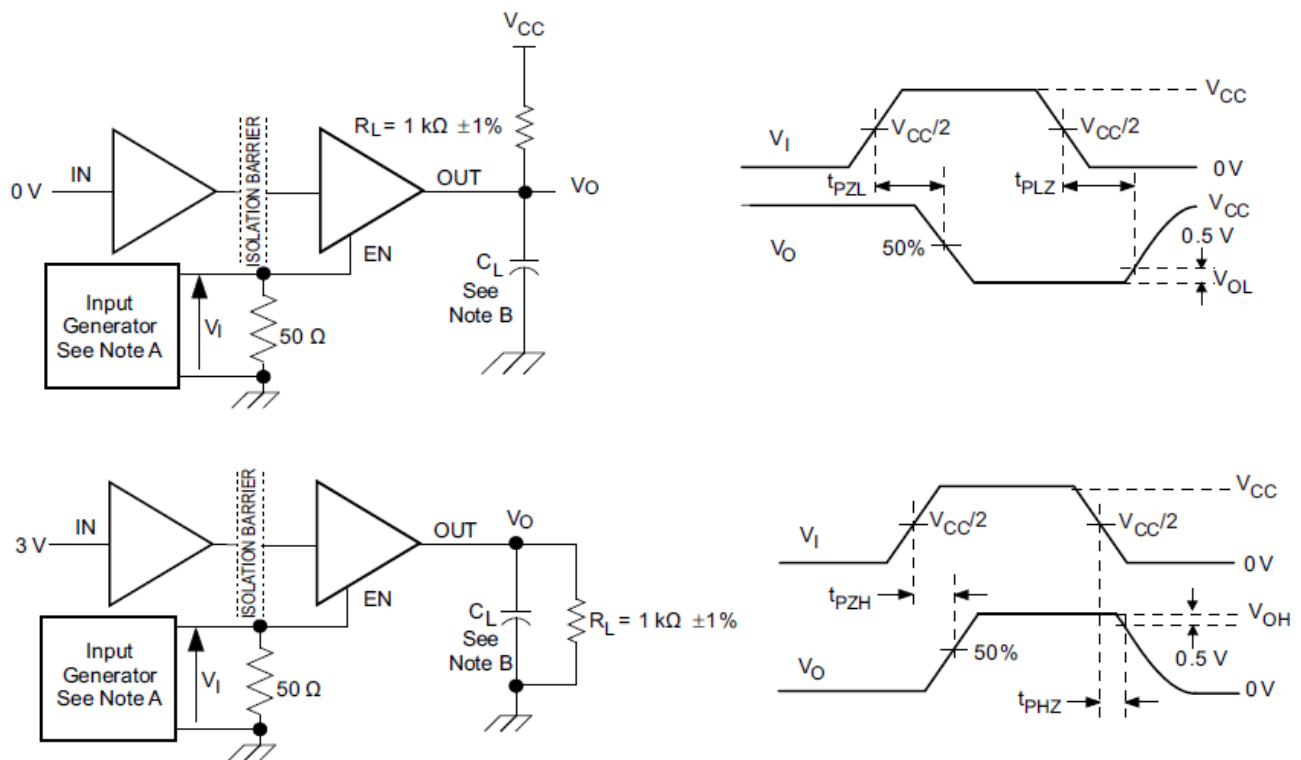


Figure 5.10 Enable/Disable Propagation Delay Time Test Circuit and Waveform

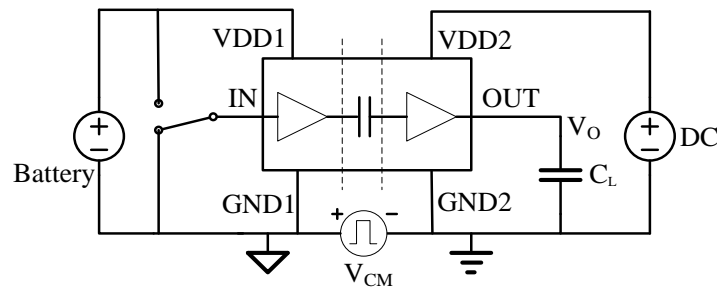


Figure 5.11 Common-Mode Transient Immunity Test Circuit

6. high voltage Feature Description

6.1. Insulation and Safety Related Specifications

Description	Test Condition	Symbol	Value		Unit
			SOP16 (300mil)	SOP16 (600mil)	
Min. External Air Gap (Clearance)		CLR	8	15	mm
Min. External Tracking (Creepage)		CPG	8	15	mm
Distance through the Insulation		DTI	32		um
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>600		V
Material Group	IEC 60112		I		
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage ≤ 150Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 600Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 1000Vrms			I to III	I to III	
Insulation Specification per DIN VDE V 0884-11:2017-01 ¹⁾					
Climatic Category			40/125/21		
Pollution Degree	per DIN VDE 0110, Table 1		2		
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1500	1500	V_{RMS}
	DC voltage		2121	2121	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	2121	2121	V_{peak}
Input to Output Test Voltage, Method B1	$V_{ini. b} = V_{IOTM}, V_{pd(m)} = V_{IORM} \times 1.875,$ $t_{ini} = t_m = 1 \text{ sec}, q_{pd} \leq 5 \text{ pC},$ 100% production test	$V_{pd(m)}$	3977	3977	V_{peak}
Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	$V_{ini. a} = V_{IOTM}, V_{pd(m)} = V_{IORM} \times 1.6,$ $t_{ini} = 60 \text{ sec}, t_m = 10 \text{ sec}, q_{pd} \leq 5 \text{ pC}$	$V_{pd(m)}$	3394	3394	V_{peak}
Input to Output Test Voltage, Method A. After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{ini. a} = V_{IOTM}, V_{pd(m)} = V_{IORM} \times 1.2,$	$V_{pd(m)}$	2545	2545	V_{peak}

Description	Test Condition	Symbol	Value		Unit
	$t_{ini} = 60 \text{ sec}, t_m = 10 \text{ sec}, q_{pd} \leq 5 \text{ pC}$				
Maximum Transient Isolation Voltage	$t = 60 \text{ sec}$	V_{IOTM}	8000	8000	V_{peak}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.6 \times V_{IOSM}$	V_{IOSM}	6250	6250	V_{peak}
Isolation Resistance	$V_{IO} = 500 \text{ V}, T_{amb} = T_S$	R_{IO}	$>10^9$		Ω
	$V_{IO} = 500 \text{ V}, 100 \text{ }^\circ\text{C} \leq T_{amb} \leq 125 \text{ }^\circ\text{C}$		$>10^{11}$		Ω
Isolation Capacitance	$f = 1\text{MHz}$	C_{IO}	1.2		pF
Insulation Specification per UL1577					
Withstand Isolation Voltage	$V_{TEST} = 1.2 \times V_{ISO}, t = 1 \text{ sec},$ 100% production test	V_{ISO}	5000	5700	V_{rms}

1) This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

6.2. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSI823x-DSWxR (SOP16(300mil)/SOP16(600mil))

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 78.9 \text{ }^\circ\text{C/W}^1$, $T_J = 150 \text{ }^\circ\text{C}$, $T_A = 25 \text{ }^\circ\text{C}$	1584	mW
Safety Supply Current	$R_{\theta JA} = 78.9 \text{ }^\circ\text{C/W}^1$, $V_I = 5\text{V}$, $T_J = 150 \text{ }^\circ\text{C}$, $T_A = 25 \text{ }^\circ\text{C}$	316.8	mA
Safety Temperature ²⁾		150	$^\circ\text{C}$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16(300mil)/SOP16(600mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

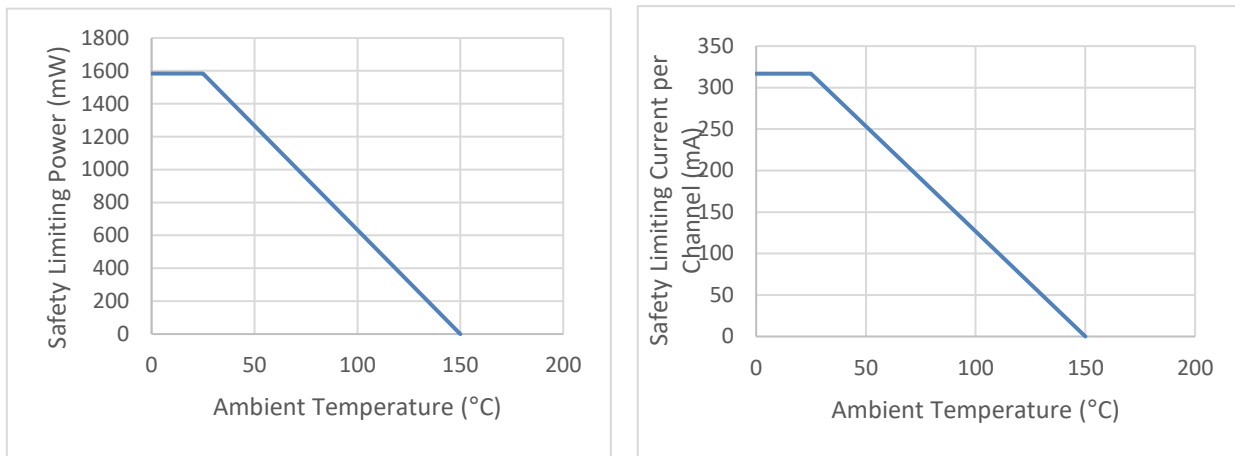


Figure 6.1 NSI823x Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Regulatory Information

The NSi823xW-DSWR are approved or pending approval by the organizations listed in table.

<i>CUL</i>		<i>VDE</i>	<i>CQC</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V _{rms} Isolation voltage	Single Protection, 5000V _{rms} Isolation voltage	Reinforce Insulation 2121Vpeak, V _{IOSM} =6250Vpeak	Reinforced insulation at 1500V _{RMS} (2121Vpeak)
File (E500602)	File (E500602)	File (40052820)	File (CQC20001264939)

The NSi823xW-DSWWR are approved or pending approval by the organizations listed in table.

<i>CUL</i>		<i>VDE</i>	<i>CQC</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5700V _{rms} Isolation voltage	Single Protection, 5700V _{rms} Isolation voltage	Reinforce Insulation 2121Vpeak, V _{IOSM} =6250Vpeak	Reinforced insulation at 1500V _{RMS} (2121Vpeak)
File (pending)	File (pending)	File (pending)	File (pending)

7. Function Description

7.1. Overview

The NSi823x is a Triple-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSi823x devices are high reliability Triple-channel digital isolator with AEC-Q100 qualified. The NSi823x device is safety certified by UL1577 support $5kV_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi823x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/us. The NSi823x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi823x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSi823x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 7.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A after powering up.

Table 7.1 Output status vs. power status

Input	EN_x	VDD1 status	VDD2 status	Output	Comment
H	H or NC	Ready	Ready	H	Normal operation.
L	H or NC	Ready	Ready	L	
X	L	Ready	Ready	Z	Output Disabled, the output is high impedance
X	H or NC	Unready	Ready	L(NSi823xW0) H(NSi823xW1)	The output follows the same status with the input after input side VDD is powered on.
X	L	Unready	Ready	Z	Output Disabled, the output is high impedance
X	X	Ready	Unready	X	The output follows the same status with the input after output side VDD2 is powered on.
Note: H=Logic high; L=Logic low; X=Logic low or logic high VDD1 is input side power; VDD2 is out side power.					

7.2. OOK Modulation

NSi823x is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Fig.1, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

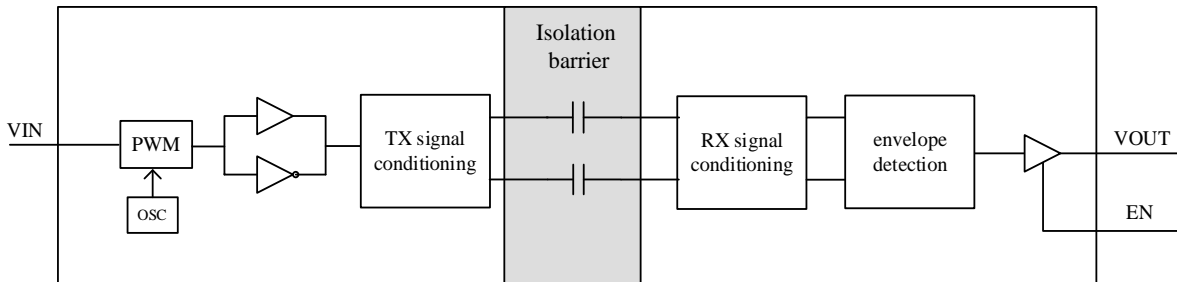


Figure 7.1 Single Channel Function Block Diagram

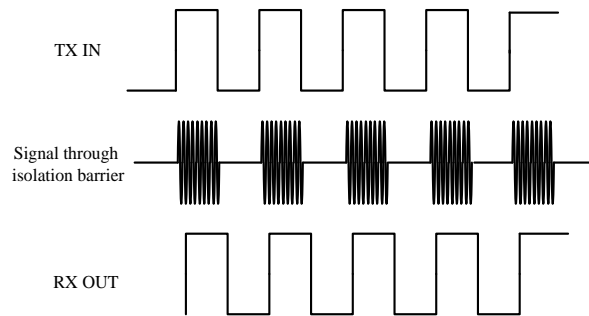


Figure 7.2 OOK Modulation

8. Application Note

8.1. Typical Application Circuit

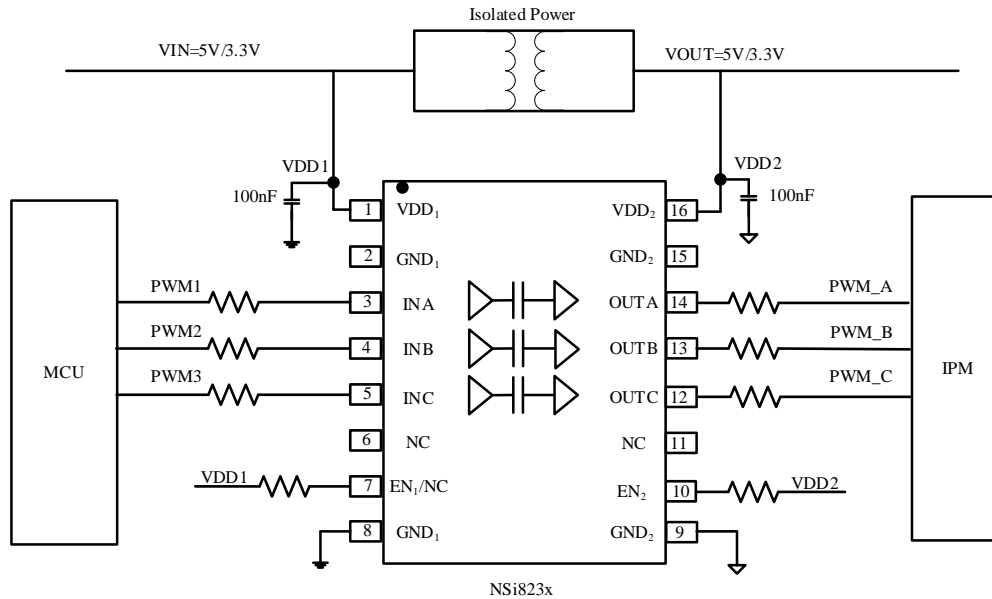


Figure 8.1 Typical PWM isolation circuit for IPM

8.2. PCB Layout

The NSi823x requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 8.2 to Figure 8.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω , $\pm 40\%$. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

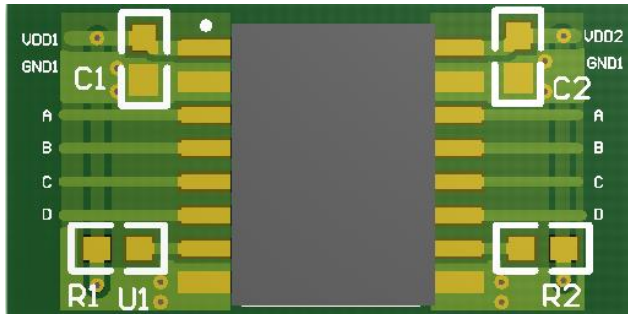


Figure8.2 Recommended PCB Layout — Top Layer

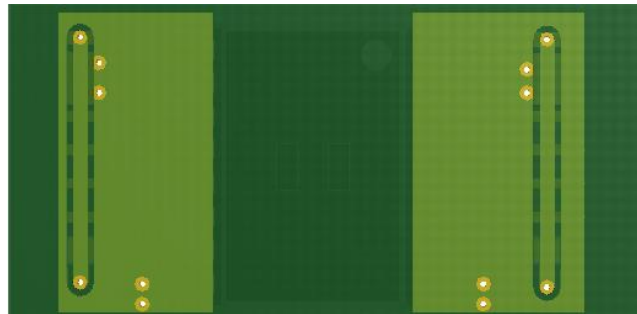


Figure8.3 Recommended PCB Layout — Bottom Layer

8.3. High Speed Performance

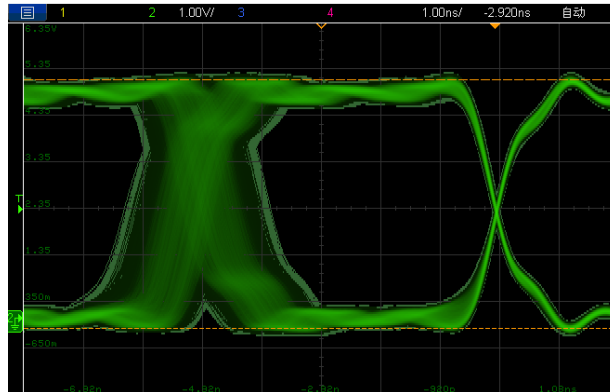


Figure8.4 Eye Diagram

8.4. Typical Supply Current Equations

The typical supply current of NSi823x can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF

NSi8230:

$$I_{DD1} = 0.19 * a1 + 1.45 * b1 + 0.82 * c1.$$

$$I_{DD2} = 1.36 + VDD1 * f * C_L * c1 * 10^{-9}$$

When $a1$ is the channel number of low input at side 1, $b1$ is the channel number of high input at side 1, $c1$ is the channel number of switch signal input at side 1.

NSi8231:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD1 * f * C_L * c1 * 10^{-9}$$

When $b1$ is the channel number of high input at side 1, $c1$ is the channel number of switch signal input at side 1, $b2$ is the channel number of high input at side 2, $c2$ is the channel number of switch signal input at side 2.

9. Package Information

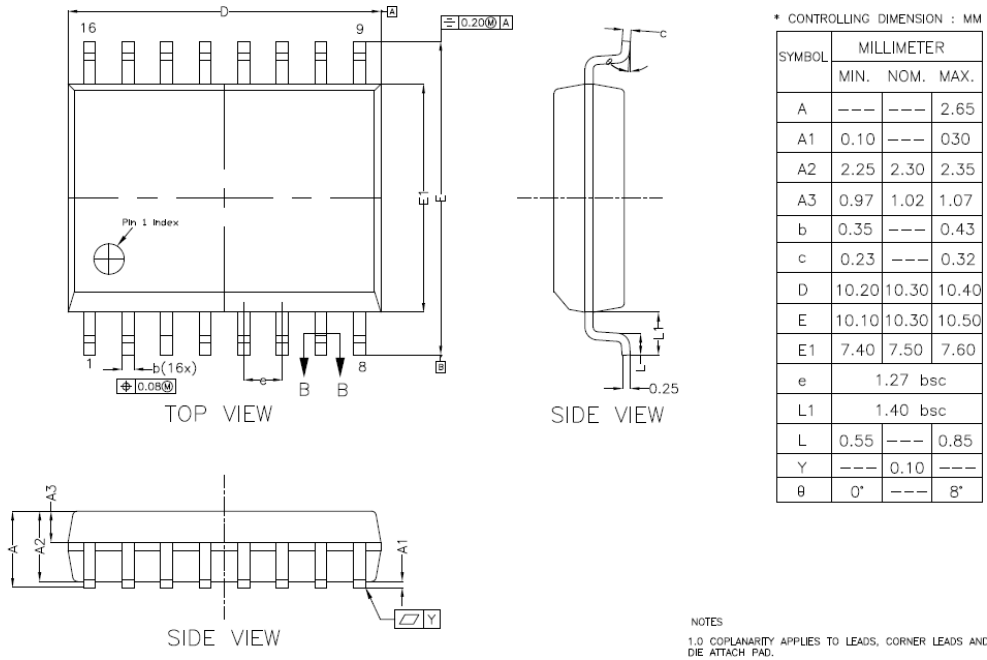


Figure 9.1 SOP16(300mil) Package Shape and Dimension in millimeters

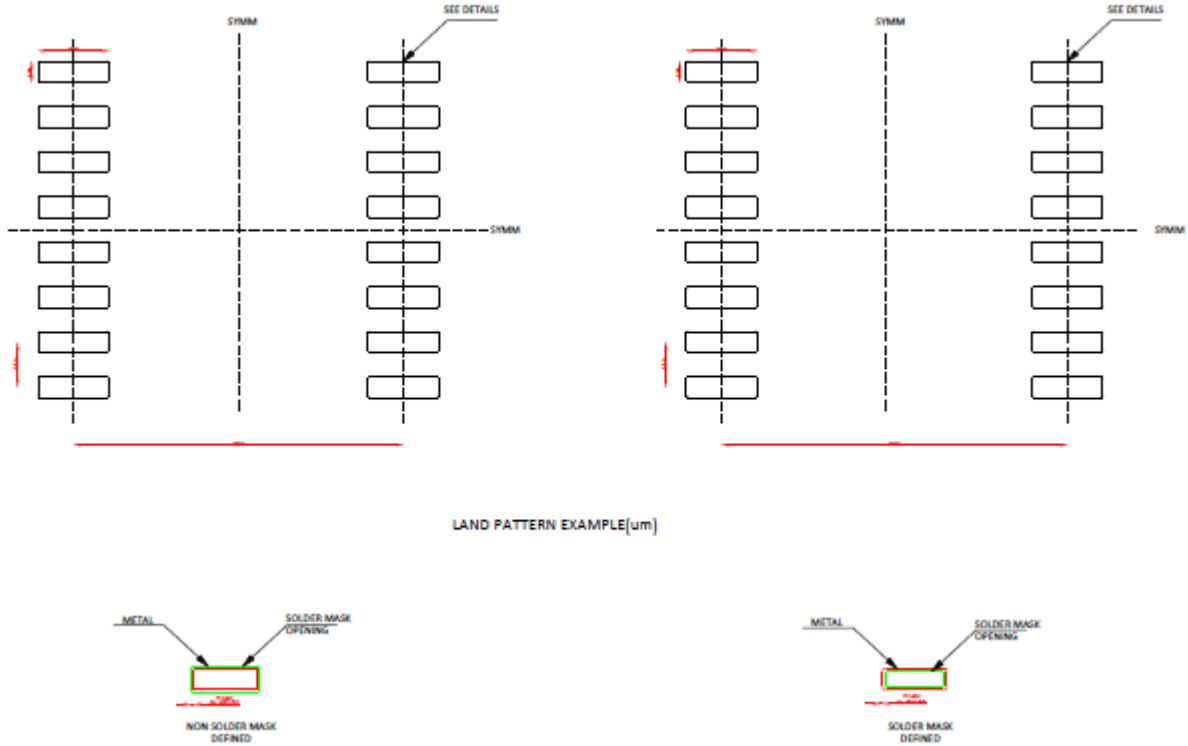


Figure 9.2 SOP16(300mil) Package Board Layout Example

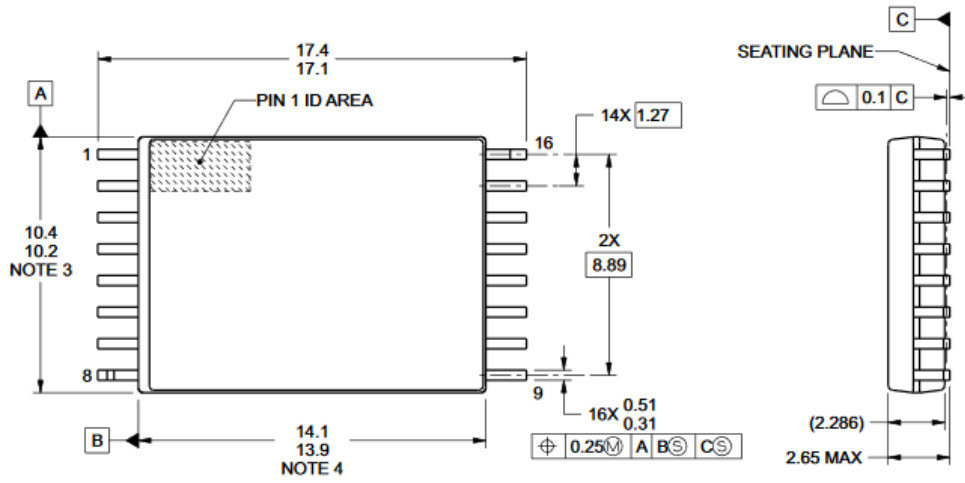


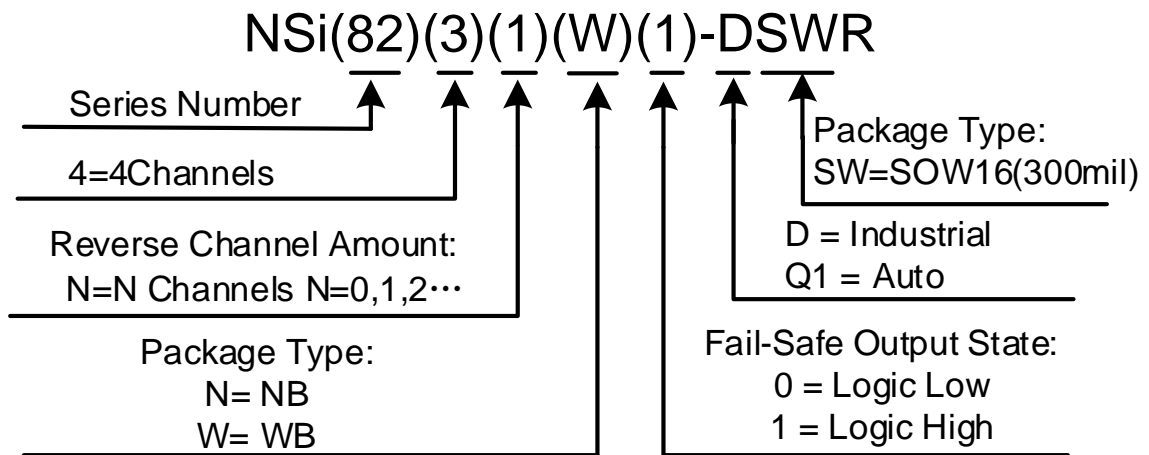
Figure 9.3 SOP16(600mil) Package Shape and Dimension in millimeters

10. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSi8230W0-DSWR	5	3	0	150	Low	-55 to 125 °C	2	SOP16 (300mil)	SOW16	1000
NSi8230W1-DSWR	5	3	0	150	High	-55 to 125 °C	2	SOP16 (300mil)	SOW16	1000
NSi8231W0-DSWR	5	2	1	150	Low	-55 to 125 °C	2	SOP16 (300mil)	SOW16	1000
NSi8231W1-DSWR	5	2	1	150	High	-55 to 125 °C	2	SOP16 (300mil)	SOW16	1000
NSi8230W0-DSWWR	5.7	3	0	150	Low	-55 to 125 °C	2	SOP16 (600mil)	SOWW16	1000
NSi8230W1-DSWWR	5.7	3	0	150	High	-55 to 125 °C	2	SOP16 (600mil)	SOWW16	1000
NSi8231W0-DSWWR	5.7	2	1	150	Low	-55 to 125 °C	2	SOP16 (600mil)	SOWW16	1000
NSi8231W1-DSWWR	5.7	2	1	150	High	-55 to 125 °C	2	SOP16 (600mil)	SOWW16	1000

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
All devices are AEC-Q100 qualified.

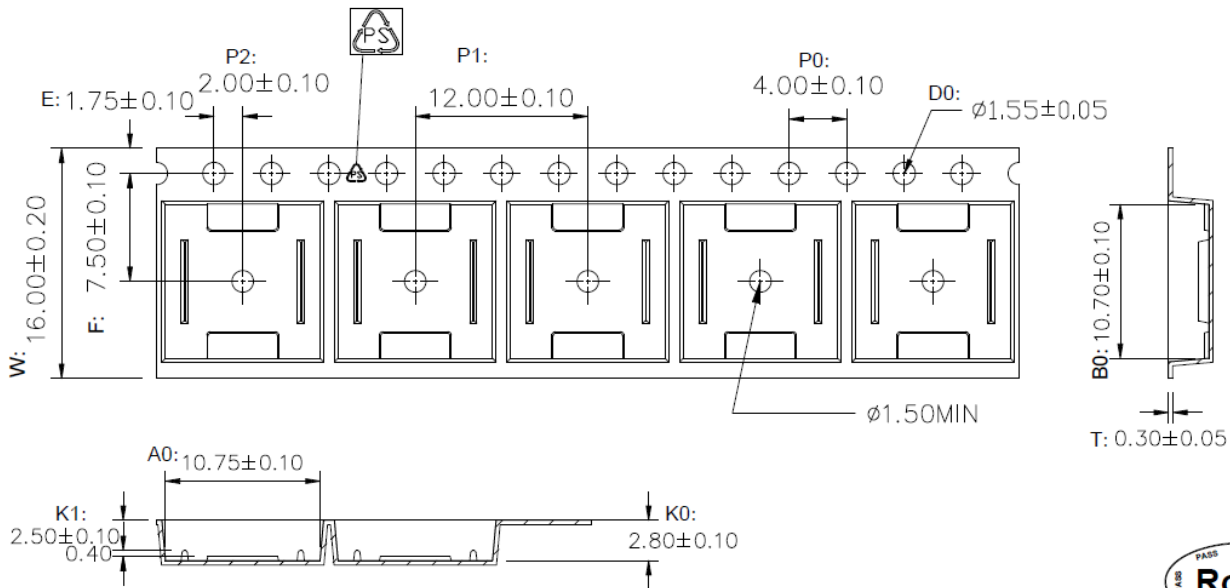
Part Number Rule:



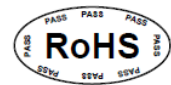
11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSi823x	Click here	Click here	Click here	Click here

12. Tape and Reel Information



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30 ± 0.05 mm.
6. Packing length per 22" reel : 378 Meters.(復卷 N=122)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : $10^5 \sim 10^{10} \Omega/\square$



W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

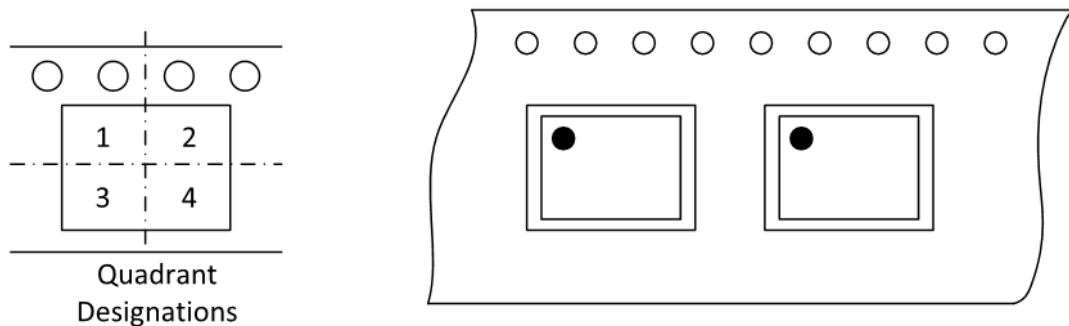


Figure 12.1 Tape and Reel Information of SOP16(300mil)

13. Revision history

Revision	Description	Date
1.0	Initial version	2020/11/20
1.1	Changed tape and reel information, changed format.	2021/2/4
1.2	Operating temperature support -55 to 125 °C	2021/7/7