裕太微电子
MotorComm

Motorcomm YT8618 Datasheet

INTEGRATED OCTAL 10/100/1000M ETHERNET TRANSCEIVER

VERSION V1.02

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Revision History

Revision	Release Date	Summary
v1.00	2021/02/01	Initial
v1.01	2021/06/23	1. Update RMS Jitter in section 7.4. 2. Add parameter L_{TX} in section 7.2.1. 3. Upadte R_Y2 and $V_{RX\text{-}DIFFp\text{-}p}$ in section 7.2.4. 4. Add section 7.2.5 and 7.2.6.
v1.02	2021/07/05	1. Add seciton 7.2.8. Serial LED Timing. 2. Modify mechanical dimensions in section 10.2. 3. Remove parameter t5 in section 8.3. 4. Remove peak to peak jitter in section 7.4.

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1. General Description

The YT8618 integrates octal independent 10/100/1000M Ethernet transceivers into a single IC, and performs all the physical layer (PHY) functions for 1000Base-T, 100Base-TX, and 10Base-Te Ethernet on category 5E UTP cable except 1000Base-T half-duplex. 10Base-Te functionality can also be achieved on standard category 3 or 4 cable.

This device includes PCS, PMA, and PMD sub-layers. They perform encoding/decoding, clock/data recovery, digital adaptive equalization, echo cancellers, crosstalk elimination, and line driver, as well as other required supporting circuit functions. The YT8618 also integrates an internal hybrid that allows the use of inexpensive 1:1 transformer modules.

Each of the four independent transceivers features an innovative QSGMII for reduced PCB trace.

1.1. TARGET APPLICATIONS

- High Port Density Switch
- QSGMII MAC

1.2. System Application

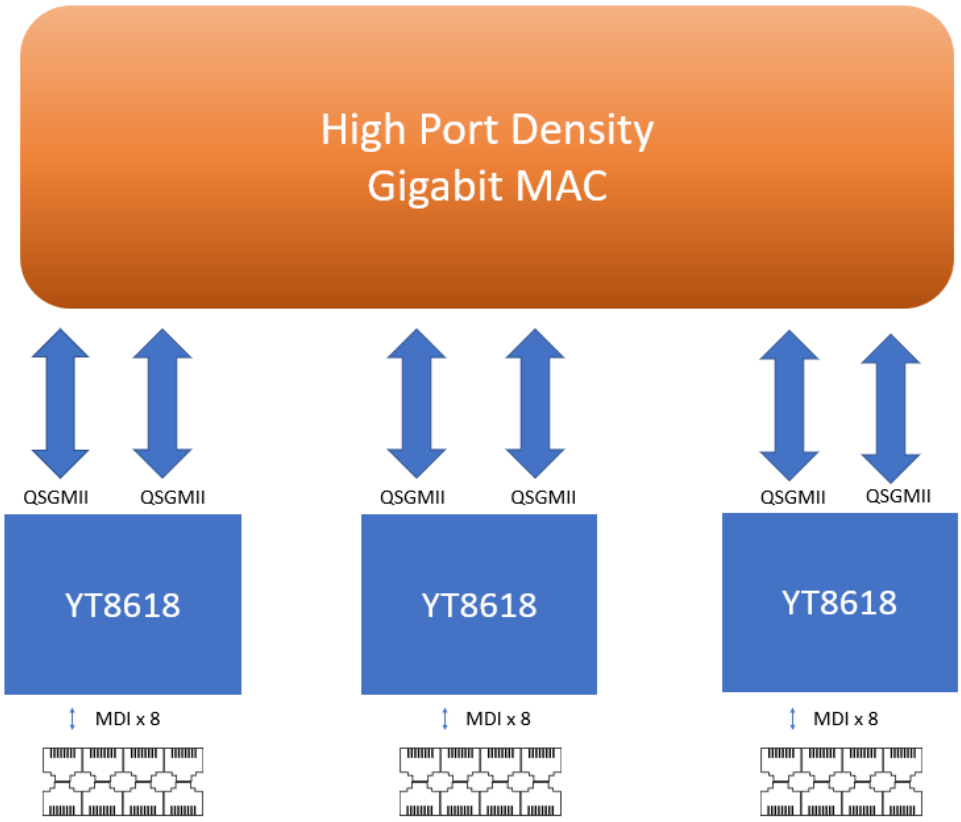


Figure 1. System Application

2. Features

- Octal-port integrated 10/100/1000M Ethernet transceiver
- Support QSGMII (Quad Serial Gigabit Media Independent Interface) in 10/100/1000M mode
- Support SGMII mode direct link to one designated Copper Giga PHY with speed adaption
- Support LRE100-4, disabled by default
  - Cable reach up to 400 meter @100Mbps
- Supports IEEE 802.3az-2010 (Energy Efficient Ethernet)
  - EEE Buffering
  - Incorporates EEE buffering for seamless support of legacy MACs
- Supports crossover detection and auto-correction
- Supports auto-detection and auto-correction of wiring pair swaps, pair skew, and pair polarity
- Supports Cable diagnostic
- Supports Link Down Power Saving (Sleep Mode)
- Supports one interrupt output to external CPU for notification
- Support fast link failure indication
- Supports 120m for CAT.5E cable in 1000BASE-T
- Support Serial LED interface
- Supports SyncE clock output Mux
  - Recover clock from either SerDes
  - Recover clock from either Copper PHY
  - From internal 25Mhz Clock
- SerDes Test pattern
  - PRBS-7/10/31
  - IDLE/K28.5/D5.6
  - Customized define by user
  - SerDes BIST
- Packet Generator and Checker
- Low power consumption
- Easy layout, good EMI/EMS, and good thermal performanc
- Supports 25MHz crystal or 3.3V OSC input
- 3.3V and 1.2V power supply
- LQPF 128 package

3. Pin assigment

3.1. YT8618 LQFP-128

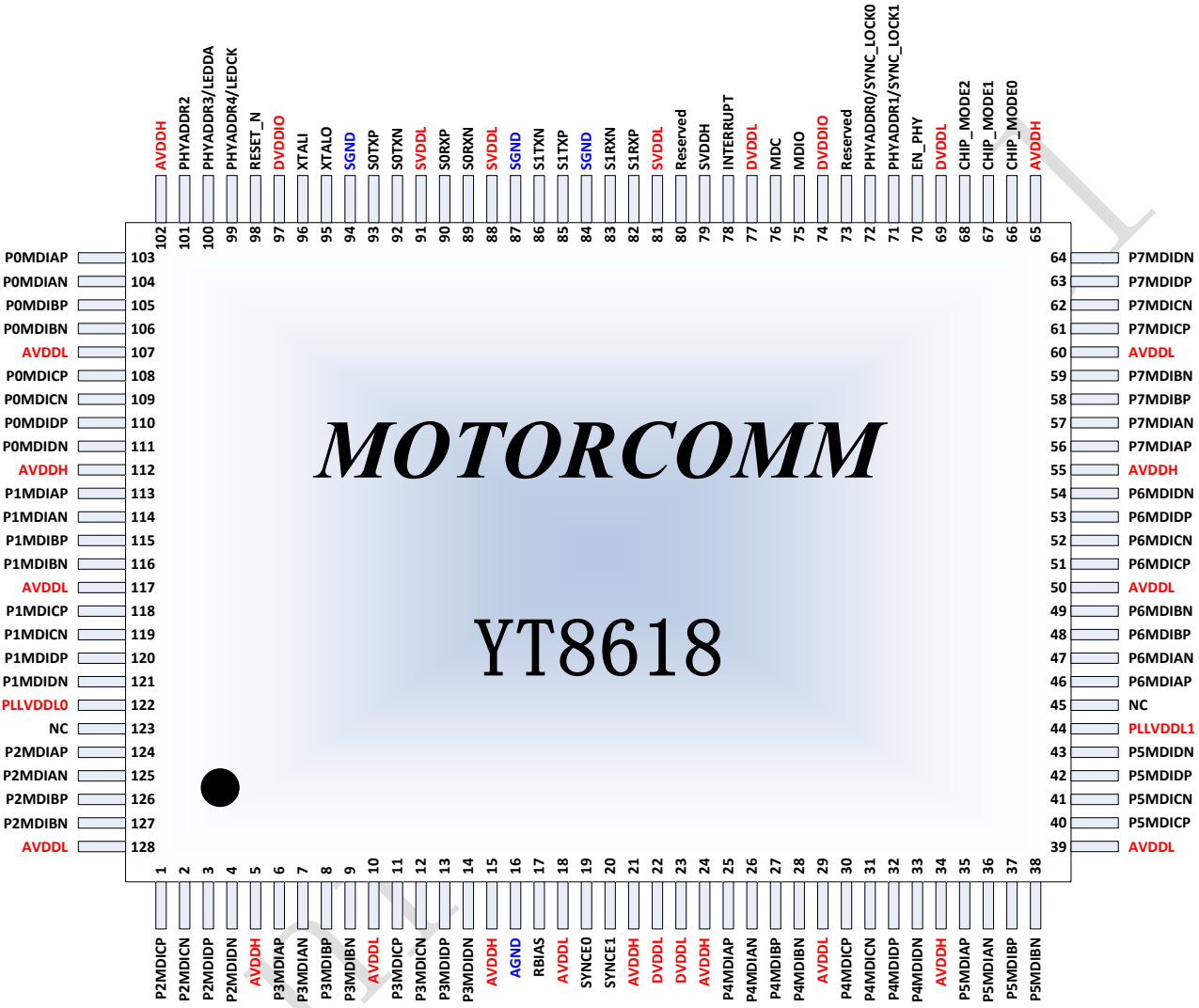


Figure 2. YT8618 Pin Assignment

3.2. Pin Descriptions

- I: Input Pin
- AI: Analog Input Pin
- O: Output Pin
- AO: Analog Output Pin
- IO: Bidirectional Input/Output Pin
- AIO: Analog Bidirectional Input/Output Pin
- LI: Latched Input During Power UP or Hardware Reset
- P: Digital Power Pin
- AP: Analog Power Pin
- A: Analog Pin
- G: Digital Ground Pin
- PD: Internal Pull-Down
- PU: Internal Pull-UP
- SP: SerDes Power
- SG: SerDes Ground
- OD: Open Drain
- XT: Crystal Related

3.2.1. All pins

Table 1. All Pins Description

No.	Pin Name	Type
1	P2MDICP	AIO
2	P2MDICN	AIO
3	P2MDIDP	AIO
4	P2MDIDN	AIO
5	AVDDH	AP
6	P3MDIAP	AIO
7	P3MDIAN	AIO
8	P3MDIBP	AIO
9	P3MDIBN	AIO
10	AVDDL	AP
11	P3MDICP	AIO
12	P3MDICN	AIO
13	P3MDIDP	AIO
14	P3MDIDN	AIO
15	AVDDH	AP
16	AGND	AG
17	RBIAS	AO
18	AVDDL	AP
19	SYNCE0	O/PD
20	SYNCE1	O/PD
21	AVDDH	AP
22	DVDDL	P
23	DVDDL	P
24	AVDDH	AP
25	P4MDIAP	AIO
26	P4MDIAN	AIO
27	P4MDIBP	AIO
28	P4MDIBN	AIO
29	AVDDL	AP
30	P4MDICP	AIO
31	P4MDICN	AIO
32	P4MDIDP	AIO
33	P4MDIDN	AIO
34	AVDDH	AP
35	P5MDIAP	AIO
36	P5MDIAN	AIO
37	P5MDIBP	AIO
38	P5MDIBN	AIO
39	AVDDL	AP
40	P5MDICP	AIO
41	P5MDICN	AIO
42	P5MDIDP	AIO
43	P5MDIDN	AIO
44	PLLVDDL1	AP
45	NC	-
46	P6MDIAP	AIO
47	P6MDIAN	AIO
48	P6MDIBP	AIO
49	P6MDIBN	AIO
50	AVDDL	AP
51	P6MDICP	AIO
52	P6MDICN	AIO
53	P6MDIDP	AIO
54	P6MDIDN	AIO
55	AVDDH	AP
56	P7MDIAP	AIO
57	P7MDIAN	AIO
58	P7MDIBP	AIO
59	P7MDIBN	AIO
60	AVDDL	AP
61	P7MDICP	AIO
62	P7MDICN	AIO
63	P7MDIDP	AIO
64	P7MDIDN	AIO
65	AVDDH	AP
66	CHIP_MODE0	LI/PU
67	CHIP_MODE1	LI/PU
68	CHIP_MODE2	LI/PU
69	DVDDL	P
70	EN_PHY	LI/PU
71	PHYADDR1/SYNC_LOCK1	LI/O/PD
72	PHYADDR0/SYNC_LOCK0	LI/O/PD

No.	Pin Name	Type
73	Reserved	IO/PD
74	DVDDIO	P
75	MDIO	IO/PU
76	MDC	IO/PD
77	DVDDL	P
78	INTERRUPT	O/OD
79	SVDDH	SP
80	Reserved	PD
81	SVDDL	SP
82	S1RXP	AO
83	S1RXN	AO
84	SGND	SG
85	S1TXP	AI
86	S1TXN	AI
87	SGND	SG
88	SVDDL	SP
89	S0RXN	AO
90	S0RXP	AO
91	SVDDL	SP
92	S0TXN	AI
93	S0TXP	AI
94	SGND	SG
95	XTALO	XT
96	XTALI	XT
97	DVDDIO	P
98	RESET_N	I/PU
99	PHYADDR4/LEDCK	LI/O/PD
100	PHYADDR3/LEDDA	LI/O/PD
101	PHYADDR2	LI/PD

No.	Pin Name	Type
102	AVDDH	AP
103	P0MDIAP	AIO
104	P0MDIAN	AIO
105	P0MDIBP	AIO
106	P0MDIBN	AIO
107	AVDDL	AP
108	P0MDICP	AIO
109	P0MDICN	AIO
110	P0MDIDP	AIO
111	P0MDIDN	AIO
112	AVDDH	AP
113	P1MDIAP	AIO
114	P1MDIAN	AIO
115	P1MDIBP	AIO
116	P1MDIBN	AIO
117	AVDDL	AP
118	P1MDICP	AIO
119	P1MDICN	AIO
120	P1MDIDP	AIO
121	P1MDIDN	AIO
122	PLLVDDL0	AP
123	NC	-
124	P2MDIAP	AIO
125	P2MDIAN	AIO
126	P2MDIBP	AIO
127	P2MDIBN	AIO
128	AVDDL	AP
EPAD	GND EPAD	G

3.2.2. Media Dependent Interface

Table 2. Media Dependent Interface

Pin Name	Pin No.	Type	Description
P0MDIAP	103	AIO	Port 0 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-Te operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P0MDIAN	104	AIO	
P0MDIBP	105	AIO	
P0MDIBN	106	AIO	
P0MDICP	108	AIO	
P0MDICN	109	AIO	
P0MDIDP	110	AIO	
P0MDIDN	111	AIO	
P1MDIAP	113	AIO	Port 1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-Te operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P1MDIAN	114	AIO	
P1MDIBP	115	AIO	
P1MDIBN	116	AIO	
P1MDICP	118	AIO	
P1MDICN	119	AIO	
P1MDIDP	120	AIO	
P1MDIDN	121	AIO	
P2MDIAP	124	AIO	Port 2 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-Te operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P2MDIAN	125	AIO	
P2MDIBP	126	AIO	
P2MDIBN	127	AIO	
P2MDICP	1	AIO	
P2MDICN	2	AIO	
P2MDIDP	3	AIO	
P2MDIDN	4	AIO	
P3MDIAP	6	AIO	Port 3 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-Te operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P3MDIAN	7	AIO	
P3MDIBP	8	AIO	
P3MDIBN	9	AIO	
P3MDICP	11	AIO	
P3MDICN	12	AIO	
P3MDIDP	13	AIO	
P3MDIDN	14	AIO	
P4MDIAP	25	AIO	Port 4 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-Te operation, only MDIAP/N and MDIBP/N are used. Auto
P4MDIAN	26	AIO	
P4MDIBP	27	AIO	
P4MDIBN	28	AIO	

P4MDICP	30	AIO	MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P4MDICN	31	AIO	
P4MDIDP	32	AIO	
P4MDIDN	33	AIO	
P5MDIAP	35	AIO	Port 5 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-Te operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P5MDIAN	36	AIO	
P5MDIBP	37	AIO	
P5MDIBN	38	AIO	
P5MDICP	40	AIO	
P5MDICN	41	AIO	
P5MDIDP	42	AIO	
P5MDIDN	43	AIO	
P6MDIAP	46	AIO	Port 6 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-Te operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P6MDIAN	47	AIO	
P6MDIBP	48	AIO	
P6MDIBN	49	AIO	
P6MDICP	51	AIO	
P6MDICN	52	AIO	
P6MDIDP	53	AIO	
P6MDIDN	54	AIO	
P7MDIAP	56	AIO	Port 7 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-Te operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P7MDIAN	57	AIO	
P7MDIBP	58	AIO	
P7MDIBN	59	AIO	
P7MDICP	61	AIO	
P7MDICN	62	AIO	
P7MDIDP	63	AIO	
P7MDIDN	64	AIO	

3.2.3. QSGMII Interface Pins

Table 3. QSGMII Interface Pins

Pin Name	Pin No.	Type	Description
S0RXP	90	AO	QSGMII Differential Output. 5GHz serial interfaces to transfer data to an External device that supports the QSGMII interface. Differential pairs have an internal 100ohm termination resistor.
S0RXN	89	AO	
S1RXP	82	AO	
S1RXN	83	AO	
S0TXP	93	AI	QSGMII Differential Input. 5GHz serial interfaces to receive data from an External device that supports the QSGMII interface. Differential pairs have an internal 100ohm termination resistor.
S0TXN	92	AI	
S1TXP	85	AI	
S1TXN	86	AI	

3.2.4. Serial LED Interface

Table 4. Serial LED Interface

Pin Name	Pin No.	Type	Description
PHYADDR4/LEDCK	99	LI/O/PD	Serial LED Clock Output
PHYADDR3/LEDDA	100	LI/O/PD	Serial LED Data Output

3.2.5. SYNCE Interface

Table 5. SYNCE Interface

Pin Name	Pin No.	Type	Description
SYNCE0	19	O/PD	SYNCE 0 clock output
SYNCE1	20	O/PD	SYNCE 1 clock output
PHYADDR0/SYNC_LOCK0	72	LI/O/PD	SyncE0 lock indicator
PHYADDR1/SYNC_LOCK1	71	LI/O/PD	SyncE1 lock indicator

3.2.6. Configuration

Table 6. Configuration

Pin Name	Pin No.	Type	Description
PHYADDR0/SYNC_LOCK0	72	LI/O/PD	PHYADDR0, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYADDR1/SYNC_LOCK1	71	LI/O/PD	PHYADDR1, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYADDR2	101	LI/PD	PHYADDR2, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYADDR3/LEDDA	100	LI/O/PD	PHYADDR3, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYADDR4/LEDCK	99	LI/O/PD	PHYADDR4, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
EN_PHY	70	LI/PU	Enable PHY Power 1: Power up all ports. 0: Power down all ports and set the MII register 0.11 power down as 1. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
CHIP_MODE2	68	LI/PU	CHIP MODE [2:0] refer to: 3'b000 or 3'b001: Reserved for feature useage; 3'b010: QSGMII x 1 and SGMII x 1 + Copper x 5 mode; 3'b011: SGMII x 2 + Copper x 2 mode; 3'b100 or 3'b101: QSGMII x 2 + Copper x 8 mode; 3'b110: SGMII x 1 + Combo x 1; 3'b111: QSGMII x 1 + Copper x 3 and Combo x 1;
CHIP_MODE1	67	LI/PU	
CHIP_MODE0	66	LI/PU	

3.2.7. Miscellaneous Interface

Table 7. Miscellaneous Interface

Pin Name	Pin No.	Type	Description
MDC	76	IO/PD	MII Management Interface Clock Input. The clock reference for the MII management interface. The maximum frequency support is 12.5MHz.
MDIO	75	IO/PU	MII Management Interface Data Input/Output. MDIO transfer management data in and out of the device synchronous to the rising edge of MDC.
INTERRUPT	78	O/OD	Interrupt output when Interrupt even occurs, active low. Always open drain, must pull-up to DVDDIO via a 4.7K resistor.
RESET_N	98	I/PU	Hardware Reset (Active Low Reset Signal). To complete the reset function, this pin must be asserted for at least 10ms. It must be pulled high for normal operation.
RBIAS	17	AO	MDI Bias Resistor. Adjusts the reference current for all PHYs. This pin must connect to AGND via a 2.49k ohm resistor.
XTALI	96	XT	25MHz Crystal Clock Input. 25MHz±50ppm tolerance crystal reference or oscillator input. When using a crystal, connect a loading capacitor from each pad to ground. When either using an oscillator or driving an external 25MHz clock from another device, XTALO should be kept floating. The maximum XTALI input voltage is 3.3V.
XTALO	95	XT	25MHz Crystal Clock Output. 25MHz±50ppm tolerance crystal output. Refer to XTALI.
Reserved	73	IO/PD	Reserved. Must be floating or tied to GND via a 1K resistor for normal operation
Reserved	80	PD	Internal pull down. Recommended to be floating or connected to GND directly.
NC	45, 123	-	-

3.2.8. Power and GND

Table 8. Power and GND

Pin Name	Pin No.	Type	Description
AVDDH	5, 15, 21, 24, 34, 55, 65, 102, 112	AP	Analog High Voltage Power
AVDDL	10,18,29.39,50,60, 107,117,128	AP	Analog Low Voltage Power
PLLVDDL0	122	AP	PLL Power This pin should be filtered with a low resistance series ferrite bead and 1000pF + 2.2μF shunt capacitors to ground
PLLVDDL1	44	AP	PLL Power This pin should be filtered with a low resistance series ferrite bead and 1000pF + 2.2μF shunt capacitors to ground
SVDDH	79	SP	QSGMII SerDes High Voltage Power
SVDDL	81,88,91	SP	QSGMII SerDes Low Voltage Power
DVDDIO	74,97	P	Digital I/O Power
DVDDL	22,23,69,77	P	Digital Low Voltage Power
AGND	16	AG	Analog Ground
SGND	84,87,94	SG	SerDes Ground
GND	EPAD	G	Digital/Analog Ground

4. Function Description

4.1. Mode selcetion

4.1.1. QSGMII x 2 + Copper x 8

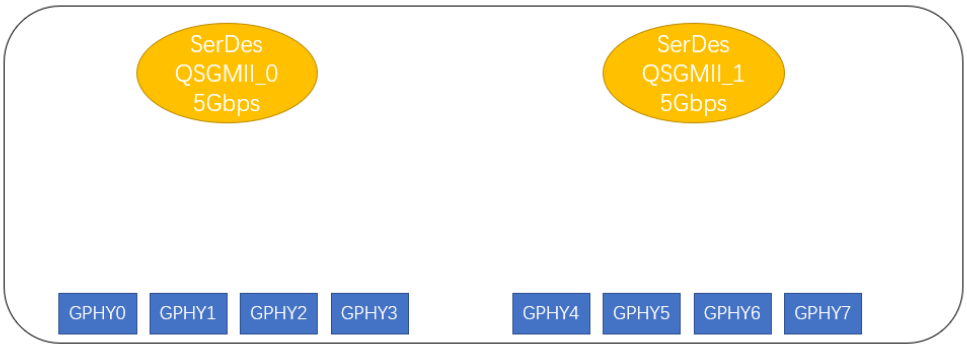


Figure 3. QSGMII x 2 + Copper x 8

4.1.2. QSGMII x 1 + SGMII x 1 + Copper x 5

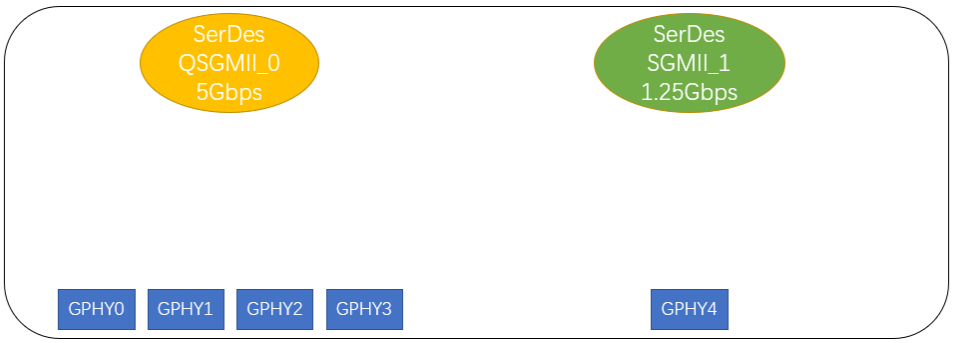


Figure 4. QSGMII x 1 + SGMII x 1 + Copper x 5

4.1.3. QSGMII x 1 + Copper x 3 + Combo x 1

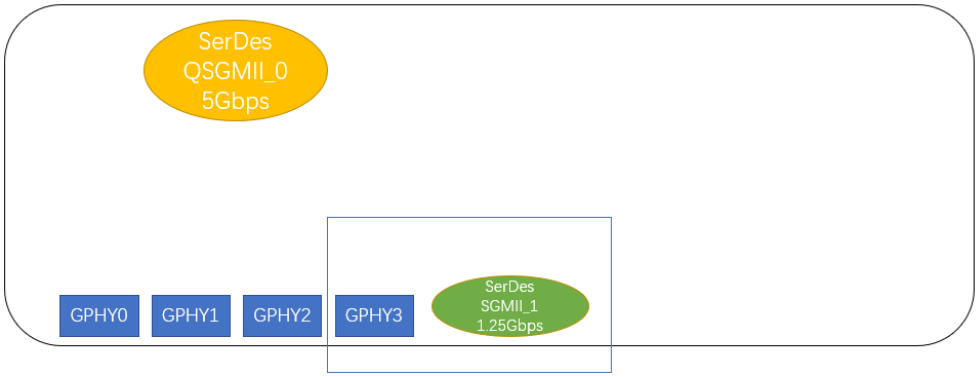


Figure 5. QSGMII x 1 + Copper x 3 + Combo x 1

4.1.4. SGMII x 2 + Copper x 2

Figure 6. SGMII x 2 + Copper x 2

4.1.5. SGMII x 1 + Combo x 1

Figure 7. SGMII x 1 + Combo x 1

4.2. Transmit Functions

4.2.1. Transmit Encoder Modes

4.2.1.1. 1000 BASE-T

In 1000 BASE-T mode, the YT8618 scrambles transmit data bytes from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT5 cable.

4.2.1.2. 100 BASE-TX

In 100 BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.

4.2.1.3. 10 BASE-Te

In 10 BASE-Te mode, the YT8618 transmits and receives Manchester-encoded data.

4.3. Receive Functions

4.3.1. Receive Decoder Modes

4.3.1.1. 1000 BASE-T

In 1000 BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately and data is output to the MAC interfaces.

4.3.1.2. 100 BASE-TX

In 100 BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/ 4B decoded to 4-bit data. This output runs to the MII receive data pins after data stream delimiters have been translated.

4.3.1.3. 10 BASE-Te

In 10 BASE-Te mode, the recovered 10 BASE-Te signal is decoded from Manchester then aligned.

4.4. LRE100-4

LRE100-4 is the Motorcomm proprietary mode in Long Reach Ethenet (LRE) application up to 400m in 100M mode by 4 pairs.

4.5. Management Interface

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and 45 and also support MDC clock rates up to 12.5 MHz.

4.6. Auto-Negoitation

The YT8618 negotiates its operation mode using the auto negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto negotiation supports choosing the mode of operation automatically by comparing its own abilities and received abilities from link partner. The advertised abilities include:

a) Speed: 10/100/1000Mbps

b) Duplex mode: full duplex and/or half duplex

Auto negotiation is initialized when the following scenarios happen:

a) Power-up/Hardware/Software reset

b) Auto negotiation restart

c) Transition from power-down to power up

d) Link down

Auto negotiation is enabled for YT8618 by default, and can be disabled by hardware or software control.

4.7. LDS (Link discovey signaling)

YT8618 supports Long Range Ethernet (LRE), which uses link discovery signaling (LDS) instead of auto negotiation since the extended cable reach attenuates the auto negotiation link pulses. LDS is an extended reach signaling scheme and protocol, which is used to

a) Master/Slave assignment

b) Estimate cable length

c) Confirm pair number and pair connectivity ordering

d) Choose highest common operation mode

IEEE-compliant PHYs will ignore LDS signal since its frequency is less than 2MHz according to IEEE802.3 clause 14. If the link partner is an IEEE legacy Ethernet PHY, YT8618 can detect the standard NLP, FLP, MLT-3 IDLE signal, or 100BASE-T4 signal, and then transits LDS mode into Clause 28 auto negotiation mode. If the link partner is an IEEE automotive ethernet PHY, YT8618 can also detect link partner’s master/slave mode, and configure itself as an opposite master/slave mode.

Forcing pair number and speed mode is also supported. The same forcing must be done at both ends of the link.

4.8. Polarity detection and auto correction

YT8618 can detect and correct two types of cable errors: swapping of pairs within the UTP cable (swapping between pair 0 and pair 1, and(or) swapping between pair 2 and pair 3) and swapping of wires within a pair.

4.9. Energy Efficient Ethernet (EEE)

EEE is IEEE 802.3az, an extension of the IEEE 802.3 standard. EEE defines support for the PHY to operate in Low Power Idle (LPI) mode which, when enabled, supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY's circuitry and save power.

4.10. Synchronous Ethernet (Sync-E)

YT8618 provides Synchronous Ethernet (Sync-E) support, and two Sync-E clock can output from SYNCE0 (pin 19) or SYNCE1 (pin 20). The Sync-E clock sources can be configured to recovery from UTP0~7 or SDS0~1 respectively. When SYNCE0 lock, the SYNC_LOCK0 (pin 70) will be high if its extenal pull down, and be low if its external pull up; When SYNCE1 lock, the SYNC_LOCK1 (pin 71) will be high if its extenal pull down, and be low if its external pull up.

The recovery clock for Sync-E can be either a 125MHz, 31.25MHz or 25MHz clock.

When the PHY is in SLAVE mode, the CLKOUT will output the recoverd clock from the MDI. If the device is in MASTER mode, the CLKOUT will output the clock based on the local free run PLL.

It's also configurable to output the 25MHz referece clock via SYNCE0 and(or) SYNCE1 pin.

4.11. Link Down Power Saving (Sleep Mode)

YT8618 supports link down power saving, also called sleep mode. When UTP port link down and no signals over UTP cable for 40 seconds, YT8618 will enter sleep mode.

For most of time in sleep mode, YT8618 will disable almost all the circuits except crystal clock and comparators for channel 0/1 of 10BASE-Te. Access by MDC/MDIO interface is available.

At a time interval in sleep mode, YT8618 will wake to transmit signals over TRXP1/TRXN1. The time interval is a random value around 2.7s.

Once detect signals over UTP cable, YT8618 will exit sleep mode.

4.12. Interrupt

YT8618 provides an active low interrupt output pin (INT_N) based on change of the PHY status. Every interrupt condition is represented by the read-only general interrupt status register (section 6.2.18. Interrupt Status Register (UTP MII register 0x13) , EXT_0xA011, EXT_0xA013 and EXT_0xA015).

The interrupts can be individually enable or disable by setting or clearing bits in the interrupt enable register (section 6.2.17. Interrupt Mask Register (UTP MII register 0x12) , EXT_0xA010, EXT_0xA012 and EXT_0xA014).

Note 1: The interrupt of the YT8618 is a level-triggered mechanism.

Note 2: The interrupt output pin (INT_N) is open drain mode, and must pull-up to DVDDIO via a 4.7K resistor.

5. Operational Description

5.1. Reset

YT8618 has a hardware reset pin(RESET_N) which is low active. RESET_N should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up.

RESET_N is also used as enable for power on strapping. During RESET_N is active, YT8618 latches input values on strappings which are used as configuration information to provide flexibility in application without MDIO access.

YT8618 also provides three kinds of software reset control registers. Two of them are in each UTP port and are used to reset this UTP port's internal logic except some mdio configuration registers, by setting bit 15 of UTP mii register (address 0x0) or LDS mii register (address 0x0). And the third is in each QSGMII/SGMII channel and is used to reset this QSGMII/SGMII channel's internal logic except CDR and some mdio configuration registers, by setting bit15 of SerDes mii register(address 0x0) to 1. These three bits are self-clear after reset process is done.

For detailed information about what register will be reset by software reset, please refer to register table.

Table 9. Reset Timing Characteristics

Symbol	Description	Min	Typ	Max	Units
T1	The duration from all powers steady to reset signal release to high	10	-	-	ms
T2	The duration of reset signal remain low timing	10	-	-	ms

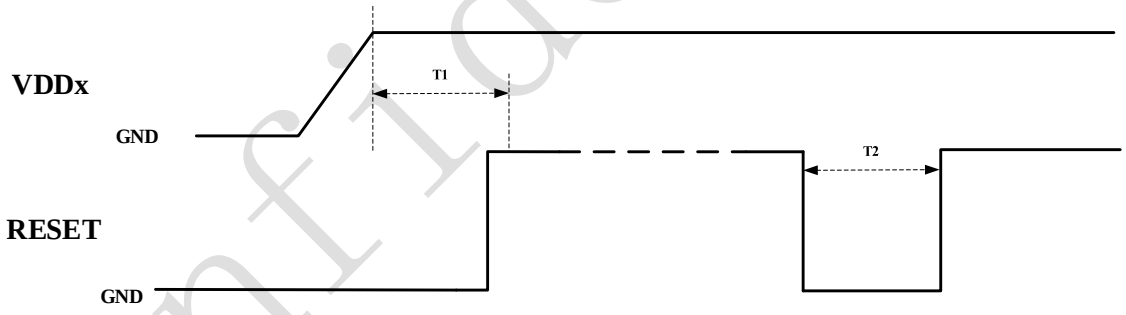


Figure 8. Reset Timing Diagram

5.2. PHY Address

For YT8618, Strapping PHYADDR[4:0] is used to generate phy address for port 0. The other port's phy address is the sum of the PHYADDR [4:0] and port number. For example, if PHYADDR [4:0] = 8, the phy address of port 3 is 11 (the sum of 8 and 3).

5.3. Loopback mode

There are three loopback modes in YT8618.

5.3.1. Digital Loopback

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the YT8618 device.

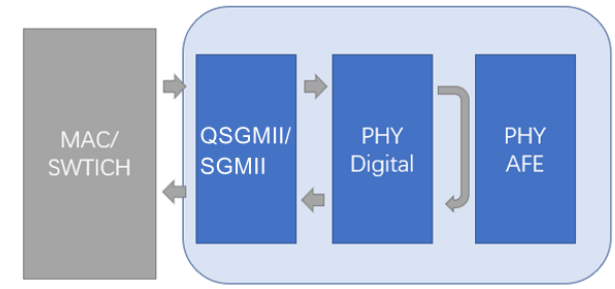


Figure 9. Digital Loopback

5.3.2. External Loopback

External cable loopback loops Tx to Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. Figure shows a block diagram of external cable loopback.

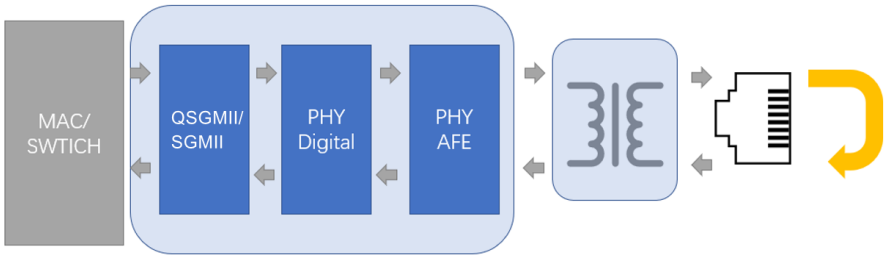


Figure 10. External Loopback

5.3.3. Remote PHY Loopback

The Remote loopback connects the MDI receive path to the MDI transmit path, near the GMII interface, thus the remote link partner can detect the connectivity in the resulting loop. Figure below, shows the path of the remote loopback.

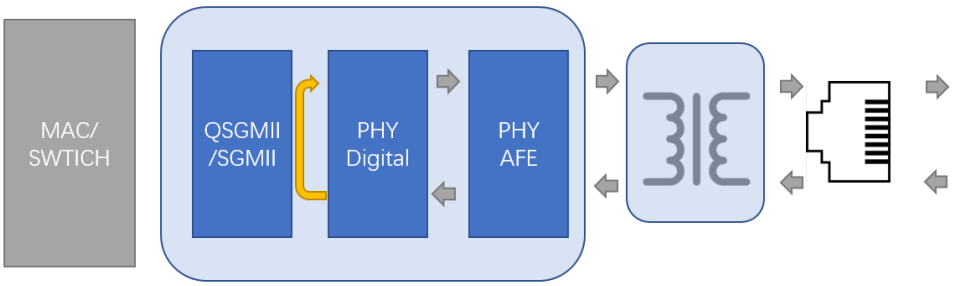


Figure 11. Remote PHY Loopback

5.4. LED

The YT8618 supports serial LED mode. In the serial LED mode, the data is clocked through a shift register and the shifted symbols are output to the 36 LED pins.

Each MDI port has three indicator symbols and each fiber port has three indicator symbols. Each symbol may have different indicator.

You can find more information from *YT8618 application note*.

5.5. Power Supplies

YT8618 requires external power supply 3.3 V and 1.2V. Please refer to *section 8. Power Requirements* for more information.

6. Register Overview

6.1. Common Register

6.1.1. SMI Mux (0xA000)

Table 10. SMI Mux (0xA000)

Bit	Symbol	Access	Default	Description
15:13	Reserved	RO	0x0	Reserved
12:8	MDIO_PHYAD	RO	0x0	the PHYAD field in current MDIO command
7:5	Reserved	RO	0x0	Reserved
4	en_brdst_phy	RW	0x0	When bit1 smi_sds_phy is 0, this bit controls to broadcast write to all PHYs. 0: disable. 1: enable broadcast write.
3	en_brdst_q	RW	0x0	When bit1 smi_sds_phy is 1, this bit controls to broadcast write to all QSGMII channels. 0: disable. 1: enable broadcast write;.
2	en_brdst_sf	RW	0x0	User should not set this register in YT8618.
1	Smi_sds_phy	RW	0x0	To control access whether phy register or sds register. 0: to access phy. 1: to access sds.
0	smi_sf	RW	0x0	User should not set this register in YT8618.

6.1.2. SLED cfg0 (0xA001)

Table . SLED cfg0 (0xA001)

Bit	Symbol	Access	Default	Description
15	led_manu_en	RW	0x0	to control serial LEDs status manually. 1: enable; 0: disable, SLED are controled by internal status then.
14:12	led_manu_st	RW	0x0	SLEDs' manul status, corresponding to each port's 3 SLEDs.
11	led_act_low	RW	0x1	control SLED's polarity. 1: active low; 0: active high.

10:8	led_bit_mask	RW	0x7	The thress mask bit for the three LED pins of each port: 1’b1: enable the pin output; 1’b0: disable pin output.
7:0	led_en_ctrl	RW	0xFF	Control to enable the eight ports' SLED: 1’b1: enable serial led output for this port; 1’b0: disable serial led output for this port.

6.1.3. SLED cfg (0xA004)

Table 11. SLED cfg (0xA004)

Bit	Symbol	Access	Default	Description
15:10	Reserved	RO	0x0	Always 0.
9	led_lsb	RW	0x1	control the SLED order; 1: LED00 first and LED35 last; 0: LED35 first and LED00 last.
8	led_seri_dis	RW	0x0	1: to disable the SLED function; 0: normal mode. See ext.A007.4 for detail.
7	led_clk_en	RW	0x1	1: enable SLED clock to output to SLED_CK pin; 0: disable SLED clock output and drive 0 on SLED_CK pin.
6	led_data_en	RW	0x1	1: enable SLED data to output to SLED_DA pin; 0: disable SLED data output and drive 0 on SLED_DA pin.
5:4	led_mode	RW	0x3	Control each port's LED indicator symbol number and the information it indicates. 2’b00, each port has one LED indicator symbols, {1st led}, to indicates: MDI: [link/act] FIBER: [link/act] 2’b01, each port has 2 LED indicator symbols, {1st led, 2nd led}, to indicate: MDI: [speed1000/act] [speed100(10)/act] FIBER: [speed1000/act] [speed100/act] 2’b10, each port has 3 LED indicator symbols, {1st led, 2nd led, 3rd led}, to indicate: MDI: [speed1000/act] [speed100/act] [speed10/act] FIBER: [speed1000/act] [speed100/act] [Disable] 2’b11, each port has 3 LED indicator symbols, {1st led, 2nd led, 3rd led}, to indicate: MDI: [link/act] [speed1000] [speed100] FIBER: [link/act] [speed1000] [speed100]

3:2	led_burst_cycle	RW	0x2	Serial led burst cycle. SLED status will be updated when the timer is done. 2'b00: 8ms 2'b01: 16ms 2'b10: 32ms 2'b11: 64ms
1:0	led_clk_cycle	RW	0x1	Serial led clock cycle: 2'b00: 80ns 2'b01: 160ns 2'b10: 240ns 2'b11: 320ns

6.1.4. mode_chg_reset (0xA005)

Table 12. mode_chg_reset (0xA005)

Bit	Symbol	Access	Default	Description
15	mode_chg_reset	RW SC	0x0	This bit will asserts when ext.a007.12 en_phy or ext.a007.3:0 changes. When this bit asserts, whole chip will be reset except MDIO configuration registers. This bit is self-cleared.
14	en_manu_porten	RW	0x0	1: enable to control *_port_en in EXT 0xA00F manually; 0: *_port_en in EXT 0xA00F is controled by chip_mode.
13	Reserved	RW	0x0	Reserved
12	iddq_mode_reg	RW	0x0	1: control to enter IDDQ mode.
11	Reserved	RW	0x0	Reserved
10	Bypass_mdio_watchdog	RW	0x0	1: bypass mdio watch dog
9:0	Reserved	RO	0x80	Reserved

6.1.5. chip_mode (0xA007)

Table 13. chip_mode (0xA007)

Bit	Symbol	Access	Default	Description
15:13	package_id	RO	0x7	The package_id for YT8618.
12	en_phy	RW POS	0x1	1: enable all the coppers port and serdes ports; 0: disable all the copper ports and serdes ports. The strapping of EN_PHY will power down all the copper ports; and the strapping value will be recorded in this register. But writing this register to 1 will not power down copper ports, but only generates a whole chip reset, (refer to EXT 0xA005 bit[15]).
11:6	reserved	RO	0x0	always 0.

5	Reserved	RW	0x0	Reserved
4	dis_sled	RW	0x0	1: to disable SLED PINs SCL/SDA; 0: to enable SLED PINs SCL/SDA. To disable SLED, ext.A004.8 shall be set to 1 first, then set this register to 1. SLEDs may behave abnormally if set this register to 1 before set EXT 0xA004 bit [8] to 1.
3:0	chip_mode	RW POS	0x7	4'b0000 Reserved for feature useage 4'b0001 Reserved for feature useage 4'b0010, Qsgmii x1 and Sgmii x1 + Copper x5 mode; 4'b0011, Sgmii x2 + Copper x2 mode; 4'b0100, Qsgmii x2 + Copper x8 mode; 4'b0101, Qsgmii x2 + Copper x8 mode; 4'b0110, SGMII x1 + Combo x1 (Combo port consist of Port3 and the other 5G Serdes works in fiber mode); 4'b0111, Qsgmii x1 + Copper x3 and Combo x1 (Combo port consist of Port3 and the other 5G Serdes works in fiber mode); Chip_mode[3] is tied to 0 and can't be changed.

6.1.6. SYNCE0 cfg (0xA006)

Table 14. SYNCE0 cfg (0xA006)

Bit	Symbol	Access	Default	Description
15	sync_clk_en_0	RW	0x0	1=enable to output the synce_clk0 to the pin SYNC0 and sync_lock0 to the pin PHYADDR0/SYNC_LOCK0. It doesn’t control whether to output the 25MHz referece clock to the SYNCE0 pin, which is only controlled by bit13 and bit10.
14	bp_sync_lock_gating_0	RW	0x0	When synce_clk0 is not locked, this bit controls whether to output the synce_clk0 to the pin SYNC0 or not. 1: to output; 0: to not output.
13	sel_synce_125m_0	RW	0x0	bit13 and bit10 controls the synce_clk0's frequence and source: {sel_synce_125m_0, sel_clk_25m_xtl_0}, 2'b00: output 25MHz syncE clock; 2'b01: output 31.25MHz syncE clock; 2'b10: output 125MHz syncE clock;

				2'b11: output 25MHz reference clock.
12:11	reserved	RO	0x0	always 0.
10	sel_clk_25m_xtl_0	RW	0x0	refer to bit13 sel_synce_125m_0 for detail.
9	sel_rclk_sds1_0	RW	0x0	bit9:0, select the source of the synce_clk0 from the recovered RX clocks. The recovered RX clocks include that from 8 port copper PHYs and two 5G serdes PHYs. MSB has the higher priority, for example, bit9:0=0x280 means to output the sds1's RX recovered clock; bit9:0=0x030 means to output the port 5's RX recovered clock. sds1, means the 5G serdes QSGMII1. sds0, means the 5G serdes QSGMII0. phy7, means the copper port 7. phy6, means the copper port 6. phy5, means the copper port 5. phy4, means the copper port 4. phy3, means the copper port 3. phy2, means the copper port 2. phy1, means the copper port 1. phy0, means the copper port 0.
8	sel_rclk_sds0_0	RW	0x0	
7	sel_rclk_phy7_0	RW	0x0	
6	sel_rclk_phy6_0	RW	0x0	
5	sel_rclk_phy5_0	RW	0x0	
4	sel_rclk_phy4_0	RW	0x0	
3	sel_rclk_phy3_0	RW	0x0	
2	sel_rclk_phy2_0	RW	0x0	
1	sel_rclk_phy1_0	RW	0x0	
0	sel_rclk_phy0_0	RW	0x0	

6.1.7. SYNCE1 cfg (0xA00E)

Table 15. SYNCE1 cfg (0xA00E)

Bit	Symbol	Access	Default	Description
15	sync_clk_en_1	RW	0x0	1=enable to output the synce_clk1 to the pin SYNC1 and sync_lock1 to the pin PHYADDR1/SYNC_LOCK1. It doesn't control whether to output the 25MHz referece clock to the SYNCE1 pin, which is only controlled by bit13 and bit10.
14	bp_sync_lock_gating_1	RW	0x0	When synce_clk1 is not locked, this bit controls whether to output the synce_clk1 or crystal clock to the pin SYNC1 or not. 1: to output; 0: to not output.
13	sel_synce_125m_1	RW	0x0	bit13 and bit10 controls the synce_clk1's frequence and source: {sel_synce_125m_1, sel_clk_25m_xtl_1}, 2'b00: output 25MHz syncE clock; 2'b01: output 31.25MHz syncE clock; 2'b10: output 125MHz syncE clock;

				2'b11: output 25MHz reference clock.
12:11	reserved	RO	0x0	always 0.
10	sel_clk_25m_xtl_1	RW	0x0	refer to bit13 sel_synce_125m_1 for detail.
9	sel_rclk_sds1_1	RW	0x0	bit9:0, select the source of the synce_clk1 from the recovered RX clocks. The recovered RX clocks include that from 8 port copper PHYs and two 5G serdes PHYs. MSB has the higher priority, for example, bit9:0=0x280 means to output the sds1's RX recovered clock; bit9:0=0x030 means to output the port 5's RX recovered clock. sds1, means the 5G serdes QSGMII1. sds0, means the 5G serdes QSGMII0. phy7, means the copper port 7. phy6, means the copper port 6. phy5, means the copper port 5. phy4, means the copper port 4. phy3, means the copper port 3. phy2, means the copper port 2. phy1, means the copper port 1. phy0, means the copper port 0.
8	sel_rclk_sds0_1	RW	0x0	
7	sel_rclk_phy7_1	RW	0x0	
6	sel_rclk_phy6_1	RW	0x0	
5	sel_rclk_phy5_1	RW	0x0	
4	sel_rclk_phy4_1	RW	0x0	
3	sel_rclk_phy3_1	RW	0x0	
2	sel_rclk_phy2_1	RW	0x0	
1	sel_rclk_phy1_1	RW	0x0	
0	sel_rclk_phy0_1	RW	0x0	

6.1.8. PHY Link Up/Down INTn Mask (0xA010)

Table 16. PHY Link Up/Down INTn Mask (0xA010)

Bit	Symbol	Access	Default	Description
15	phy7_link_up_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy7_link_up_int. 1: to enable the interrupt.
14	phy6_link_up_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy6_link_up_int. 1: to enable the interrupt.
13	phy5_link_up_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy5_link_up_int. 1: to enable the interrupt.
12	phy4_link_up_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy4_link_up_int. 1: to enable the interrupt.
11	phy3_link_up_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy3_link_up_int. 1: to enable the interrupt.
10	phy2_link_up_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy2_link_up_int. 1: to enable the interrupt.
9	phy1_link_up_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy1_link_up_int. 1: to enable the interrupt.
8	phy0_link_up_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy0_link_up_int. 1: to enable the interrupt.

7	phy7_link_down_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy7_link_down_int. 1: to enable the interrupt.
6	phy6_link_down_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy6_link_down_int. 1: to enable the interrupt.
5	phy5_link_down_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy5_link_down_int. 1: to enable the interrupt.
4	phy4_link_down_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy4_link_down_int. 1: to enable the interrupt.
3	phy3_link_down_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy3_link_down_int. 1: to enable the interrupt.
2	phy2_link_down_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy2_link_down_int. 1: to enable the interrupt.
1	phy1_link_down_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy1_link_down_int. 1: to enable the interrupt.
0	phy0_link_down_int_mask	RW	0x0	the interrupt mask bit for EXT A011 phy0_link_down_int. 1: to enable the interrupt.

6.1.9. PHY Link Up/Down INTn Status (0xA011)

Table 17. PHY Link Up/Down INTn Status (0xA011)

Bit	Symbol	Access	Default	Description
15	phy7_link_up_int	RO	0x0	It's the copper port #7 link up interrupt status.
14	phy6_link_up_int	RO	0x0	It's the copper port #6 link up interrupt status.
13	phy5_link_up_int	RO	0x0	It's the copper port #5 link up interrupt status.
12	phy4_link_up_int	RO	0x0	It's the copper port #4 link up interrupt status.
11	phy3_link_up_int	RO	0x0	It's the copper port #3 link up interrupt status.
10	phy2_link_up_int	RO	0x0	It's the copper port #2 link up interrupt status.
9	phy1_link_up_int	RO	0x0	It's the copper port #1 link up interrupt status.
8	phy0_link_up_int	RO	0x0	It's the copper port #0 link up interrupt status.
7	phy7_link_down_int	RO	0x0	It's the copper port #7 link down interrupt status.
6	phy6_link_down_int	RO	0x0	It's the copper port #6 link down interrupt status.
5	phy5_link_down_int	RO	0x0	It's the copper port #5 link down interrupt status.
4	phy4_link_down_int	RO	0x0	It's the copper port #4 link down interrupt status.
3	phy3_link_down_int	RO	0x0	It's the copper port #3 link down interrupt status.
2	phy2_link_down_int	RO	0x0	It's the copper port #2 link down interrupt status.

1	phy1_link_down_int	RO	0x0	It's the copper port #1 link down interrupt status.
0	phy0_link_down_int	RO	0x0	It's the copper port #0 link down interrupt status.

6.1.10. UTP Legacy Interrupt Mask (0xA012)

Table 18. UTP Legacy Interrupt Mask (0xA012)

Bit	Symbol	Access	Default	Description
15	en_clr_all_phys_intn	RW	0x0	1: reading EXT 0xA013 will clear itself and all UTP legacy interrupts' status in MII 0x13; 0: to clear EXT 0xA013, UTP legacy interrupts' status in MII 0x13 should be read clear first, then read clear 0xA013.
14:8	Reserved	RW	0x0	not used.
7	utp7_legacy_int_mask	RW	0x0	the interrupt mask bit for EXT 0xA013 utp7_legacy_int. 1: to enable the interrupt.
6	utp6_legacy_int_mask	RW	0x0	the interrupt mask bit for EXT 0xA013 utp6_legacy_int. 1: to enable the interrupt.
5	utp5_legacy_int_mask	RW	0x0	the interrupt mask bit for EXT 0xA013 utp5_legacy_int. 1: to enable the interrupt.
4	utp4_legacy_int_mask	RW	0x0	the interrupt mask bit for EXT 0xA013 utp4_legacy_int. 1: to enable the interrupt.
3	utp3_legacy_int_mask	RW	0x0	the interrupt mask bit for EXT 0xA013 utp3_legacy_int. 1: to enable the interrupt.
2	utp2_legacy_int_mask	RW	0x0	the interrupt mask bit for EXT 0xA013 utp2_legacy_int. 1: to enable the interrupt.
1	utp1_legacy_int_mask	RW	0x0	the interrupt mask bit for EXT 0xA013 utp1_legacy_int. 1: to enable the interrupt.
0	utp0_legacy_int_mask	RW	0x0	the interrupt mask bit for EXT 0xA013 utp0_legacy_int. 1: to enable the interrupt.

6.1.11. UTP Legacy Interrupt Status (0xA013)

Table 19. UTP Legacy Interrupt Status (0xA013)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	always 0.
7	utp7_legacy_int	RO	0x0	the UTP legacy interrupt status bit for EXT 0xA013 utp7_legacy_int. It's asserted when copper port #7 MII 0x13 is not 0. When EXT 0xA012 bit[15] is 1, it's read clear; else, copper port #7 MII 0x13 should be read clear first, then it will be cleared when read out.

6	utp6_legacy_int	RO	0x0	the UTP legacy interrupt status bit for EXT 0xA013 utp6_legacy_int. It's asserted when copper port #6 MII 0x13 is not 0. When EXT 0xA012 bit[15] is 1, it's read clear; else, copper port #6 MII 0x13 should be read clear first, then it will be cleared when read out.
5	utp5_legacy_int	RO	0x0	the UTP legacy interrupt status bit for EXT 0xA013 utp5_legacy_int. It's asserted when copper port #5 MII 0x13 is not 0. When EXT 0xA012 bit[15] is 1, it's read clear; else, copper port #5 MII 0x13 should be read clear first, then it will be cleared when read out.
4	utp4_legacy_int	RO	0x0	the UTP legacy interrupt status bit for EXT 0xA013 utp4_legacy_int. It's asserted when copper port #4 MII 0x13 is not 0. When EXT 0xA012 bit15 is 1, it's read clear; else, copper port #4 MII 0x13 should be read clear first, then it will be cleared when read out.
3	utp3_legacy_int	RO	0x0	the UTP legacy interrupt status bit for EXT 0xA013 utp3_legacy_int. It's asserted when copper port #3 MII 0x13 is not 0. When EXT 0xA012 bit[15] is 1, it's read clear; else, copper port #3 MII 0x13 should be read clear first, then it will be cleared when read out.
2	utp2_legacy_int	RO	0x0	the UTP legacy interrupt status bit for EXT 0xA013 utp2_legacy_int. It's asserted when copper port #2 MII 0x13 is not 0. When EXT 0xA012 bit[15] is 1, it's read clear; else, copper port #2 MII 0x13 should be read clear first, then it will be cleared when read out.
1	utp1_legacy_int	RO	0x0	the UTP legacy interrupt status bit for EXT 0xA013 utp1_legacy_int. It's asserted when copper port #1 MII 0x13 is not 0. When EXT 0xA012 bit[15] is 1, it's read clear; else, copper port #1 MII 0x13 should be read clear first, then it will be cleared when read out.
0	utp0_legacy_int	RO	0x0	the UTP legacy interrupt status bit for EXT 0xA013 utp0_legacy_int. It's asserted when copper port #0 MII 0x13 is not 0. When EXT 0xA012 bit[15] is 1, it's read clear; else, copper port #0 MII 0x13 should be read clear first, then it will be cleared when read out.

6.1.12. QSGMII Legacy Interrupt Mask (0xA014)

Table 20. QSGMII Legacy Interrupt Mask (0xA014)

Bit	Symbol	Access	Default	Description
15	q1_ch3_link_up_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q1_ch3_link_up_int. 1: to enable the interrupt.
14	q1_ch2_link_up_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q1_ch2_link_up_int. 1: to enable the interrupt.
13	q1_ch1_link_up_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q1_ch1_link_up_int. 1: to enable the interrupt.
12	q1_ch0_link_up_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q1_ch0_link_up_int. 1: to enable the interrupt.
11	q0_ch3_link_up_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch3_link_up_int. 1: to enable the interrupt.
10	q0_ch2_link_up_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch2_link_up_int. 1: to enable the interrupt.
9	q0_ch1_link_up_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch1_link_up_int. 1: to enable the interrupt.
8	q0_ch0_link_up_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch0_link_up_int. 1: to enable the interrupt.
7	q1_ch3_link_down_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q1_ch3_link_down_int. 1: to enable the interrupt.
6	q1_ch2_link_down_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q1_ch2_link_down_int. 1: to enable the interrupt.
5	q1_ch1_link_down_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q1_ch1_link_down_int. 1: to enable the interrupt.
4	q1_ch0_link_down_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q1_ch0_link_down_int. 1: to enable the interrupt.
3	q0_ch3_link_down_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch3_link_down_int. 1: to enable the interrupt.
2	q0_ch2_link_down_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch2_link_down_int. 1: to enable the interrupt.
1	q0_ch1_link_down_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch1_link_down_int. 1: to enable the interrupt.

0	q0_ch0_link_down_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch0_link_down_int. 1: to enable the interrupt.

6.1.13. QSGMII Legacy Interrupt Status (0xA015)

Table 21. QSGMII Legacy Interrupt Status (0xA015)

Bit	Symbol	Access	Default	Description
15	q1_ch3_link_up_int	RO	0x0	It's the QSGMII #1 channel #3 link up interrupt status.
14	q1_ch2_link_up_int	RO	0x0	It's the QSGMII #1 channel #2 link up interrupt status.
13	q1_ch1_link_up_int	RO	0x0	It's the QSGMII #1 channel #1 link up interrupt status.
12	q1_ch0_link_up_int	RO	0x0	It's the QSGMII #1 channel #0 link up interrupt status.
11	q0_ch3_link_up_int	RO	0x0	It's the QSGMII #0 channel #3 link up interrupt status.
10	q0_ch2_link_up_int	RO	0x0	It's the QSGMII #0 channel #2 link up interrupt status.
9	q0_ch1_link_up_int	RO	0x0	It's the QSGMII #0 channel #1 link up interrupt status.
8	q0_ch0_link_up_int	RO	0x0	It's the QSGMII #0 channel #0 link up interrupt status.
7	q1_ch3_link_down_int	RO	0x0	It's the QSGMII #1 channel #3 link down interrupt status.
6	q1_ch2_link_down_int	RO	0x0	It's the QSGMII #1 channel #2 link down interrupt status.
5	q1_ch1_link_down_int	RO	0x0	It's the QSGMII #1 channel #1 link down interrupt status.
4	q1_ch0_link_down_int	RO	0x0	It's the QSGMII #1 channel #0 link down interrupt status.
3	q0_ch3_link_down_int	RO	0x0	It's the QSGMII #0 channel #3 link down interrupt status.
2	q0_ch2_link_down_int	RO	0x0	It's the QSGMII #0 channel #2 link down interrupt status.
1	q0_ch1_link_down_int	RO	0x0	It's the QSGMII #0 channel #1 link down interrupt status.
0	q0_ch0_link_down_int	RO	0x0	It's the QSGMII #0 channel #0 link down interrupt status.

6.1.14. pkg_cfg0 (0xA0a0)

Port Index : 0 - 7

Port Offset : 0x100

Table 22. pkg_cfg0 (0xA0a0)

Bit	Symbol	Access	Default	Description
15	u0_pkg_chk_en	RW	0x0	1: to enable RX/TX package checker. For RX checker, if EXT 0xA0B7 bit[15] is 0, RX checker checks the downstream media's GMII RX data, else it checks upstream media's GMII RX data; For TX checker, if EXT 0xA0B7 bit[10] is 1, TX checker checks the pkg_gen's TX data; else if EXT 0xA0B7 bit[14] is 0, TX checker checks the downstream media's GMII TX data, else, it checks upstream media's GMII TX data.
14	u0_pkg_en_gate	RW	0x1	1: to enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0;
13	u0_bp_pkg_gen	RW	0x1	1: normal function; 0: test function, the TX data is sourced from pkg_gen;
12	u0_pkg_gen_en	RW SC	0x0	1: to enable pkg_gen generating GMII/MII packages. But, the data will only be sent to transceiver when bit13 bp_pkg_gen is 1'b0.
11:8	u0_pkg_prm_lth	RW	0x8	The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
7:4	u0_pkg_ipg_lth	RW	0xc	The IPG of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
3	u0_Xmit_mac_force_gen	RW	0x0	1: To enable pkg_gen to send out the generated data even when the link is not established.
2	u0_pkg_corrupt_crc	RW	0x0	1: to make pkg_gen to send out CRC error packages.
1:0	u0_pkg_payload	RW	0x0	Control the payload of the generated packages, excluding the DA/SA field if EXT 0xA0B7 bit[12] is 1. 00: the payload is increase byte; 01: the payload is random data; 10: the payload is periodic 0x5A 0xA5; 11: the payload is all 0x00.

6.1.15. pkg_cfg1 (0xA0a1)

Port Index : 0 – 7

Port Offset : 0x100

Table 23. pkg_cfg1 (0xA0a1)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_length	RW	0x40	To set the length of the generated packages.

6.1.16. pkg_cfg2 (0xA0a2)

Port Index : 0 – 7

Port Offset : 0x100

Table 24. pkg_cfg2 (0xA0a2)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_burst_size	RW	0x0	To set the number of packages in a burst of package generation. 0: to generate package continuously untill EXT 0xA0A0 bit[15] is changed to 0;

6.1.17. pkg_rx_valid0 (0xA0a3)

Port Index : 0 – 7

Port Offset : 0x100

Table 25. pkg_rx_valid0 (0xA0a3)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_valid_high	RO RC	0x0	Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

6.1.18. pkg_rx_valid1 (0xA0a4)

Port Index : 0 – 7

Port Offset : 0x100

Table 26. pkg_rx_valid1 (0xA0a4)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_valid_low	RO RC	0x0	Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

6.1.19. pkg_rx_os0 (0xA0a5)

Port Index : 0 – 7

Port Offset : 0x100

Table 27. pkg_rx_os0 (0xA0a5)

Bit	Symbol	Access	Default	Description

15:0	u0_pkg_ib_os_good_high	RO RC	0x0	Pkg_ib_os_good[31:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.1.20. pkg_rx_os1 (0xA0a6)

Port Index : 0 – 7

Port Offset : 0x100

Table 28. pkg_rx_os1 (0xA0a6)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_os_good_low	RO RC	0x0	Pkg_ib_os_good[15:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.1.21. pkg_rx_us0 (0xA0a7)

Port Index : 0 – 7

Port Offset : 0x100

Table 29. pkg_rx_us0 (0xA0a7)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_us_good_high	RO RC	0x0	Pkg_ib_us_good[31:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte.

6.1.22. pkg_rx_us1 (0xA0a8)

Port Index : 0 – 7

Port Offset : 0x100

Table 30. pkg_rx_us1 (0xA0a8)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_us_good_low	RO RC	0x0	Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte.

6.1.23. pkg_rx_err (0xA0a9)

Port Index : 0 – 7

Port Offset : 0x100

Table 31. pkg_rx_err (0xA0a9)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_err	RO RC	0x0	pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518Byte.

6.1.24. pkg_rx_os_bad (0xA0aa)

Port Index : 0 – 7

Port Offset : 0x100

Table 32. pkg_rx_os_bad (0xA0aa)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_os_bad	RO RC	0x0	pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length are >1518Byte.

6.1.25. pkg_rx_fragment (0xA0ab)

Port Index : 0 – 7

Port Offset : 0x100

Table 33. pkg_rx_fragment (0xA0ab)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_frag	RO RC	0x0	pkg_ib_frag is the number of RX packages from wire whose CRC are wrong and length are <64Byte.

6.1.26. pkg_rx_nosfd (0xA0ac)

Port Index : 0 – 7

Port Offset : 0x100

Table 34. pkg_rx_nosfd (0xA0ac)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_nosfd	RO RC	0x0	pkg_ib_nosfd is the number of RX packages from wire whose SFD are missed.

6.1.27. pkg_tx_valid0 (0xA0ad)

Port Index : 0 – 7

Port Offset : 0x100

Table 35. pkg_tx_valid0 (0xA0ad)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_valid_high	RO RC	0x0	Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

6.1.28. pkg_tx_valid1 (0xA0ae)

Port Index : 0 – 7

Port Offset : 0x100

Table 36. pkg_tx_valid1 (0xA0ae)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_valid_low	RO RC	0x0	Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose CRC

				are good and length are >=64Byte and <=1518Byte.

6.1.29. pkg_tx_os0 (0xA0af)

Port Index : 0 – 7

Port Offset : 0x100

Table 37. pkg_tx_os0 (0xA0af)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_os_good_high	RO RC	0x0	Pkg_ob_os_good[31:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.1.30. pkg_tx_os1 (0xA0b0)

Port Index : 0 – 7

Port Offset : 0x100

Table 38. pkg_tx_os1 (0xA0b0)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_os_good_low	RO RC	0x0	Pkg_ob_os_good[15:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.1.31. pkg_tx_us0 (0xA0b1)

Port Index : 0 – 7

Port Offset : 0x100

Table 39. pkg_tx_us0 (0xA0b1)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_us_good_high	RO RC	0x0	Pkg_ob_us_good[31:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are <64Byte.

6.1.32. pkg_tx_us1 (0xA0b2)

Port Index : 0 – 7

Port Offset : 0x100

Table 40. pkg_tx_us1 (0xA0b2)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_us_good_low	RO RC	0x0	Pkg_ob_us_good[15:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are <64Byte.

6.1.33. pkg_tx_err (0xA0b3)

Port Index : 0 – 7

Port Offset : 0x100

Table 41. pkg_tx_err (0xA0b3)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_err	RO RC	0x0	pkg_ob_err is the number of TX packages from MII whose CRC are wrong and length are >=64Byte, <=1518Byte.

6.1.34. pkg_tx_os_bad (0xA0b4)

Port Index : 0 – 7

Port Offset : 0x100

Table 42. pkg_tx_os_bad (0xA0b4)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_os_bad	RO RC	0x0	pkg_ob_os_bad is the number of TX packages from MII whose CRC are wrong and length are >1518Byte.

6.1.35. pkg_tx_fragment (0xA0b5)

Port Index : 0 – 7

Port Offset : 0x100

Table 43. pkg_tx_fragment (0xA0b5)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_frag	RO RC	0x0	pkg_ob_frag is the number of TX packages from MII whose CRC are wrong and length are <64Byte.

6.1.36. pkg_tx_nosfd (0xA0b6)

Port Index : 0 – 7

Port Offset : 0x100

Table 44. pkg_tx_nosfd (0xA0b6)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_nosfd	RO RC	0x0	pkg_ob_nosfd is the number of TX packages from MII whose SFD are missed.

6.1.37. pkg_cfg3 (0xA0b7)

Port Index : 0 – 7

Port Offset : 0x100

Table 45. pkg_cfg3 (0xA0b7)

Bit	Symbol	Access	Default	Description
15	u0_pkgchk_rxsrc_sel	RW	0x0	control RX checker's data source. =0, RX checker checks the downstream media's GMII RX data, =1, it checks upstream media's GMII RX data .

14	u0_pkgchk_txsrc_sel	RW	0x0	When ext.A0b7.10 is 0, it controls TX checker's data source. =0, TX checker checks the downstream media's GMII TX data; =1, it checks upstream media's GMII TX data. It is not valid when EXT 0xA0B7 bit[10] is 1.
13	u0_pkgen_txdir_sel	RW	0x0	Control the forward direction of the generated packages; 0=to downstream; 1=to upstream.
12	u0_en_pkgen_da_sa	RW	0x0	1: set the DA/SA of the packet generated by pkg_gen to a programmed value; For DA, if EXT 0xA0B7 bit[11] is 1, the DA is set to broadcase address FF-FF-FF-FF-FF-FF; else, the highest 5 Bytes are 00-00-00-00-00, and the lowest 1 Byte is programmed by EXT 0xA0B9 bit[15:8]. For SA, the highest 5 Bytes are 00-00-00-00-00, and the lowest 1 Byte is programmed by EXT 0xA0B9 bit[7:0]. 0: the DA/SA is not programmed value
11	u0_pkg_brdcst	RW	0x0	Valid when EXT 0xA0B7 bit[12] is 1. 1: set the DA to broadcase address FF-FF-FF-FF-FF-FF 0: set the DA to a fixed programmed value.
10	u0_pkgchk_txsrc_pkgen	RW	0x0	1: the package checker on TX side will check the tx data generated by pkg_gen; 0: the package checker on TX side will not check the tx data generated by pkg_gen. TX checker's data source is then controled by EXT 0xA0B7 bit[14].
9	u0_pkg_en_az	RW	0x0	1: enable to generate and send out LPI pattern during IPG;
8:0	u0_pkg_in_az_t	RW	0x1ff	control the time dewll in LPI; When speed is 1000Mbps, the timer’s unit is 1024ns; when speed is 100Mbps, the timer’s unit is 1280ns.

6.1.38. pkg_az_cfg (0xA0b8)

Port Index : 0 – 7

Port Offset : 0x100

Table 46. pkg_az_cfg (0xA0b8)

Bit	Symbol	Access	Default	Description

15:8	u0_pkgen_pre_az_t	RW	0x20	control the time after last package done and before sending LPI pattern; When speed is 1000Mbps, the timer's unit is 1024ns; when speed is 100Mbps, the timer's unit is 1280ns.
7:0	u0_pkgen_aft_az_t	RW	0x19	control the time after sending LPI pattern and before the next burst package; When speed is 1000Mbps, the timer's unit is 1024ns; when speed is 100Mbps, the timer's unit is 1280ns.

6.1.39. pkg_da_sa_cfg (0xA0b9)

Port Index : 0 – 7

Port Offset : 0x100

Table 47. pkg_da_sa_cfg (0xA0b9)

Bit	Symbol	Access	Default	Description
15:8	u0_pkgen_da	RW	0x0	Lowest 8 bits of DA, others are zero. Refer to EXT 0xA0B7 bit[12] for detail.
7:0	u0_pkgen_sa	RW	0x0	Lowest 8 bits of SA, others are zero. Refer to EXT 0xA0B7 bit[12] for detail.

6.1.40. manu_hw_reset (0xA0c0)

Table 48. manu_hw_reset (0xA0c0)

Bit	Symbol	Access	Default	Description
15	manu_hw_reset	RW	0x0	1: to reset whole chip including all register space except itself. The power on strapping will not be triggerd but the last strapped value will be reloaded.
14:0	reserved	RO	0x0	Reserved.

6.2. UTP MII Register

The YT8618 transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification.

The MII management interface registers are written and read serially, using the MDIO and MDC pins.

A clock of up to 12.5 MHz must drive the MDC pin of the YT8618. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

6.2.1. Basic control register (0x00)

Table 49. Basic control register (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically. 0: Normal operation 1: PHY reset
14	Loopback	RW SWC	0x0	Internal loopback control 1'b0: disable loopback 1'b1: enable loopback
13	Speed_Selection(LSB)	RW	0x0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero. Bit6 bit13 1 1 = Reserved 1 0 = 1000Mb/s 0 1 = 100Mb/s 0 0 = 10Mb/s
12	Autoneg_En	RW	0x1	1: to enable auto-negotiation; 0: auto-negotiation is disabled.
11	Power_down	RW SWC	0x0	1 = Power down 0 = Normal operation When the port is switched from power down to normal operation, software reset and Auto-Negotiation are performed even bit[15] Reset and bit[9] Re_Autoneg are not set by the user.
10	Isolate	RW SWC	0x0	Isolate phy from QSGMII/SGMII/FIBER. 1'b0: Normal mode 1'b1: Isolate mode
9	Re_Autoneg	RW SC SWS	0x0	Auto-Negotiation automatically restarts after hardware or software reset regardelss of bit[9]. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Duplex_Mode	RW	0x1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] to 0.

				1 = Full Duplex 0 = Half Duplex
7	Collision_Test	RW SWC	0x0	Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted. 1 = Enable COL signal test 0 = Disable COL signal test
6	Speed_ Selection(MSB)	RW	0x1	See bit13.
5:0	Reserved	RO	0x0	Reserved. Write as 0, ignore on read

6.2.2. Basic status register (0x01)

Table 50. Basic status register (0x01)

Bit	Symbol	Access	Default	Description
15	100Base-T4	RO	0x0	PHY doesn't support 100BASE-T4
14	100Base-X_Fd	RO	0x1	PHY supports 100BASE-X_FD
13	100Base-X_Hd	RO	0x1	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	0x1	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	0x1	PHY supports 10Mbps_Hd
10	100Base-T2_Fd	RO	0x0	PHY doesn't support 100Base-T2_Fd
9	100Base-T2_Hd	RO	0x0	PHY doesn't support 100Base-T2_Hd
8	Extended_Status	RO	0x1	Whether support Extended status register in 0Fh 0: Not supported 1: Supported
7	Unidirect_Ability	RO	0x0	1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established 1’b1: PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	0x1	1'b0: PHY will not accept management frames with preamble suppressed 1’b1: PHY will accept management frames with preamble suppressed
5	Autoneg_Complete	RO SWC	0x0	1'b0: Auto-negotiation process not completed 1’b1: Auto-negotiation process completed
4	Remote_Fault	RO RC SWC LH	0x0	1'b0: no remote fault condition detected 1’b1: remote fault condition detected
3	Autoneg_Ability	RO	0x1	1'b0: PHY not able to perform Auto-negotiation 1’b1: PHY able to perform Auto-negotiation
2	Link_Status	RO SWC LL	0x0	Link status 1’b0: Link is down 1’b1: Link is up

1	Jabber_Detect	RO RC SWC LH	0x0	10Baset jabber detected. It would assert if TX activity lasts longer than 42ms. 1'b0: no jabber condition detected 1'b1: Jabber condition detected.
0	Extended_Capability	RO	0x1	To indicate whether support Extended registers, to access from address register 1Eh and data register 1Fh 1'b0: Not supported 1'b1: Supported

6.2.3. PHY identification register1 (0x02)

Table 51. PHY identification register1 (0x02)

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	0x4F51	Bits 3 to 18 of the Organizationally Unique Identifier

6.2.4. PHY identification register2 (0x03)

Table 52. PHY identification register2 (0x03)

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	0x3A	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	0x8	6 bits manufacturer's type number.
3:0	Revision_No	RO	0x9	4 bits manufacturer's revision number.

6.2.5. Auto-Negotiation advertisement (0x04)

Table 53. Auto-Negotiation advertisement (0x04)

Bit	Symbol	Access	Default	Description
15	Next_Page	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down If 1000BASE-T is advertised, the required Next Pages are automatically transmitted. This bit

				must be set to 0 if no additional Next Page is needed. 1 = Advertise 0 = Not advertised
14	Ack	RO	0x0	Always 0.
13	Remote_Fault	RW	0x0	1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
12	Extended_Next_Page	RW	0x1	Extended Next Page enable control bit 1 = Local device supports transmission of extended Next Pages 0 = Local device does not support transmission of extended Next Pages.
11	Asymmetric_Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Asymmetric Pause 0 = No asymmetric Pause
10	Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Symmetric Pause 0 = No symmetric Pause
9	100BASE-T4	RO	0x0	1 = Able to perform 100BASE-T4 0 = Not able to perform 100BASE-T4 Always 0
8	100BASE-TX_Full_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not

				take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
7	100BASE-TX_Half_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
6	10BASE-Te_Full_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
5	10BASE-Te_Half_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]

				• The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
4:0	Selector_Field	RW	0x1	Selector Field mode. 00001 = IEEE 802.3

6.2.6. Auto-Negotiation link partner ability (0x05)

Table 54. Auto-Negotiation link partner ability (0x05)

Bit	Symbol	Access	Default	Description
15	1000Base-X_Fd	RO SWC	0x0	Received Code Word Bit 15 1 = Link partner is capable of Next Page 0 = Link partner is not capable of Next Page
14	ACK	RO SWC	0x0	Acknowledge. Received Code Word Bit 14 1 = Link partner has received link code word 0 = Link partner has not received link code word
13	REMOTE_FAULT	RO SWC	0x0	Remote Fault. Received Code Word Bit 13 1 = Link partner has detected remote fault 0 = Link partner has not detected remote fault
12	RESERVED	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 12
11	ASYMMETRIC_PAUSE	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
10	PAUSE	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 10 1 = Link partner supports pause operation 0 = Link partner does not support pause operation
9	100BASE-T4	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 9 1 = Link partner supports 100BASE-T4 0 = Link partner does not support100BASE-T4
8	100BASE-TX_FULL_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 8 1 = Link partner supports 100BASE-TX full-duplex 0 = Link partner does not support 100BASE-TX full-duplex

7	100BASE-TX_HALF_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 7 1 = Link partner supports 100BASE-TX half-duplex 0 = Link partner does not support 100BASE-TX half-duplex
6	10BASE-Te_FULL_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 6 1 = Link partner supports 10BASE-Te full-duplex 0 = Link partner does not support 10BASE-Te full-duplex
5	10BASE-Te_HALF_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 5 1 = Link partner supports 10BASE-Te half-duplex 0 = Link partner does not support 10BASE-Te half-duplex
4:0	SELECTOR_FIELD	RO SWC	0x0	Selector Field Received Code Word Bit 4:0

6.2.7. Auto-Negotiation expansion register (0x06)

Table 55. Auto-Negotiation expansion register (0x06)

Bit	Symbol	Access	Default	Description
15:5	Reserved	RO	0x0	Reserved
4	Parallel Detection fault	RO RC SWC LH	0x0	1 = Fault is detected 0 = No fault is detected
3	Link partner Next Page able	RO SWC LH	0x0	1 = Link partner supports Next Page e 0 = Link partner does not support Next Page
2	Local Next Page able	RO	0x1	1 = Local Device supports Next Page 0 = Local Device does not Next Page
1	Page received	RO RC LH	0x0	1 = A new page is received 0 = No new page is received
0	Link Partner Auto negotiation able	RO	0x0	1 = Link partner supports auto-negotiation 0 = Link partner does not support auto-negotiation

6.2.8. Auto-Negotiation Next Page register (0x07)

Table 56. Auto-Negotiation Next Page register (0x07)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RW	0x0	Transmit Code Word Bit 15 1 = The page is not the last page 0 = The page is the last page

14	Reserved	RO	0x0	Transmit Code Word Bit 14
13	Message page mode	RW	0x1	Transmit Code Word Bit 13 1 = Message Page 0 = Unformatted Page
12	Ack2	RW	0x0	Transmit Code Word Bit 12 1 = Comply with message 0 = Cannot comply with message
11	Toggle	RO	0x0	Transmit Code Word Bit 11 1 = This bit in the previously exchanged Code Word is logic 0 0 = The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message/Unformatte	RW	0x1	Transmit Code Word Bits [10:0]. These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

6.2.9. Auto-Negotiation link partner Received Next Page register (0x08)

Table 57. Auto-Negotiation link partner Received Next Page register (0x08)

Bit	Symbol	Access	Default	Description
15	Next Page	RO	0x0	Received Code Word Bit 15 1 = This page is not the last page 0 = This page is the last page
14	Reserved	RO	0x0	Received Code Word Bit 14
13	Message page mode	RO	0x0	Received Code Word Bit 13 1 = Message Page 0 = Unformatted Page
12	Ack2	RO	0x0	Received Code Word Bit 12 1 = Comply with message 0 = Cannot comply with message
11	Toggle	RO	0x0	Received Code Word Bit 11 1 = This bit in the previously exchanged Code Word is logic 0 0 = The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message/Unformatte	RO	0x0	Received Code Word Bit 10:0 These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

6.2.10. MASTER-SLAVE control register (0x09)

Table 58. MASTER-SLAVE control register (0x09)

Bit	Symbol	Access	Default	Description
15:13	Test mode	RW	0x0	The TX_TCLK signals from the RX_CLK pin is for jitter testing in test modes 2 and 3. When exiting the test mode, hardware reset or software reset through writing register 0x0 bit[15] must be performed to ensure normal operation. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 110, 111 = Reserved normal operation.
12	Master/Slave Manual configuration Enable	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration.
11	Master/Slave configuration	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down This bit is ignored if bit[12] is 0. 1 = Manual configuration as MASTER 0 = Manual configuration as SLAVE.

10	Port Type	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down This bit is ignored if bit[12] is 1. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)
9	1000BASE-T Full	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
8	1000BASE-T Half-	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised (default)
7:0	Reserved	RW	0x0	Write as 0, ignore on read.

6.2.11. MASTER-SLAVE status register (0x0A)

Table 59. MASTER-SLAVE status register (0x0A)

Bit	Symbol	Access	Default	Description
15	Master/Slave_cfg_error	RO RC SWC LH	0x0	This register bit will clear on read, rising of MII 0.12 and rising of AN complete.

				1 = Master/Slave configuration fault detected 0 = No fault detected
14	Master/Slave	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Local PHY configuration resolved to Master 0 = Local PHY configuration resolved to Slave
13	Local Receiver Status	RO	0x0	1 = Local Receiver OK 0 = Local Receiver not OK
12	Remote Receiver	RO	0x0	1 = Remote Receiver OK 0 = Remote Receiver not OK
11	Link Partner	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Link Partner supports 1000BASE-T half duplex 0 = Link Partner does not support 1000BASE-T half duplex
10	Link Partner	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Link Partner supports 1000Base-T full duplex 0 = Link Partner does not support 1000Base-T full duplex
9:8	Reserved	RO	0x0	Reserved
7:0	Idle Error Count	RO RC	0x0	MSB of Idle Error Counter. The register indicates the idle error count since the last read operation performed to this register. The counter pegs at 11111111 and does not roll over.

6.2.12. MMD access control register (0x0D)

Table 60. MMD access control register (0x0D)

Bit	Symbol	Access	Default	Description
15:14	Function	RW	0x0	00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only
13:5	Reserved	RO	0x0	Reserved
4:0	DEVAD	RW	0x0	MMD register device address. 00001 = MMD1 00011 = MMD3 00111 = MMD7

6.2.13. MMD access data register (0x0E)

Table 61. MMD access data register (0x0E)

Bit	Symbol	Access	Default	Description

15:0	Address data	RW	0x0	If register 0xD bits [15:14] are 00, this register is used as MMD DEVAD address register. Otherwise, this register is used as MMD DEVAD data register as indicated by its address register.

6.2.14. Extended status register (0x0F)

Table 62. Extended status register (0x0F)

Bit	Symbol	Access	Default	Description
15	1000BASE-X Full Duplex	RO	0x0	1 = PHY supports 1000BASE-X Full Duplex 0 = PHY does not supports 1000BASE-X Full Duplex Always 0.
14	1000BASE-X Half Duplex	RO	0x0	1 = PHY supports 1000BASE-X Half Duplex. 0 = PHY does not support 1000BASE-X Half Duplex. Always 0
13	1000BASE-T Full Duplex	RO	0x1	1 = PHY supports 1000BASE-T Full Duplex 0 = PHY does not supports 1000BASE-T Full Duplex Always 1
12	1000BASE-T Half Duplex	RO	0x0	1 = PHY supports 1000BASE-T Half Duplex 0 = PHY does not support 1000BASE-T Half Duplex Always 0.
11:0	Reserved	RO	0x0	Always 0

6.2.15. PHY specific function control register (0x10)

Table 63. PHY specific function control register (0x10)

Bit	Symbol	Access	Default	Description
15:7	Reserved	RO	0x0	Reserved
6:5	Cross_md	RW	0x3	Changes made to these bits disrupt normal operation, thus a software reset is mandatory after the change. And the configuration does not take effect until software reset. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Int_polar_sel	RW	0x0	Reserved
3	Crs_on_tx	RW	0x0	This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode:

				1 = Assert CRS on transmitting or receiving 0 = Never assert CRS on transmitting, only assert it on receiving.
2	En_sqe_test	RW	0x0	1 = SQE test enabled, 0 = SQE test disabled Note: SQE Test is automatically disabled in full-duplex mode regardless the setting in this bit.
1	En_pol_inv	RW	0x1	If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te. 1 = 10BASE-Te Polarity Reversal Enabled 0 = 10BASE-Te Polarity Reversal Disabled
0	Dis_jab	RW	0x0	Jabber takes effect only in 10BASE-Te half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function

6.2.16. PHY specific status register (0x11)

Table 64. PHY specific status register (0x11)

Bit	Symbol	Access	Default	Description
15:14	Speed_mode	RO	0x0	These status bits are valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page Received real-time	RO	0x0	1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	When Auto-Negotiation is disabled, this bit is set to 1 for force speed mode. 1 = Resolved 0 = Not resolved
10	Link status real-time	RO	0x0	1 = Link up 0 = Link down
9:7	Reserved	RO	0x0	Reserved
6	MDI Crossover Status	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.

				The bit value depends on register 0x10 “PHY specific function control register” bits6~bit5 configurations. Register 0x10 configurations take effect after software reset. 1 = MDIX 0 = MDI
5	Wirespeed downgrade	RO	0x0	1 = Downgrade 0 = No Downgrade
4:2	Reserved	RO	0x0	Reserved
1	Polarity Real Time	RO	0x0	1 = Reverted polarity 0 = Normal polarity
0	Jabber Real Time	RO	0x0	1 = Jabber 0 = No jabber

6.2.17. Interrupt Mask Register (0x12)

Table 65. Interrupt Mask Register (0x12)

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation Error INT mask	RW	0x0	1 = Interrupt enable 0 = Interrupt disable
14	Speed Changed INT mask	RW	0x0	same as bit 15
13	Duplex changed INT mask	RW	0x0	same as bit 15
12	Page Received INT mask	RW	0x0	same as bit 15
11	Link Failed INT mask	RW	0x0	same as bit 15
10	Link Succeed INT mask	RW	0x0	same as bit 15
9:6	reserved	RW	0x0	No used.
5	Wirespeed downgraded INT mask	RW	0x0	same as bit 15
4:2	Reserved	RW	0x0	No used.
1	Polarity changed INT mask	RW	0x0	same as bit 15
0	Jabber Happened INT mask	RW	0x0	same as bit 15

6.2.18. Interrupt Status Register (0x13)

Table 66. Interrupt Status Register (0x13)

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation Error INT	RO	0x0	Error can take place when any of the following happens: • MASTER/SLAVE does not resolve correctly • Parallel detect fault • No common HCD • Link does not come up after negotiation is complete

				• Selector Field is not equal • flp_receive_idle=true while Autoneg Arbitration FSM is in NEXT PAGE WAIT state 1 = Auto-Negotiation Error takes place 0 = No Auto-Negotiation Error takes place
14	Speed Changed INT	RO	0x0	1 = Speed changed 0 = Speed not changed
13	Duplex changed INT	RO	0x0	1 = duplex changed 0 = duplex not changed
12	Page Received INT	RO	0x0	1 = Page received 0 = Page not received
11	Link Failed INT	RO	0x0	1 = Phy link down takes place 0 = No link down takes place
10	Link Succeed INT	RO	0x0	1 = Phy link up takes place 0 = No link up takes place
9:6	Reserved	RO	0x0	reserved
5	Wirespeed downgraded INT	RO	0x0	1 = speed downgraded. 0 = Speed didn't downgrade.
4:2	Reserved	RO	0x0	reserved
1	Polarity changed INT	RO	0x0	1 = PHY revered MDI polarity 0 = PHY didn't revert MDI polarity
0	Jabber Happened INT	RO	0x0	1 = 10BaseT TX jabber happened 0 = 10BaseT TX jabber didn't happen Please refer to mii.1.1 Jabber_Detect.

6.2.19. Speed Auto Downgrade Control Register (0x14)

Table 67. Speed Auto Downgrade Control Register (0x14)

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	0x0	Reserved
11:6	Reserved	RO	0x0	Reserved
5	En_speed_downgrade	RW POS	0x1	When this bit is set to 1, the PHY enables smart-speed function. Writing this bit requires a software reset to update.
4:2	Autoneg retry limit pre-downgrade	RW	0x3	If these bits are set to 3, the PHY attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits. only take effect after software reset
1	Bp_autospd_timer	RW	0x0	1 = the wirespeed downgrade FSM will bypass the timer used for link stability check; only take effect after software reset 0 = not bypass the timer, then links that

				established but hold for less than 2.5s would still be taken as failure, autoneg retry counter will increase by 1.
0	Reserved	RO	0x0	Reserved

6.2.20. Rx Error Counter Register (0x15)

Table 68. Rx Error Counter Register (0x15)

Bit	Symbol	Access	Default	Description
15:0	Rx_err_counter	RO	0x0	Only valid for 1000M/s and 100M/s. This counter increase by 1 at the 1st rising of RX_ER when RX_DV is 1. The counter will hold at maximum 16'hFFFF and not roll over.

6.2.21. Debug Register's Address Offset Register (0x1E)

Table 69. Debug Register's Address Offset Register (0x1E)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	Reserved
7:0	Debug Register Address Offset	RW	0x0	It's the address offset of the debug register that will be Write or Read

6.2.22. Debug Register's Data Register (0x1F)

Table 70. Debug Register's Data Register (0x1F)

Bit	Symbol	Access	Default	Description
15:0	Debug Register Datas	RW	0x0	It's the data to be written to the debug register indicated by the address offset in register 0x1E, or the data read out from that debug register.

6.3. LDS MII Register

6.3.1. LRE control (0x00)

Table 71. LRE control (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically.; 1'b0: Normal operation; 1'b1: PHY reset
14	Loopback	RW	0x0	Loopback control; 1'b0: disable loopback; 1'b1: enable loopback
13	Restart_LDS	RW SC	0x0	1'b1: restart LDS process

12	LDS_Enable	RW	0x0	1'b1: LDS enabled; 1'b0: LDS disabled
11	Power_down	RW	0x0	1 = Power down; 0 = Normal operation; When the port is switched from power down to; normal operation, software reset and Auto-; Negotiation are performed even bit[15] RESET and bit[9] RESTART_AUTO_NEGOTIATION are not set by the user.
10	Isolate	RW	0x0	Isolate phy from MII/GMII/RGMII: PHY will not respond to RGMII TXD/TX_CTL, and present high impedance on RXD/RX_CTL.; 1'b0: Normal mode; 1'b1: Isolate mode
9:6	Speed_selection	RW	0x0	4'b0000: 10Mbps; 4'b1000: 100Mbps; Others: reserved
5:4	Pair_selection	RW	0x0	2'b00: 1 pair connection; 2'b01: 2 pair connections; 2'b10: 4 pair connections; 2'b11: reserved
3	M/S_selection	RW	0x0	1'b1: manually force local device to master, when reg0.12 = 0; 1'b0: manually force local device to slave, when reg0.12 = 0
2	Force auto negotiation	RW	0x0	1'b1: manually force local device to auto negotiation state, when reg0.12 = 0
1:0	Reserved	RO	0x0	Reserved. Write as 0, ignore on read

6.3.2. LRE status (0x01)

Table 72. LRE status (0x01)

Bit	Symbol	Access	Default	Description
15:14	Reserved	RO	0x0	Ignore on read
13	100Mbps_1-pair capable	RO	0x0	1'b1: 100Mbps 1-pair capable; 1'b0: Not 100Mbps 1-pair capable
12	100Mbps_4-pair capable	RO	0x1	1'b1: 100Mbps 4-pair capable; 1'b0: Not 100Mbps 4-pair capable
11	100Mbps_2-pair capable	RO	0x0	1'b1: 100Mbps 2-pair capable; 1'b0: Not 100Mbps 2-pair capable
10	10Mbps_2-pair capable	RO	0x0	1'b1: 10Mbps 2-pair capable; 1'b0: Not 10Mbps 2-pair capable
9	10Mbps_1-pair capable	RO	0x0	1'b1: 10Mbps 1-pair capable; 1'b0: Not 10Mbps 1-pair capable
8	Extended_Status	RO	0x1	Whether support EXTended status register in 0Fh; 0: Not supported; 1: Supported
7	Reserved	RO	0x1	None
6	Mf_Preamble_Suppression	RO	0x1	1'b0: PHY will not accept management frames with preamble suppressed; 1'b1: PHY will

				accept management frames with preamble suppressed
5	LDS_Complete	RO	0x0	1'b1: LDS auto-negotiation complete; 1'b0: LDS auto-negotiation not complete
4	Support_IEEE_802.3 _PHY	RO	0x1	1'b1: Support IEEE 802.3 PHY operation; 1'b0: Not Support IEEE 802.3 PHY operation
3	LDS_Ability	RO	0x1	1'b1: LDS auto-negotiation capable; 1'b0: Not LDS auto-negotiation capable
2	Link_Status	RO	0x0	Link status; 1'b0: Link is down; 1'b1: Link is up
1	Jabber_Detect	RO LH	0x0	10Baset jabber detected; 1'b0: no jabber condition detected; 1'b1: Jabber condition detected
0	Extended_Capability	RO LH	0x1	To indicate whether support EXTended registers, to access from address register 1Eh and data register 1Fh; 1'b0: Not supported; 1'b1: Supported

6.3.3. PHY ID (0x02)

Table 73. PHY ID (0x02)

Bit	Symbol	Access	Default	Description
15:0	PHY_ID	RO	0x4f51	None

6.3.4. PHY ID (0x03)

Table 74. PHY ID (0x03)

Bit	Symbol	Access	Default	Description
15:0	PHY_ID	RO	0xe889	None

6.3.5. LDS auto-negotiation advertised ability (0x04)

Table 75. LDS auto-negotiation advertised ability (0x04)

Bit	Symbol	Access	Default	Description
15	Asymmetric_pause	RW	0x0	1'b1: Advertise asymmetric pause; 1'b0: Advertise no asymmetric pause
14	Pause_capable	RW	0x0	1'b1: Advertise pause capable; 1'b0: Advertise no pause capable
13:6	Reserved	RO	0x0	reserved
5	100Mbps_1-pair capable	RW	0x0	1'b1: 100Mbps 1-pair capable; 1'b0: Not 100Mbps 1-pair capable
4	100Mbps_4-pair capable	RW	0x1	1'b1: 100Mbps 4-pair capable; 1'b0: Not 100Mbps 4-pair capable
3	100Mbps_2-pair capable	RW	0x0	1'b1: 100Mbps 2-pair capable; 1'b0: Not 100Mbps 2-pair capable

2	10Mbps_2-pair capable	RW	0x0	1'b1: 10Mbps 2-pair capable; 1'b0: Not 10Mbps 2-pair capable
1	10Mbps_1-pair capable	RW	0x0	1'b1: 10Mbps 1-pair capable; 1'b0: Not 10Mbps 1-pair capable
0	Auto negotiation capable	RW	0x1	1'b1: Auto negotiation capable; 1'b0: Auto negotiation capable

6.3.6. LDS auto-negotiation advertised control (0x05)

Table 76. LDS auto-negotiation advertised control (0x05)

Bit	Symbol	Access	Default	Description
15:13	Test_Mode	RW	0x0	Test Mode control
12:10	Reserved	RO	0x0	Reserved
9	Port_type_preference	RW	0x0	1'b1: multiport device (Mater); 1'b0: single-port device (Salve)
8	Ability_field_update	RW SC	0x0	1'b1: Contents of register 06h are updated; 1'b0: No updates
7:0	Local_field_number	RW	0x0	Local field number of Next Page message

6.3.7. LDS ability nEXT page transmit (0x06)

Table 77. LDS ability Next Page transmit (0x06)

Bit	Symbol	Access	Default	Description
15:0	Next_Page_message	RW	0x0	LDS Next Page message

6.3.8. LDS link partner ability (0x07)

Table 78. LDS link partner ability (0x07)

Bit	Symbol	Access	Default	Description
15	Asymmetric_pause	RO	0x0	1'b1: link partner supports asymmetric pause; 1'b0: link partner doesn’t support asymmetric pause
14	Pause_capable	RO	0x0	1'b1: link partner supports pause capable; 1'b0: link partner doesn’t support pause capable
13:6	Reserved	RO	0x0	None
5	100Mbps_1-pair_capable	RO	0x0	1'b1: link partner 100Mbps 1-pair capable; 1'b0: link partner not 100Mbps 1-pair capable
4	100Mbps_4-pair_capable	RO	0x0	1'b1: link partner 100Mbps 4-pair capable; 1'b0: link partner not 100Mbps 4-pair capable
3	100Mbps_2-pair_capable	RO	0x0	1'b1: link partner 100Mbps 2-pair capable; 1'b0: link partner not 100Mbps 2-pair capable
2	10Mbps_2-pair_capable	RO	0x0	1'b1: link partner 10Mbps 2-pair capable; 1'b0: link partner not 10Mbps 2-pair capable

1	10Mbps_1-pair_capable	RO	0x0	1'b1: link partner 10Mbps 1-pair capable; 1'b0: link partner not 10Mbps 1-pair capable
0	Reserved	RO	0x0	None

6.3.9. LDS link partner nEXT page message (0x08)

Table 79. LDS link partner Next Page message (0x08)

Bit	Symbol	Access	Default	Description
15:0	Link_partner_Next_Page_message	RO	0x0	LDS link partner Next Page message

6.3.10. LDS link partner Next Page message control (0x09)

Table 80. LDS link partner Next Page message control (0x09)

Bit	Symbol	Access	Default	Description
15	Next_Page_read_flag	RW SC	0x0	1'b1: Next Page has been read
14:9	Reserved	RO	0x0	None
8	Remote_acknowledge	RO RC	0x0	1'b1: acknowledge from link partner;
7:0	Remote_field_number	RO	0xff	Remote field number of Next Page message

6.3.11. LDS expansion (0x0A)

Table 81. LDS expansion (0x0A)

Bit	Symbol	Access	Default	Description
15	Downgrade_ability	RO	0x0	1'b1: LDS speed downgrade
14	Master/Slave	RO	0x0	1 = Local PHY configuration resolved to Master; 0 = Local PHY configuration resolved to Slave
13:12	Connections_pairs	RO	0x0	Number of pairs; 2'b00: 1 pair; 2'b01: 2 pairs; 2'b10: 4 pairs; 2'b11: reserved
11:0	Estimated_cable_length	RO	0x0	None

6.3.12. LDS Results (0x0B)

Table 82. LDS Results (0x0B)

Bit	Symbol	Access	Default	Description
15:6	Reserved	RO	0x0	None
5	4-pair_100M	RO	0x0	1'b1: local PHY configuration resolved to 4-pair 100M
4	Auto_negotiation	RO	0x0	1'b1: local PHY configuration resolved to AN
3	1-pair_100M	RO	0x0	1'b1: local PHY configuration resolved to 1-pair 100M
2	1-pair_10M	RO	0x0	1'b1: local PHY configuration resolved to 1-pair 10M

1	2-pair_100M	RO	0x0	1'b1: local PHY configuration resolved to IEEE 100M
0	2-pair_10M	RO	0x0	1'b1: local PHY configuration resolved to IEEE 10M

6.3.13. LDS Extended status (0x0F)

Table 83. LDS Extended status (0x0F)

Bit	Symbol	Access	Default	Description
15:10	Reserved	RO	0x0	Reserved
9	Local_receiver status	RO	0x0	1'b1: local receiver ok; 1'b0: local receiver not ok
8	Remote_receiver status	RO	0x0	1'b1: remote receiver ok; 1'b0: remote receiver not ok
7:0	Idle_error_count	RO	0x0	Number of idle errors since last read

6.4. UTP MMD Register

6.4.1. PCS control 1 register (MMD3, 0x00)

Table 84. PCS control 1 register (MMD3, 0x00)

Bit	Symbol	Access	Default	Description
15	Pcs_rst	RW SC	0x0	Setting this bit will set all PCS registers to their default states. This action also initiate a reset in MII 0x0 bit15, MMD1 and MMD7.
14:11	Reserved	RO	0x0	Reserved
10	Clock_stoppable	RW SWC	0x0	Not used.
9:0	Reserved	RO	0x0	Reserved

6.4.2. PCS status 1 register (MMD3, 0x01)

Table 85. PCS status 1 register (MMD3, 0x01)

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	0x0	Reserved
11	Tx_lpi_rxed	RO LH	0x0	When read as 1, it indicates that the transmit PCS has received low power idle signaling one or more times since the register was last read. Latch High.
10	Rx_lpi_rxed	RO LH	0x0	When read as 1, it indicates that the receive PCS has received low power idle signaling one or more times since the register was last read. Latch High.

9	Tx_lpi_indic	RO	0x0	When read as 1, it indicates that the transmit PCS is currently receiving low power idle signals.
8	Rx_lpi_indic	RO	0x0	When read as 1, it indicates that the receive PCS is currently receiving low power idle signals.
7:3	Reserved	RO	0x0	Reserved
2	Pcsrx_lnk_status	RO LL	0x0	PCS status, latch low.
1:0	Reserved	RO	0x0	Reserved

6.4.3. EEE control and capability register (MMD3, 0x14)

Table 86. EEE control and capability register (MMD3, 0x14)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	1000BASE-T EEE	RO	0x1	Always 1. EEE is supported for 1000BASE-T
1	100BASE-TX EEE	RO	0x1	Always 1. EEE is supported for 100BASE-TX
0	Reserved	RO	0x0	Reserved

6.4.4. EEE wake error counter (MMD3, 0x16)

Table 87. EEE wake error counter (MMD3, 0x16)

Bit	Symbol	Access	Default	Description
15:0	Lpi_wake_err_cnt	RO RC SWC	0x0	Count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type.

6.4.5. Local Device EEE Ability (MMD7, 0x3C)

Table 88. Local Device EEE Ability (MMD7, 0x3C)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	EEE_1000BT	RW	0x0	PHY's 1000BASE-T EEE ability.
1	EEE_100BT	RW	0x0	PHY's 100BASE-TX EEE ability.
0	Reserved	RO	0x0	Reserved

6.4.6. Link Partner EEE Ability (MMD7, 0x3D)

Table 89. Link Partner EEE Ability (MMD7, 0x3D)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	LP_ge_eee_ability	RO	0x0	Link partner's 1000BASE-T EEE ability.
1	LP_ge_eee_ability	RO	0x0	Link partner's 100BASE-TX EEE ability.
0	Reserved	RO	0x0	Reserved

6.4.7. Autoneg Result of EEE (MMD7, 0x8000)

Table 90. Autoneg Result of EEE (MMD7, 0x8000)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	En_ge_eee	RO	0x0	The autoneg result of whether 1000BASE-T EEE is supported by both sides.
1	En_fe_eee	RO	0x0	The autoneg result of whether 100BASE-TX EEE is supported by both sides.
0	Reserved	RW	0x0	Reserved

6.5. UTP EXT Register

6.5.1. 10BT Debug, LPBKs Register (0x0A)

Table 91. 10BT Debug, LPBKs Register (0x0A)

Bit	Symbol	Access	Default	Description
15:9	Reserved	RO	0x0	Reserved
8:6	phy_reg	RW	0x0	Reserved
5	rem_phy_lpbk	RW	0x0	control to set UTP to remote phy loopback mode or not.
4	Ext_lpbk	RW	0x0	control to set UTP to external loopback mode or not.
3	Reserved	RO	0x1	Reserved
2:0	Test_mode_10bt	RW SWC	0x0	Test_mode[2:0] is for 10BASE-Te test mode select:

6.5.2. Sleep Control1 (0x27)

Table 92. Sleep Control1 (0x27)

Bit	Symbol	Access	Default	Description
15	En_sleep_sw	RW	0x1	1 = enable sleep mode: PHY will enter sleep mode and close AFE after unplug cable for a timer;
14	Pllon_in_slp	RW	0x0	1 = keep PLL on in sleep mode; 0 = PLL will be ON and OFF periodly.
13:6	Reserved	RO	0x0	Reserved
5	Sleeping	RO	0x0	1 = PHY is slept; 0 = PHY is waked.
4	Gate_25m	RO	0x0	Not used.
3:0	Reserved	RO	0x0	Reserved

6.5.3. debug mon1 (0x5A)

Table 93. debug mon1 (0x5A)

Bit	Symbol	Access	Default	Description
15	Hold_snap_shot	RO	0x0	Valid when EXT 0x58 bit14 en_snap_shot is set.
14:0	Mse0	RO	0x0	Valid when EXT 0x58 bit14 en_snap_shot is set, or EXT 0x59 bit15 prob_auto is set. Corresponding to these two setting, it is MDI channel 0's MSE at the time snap shot condition is met, or at the time this EXT register is being read.

6.5.4. debug mon2 (0x5B)

Table 94. debug mon2 (0x5B)

Bit	Symbol	Access	Default	Description
15	Hold_snap_shot_az	RO	0x0	Valid when EXT 0x58 bit15 en_snap_shot_az is set. 1 = the snap shot condition is met and triggerd
14:0	Mse1	RO	0x0	Valid when EXT 0x58 bit14 en_snap_shot is set, or EXT 0x59 bit15 prob_auto is set. Corresponding to these two setting, it is MDI channel 1's MSE at the time snap shot condition is met, or at the time this EXT register is being read.

6.5.5. debug mon3 (0x5C)

Table 95. debug mon3 (0x5C)

Bit	Symbol	Access	Default	Description
15	Reserved	RO	0x0	Reserved
14:0	Mse2	RO	0x0	Valid when EXT 0x58 bit14 en_snap_shot is set, or EXT 0x59 bit15 prob_auto is set. Corresponding to these two setting, it is MDI channel 2's MSE at the time snap shot condition is met, or at the time this EXT register is being read.

6.5.6. debug mon4 (0x5D)

Table 96. debug mon4 (0x5D)

Bit	Symbol	Access	Default	Description
15	Reserved	RO	0x0	Reserved

14:0	Mse3	RO	0x0	Valid when EXT 0x58 bit14 en_snap_shot is set, or EXT 0x59 bit15 prob_auto is set. Corresponding to these two setting, it is MDI channel 3's MSE at the time snap shot condition is met, or at the time this EXT register is being read.

6.6. SDS(1.25G/5G) MII Register

6.6.1. Basic control register (0x00)

Table 97. Basic control register (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically.
14	Loopback	RW	0x0	Internal loopback control, , when it's set, SGMII/Fiber's TX data will be loopbaced to RX.
13	Speed_Selection(LSB)	RW	0x0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero.
12	Autoneg_En	RW	0x1	1: to enable auto-negotiation;
11	Power_down	RW	0x0	1 = Power down
10	Isolate	RW	0x0	Isolate SerDes from UTP or other SerDes interface.
9	Re_Autoneg	RW SC	0x0	1 = to restart auto-negotiation;
8	Duplex_Mode	RW	0x1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] Autoneg_En to 0.
7	Reserved	RW	0x0	Reserved
6	Speed_ Selection(MSB)	RW	0x1	See bit13.
5:0	Reserved	RO	0x0	Reserved. Write as 0, ignore on read

6.6.2. Basic status register (0x01)

Table 98. Basic status register (0x01)

Bit	Symbol	Access	Default	Description
15	100Base-T4	RO	0x0	PHY doesn't support 100BASE-T4
14	100Base-X_Fd	RO	0x1	PHY supports 100BASE-X_FD
13	100Base-X_Hd	RO	0x0	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	0x0	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	0x0	PHY supports 10Mbps_Hd
10	100Base-T2_Fd	RO	0x0	PHY doesn't support 100Base-T2_Fd
9	100Base-T2_Hd	RO	0x0	PHY doesn't support 100Base-T2_Hd
8	Extended_Status	RO	0x1	1 = Extended status information in Register 15 0 = No extended status information in Register 15
7	Unidirect_Ability	RO	0x1	1 = PHY able to transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established; 0 = PHY able to transmit from media independent interface only when the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	0x1	1 = PHY will accept management frames with preamble suppressed; 0 = PHY will not accept management frames with preamble suppressed.
5	Autoneg_Complete	RO	0x0	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed
4	Remote_Fault	RO RC SWC LH	0x0	1 = remote fault condition detected 0 = no remote fault condition detected
3	Autoneg_Ability	RO	0x1	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform
2	Link_Status	RO SWC LL	0x0	1 = link is up 0 = link is down
1	Jabber_Detect	RO	0x0	always 0
0	Extended_Capability	RO	0x1	To indicate whether support EXTended registers, to access from address register 1Eh and data register 1Fh

6.6.3. Sds identification register1 (0x02)

Table 99. Sds identification register1 (0x02)

Bit	Symbol	Access	Default	Description

15:0	Phy_Id	RO	0x4f51	Bits 3 to 18 of the Organizationally Unique Identifier

6.6.4. Sds identification register2 (0x03)

Table 100. Sds identification register2 (0x03)

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	0x3a	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	0x8	6 bits manufacturer's type number
3:0	Revision_No	RO	0x9	4 bits manufacturer's revision number

6.6.5. Auto-Negotiation advertisement (0x04)

Table 101. Auto-Negotiation advertisement (0x04)

Bit	Symbol	Access	Default	Description
15	Next_Page	RW	0x0	Reserved. Next page exchange of SGMII/1000BASE-X Auto-negotiation is not supported in this IC
14	Ack	RO	0x0	Always 0
13:12	Remote_Fault	RO	0x0	Always 0
11:9	Reserved	RO	0x0	Reserved
8	Asymmetric_Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Asymmetric Pause 0 = No asymmetric Pause
7	Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down

				1 = Symmetric Pause 0 = No symmetric Pause
6	Half_duplex	RW	0x0	Half duplex ability
5	Full_duplex	RW	0x1	Full duplex ability
4:0	Reserved	RO	0x0	Reserved

6.6.6. Auto-Negotiation link partner ability (0x05)

Table 102. Auto-Negotiation link partner ability (0x05)

Bit	Symbol	Access	Default	Description
15	Next_Page_or_Link	RO SWC	0x0	Received Code Word Bit 15. It's Next page in 1000BASE-X auto-negotiation, and link status or 0 in SGMII auto-negotiation.
14	ACK	RO SWC	0x0	Acknowledge. Received Code Word Bit 14
13:12	REMOTE_FAULT	RO SWC	0x0	Remote Fault. Received Code Word Bit 13:12
11:9	RESERVED	RO	0x0	Reserved. Received Code Word Bit 11:9
8:7	PAUSE	RO SWC	0x0	Pause. Received Code Word Bit 8:7
6	HALF_DUPLEX	RO SWC	0x0	Half duplex. Received Code Word Bit 6
5	FULL_DUPLEX	RO SWC	0x0	Full duplex. Received Code Word Bit 5
4:0	RESERVED	RO	0x0	Reserved. Received Code Word Bit 4:0

6.6.7. Auto-Negotiation expansion register (0x06)

Table 103. Auto-Negotiation expansion register (0x06)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	Local Next Page able	RO	0x0	1 = Local Device supports Next Page
1	Page received	RO RC LH	0x0	1 = A new page is received
0	Reserved	RO	0x0	Reserved

6.6.8. Auto-Negotiation NEXT Page register (0x07)

Table 104. Auto-Negotiation Next Page register (0x07)

Bit	Symbol	Access	Default	Description
15:0	Next Page	RO	0x0	always be 0

6.6.9. Auto-Negotiation link partner Received Next Page register (0x08)

Table 105. Auto-Negotiation link partner Received Next Page register (0x08)

Bit	Symbol	Access	Default	Description
15:0	Link Partner Next Page	RO	0x0	always be 0

6.6.10. Extended status register (0x0F)

Table 106. Extended status register (0x0F)

Bit	Symbol	Access	Default	Description
15	1000BASE-X Full Duplex	RO	0x1	1 = PHY supports 1000BASE-X Full Duplex
14	1000BASE-X Half Duplex	RO	0x0	1 = PHY supports 1000BASE-X Half Duplex.
13	1000BASE-T Full Duplex	RO	0x0	1 = PHY supports 1000BASE-T Full Duplex
12	1000BASE-T Half Duplex	RO	0x0	1 = PHY supports 1000BASE-T Half Duplex
11:0	Reserved	RO	0x0	Always 0

6.6.11. Sds specific status register (0x11)

Table 107. Sds specific status register (0x11)

Bit	Symbol	Access	Default	Description
15:14	Speed_mode	RO	0x0	11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	1 = Full-duplex 0 = Half-duplex
12:11	Pause	RO	0x0	Pause to mac
10	Link status real-time	RO	0x0	1 = Link up 0 = Link down
9	Rx_lpi_active	RO	0x0	rx LPI is active
8	Duplex_error	RO	0x0	realtime duplex error
7	En_flowctrl_rx	RO	0x0	1 = Transmit pause enabled 0 = Transmit pause disabled
6	En_flowctrl_tx	RO	0x0	1 = Receive pause enabled 0 = Receive pause disabled
5:4	Ser_mode_cfg	RO	0x0	realtime serdes working mode. 00: SG_MAC; 01: SG_PHY; 10: FIB_1000; 11: FIB_100.
3:1	Xmit	RO	0x0	realtime transmit statemachine. 001: Xmit Idle; 010: Xmit Config; 100: Xmit Data.
0	Syncstatus	RO	0x0	realtime Serdes PCS syncstatus

6.6.12. 100fx cfg (0x14)

Table 108. 100fx cfg (0x14)

Bit	Symbol	Access	Default	Description
15	Force_sg_status	RW	0x1	Reserved
13:12	Pause_to_mac_100fx	RW	0x3	Pause setting to mac in 100fx mode
11:0	Reserved	RO	0x0	Reserved

6.6.13. receive err counter mon (0x15)

Table 109. receive err counter mon (0x15)

Bit	Symbol	Access	Default	Description
15:0	error_counter_rx	RO SWC	0x0	This counter increase by 1 at the 1st rising of RX_ER when RX_DV is 1. The counter will hold at maximum 16'hFFFF and not roll over.

6.6.14. lint fail counter mon (0x16)

Table 110. lint fail counter mon (0x16)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	Reserved
7:0	Link_fail_cnt	RO SWC RC	0x0	link fail counter. This counter increases by 1 each time the SerDes link goes down.

6.7. SDS(5G) EXT Register

6.7.1. bp_serdes_link_rst (0x00)

Table 111. bp_serdes_link_rst (0x00)

Bit	Symbol	Access	Default	Description
15	bp_serdes_link_rst	RW	0x0	1: to not reset the bridge between PHY and serdes when serdes is link down; 0: to reset the bridge.
14	sgtx_fifo_en	RW	0x0	1: to enable the SGMII TX FIFO so preamble will not be dropped to align tx_even; 0: to bypass the SGMII TX FIFO.
13	en_swrst_selfclr	RW	0x0	1: serdes SW reset in EXT 0x2 bit15 is self cleared; 0: it's not selfcleared, should be write as 0 to clear.
12	en_pcsrst_selfclr	RW	0x0	1: serdes PCS SW reset in EXT 0x2 bit8 is selfcleared; 0: it's not selfcleared, should be write as 0 to clear.

11	en_sw_reset_ana	RW	0x0	1: to enable serdes SW reset to reset analog TX/RX divider, TX/RX data path and PI code; 0: to disable serdes SW reset to reset analog TX/RX divider, TX/RX data path and PI code.
10	en_an_on_align_done	RW	0x1	1: to enable SGMII/1000BASE-X restart autoneg when RX alignment is done; 0: to disable.
9:0	Reserved	RO	0x0	Reserved

6.7.2. sds analog digital interface cfg (0x02)

Table 112. sds analog digital interface cfg (0x02)

Bit	Symbol	Access	Default	Description
15	Sw_reset	RW	0x0	SerDes software reset, high active; ext.0.13 control it to be self clear or not, by default it's not self clear.
14	Tx_clk_sel	RW	0x0	select tx clock phase from analog. 1: inverted; 0: non-inverted.
13	Rx_clk_sel	RW	0x1	select rx clock phase from analog, 1: inverted; 0: non-inverted.
12	Rx_clk_cdr_sel	RW	0x1	select CDR's rx clock phase from analog, 1: inverted; 0: non-inverted.
11	Rot_clk_sel	RW	0x0	select rx clock phase used to latch rotator setting, 1: inverted; 0: non-inverted.
10	Loopback	RW	0x0	sds internal loopback, for QSGMII, all 4 channels' TX are loopbacked to RX.
9	Reserved	RO	0x0	always 0.
8	pcs_sw_reset	RW	0x0	SerDes PCS software reset, high active; ; ext.0.12 control it to be self clear or not, by default it's not self clear.
7	Tx_data_mlsb_sel	RW	0x0	1: swap msb and lsb for tx data to analog
6	Rx_data_mlsb_sel	RW	0x1	1: swap msb and lsb of rx data from analog.
5	Tx_data_pol_sel	RW	0x0	1: 1 map to 0 and 0 map to 1 for tx data to analog
4	Rx_data_pol_sel	RW	0x0	1: 1 map to 0 and 0 map to 1 for rx data from analog
3	Cdr_data_mlsb_sel	RW	0x0	1: swap msb and lsb of rx data for cdr from analog
2:1	Reserved	RW	0x0	Reserved
0	Reserved	RO	0x0	Reserved

6.7.3. sds prbs cfg1 (0x05)

Table 113. sds prbs cfg1 (0x05)

Bit	Symbol	Access	Default	Description
15	En_prbs	RW	0x0	enable TX PRBS or self-defined pattern, the pattern type is determined by bit8 Test_mode_prbs31 and bit7:5 test_mode.
14	En_bert	RW	0x0	enable Bit Error Rate Test;
13	Prbs_invert	RW	0x0	TX error injection function, it has highest polarity than prbs_err_once and prbs_err_cont. 1: to send polarity inverted PRBS or self-defined pattern;
12	Prbs_err_cont	RW	0x0	TX error injection function, it has the lowest polarity.1: to inject error on TX pattern continuously and periodic, the period is controlled by prbs_err_rate.
11:10	Prbs_err_rate	RW	0x0	It's valid only when prbs_err_cont is 1. 2'b00: inject one error every 1024 cycles; 2'b01: inject one error every 2048 cycles; 2'b10: inject one error every 4096 cycles; 2'b11: inject one error every 8192 cycles;
9	Prbs_err_once	RW	0x0	TX error injection function.At the rising of this bit, to send polarity inverted PRBS or self-defined pattern for one cycle;
8	Test_mode_prbs31	RW	0x0	1: PRBS31, bit7:5 test_mode[2:0] has no effect.0: not PRBS31, bit7:5 test_mode[2:0] take effect then.
7:5	Test_mode	RW	0x0	Control the TX pattern in test mode: 3'h0, PRBS7; 3'h1, PRBS10; 3'h2, Fix pattern, the fix pattern is controlled by Ext.6;3'h3, 010101…; 3'h4, 00110011…; 3'h5, 00000_11111_00000_11111…; 3'h6, 0000_0000_00_1111_1111_11…; 3'h7, Increase pattern, 0->1023->0->1023…
4:0	Reserved	RO	0x0	Reserved

6.7.4. sds prbs cfg2 (0x06)

Table 114. sds prbs cfg2 (0x06)

Bit	Symbol	Access	Default	Description
15:0	Fix_pattern_15_0	RW	0x0	fix pattern transmited in test_mode 2

6.7.5. sds prbs cfg2 (0x07)

Table 115. sds prbs cfg2 (0x07)

Bit	Symbol	Access	Default	Description
15:4	Reserved	RO	0x0	Reserved
3:0	Fix_pattern_19_16	RW	0x0	fix pattern transmited in test_mode 2

6.7.6. sds prbs mon1 (0x08)

Table 116. sds prbs mon1 (0x08)

Bit	Symbol	Access	Default	Description
15:9	Reserved	RO	0x0	Reserved
8	Err	RO	0x0	Err flag after PRBS has synchronized
7:2	Reserved	RO	0x0	Reserved
1	bisync_latch_low	RO LL	0x0	PRBS test synchronization status, once the sync is lost, this bit will latch low, until it's been read out.
0	Bitsync	RO	0x0	real time PRBS test synchronization status

6.7.7. sds prbs mon2 (0x09)

Table 117. sds prbs mon2 (0x09)

Bit	Symbol	Access	Default	Description
15:0	Err_cnt_15_0	RO	0x0	real time lowest 16 bits received error bit counter

6.7.8. sds prbs mon3 (0x0A)

Table 118. sds prbs mon3 (0x0A)

Bit	Symbol	Access	Default	Description
15:0	Err_cnt_31_16	RO	0x0	real time highest 16 bits received error bit counter

6.7.9. sds prbs mon4 (0x0B)

Table 119. sds prbs mon4 (0x0B)

Bit	Symbol	Access	Default	Description
15:0	Good_cnt_15_0	RO	0x0	real time lowest 16 bits received good bit counter

6.7.10. sds prbs mon5 (0x0C)

Table 120. sds prbs mon5 (0x0C)

Bit	Symbol	Access	Default	Description
15:0	Good_cnt_31_16	RO	0x0	real time highest 16 bits received good bit

				counter

6.7.11. analog cfg2 (0xA1)

Table 121. analog cfg2 (0xA1)

Bit	Symbol	Access	Default	Description
15:12	Tx_driver_stg2	RW	0xA	TX driver stage2 amplitude control bit<3:2>: 00 +0mA 01: +2.5mA 10:+2.5mA 11:+5mA bit<1:0>: 00 +0mA 01: +0.625mA 10: +1.25mA 11:+2.5mA
11	Tx_driver_stg1	RW	0x1	TX driver stage1 amplitude control
10:8	Reserved	RO	0x0	Reserved
7:6	vb_tx_term	RW	0x2	tx output common mode voltage when tx power down 00: 0.7V 01:0.8V 10:0.9V 11:1V
5	tx_vamp_post	RW	0x0	TX driver post stage1 amplitude control.
4	Reserved	RO	0x0	always 0.
3:1	tx_driver_post	RW	0x7	TX driver stage2 de-emphasize control bit<2>: 0 +0mA, 1: +2.5mA bit<1:0>: 00: +0mA 01: +0.625mA 10: +1.25mA 11:+2.5mA
0	Tx_pd	RW	0x0	power down analog tx

7. Timing and DC/AC Characteristics

7.1. DC Characteristics

Table 122. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
DVDDIO, AVDDH, SVDDH	3.3V Supply Voltage	3.135	3.30	3.465	V
DVDDL, AVDDL, SVDDL, PLLVDDL	1.2V Supply Voltage	1.14	1.20	1.26	V
Voh	High Level Output Voltage	2.4	-	-	V
Vol	Low Level Output Voltage	-	-	0.4	V
Vih	High Level Input Voltage	DVDDIO-0.7	-	-	V
Vil	Low Level Input Voltage	-	-	GND+0.7	V

7.2. AC Characteristics

7.2.1. QSGMII Differential Transmitter Characteristics

Table 123. QSGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval	-	200	-	ps
T_X1	Eye Mask	-	-	0.15	UI
T_X2	Eye Mask	-	-	0.4	UI
T_Y1	Eye Mask	200	-	-	mV
T_Y2	Eye Mask	-	-	450	mV
$T_{TX-JITTER}$	Output Jitter	-	-	0.30	UI
$T_{Tx-RISE}$	Output Rise Time	30	-	-	ps
$T_{TX-FALL}$	Output Fall Time	30	-	-	ps
R_{TX}	Differential Resistance	80	100	120	ohm
C_{TX}	AC Coupling Capacitor	75	100	200	nF
L_{TX}	Transmit Length in PCB(FR4)	-	-	10	inch

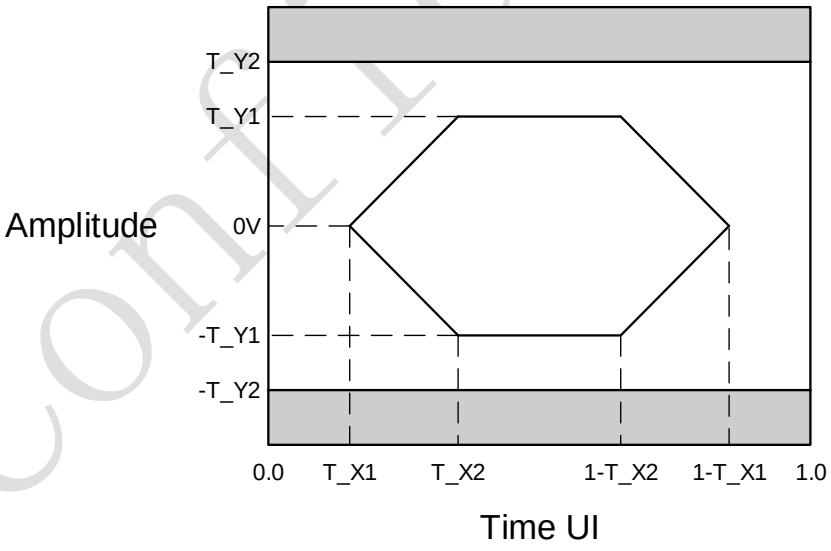


Figure 12. QSGMII Differential Transmitter Eye Diagram

7.2.2. QSGMII Differential Receiver Characteristics

Table 124. QSGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units

UI	Unit Interval	-	200	-	ps
R_X1	Eye Mask	-	-	0.3	UI
R_Y1	Eye Mask	50	-	-	mV
R_Y2	Eye Mask	-	-	600	mV
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.60	UI
R_{RX}	Differential Resistance	80	100	120	ohm

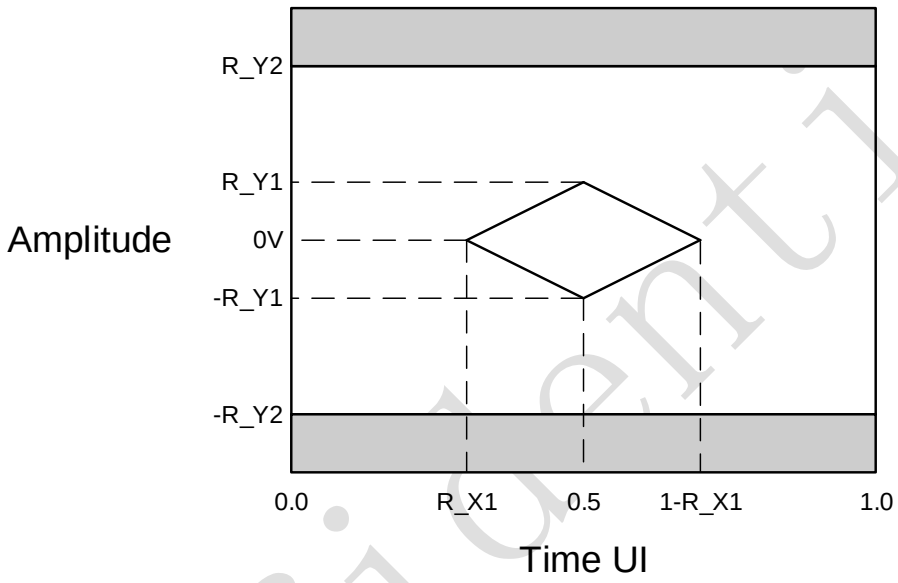


Figure 13. QSGMII Differential Receiver Eye Diagram

7.2.3. SGMII Differential Transmitter Characteristics

Table 125. SGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ± 75ppm
T_X1	Eye Mask	-	-	0.1875	UI	-

T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	200	-	-	mV	-
T_Y2	Eye Mask	-	-	450	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	700	900	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.625	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.375	UI	$T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.375UI
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling Capacitor	75	100	200	nF	-
L_{TX}	Transmit Length in PCB(FR4)	-	-	10	inch	-

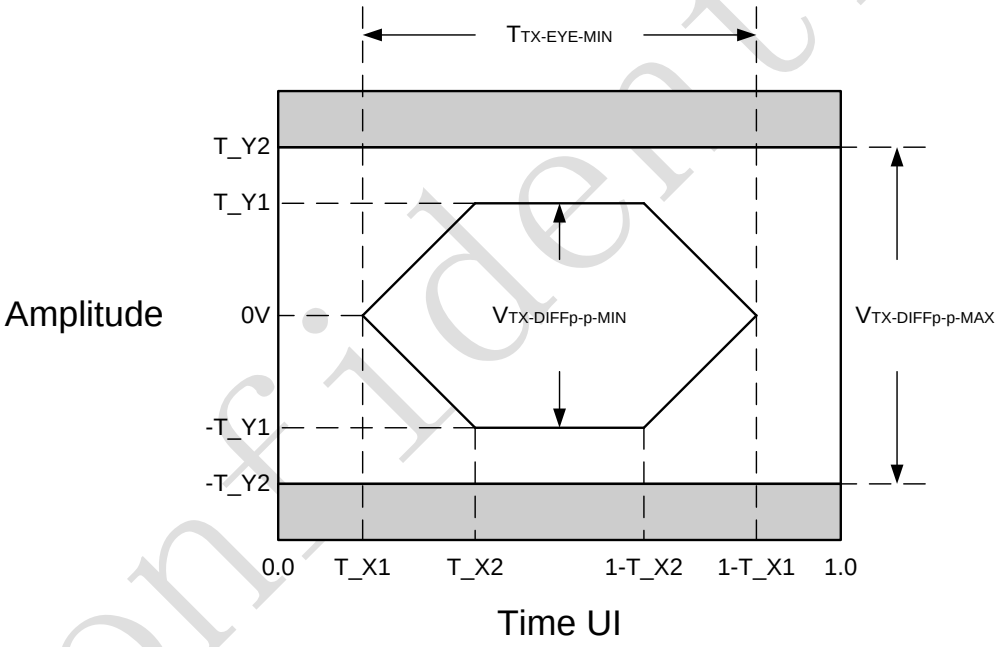


Figure 14. SGMII Differential Transmitter Eye Diagram

7.2.4. SGMII Differential Receiver Characteristics

Table 126. SGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ± 75ppm
R_X1	Eye Mask	-	-	0.3125	UI	-

R_Y1	Eye Mask	50	-	-	mV	-
R_Y2	Eye Mask	-	-	1000	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	100	-	2000	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.625	UI	$T_{RX-JITTER-MAX}$ = 1 - $T_{RX-EYE-MIN}$ = 0.625UI
R_{RX}	Differential Resistance	80	100	120	ohm	-

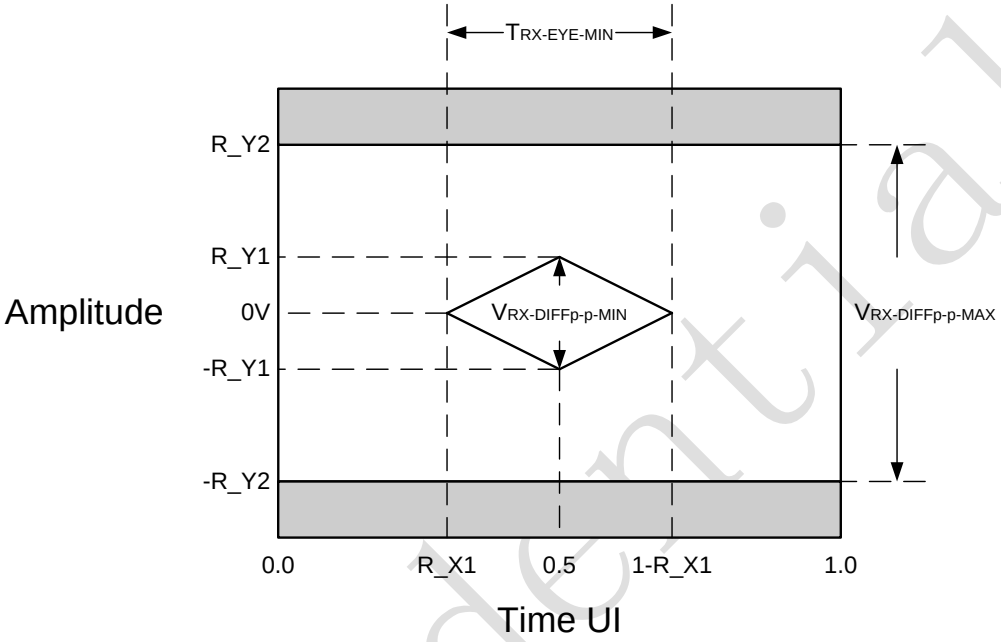


Figure 15. SGMII Differential Receiver Eye Diagram

7.2.5. 1000BASE-X Differential Transmitter Characteristics

Table 127. 1000BASE-X Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ± 75ppm
T_X1	Eye Mask	-	-	0.1875	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-

T_Y1	Eye Mask	200	-	-	mV	-
T_Y2	Eye Mask	-	-	450	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	700	900	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.625	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.375	UI	$T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.375UI
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling Capacitor	75	100	200	nF	-
L_{TX}	Transmit Length in PCB(FR4)	-	-	10	inch	-

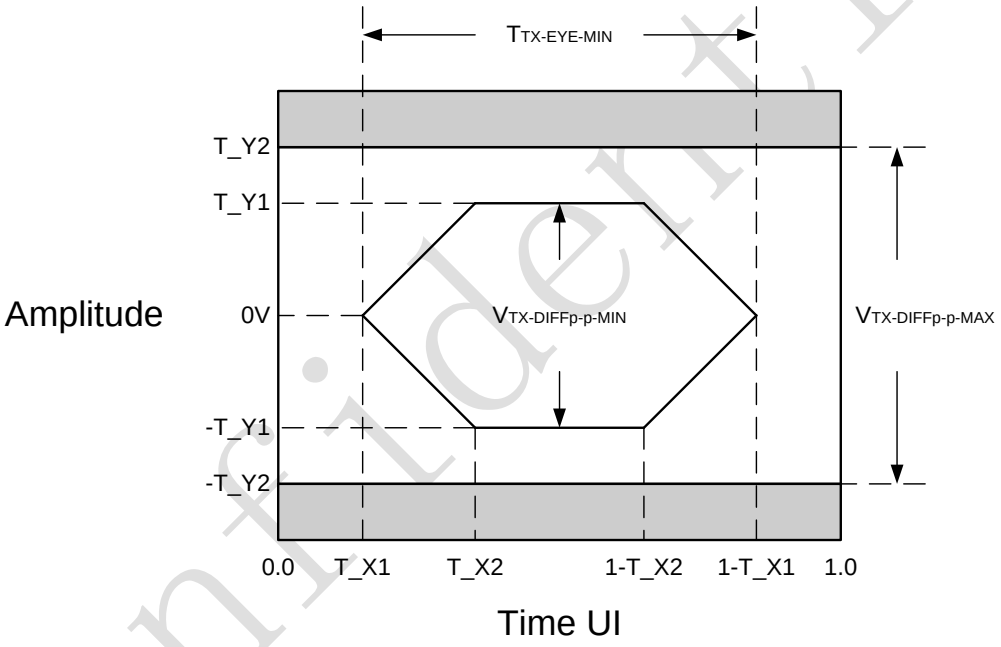


Figure 16. 1000BASE-X Differential Transmitter Eye Diagram

7.2.6. 1000BASE-X Differential Receiver Characteristics

Table 128. 1000BASE-X Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ± 75ppm
R_X1	Eye Mask	-	-	0.3125	UI	-
R_Y1	Eye Mask	50	-	-	mV	-
R_Y2	Eye Mask	-	-	1000	mV	-

$V_{RX-DIFFp-p}$	Input Differential Voltage	100	-	2000	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.625	UI	$T_{RX-JITTER-MAX}$ = 1 - $T_{RX-EYE-MIN}$ = 0.625UI
R_{RX}	Differential Resistance	80	100	120	ohm	-

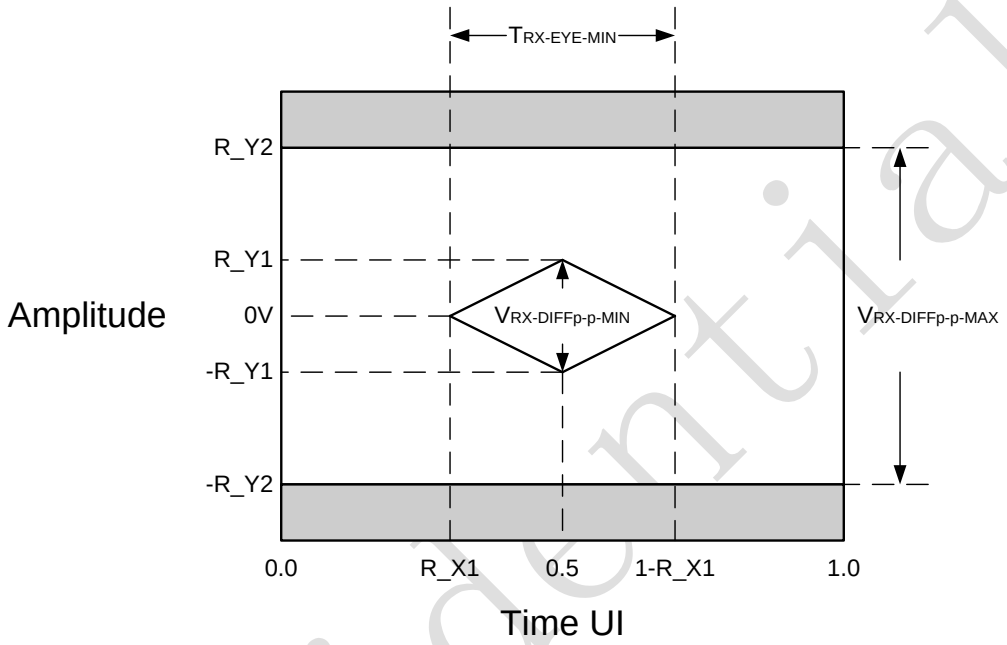


Figure 17. 1000BASE-X Differential Receiver Eye Diagram

7.2.7. MDC/MDIO Interface Characteristics

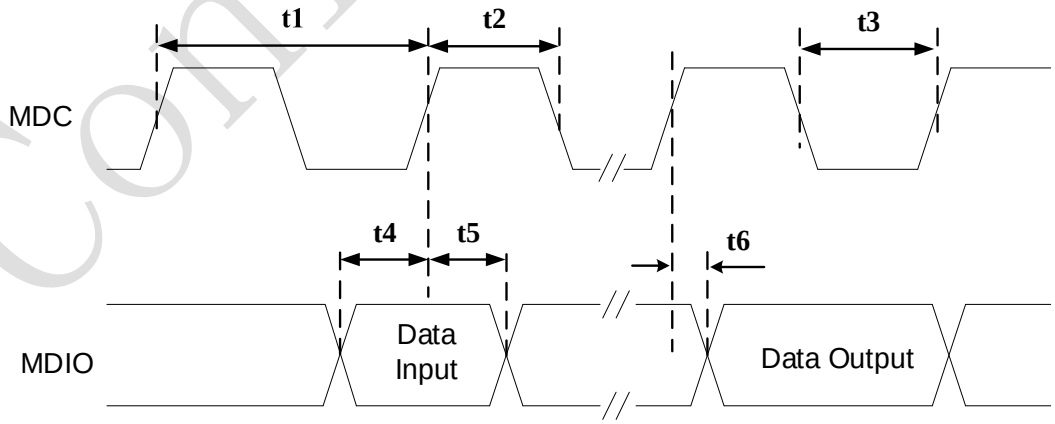


Figure 18. MDC/MDIO Timing Parameters

Table 129. MDC/MDIO Interface Characteristics

Symbol	Description	Min	Typ	Max	Units
t1	MDC Clock Period	80	-	-	ns

t2	MDC High Time	32	-	-	ns
t3	MDC Low Time	32	-	-	ns
t4	MDIO to MDC Rising Setup Time (Data Input)	10	-	-	ns
t5	MDIO to MDC Rising Hold Time (Data Input)	10	-	-	ns
t6	MDIO Valid from MDC rising edge (Data Output)	0	-	20	ns

7.2.8. Serial LED Timing

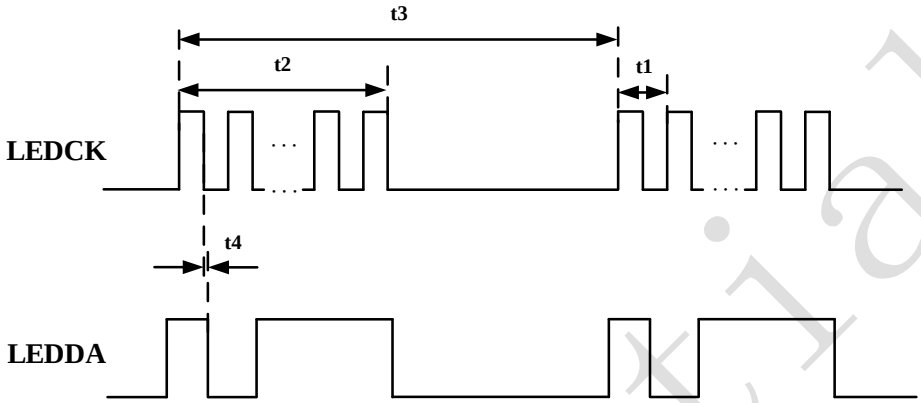


Figure 19. MDC/MDIO Timing Parameters

Table 130. MDC/MDIO Interface Characteristics

Symbol	Description	Min	Typ	Max	Units
t1	Serial LED Clock Cycle Time	-	160	-	ns
t2	Serial LED Clock On/Off Duration	-	5.68	-	us
t3	Serial LED Burst Cycle Time	-	32	-	ms
t4	LEDDA Valid from LEDCK falling edge	0	-	-	ns

7.3. Crystal Requirement

Table 131. Crystal Requirement

Symbol	Description	Min	Typ	Max	Unit
Fref	Parallel Resonant Crystal Reference Frequency	-	25	-	MHz
Fref Tolerance	Parallel Resonant Crystal Reference Frequency Tolerance	-50	-	50	ppm
Fref Duty Cycle	Reference Clock Input Duty Cycle	40	-	60	%
ESR	Equivalent Series Resistance	-	-	50	ohm
DL	Drive Level	-	-	0.5	mW
Vih	Crystal output high level	1.5	-	-	V
Vil	Crystal output low level	-	-	0.4	V

7.4. Oscillator/External Clock Requirement

Table 132. Oscillator/External Clock Requirement

Parameter	Min	Typ	Max	Unit
Frequency	-	25	-	MHz
Frequency tolerance	-50	-	50	PPM
Duty Cycle	40	-	60	%
Vih	1.5	-	-	V
Vil	-	-	0.4	V
Rise Time (10%~90%)	-	-	10	ns
Fall Time (10%~90%)	-	-	10	ns
RMS Jitter (12kHz~20MHz)	-	-	1	ps

8. Power Requirements

8.1. Absolute Maximum Ratings

Table 133. Absolute Maximum Ratings

Description	Symbol	Min	Max	Unit
3.3 V power supply	DVDDIO, AVDDH, SVDDH	-0.3	3.63	V
1.2 V power supply	DVDDL, AVDDL,SVDDL, PLLVDDL	-0.2	1.32	V
Junction Temperature		-	125	℃
Storage Temperature		-45	125	℃

8.2. Recommended Operating Conduction

Table 134. Recommended Operating Conduction

Description	Symbol	Min	Typ	Max	Unit
3.3 V power supply	DVDDIO, AVDDH, SVDDH	3.135	3.30	3.465	V
1.2 V power supply	DVDDL, AVDDL, SVDDL, PLLVDDL	1.14	1.20	1.26	V
Ambient Operation Temperature Ta Commercial		0.00	-	70.00	℃
Ambient Operation Temperature Ta Industry		-40.00	-	85.00	℃

8.3. Power and Reset Sequence

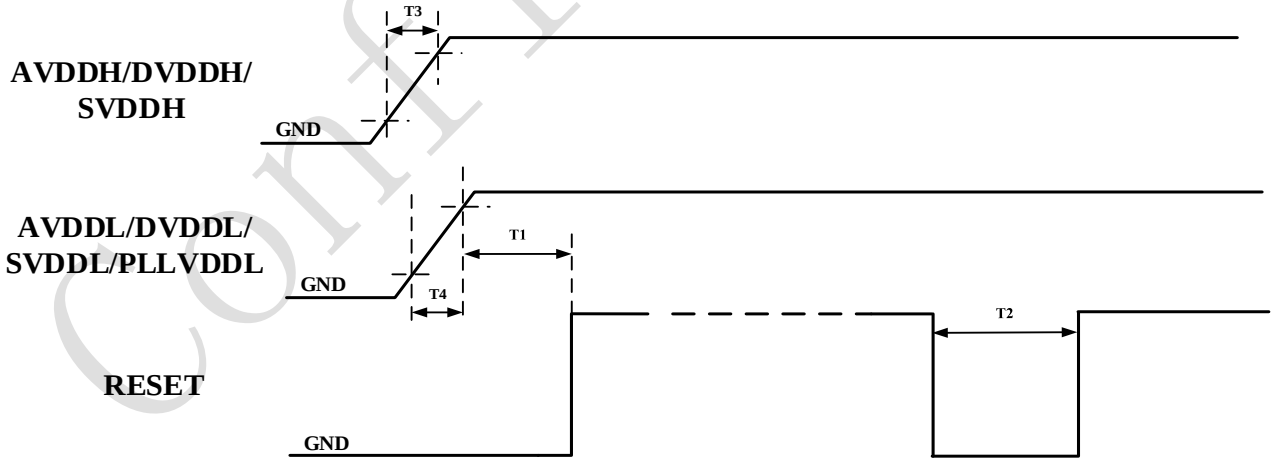


Figure 20. Power and Reset Sequence

Table 135. Power and Reset Sequence

Symbol	Description	Min	Typ	Max	Units
T1	The duration from all powers steady to reset signal release to high.	10	-	-	ms

T2	The duration of reset signal remain low timing.	10	-	-	ms
T3	AVDDH/DVDDH/SVDDH power rising time.	0.5	-	-	ms
T4	AVDDL/DVDDL/SVDDL/PLLVDDL power rising time.	0.5	-	-	ms

8.4. Power Ripple

The ripple of AVDDH/DVDDH/SVDDH should be less then 50mV.

The ripple of AVDDL/DVDDL/SVDDL/PLLVDDL should be less than 30mV.

8.5. Power Consumption

8.5.1. QSGMII x 2 + Copper x 8

Table 136. QSGMII x 2 + Copper x 8 Power Consumption

Condition	AVDDH (mA)	DVDDH (mA)	SVDDH (mA)	AVDDL (mA)	DVDDL (mA)	SVDDL (mA)	Power Consumption (mW)
Reset	46.2	0.1	2.1	2.2	12.1	6	184.08
Power Down	46.8	0	2.1	2.8	11.8	6.8	187.05
Link Up @1000Mbps	557.6	5.9	30.7	360.4	775.9	106.5	3452.22
Traffic @1000Mbps	556.2	5.9	30.8	361	890.2	106.9	3586.29

Note: Test by TT IC with VDDH = 3.3V and VDDL = 1.2V at room temperature.

8.5.2. QSGMII x 1 + SGMII x 1 + Copper x 5

Table 137. QSGMII x 1 + SGMII x 1 + Copper x 5 Power Consumption

Condition	AVDDH (mA)	DVDDH (mA)	SVDDH (mA)	AVDDL (mA)	DVDDL (mA)	SVDDL (mA)	Power Consumption (mW)
Power Down	46.8	0	2.1	2.8	11.7	7.5	187.77
Link Up @1000Mbps	370.4	5.9	30.4	231.2	496.4	99.6	2334.75
Traffic @1000Mbps	369.3	5.9	30.4	231.5	572	100	2422.68

Note: Test by TT IC with VDDH = 3.3V and VDDL = 1.2V at room temperature.

8.5.3. QSGMII x 1 + Copper x 3 + Combo x 1

Table 138. QSGMII x 1 + Copper x 3 + Combo x 1 Power Consumption

Condition	AVDDH (mA)	DVDDH (mA)	SVDDH (mA)	AVDDL (mA)	DVDDL (mA)	SVDDL (mA)	Power Consumption (mW)

Power Down	46.8	0	2.1	2.8	11.7	7.5	187.77
Link Up @1000Mbps (Combo is Copper)	300.1	5.9	30.4	182.2	403.8	56.3	1880.88
Traffic @1000Mbps (Combo is Copper)	299.3	5.9	30.4	182.3	465.3	56.8	1952.76
Link Up @1000Mbps (Combo is Fiber)	235.2	5.9	30.4	137.1	316.7	99.4	1559.79
Traffic @1000Mbps (Combo is Fiber)	234.7	5.9	30.4	137.2	364.6	100	1616.46

Note: Test by TT IC with VDDH = 3.3V and VDDL = 1.2V at room temperature.

8.5.4. SGMII x 2 + Copper x 2

Table 139. SGMII x 2 + Copper x 2 Power Consumption

Condition	AVDDH (mA)	DVDDH (mA)	SVDDH (mA)	AVDDL (mA)	DVDDL (mA)	SVDDL (mA)	Power Consumption (mW)
Power Down	46.8	0	2.1	2.8	11.7	8.2	188.61
Link Up @1000Mbps	182.4	5.9	30.2	101.7	213.2	93.3	1210.89
Traffic @1000Mbps	182.1	5.9	30.2	101.8	245.9	93.8	1249.86

Note: Test by TT IC with VDDH = 3.3V and VDDL = 1.2V at room temperature.

8.5.5. SGMII x 1 + Combo x 1

Table 140. SGMII x 1 + Combo x 1 Power Consumption

Condition	AVDDH (mA)	DVDDH (mA)	SVDDH (mA)	AVDDL (mA)	DVDDL (mA)	SVDDL (mA)	Power Consumption (mW)
Power Down	46.8	0	2.1	2.8	11.7	8.2	188.61
Link Up @1000Mbps (Combo is Copper)	117.6	0	30.1	52.1	115.7	50.4	749.25
Traffic @1000Mbps (Combo is Copper)	117.5	0	30.1	52.1	132.6	50.6	769.44
Link Up @1000Mbps (Combo is Fiber)	46.8	0	30.1	2.8	24	93	397.53
Traffic @1000Mbps (Combo is Fiber)	46.8	0	30.1	2.8	24.9	93.4	399.09

Note: Test by TT IC with VDDH = 3.3V and VDDL = 1.2V at room temperature.

8.6. Maximum Power Consumption

Table 141. Maximum Power Consumption

Condition	AVDDH (mA)	DVDDH (mA)	SVDDH (mA)	AVDDL (mA)	DVDDL (mA)	SVDDL (mA)	Power Consumption (mW)
Reset	49	0.1	2.2	2.3	12.8	6.4	195.09
Power Down	49.6	0	2.2	3	12.5	7.2	198.18
Link Up @1000Mbps	591.1	6.3	32.5	382	822.5	112.9	3659.55
Traffic @1000Mbps	589.6	6.3	32.6	382.7	943.6	113.3	3801.57

*Note: Test by FF corner IC in **QSGMII x 2 + Copper x 8** mode with VDDH = 3.3V and VDDL = 1.2V at high temperature 85℃.*

9. Thermal Characteristics

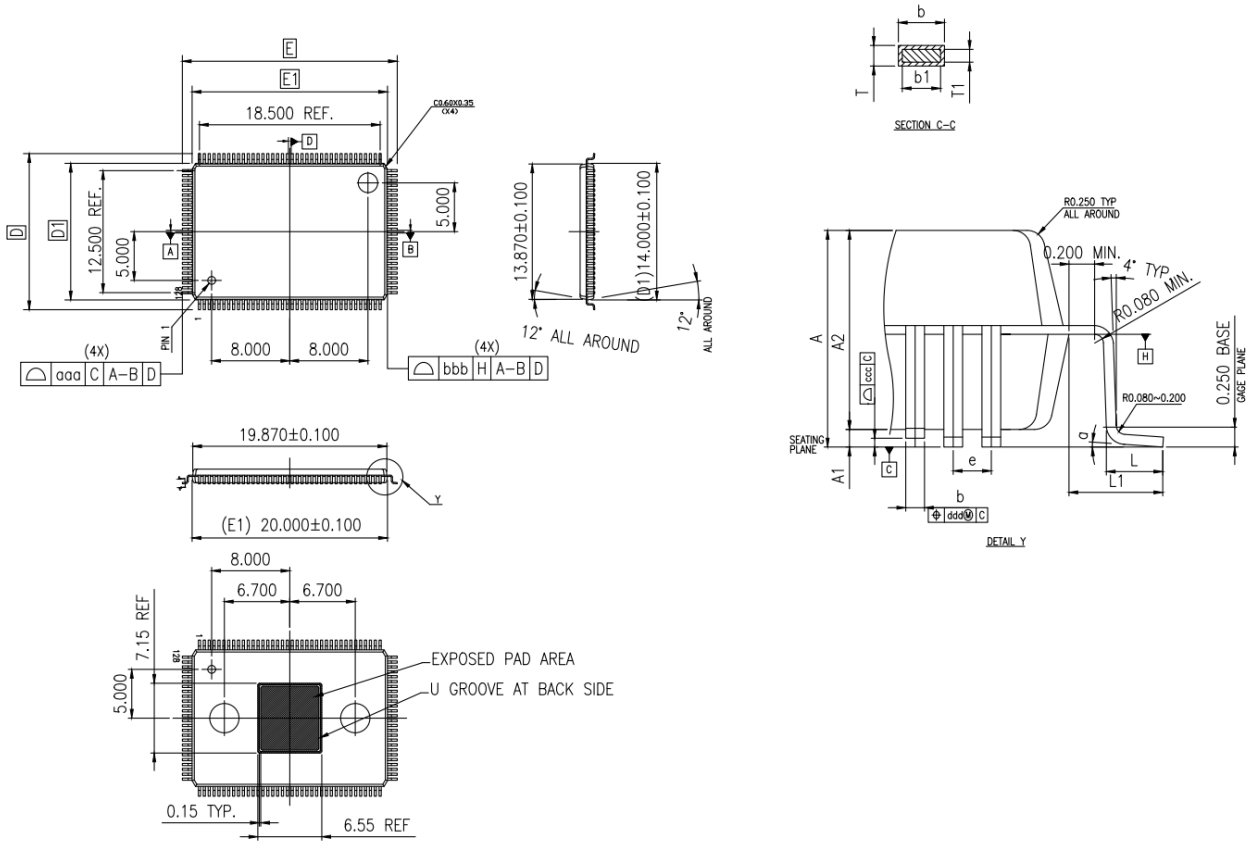
9.1. Thermal Resistance

Table 142. Thermal Resistance

Symbol	Parameter	Condition	Typ	Units
θJA	Thermal resistance - junction to ambient θJA = (TJ - TA)/ P P = Total power dissipation	JEDEC 3.0 in. x 4.5 in. 4-layer PCB with no air flow TA=25°C	20.79	°C/W
		JEDEC 3.0 in. x 4.5 in. 4-layer PCB with no air flow TA=85°C	18.98	°C/W
θJC	Thermal resistance - junction to case θJC = (TJ - TC)/ Ptop Ptop = Power dissipation from the top of the package	JEDEC with no air flow	14.69	°C/W
θJB	Thermal resistance - junction to board θJB = (TJ - TB)/ Pbottom Pbottom = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow	9.78	°C/W

10. Package Information

10.1. LQFP-128 E-PAD



10.2. Mechanical Dimensions

DIMENSION LIST (FOOTPRINT: 2.00)

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.10±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	16.00±0.10	LEAD TIP TO TIP
5	D1	14.00±0.10	PKG LENGTH
6	E	22.00±0.10	LEAD TIP TO TIP
7	E1	20.00±0.10	PKG WIDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF.	LEAD LENGTH
10	T	$0.15^{+0.05}_{-0.06}$	FRAME THICKNESS
11	T1	0.127±0.030	FRAME BASE METAL THICKNESS
12	α	0°~7°	FOOT ANGLE
13	b	0.22±0.05	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH

11. Ordering Information

Motorcomm offers an RoHS package that is compliant with RoHS

Part Number	Grade	Package	Pack	Status	Operation Temp
YT8618C	Consumer	LQFP-128 E-PAD	Tray 720ea	Mass Production	0 ~70°C
YT8618H	Industrial	LQFP-128 E-PAD	Tray 720ea	Mass Production	-40 ~ 85°C