CA-IF1051H +5V, ±70V Fault Protected CAN Transceiver with CAN FD

1. Features

- **Meets the ISO 11898-2:2016 and ISO 11898-5:2007 physical layer standards**
- **'Turbo' CAN:**
  - Support classic CAN and 5 Mbps CAN FD (flexible data rate)
  - Short and symmetrical propagation delay times and fast loop times for enhanced timing margin
  - Higher data rates in loaded CAN networks
- **Ideal passive behavior when unpowered**
  - Bus and logic terminals are high impedance (no load)
  - Power up/down with glitch free operation on bus and RXD output
- **Integrated protection increases robustness**
  - ±70V fault-tolerant CANH and CANL
  - ±30V extended common-mode input range (CMR)
  - Undervoltage protection on V_{CC} supply terminal
  - Transmitter dominant timeout prevents lockup, data rates down to 5.5 kbps
  - Thermal shutdown
  - Junction temperatures from –55°C to 150°C
- **Typical loop delay: 130ns**
- **Available in SOIC(8) package**

2. Applications

- Industrial automation
- Building automation
- HVAC systems
- Distribution automation
- Vending machines
- Security systems

3. General Description

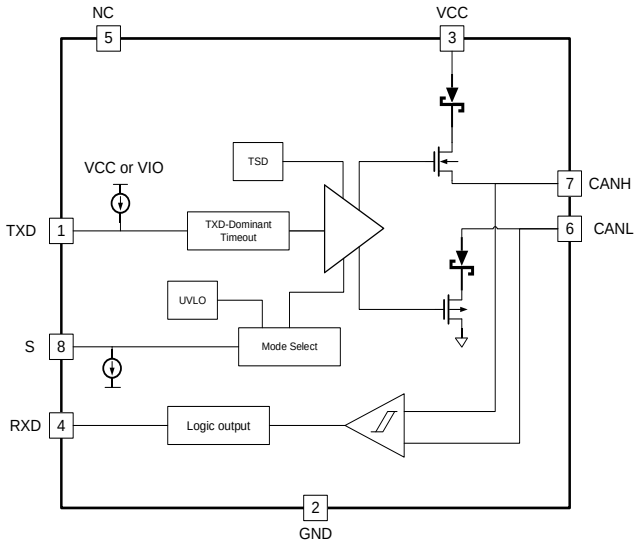
CA-IF1051H is +5V control area network (CAN) transceivers with integrated protection for industrial applications. This device is designed for using in CAN FD networks up to 5 Mbps and features extended ±70V fault protection on the CAN bus for equipment where overvoltage protection is required. This CAN device also incorporates an input common-mode range (CMR) of ±30V, exceeding the ISO 11898 specification of -2V to +7V, and well suited for applications where ground planes from different systems are shifting relative to each other.

The transceivers include a dominant timeout to prevent bus lockup caused by controller error or by a fault on the TXD input. When TXD remains in the dominant state (low) for longer than t_{DOM}, the driver is switched to the recessive state, releasing the bus. In addition, this device comes with silent mode which is also commonly referred to as listen-only mode.

The CA-IF1051H is in a standard 8-pin narrow-body SOIC package and operates over the -55°C to +150°C junction temperature range.

Device Information

Part number	Package	Package size (NOM)
CA-IF1051HS	SOIC8(S)	4.9mm x 3.9mm



Simplified Block Diagram

4. Ordering Information

Table 4-1 Ordering Information

Part Number	Package	Size (NOM)
CA-IF1051HS	SOIC8	4.9mm*3.91mm

Contents

5. Revision History

Revision Number	Description	Page Changed
Version 1.0	N/A	N/A
Version 1.01	Updated previous of Version 1.0 to Version 1.01	N/A
Version 1.02	Changed in the logic interface table Pin S and TXD: V_{IH} min value to 2.8V, V_{IL} max value to 1.4V	6

6. Pin Configuration and Functions

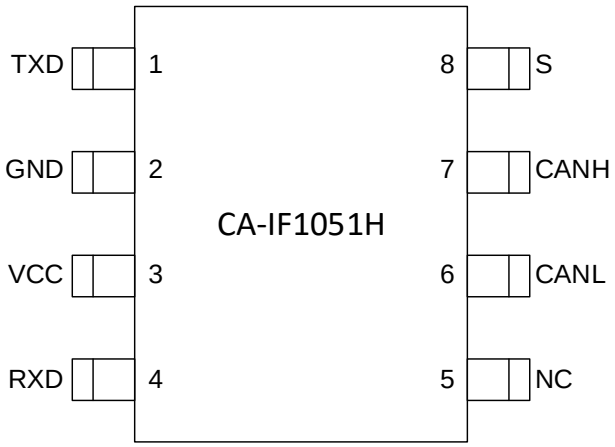


Figure 6-1 CA-IF1051H Pin Configuration

Table 6-1 CA-IF1051H Pin Configuration and Description

Pin Name	Pin #	Type	Description
TXD	1	Digital Input	Transmit Data Input, LOW for dominant and HIGH for recessive bus states. TXD is a CMOS/TTL compatible input from a CAN controller with an internal pull-up to V_{CC}.
GND	2	GND	Ground.
VCC	3	Power	+5V Supply Voltage. Bypass V_{CC} to GND with an at least 0.1μF capacitor.
RXD	4	Digital Output	Receive Data Output, LOW for dominant and HIGH for recessive bus states. RXD is a CMOS/TTL compatible output from the physical bus lines CANH and CANL.
NC	5	NC	No connect.
CANL	6	Bus I/O	CAN bus line low.
CANH	7	Bus I/O	CAN bus line high.
S	8	Digital Input	Silent Mode Input. Drive S low or leave it open to enable driver and to operate in normal mode. Drive S high to disable the transmitter.

7. Specifications

7.1. Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNIT
V_{CC}	5-V Bus Supply Voltage Range	-0.3	7	V
V_{BUS}	CAN Bus I/O voltage range (CANH,CANL)	-70	70	V
$V_{(DIFF)}$	Max differential voltage between CANH and CANL	-70	70	V
$V_{(Logic\_Input)}$	Logic input terminal voltage range (TXD, S)	-0.3	+7	V
$V_{(Logic\_Output)}$	Logic output terminal voltage range (RXD)	-0.3	+7	V
$I_{O(RXD)}$	RXD (receiver) terminal output current	-8	8	mA
T_J	Virtual junction temperature range	-55	150	℃
T_{STG}	Storage temperature range	-65	150	℃

Note:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

7.2. ESD Ratings

Parameters	TEST CONDITIONS		VALUE	UNIT
CA-IF1051HS				
HBM[1] ESD	CAN bus terminals (CANH, CANL) to GND		±6000	V
	Other pins		±4000	
CDM ESD	All pins		±1500	V
System Level ESD	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-2: unpowered contact discharge.	±4000[2]	V
ISO7637 transient per GIFT-ICT CAN EMC test	CAN bus terminals (CANH, CANL) to GND	ISO Pulse 1	-100	V
		ISO Pulse 2	+75	V
		ISO Pulse 3a	-150	V
		ISO Pulse 3b	+100	V
ISO7637-3 transient	CAN bus terminals (CANH, CANL) to GND	Slow transient with 100nF coupling — powered	±85	V

Note:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Testing on System Board Level.

7.3. Recommended Operating Conditions

PARAMETER		MIN	MAX	UNIT
V_{CC}	Supply Voltage Range	4.5	5.5	V
$I_{OH(RXD)}$	RXD terminal high level output current	-2		mA
$I_{OL(RXD)}$	RXD terminal low level output current		2	mA

7.4. Thermal Information

Thermal Metric		SOIC8-NB	UNIT
$R_{\theta JA}$	Junction to Ambient	125	°C/W

7.5. Electrical Characteristics

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{cc}	5V Supply Current	TXD=0V, R_L = 60 Ω (dominant), see Figure 8-1		45	80	mA
		TXD=0V, R_L = 50 Ω (dominant), see Figure 8-1		50	90	mA
		TXD=0V, CANH = -12V (dominant), see Figure 8-1			180	mA
		TXD=V_{CC}, R_L = 50Ω (recessive), see Figure 8-1		0.7	2.0	mA
		S=V_{CC} (silent mode), seeFigure 8-1		0.6	2.0	mA
V_{uv_vcc}	UVLO Threshold	Rising		4.2	4.4	V
V_{uv_vcc}	UVLO Threshold	Falling	3.8	4.0	4.25	V
$V_{uv\_vcc\_hys}$	UVLO Threshold	Hysteresis		0.2		V
LOGIC INTERFACE (Mode select input, S)						
V_{IH}	High-level input voltage		2.8			V
V_{IL}	Low-level input voltage				1.4	V
I_{IH}	High-level input leakage current	S = V_{CC}			30	µA
I_{IL}	Low-level input leakage current	S = 0V, V_{CC} = 5.5V	-2		2	µA
$I_{lek(off)}$	Unpowered leakage current	S = 5.5V, V_{CC} = 0V	-1		1	µA
LOGIC INTERFACE (CAN transmit data input, TXD)						
V_{IH}	High-level input voltage		2.8			V
V_{IL}	Low-level input voltage				1.4	V
I_{IH}	High-level input leakage current	S = V_{CC}	-2.5	0	1	µA
I_{IL}	Low-level input leakage current	S = 0V, V_{CC} = 5.5V	-100	-47	-7	µA
$I_{lek(off)}$	Unpowered leakage current	S = 5.5V, V_{CC} = 0V	-1	0	1	µA
C_i	Input capacitance	V_{IN} = 0.4 * sin(4E6*π*t) + 2.5V		5		pF
LOGIC INTERFACE (CAN receive data output, RXD)						
V_{OH}	High-level output voltage	Io = -2mA, seeFigure 8-2	0.8xV_{CC}			V
V_{OL}	Low-level output voltage	Io = +2mA, see Figure 8-2			0.2xV_{CC}	V
$I_{lek(off)}$	Unpowered leakage current	S = 5.5V, V_{CC} = 0V	-1	0	1	µA

Electrical Characteristics (continued)

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN BUS DRIVER						
$V_{O(DOM)}$	Bus output voltage (dominant)	TXD = low, S = 0V, R_L=50 -65 Ω, CANH, see Figure 8-1	2.75		4.5	V
		TXD = low, S = 0V, R_L = 50 -65 Ω, CANL, see Figure 8-1	0.5		2.25	V
$V_{OD(DOM)}$	Bus output differential voltage (dominant)	TXD = low, R_L = 60 Ω , R_{CM} =156 Ω, -5V≤V_{CM} ≤+10V, see Figure 8-1	1.5		3.0	V
		TXD = low, R_L=45-50 Ω , R_{CM} open, see Figure 8-1	1.4		3.0	V
		TXD = low, R_L=45-50 Ω , R_{CM} open, see Figure 8-1	1.5		3.0	V
		TXD = low, R_L=2240 Ω , R_{CM} open, see Figure 8-1	1.5		5.0	V
$V_{O(REC)}$	Bus output voltage (recessive)	TXD = high, no load, CANH, see Figure 8-1	2		3	V
		TXD = high, no load, CANL, see Figure 8-1	2		3	V
$V_{OD(REC)}$	Bus output differential voltage (recessive)	TXD = high, S=0V, R_L=60 Ω, see Figure 8-1	-120		12	mV
		TXD = high, S=0V, no load, see Figure 8-1	-50		+50	mV
$I_{OS(SS\_DOM)}$	Short-circuit current (dominant)	TXD = low, CANL open,V_{CANH}= -15Vto 40V, see Figure 8-7	-100			mA
		TXD = low, CANH open, V_{CANL} = -15V to 40V, see Figure 8-7			100	mA
$I_{OS(SS\_rec)}$	Short-circuit current (recessive)	TXD = high, V_{BUS}= -27V to 32V, see Figure 8-7	-5		5	mA
V_{SYM}	Transient symmetry (dominant or recessive)	R_L = 60 Ω, R_{CM} open , TXD = 250kHz, 1MHz, see Figure 8-1		0.9		V/V
V_{SYM_DC}	DC Output symmetry (dominant or recessive)	RL =60 Ω, R_{CM} open, see Figure 8-1		-0.2		V
CAN RECEIVER						
V_{CM}	Common-mode input range	CANH or CANL to GND, RXD output valid, see Figure 8-2	-30		+30	V
V_{DIFF_R}	Input differential threshold voltage (recessive)	TXD = high, V_{CM} = -20V to 20V, see Figure 8-2	0.5			V
V_{DIFF_D}	Input differential threshold voltage (dominant)	TXD = high, V_{CM} = -20V to 20V, see Figure 8-2			0.9	V
V_{DIFF_R}	Input differential threshold voltage (recessive)	TXD = high, V_{CM} = -30V to 30V, see Figure 8-2	0.4			V
V_{DIFF_D}	Input differential threshold voltage (dominant)	TXD = high, V_{CM} = -30V to 30V, see Figure 8-2			1	V
$V_{DIFF\_(HYS)}$	Input differential hysteresis	S = 0 or V_{CC} or V_{IO}		120		mV
R_{IN}	CANH/CANL input resistance	TXD = high, V_{CM} = -30V to 30V	15		40	kΩ
R_{DIFF}	Differential input resistance	TXD = high, V_{CM} = -30V to 30V	30		80	kΩ
$R_{DIFF\ (M)}$	Input resistance matching	V_{CANH} = V_{CANL} =5V	-2		2	%
I_{LKG}	Input Leakage Current	V_{CC} = 0V, V_{CANH} = V_{CANL} =5V		4.8		μA
C_{IN}	Input capacitance	CANH or CANL to GND		24		pF
C_{IN_DIFF}	Differential input capacitance	CANH to CANL		12		pF

7.6. Switching Characteristics

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
t_R	Driver rise time	R_L=60 Ω, C_L=100pF , see Figure 8-1		55		ns
t_F	Driver fall time	R_L=60 Ω, C_L=100pF, see Figure 8-1		60		ns
t_{ONTXD}	TXD propagation delay (recessive to dominant)	R_L=60 Ω, C_L=100pF, see Figure 8-1		55		ns
t_{OFFTXD}	TXD propagation delay (dominant to recessive)	R_L=60 Ω, C_L=100pF, see Figure 8-1		40		ns
Tsk(p)	Pulse skew	R_L=60 Ω, C_L=100pF, see Figure 8-1		20		ns
t_{DOM}	TXD-dominant Timeout	R_L=60 Ω, C_L open, see Figure 8-5	2	5	8	ms
RECEIVER						
t_{ONRXD}	RXD propagation delay (recessive to dominant)	C_L=15pF, see Figure 8-2		95		ns
t_{OFFRXD}	RXD Propagation delay (dominant to recessive)	C_L=15pF, see Figure 8-2		65		ns
t_R	RXD Output signal rise time	C_L=15pF, see Figure 8-2		40		ns
t_F	RXD Output signal fall time	C_L=15pF, see Figure 8-2		30		ns
DEVICE						
t_{loop1}	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	R_L=60 Ω,C_L=100pF, see Figure 8-3		120	160	ns
t_{loop2}	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	R_L=60 Ω,C_L=100pF, see Figure 8-3		130	175	ns
t_{MODE}	Mode change time, from normal to silent or from silent to normal	see Figure 8 -4		0.13	10	µs
FD TIMING						
$t_{bit(bus)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L=100pF, C_{LRX}=15pF, see Figure 8-6	435		550	ns
$t_{bit(bus)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns	R_L = 60 Ω, C_L=100pF, C_{LRX}=15pF, see Figure 8-6	155		240	ns
$t_{bit(rxd)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L=100pF, C_{LRX}=15pF, see Figure 8-6	400		550	ns
$t_{bit(rxd)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns	R_L = 60 Ω, C_L=100pF, C_{LRX}=15pF, see Figure 8-6	120		220	ns
t_{rec}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500ns	R_L = 60 Ω, C_L=100pF, C_{LRX}=15pF, see Figure 8-6	-70		40	ns
t_{rec}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200ns	R_L = 60 Ω, C_L=100pF, C_{LRX}=15pF, see Figure 8-6	-40		15	ns

7.7. Typical Characteristics

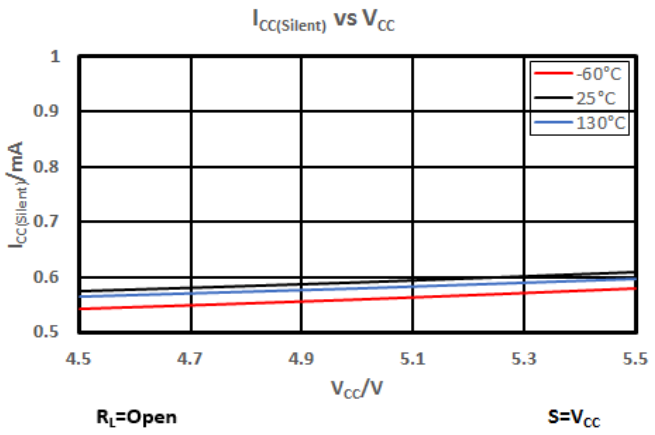


Figure 7-1 Supply Current @ Silent Mode

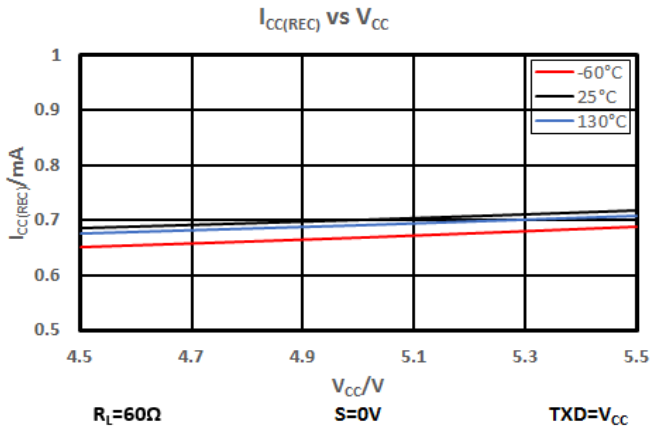


Figure 7-2 Supply Current Recessive

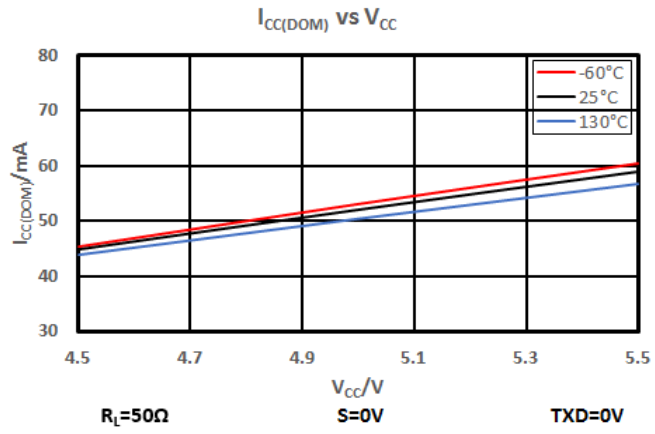


Figure 7-3 Supply Current Dominant (R_L = 50Ω)

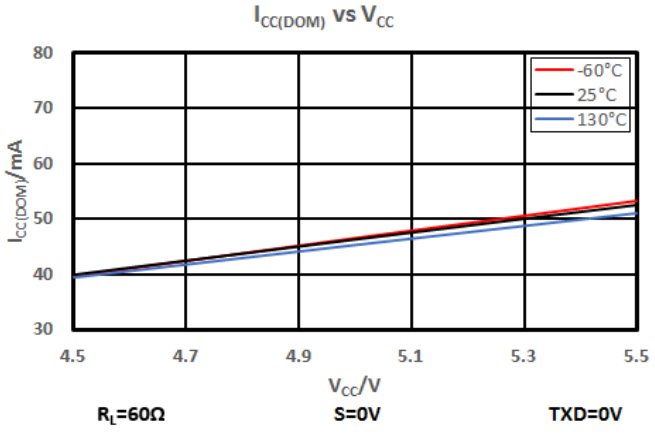


Figure 7-4 Supply Current Dominant (R_L = 50Ω)

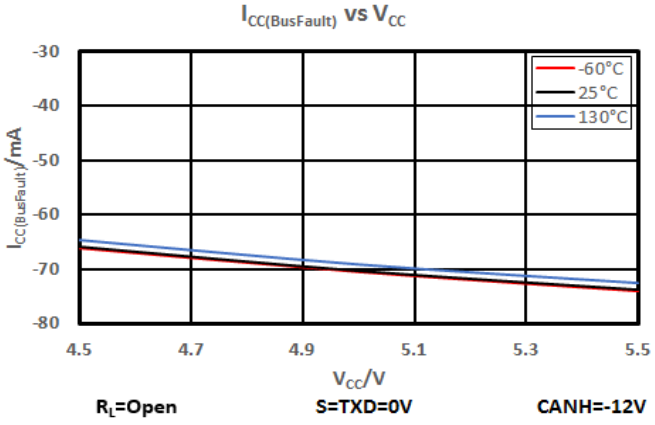


Figure 7-5 Bus Fault Current

Typical Characteristics (continued)

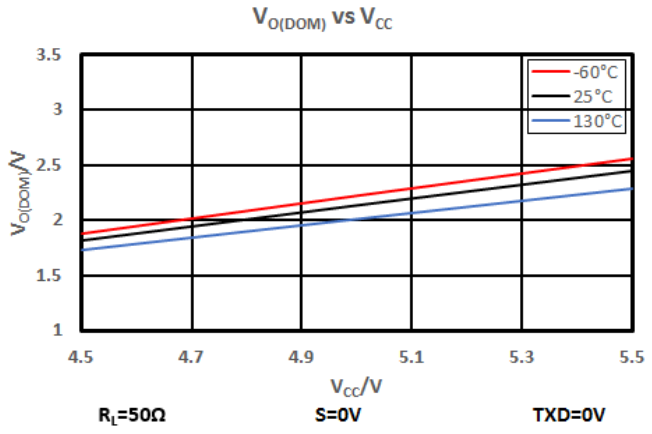


Figure 7-6 Differential Output Voltage vs. V_{CC} (R_L = 50Ω)

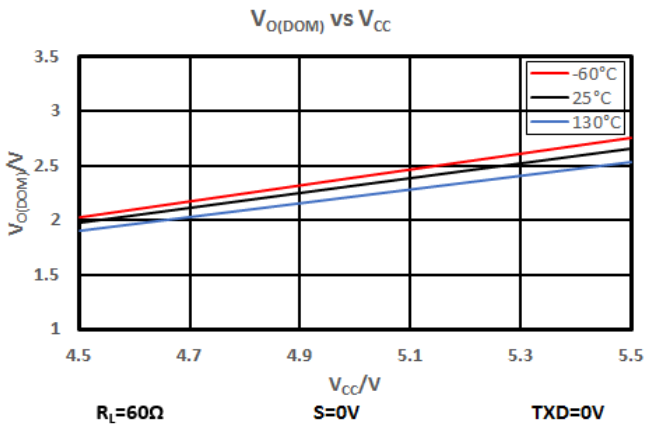


Figure 7-7 Differential Output Voltage vs. V_{CC} (R_L = 60Ω)

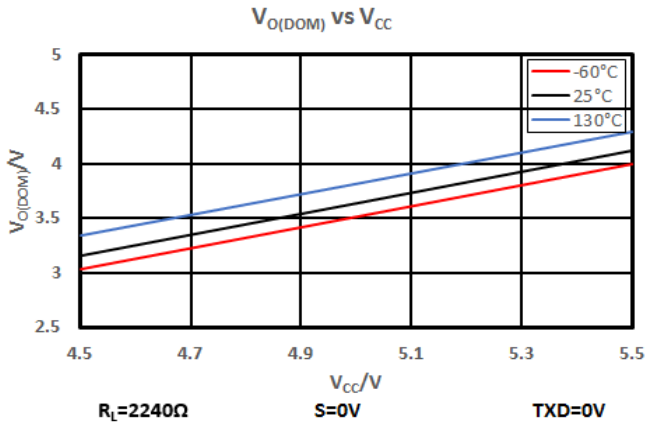


Figure 7-8 Differential Output Voltage vs. V_{CC} (R_L = 240Ω)

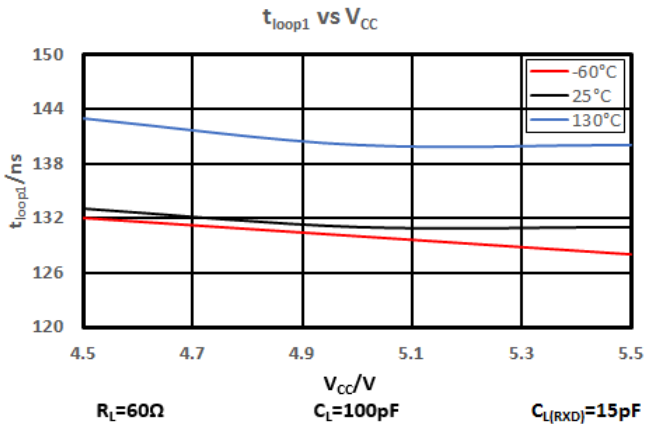


Figure 7-9 Loop Delay, Recessive to Dominant

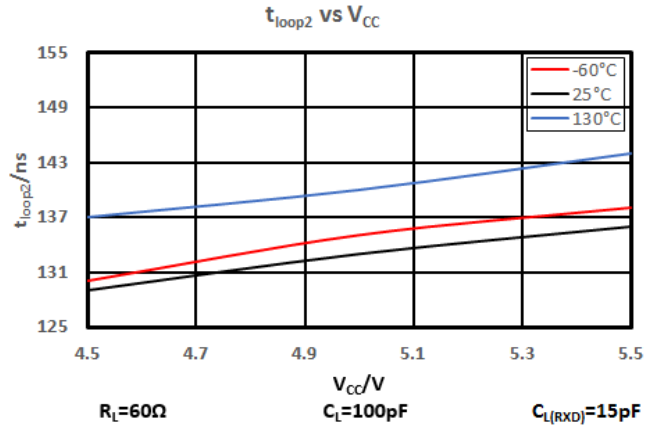


Figure 7-10 Loop Delay, Dominant to Recessive

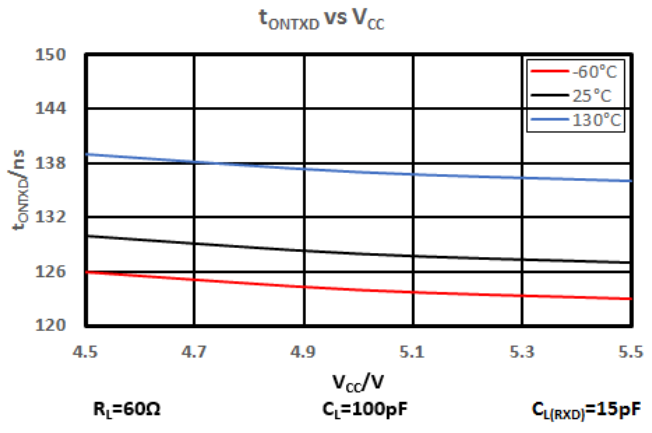


Figure 7-11 Mode Change Time

8. Parameter Measurement Information

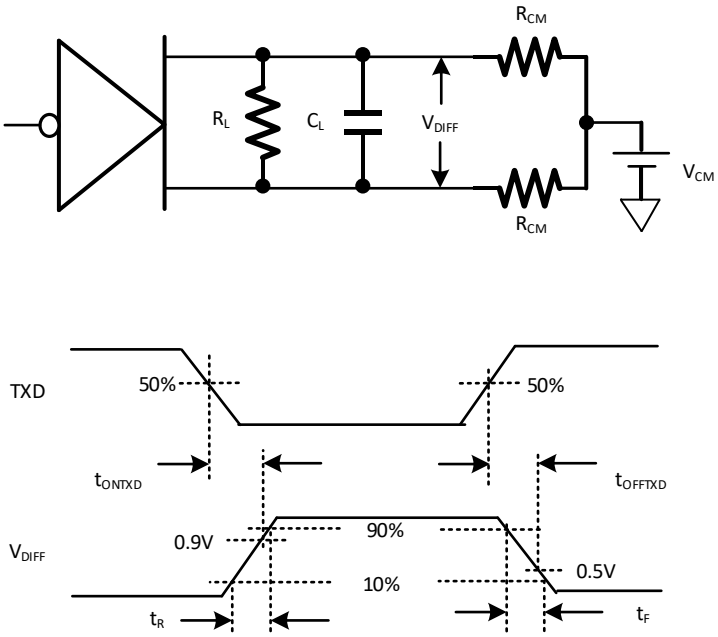


Figure 8-1 Transmitter Test Circuit and Timing Diagram

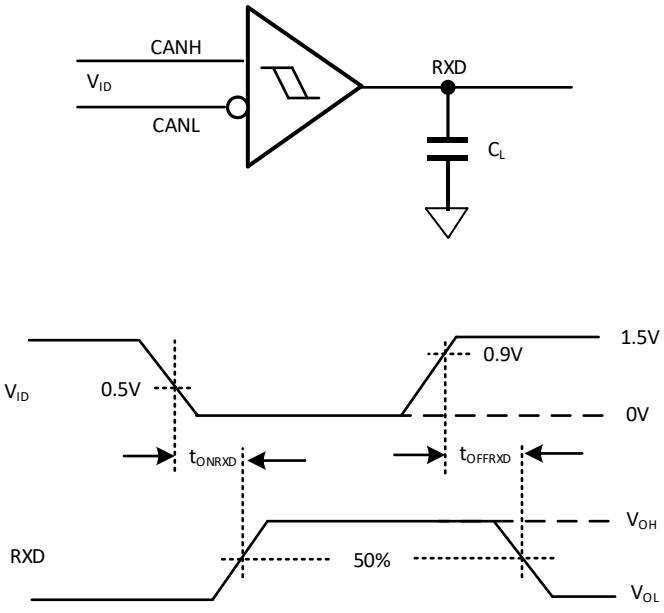


Figure 8-2 Receiver Test Circuit and Measurement

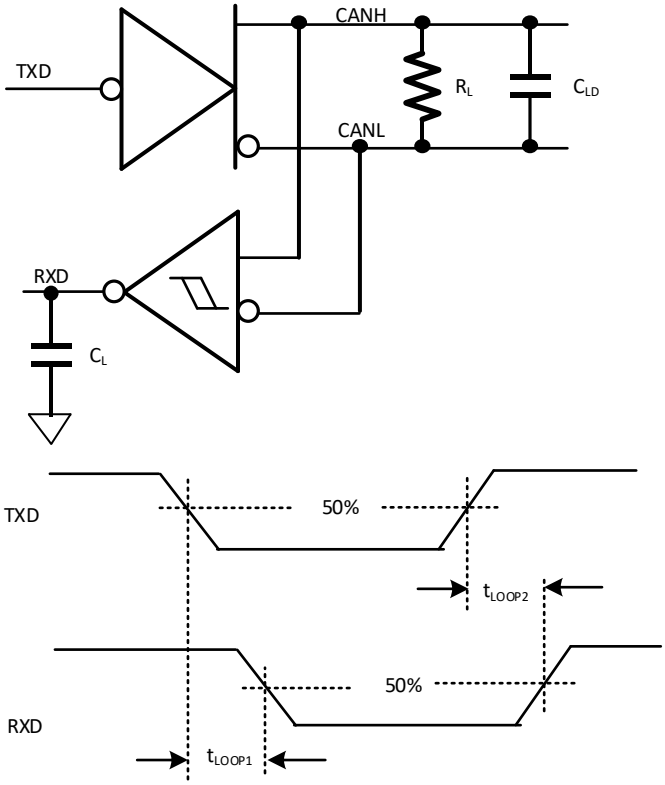


Figure 8-3 TXD to RXD Loop Delay

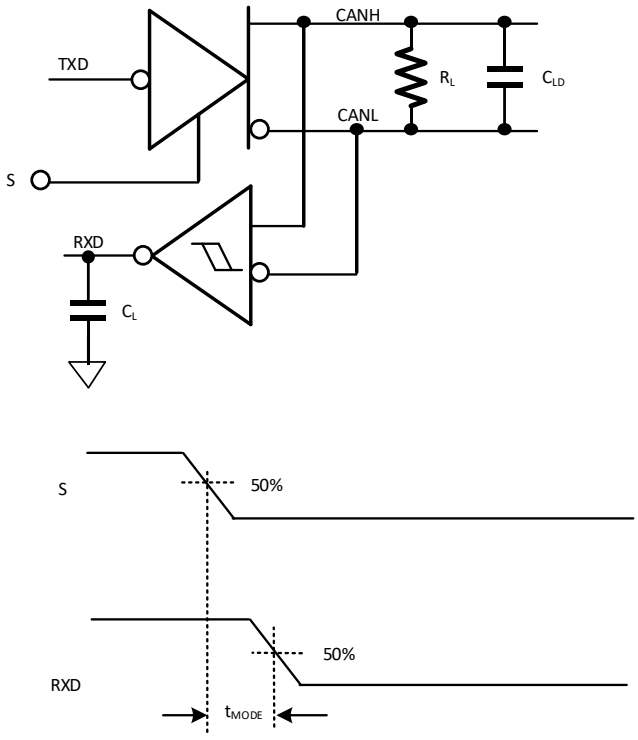


Figure 8 -4 Mode Change Test Circuit and Measurement

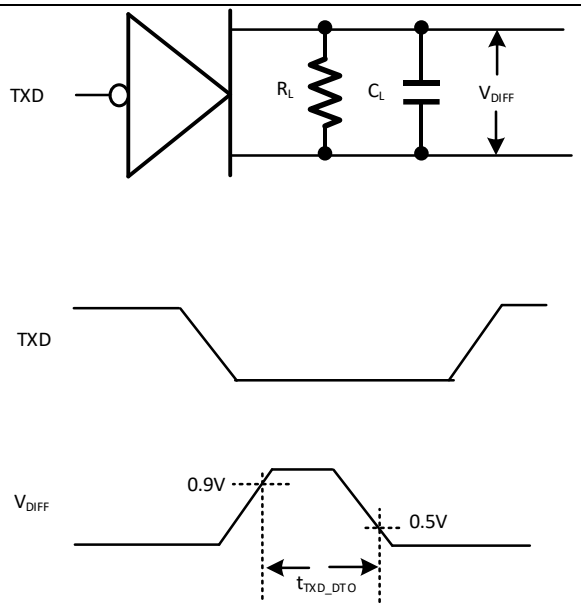


Figure 8-5 Transmitting Dominant Timeout Timing Diagram

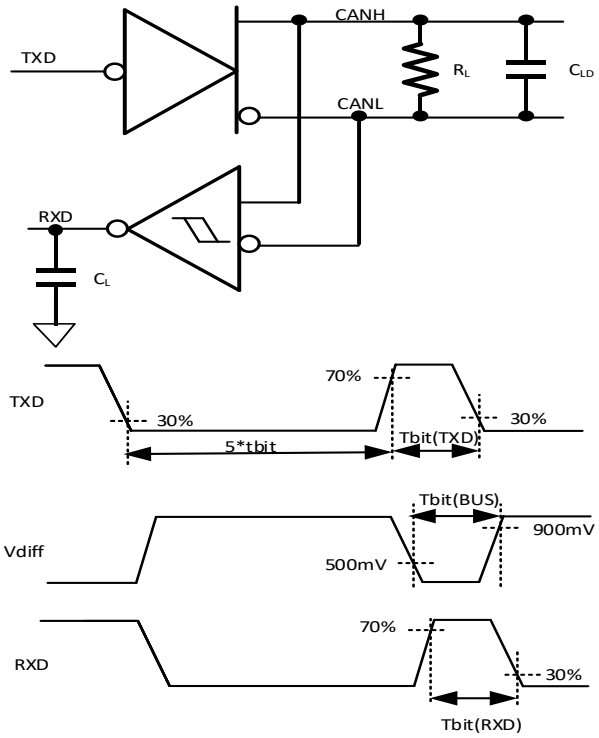


Figure 8-6 CAN FD Timing Parameter Measurement

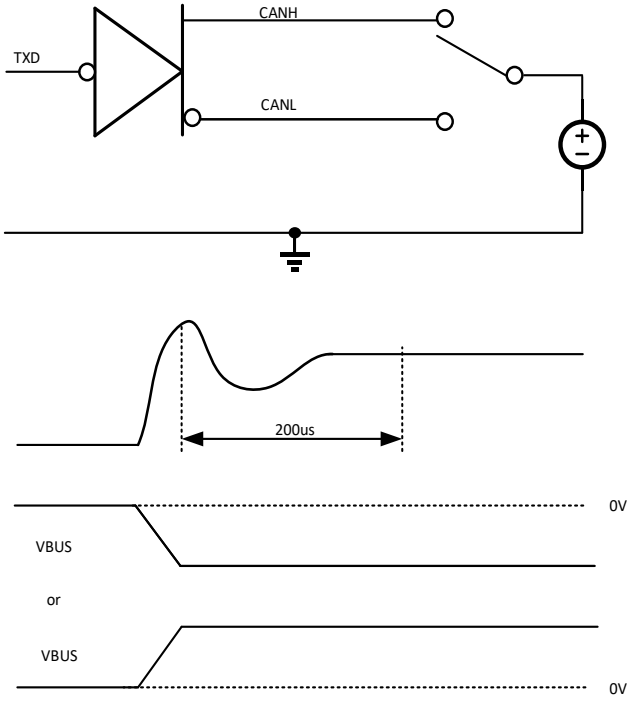


Figure 8-7 Driver Short Circuit Current Test Circuit and Measurement

9. Detailed Description

The CA-IF1051H is +5V, fault-protected Controller Area Network (CAN) transceiver, meets the ISO11898-2 (2016) high speed CAN physical layer standard. It is designed for harsh industrial applications with a number of integrated robust protection feature set that improve the reliability of end equipment. This device is fault protected up to ±70V, making it ideal for applications where overvoltage protection is required. A common-mode voltage range of ±30V enables communication in noisy environments where there are ground plane differences between different systems. Dominant timeout prevents the bus from being blocked by a hung-up microcontroller, and the outputs CANH and CANL are short-circuit current-limited and protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs in a high-impedance state.

This device can operate up to 5Mbps data rate and support CAN FD. However, the maximum data rate is limited by the bus loading, number of nodes, cable length etc. factors, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower.

9.1. CAN Bus Status

The CAN bus has two states: dominant and recessive. In the dominant state (a zero bit, used to determine message priority), CANH-CANL are defined to be logic '0' when the voltage across them is between +1.5V and +3V (higher than 0.9V). In the recessive state (a 1-bit and the state of the idle bus), the driver is defined to be logic '1' when differential voltage is between -120mV and +12mV, or when it is near zero(lower than 0.5V), see *Figure 9-1* for the bus logic state voltage definition.

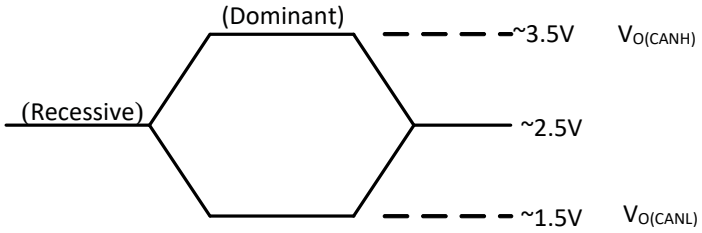


Figure. 9-1 Bus Logic State Voltage Definition

9.2. Receiver

The receiver reads the differential input from the bus line (CANH and CANL) and transfers this data as a single-ended output RXD to the CAN controller. The internal comparator senses the difference voltage V_{DIFF} = (V_{CANH}-V_{CANL}), with respect to an internal threshold of 0.7V. If V_{DIFF} > 0.9V, a logic-low is present on RXD; If V_{DIFF} < 0.5V, a logic-high is present.

Table 9-1 Receiver Truth Table

DEVICE MODE	V_{ID} = V_{CANH}-V_{CANL}	BUS STATE	RXD
Normal or Silent	V_{ID} ≥ 0.9V	Dominant	Low
	0.5V < V_{ID} <0.9V	Indeterminate	Indeterminate
	V_{ID} ≤ 0.5V	Recessive	High
	Open (V_{ID} ≈ 0V)	Open	High

The CANH and CANL common-mode range is ±30V in normal mode. RXD is a logic-high when CANH and CANL are shorted or terminated and un-driven.

9.3. Transmitter

The CAN bus has two states: dominant and recessive. In the dominant state (a zero bit, used to determine message priority), CANH-CANL are defined to be logic '0' when the voltage across them is between +1.5V and +3V (higher than 0.9V). In the recessive state (a 1-bit and the state of the idle bus), the driver is defined to be logic '1' when differential voltage is between -120mV and +12mV, or when it is near zero (lower than 0.5V).

The transmitter converts a single-ended input signal (TXD) from the local CAN controller to differential outputs for the bus lines CANH and CANL. The truth table for the transmitter is provided in *Table 9-1*. The CA-IF1051H protects the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the short is removed.

Table 9-2 Transmitter Truth Table (When Not Connected to the Bus)

INPUT		TXD LOW TIME	OUTPUT		BUS STATE
S	TXD		CANH	CANL	
Low or Open	Low	< t_{DOM}	High	Low	Dominant
	Low	> t_{DOM}	V_{CC}/2	V_{CC}/2	Recessive
	High or Open	X	V_{CC}/2	V_{CC}/2	Recessive
High	X	X	V_{CC}/2	V_{CC}/2	Recessive

X = Don't care

9.4. Protection Functions

9.4.1. Undervoltage Lockout

The supply terminal V_{CC} has undervoltage detection that places the device in protected mode during an undervoltage event on V_{CC}.

Table 9-3 Undervoltage Lockout

V_{CC}	DEVICE STATE	BUS OUTPUT	RXD
> V_{UV_VCC}	Normal	Per TXD	Mirrors Bus
< V_{UV_VCC}	Protected	High Impedance	High Impedance

9.4.2. Fault Protection

The CA-IF1051HS device has an internal ±70V overvoltage circuit on the driver output and receiver inputs to protect the devices from accidental shorts between a local power supply and the data lines of the transceivers. This level of protection is present whether the transceiver is powered or un-powered.

9.4.3. Thermal Shutdown

If the junction temperature of the device exceeds the thermal shutdown threshold, the device turns off the CAN driver circuits thus blocking the TXD-to-bus transmission path. The CAN bus terminals are biased to the recessive level during a thermal shutdown, and the receiver-to-RXD path remains operational. The shutdown condition is cleared when the junction temperature drops to normal operation temperature range of the device.

9.4.4. Current-Limit

The CA-IF1051H protect the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. However, this will cause large supply current and dissipation. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the short is removed.

9.4.5. Transmitter-Dominant Timeout

The CA-IF1051H features a transmitter-dominant timeout (t_{DOM}) that prevents erroneous CAN controllers from clamping the bus to a dominant level by maintaining a continuous low TXD signal. When TXD remains in the dominant state (low) for greater than t_{DOM}, the transmitter is disabled, releasing the bus to a recessive state (see *Figure 9-2*). After a dominant timeout fault, the transmitter is re-enabled when receiving a rising edge at TXD. The transmitter-dominant timeout limits the minimum possible data rate to 5.5kbps.

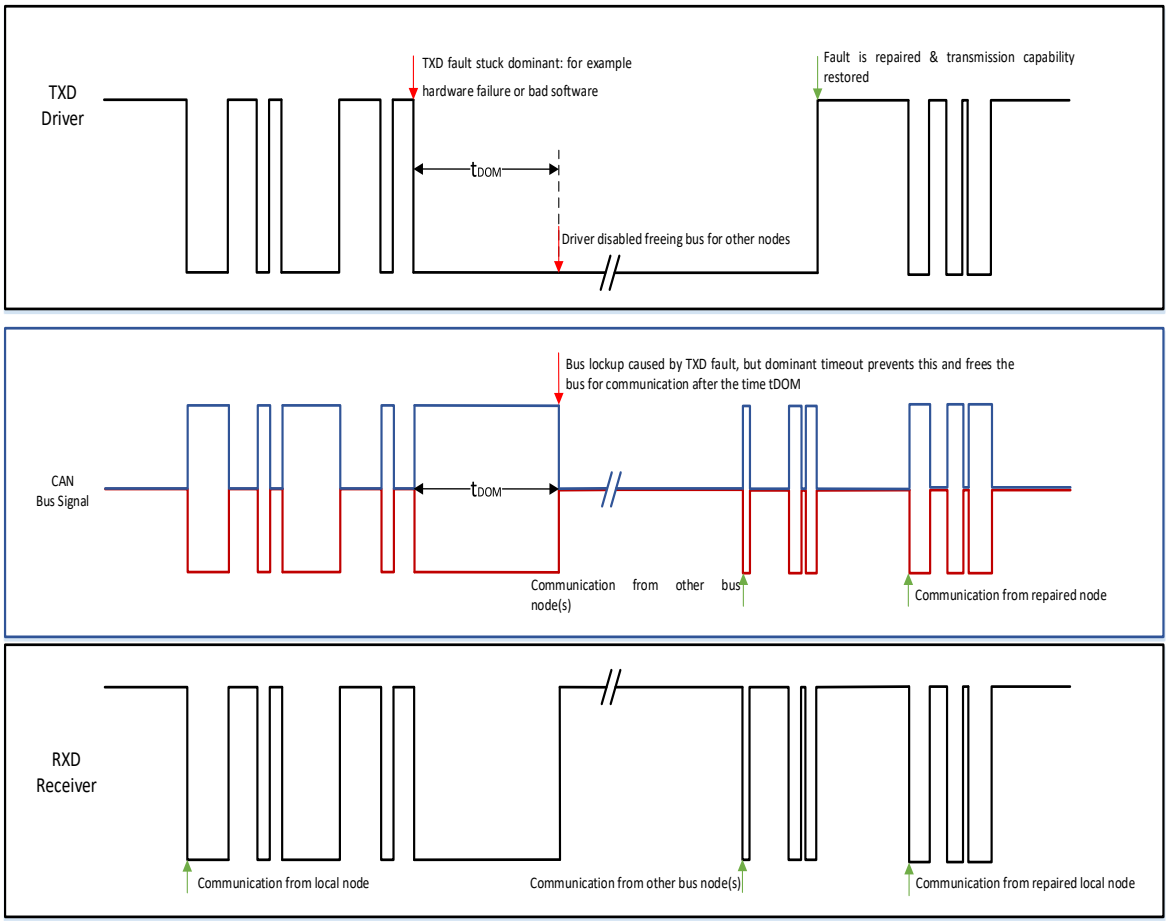


Figure 9-2 Transmitter-Dominant Timeout Protection

9.5. Unpowered Device

The device is designed to be 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus.

9.6. Floating Terminals

This device has internal pull-up or pull-down on critical terminals to place the device into known states if the terminals float. The TXD terminal is pulled up to V_{CC} to force a recessive input level if the terminal floats. The pin S is also pulled down to force the device into normal mode if the terminal floats.

9.7. Operating Mode

The device has two operating modes: Normal mode and Silent mode. Operating mode selection is made via the S input.

9.7.1. Normal Mode

Select the Normal mode of device operation by setting S terminal low or leave it open. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver translates a digital input on TXD to a differential output on CANH and CANL. The receiver translates the differential signal from CANH and CANL to a single-ended output on RXD.

9.7.2. Silent Mode

Drive S high to place the device in silent mode and disable the transmitter regardless of the voltage level at TXD. However, RXD is still active and monitors activity on the bus line.

Table 9-4 Operating Mode

S	MODE	DRIVER	RECEIVER
Low or open	Normal	Enabled	Enabled
High	Silent	Disabled	Enabled

10. Application Information

The CA-IF1051H CAN transceiver is typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. Below is typical application circuit. The bus termination is shown for illustrative purposes. In multi-drop CAN applications, it is important to maintain a single linear bus of uniform impedance that is properly terminated at each end, see *Figure 10-1*, the typical CAN bus operating circuit, termination may be a single 120Ω resistor at the end of the bus, either on the cable or in a terminating node; or split termination, the two 60Ω termination resistors in parallel may be used if filtering and stabilization of the common mode voltage of the bus is desired. A star, ring, or tree configuration should never be used. Any deviation from the end-to-end wiring scheme creates a stub. High-speed data edges on a stub can create reflections back down to the bus. These reflections can cause data errors by eroding the noise margin of the system. Although stubs are unavoidable in a multi-drop system, care should be taken to keep these stubs as short as possible, especially when operating with high data rates.

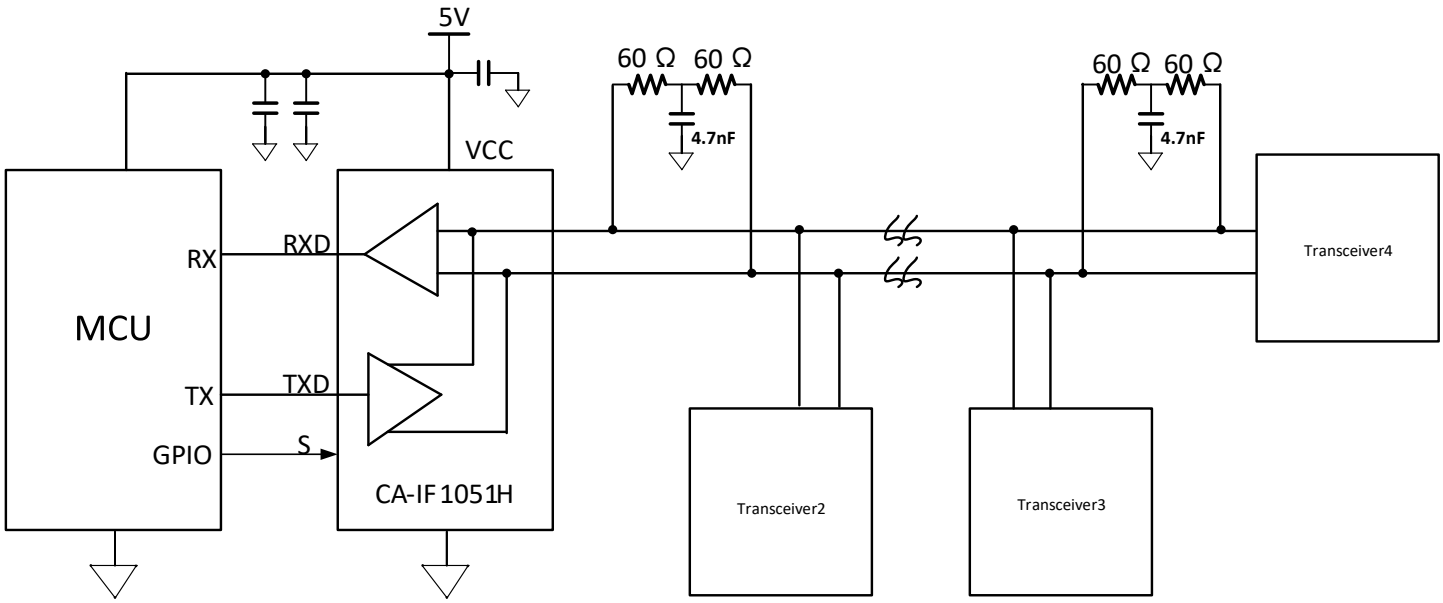
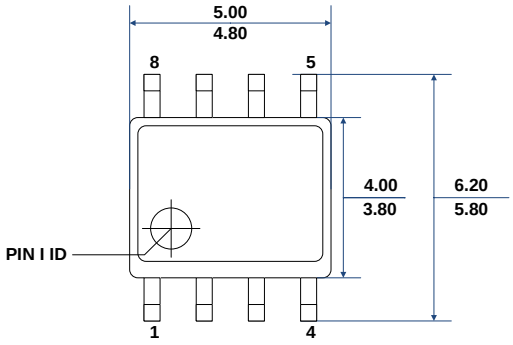


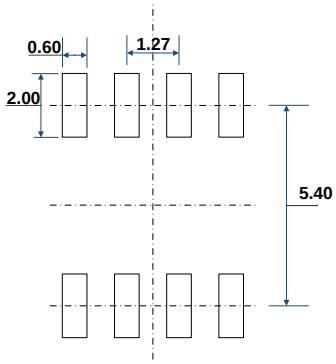
Figure 10-1 Typical Application Circuit

11. Package Information

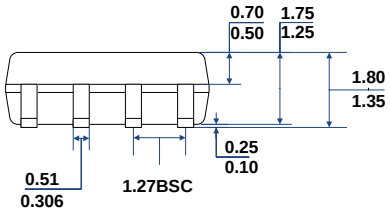
SOIC8 Package Outline



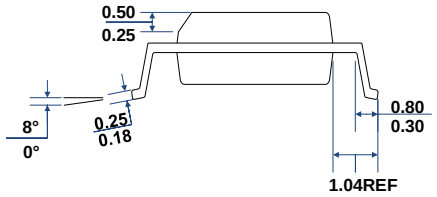
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

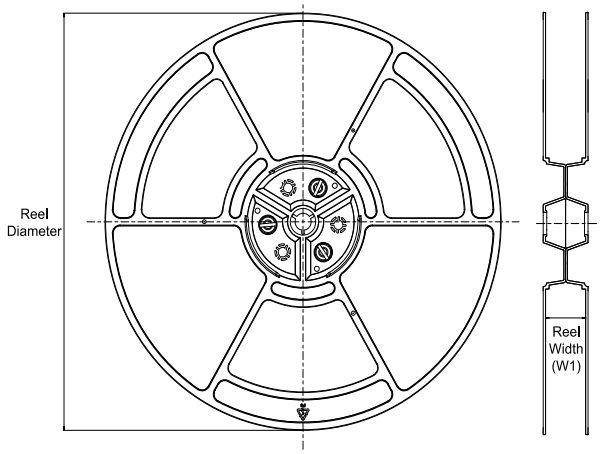
Note:

1. Controlling dimensions are in millimeters.

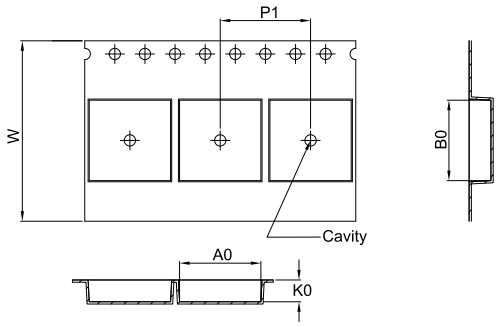
Figure 11-1 SOIC8 Package Outline

12. Tape and Reel Information

REEL DIMENSIONS

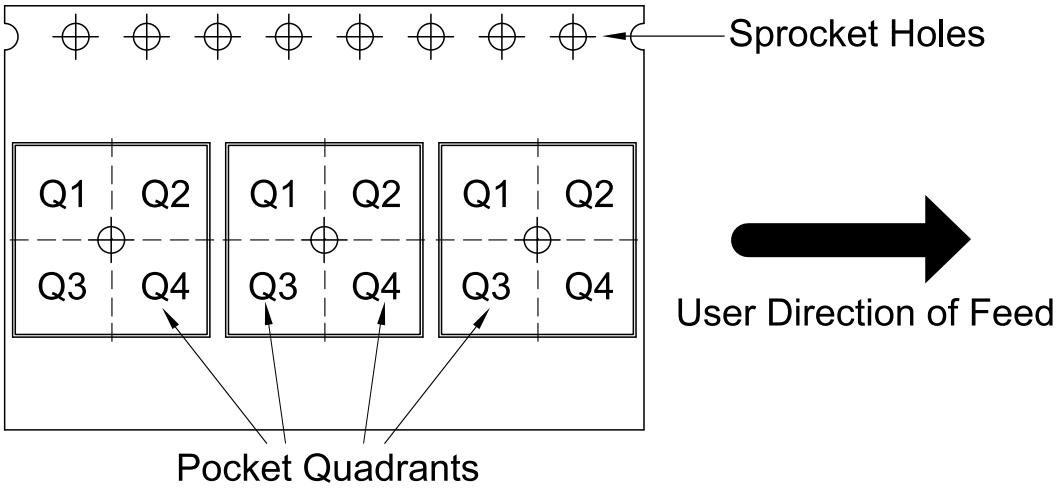


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF1051HS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1

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