

Features

- Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange
- Low-Voltage Differential 30-Ω to 55-Ω Line Drivers and Receivers for Signaling Rates, Up to 200 Mbps
- Type-2 Receivers Provide an Offset (100 mV) Threshold to Detect Open-Circuit and Idle-Bus
- Conditions
- -1 V to 3.4 V Common-Mode Voltage Range
- Allows Data Transfer With 2 V of Ground Noise
- Bus Pins High Impedance When Disabled or $V_{CC} \leq 1.5$ V
- Bus-Pin Protection: ± 8 kV HBM model
- -40°C to 85°C Operation Temperature Range

Description

The TPT9H221 is a 3.3V Multipoint-Low-Voltage Differential (M-LVDS) line driver and receiver, which can operate at signaling rates up to 200 Mbps. Driver outputs and receiver inputs are protected against $\pm 8\text{kV}$ ESD strikes without latch-up. The driver output has been designed to support multipoint buses presenting loads as low as 30 Ω , and incorporates controlled transition times to allow for stubs off of the backbone transmission line.

The TPT9H221 is Type-2 receiver that detect the bus state with a differential input of 50 mV over a common-mode voltage range of -1 V to 3.4 V. Type-2 receiver includes an offset threshold to provide a known output state under open-circuit fail-safe, idle-bus fail-safe. The device is characterized for operation from -40°C to 85°C . The device is available as half-duplex in an 8-lead SOP package.

Applications

- Backplane Multipoint Data/Clock Transmission
- Cellular Base Stations
- Network Switches and Routers
- Industrial Control
- Communication Infrastructure

Simplified Schematic

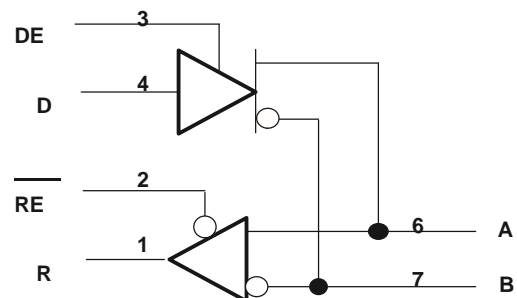


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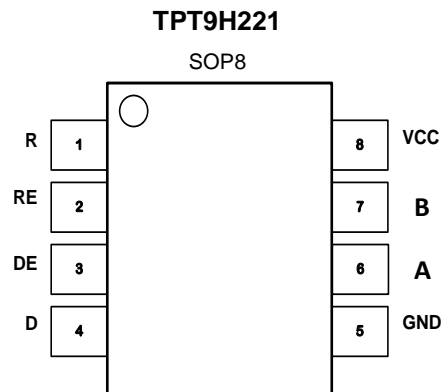
Revision History

Date	Revision	Notes
2018/11/12	Prelim Rev. 0.1	Definition Draft
2019/01/24	Prelim Rev. 0.2	Add package information
2019/03/11	Prelim Rev. 0.3	Update ordering and package information
2019/03/25	Prelim Rev. 0.4	Update electrical parameter and thermal parameter θ_{JA}
2019/03/27	Rev.0	Release Version, confirm spec limit

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TPT9H221L1-SO1R	-40 to 85°C	SO1R 8-Pin SOP	T9H221	1	Tape and Reel, 4000

Pin Configuration and Functions



in No.	Pin Name	I/O	Description
1	R	Digital output	Receiver Output
2	/RE	Digital input	Receiver Output Enable
3	DE	Digital input	Driver Output Enable
4	D	Digital input	Driver Input
5	GND	Ground	Ground
6	A	Bus input	Noninverting Receiver Input
7	B	Bus input	Inverting Receiver Input
8	V _{CC}	Power	Power Supply

Device Function Tables

Table 1. Truth Table Abbreviations

Abbreviation	Description
H	High level
L	Low level
X	Don't care
I	Indeterminate
Z	High impedance (off)
NC	Disconnected

Table 2. DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
L	H	L	H
H	H	H	L
OPEN	H	L	H
X	OPEN	Z	Z
X	L	Z	Z

H = high level, L = low level, Z = high impedance,
X = Don't care, ? = indeterminate

Table 3. TYPE-2 RECEIVER

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	RE	R
$V_{ID} \geq 150 \text{ mV}$	L	H
$50 \text{ mV} < V_{ID} < 150 \text{ mV}$	L	?
$V_{ID} \leq 50 \text{ mV}$	L	L
X	H	Z
X	Open	Z
Open Circuit	L	L

Table 4. Type-2 Receiver Input Threshold Test Voltages

Applied Voltage		Differential Input Voltages	Common Mode Input Voltage	Receiver Output ⁽¹⁾
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	-2.400	1.200	L
3.800	3.650	0.150	3.725	H
3.800	3.750	0.050	3.775	L
-1.250	-1.400	0.150	-1.325	H
-1.350	-1.400	0.050	-1.375	L

(1)H = high level, L = low level, output state assumes receiver is enabled (RE = L)

Absolute Maximum Ratings

Parameters	Rating
V _{CC} to GND	-0.5 V to 4 V
Voltage at Logic pin: D, DE, /RE, R ^{Note 2}	-0.3V to 4V
Voltage at Bus pin: A, B	-1.8V to +4V
Operating Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C

* **Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

ESD Rating

		Value	Unit
HBM, ANSI/ESDA/JEDEC JS-001	Bus Pin	8	kV
	All Pin Except Bus Pin	4	kV
CDM, ANSI/ESDA/JEDEC JS-002	All Pin	1	kV

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
8-Pin SOP	130		°C/W

Note: θ_{JA} =130°C/W is typical value of SOP8 provided by package assembly house

Recommended Operation Conditions

	Min	Typ	Max	Unit
V _{CC} Supply voltage	3	3.3	3.6	V
V _{IH} High-level input voltage	2		V _{CC}	V
V _{IL} Low-level input voltage	GND		0.8	V
Voltage at any bus terminal V _A , V _B	-1.4		3.8	V
V _{ID} Magnitude of differential input voltage	0.05		V _{CC}	V
T _A Operating free-air temperature	-40		85	°C

Electrical Characteristics

All test condition is $V_{CC} = 3.0$ to $3.6V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
V_{CC}	Supply voltage		3.0		3.6	V
I_{CC} Supply current	Driver only	RE and DE at V_{CC} , $R_L = 50 \Omega$, All others open		13	22	mA
	Both disabled	RE at V_{CC} , DE at 0 V, $R_L =$ No Load, All others open		2	4	mA
	Both enabled	RE at 0 V, DE at V_{CC} , $R_L = 50 \Omega$, All others open		15	24	mA
	Receiver only	RE at 0 V, DE at 0 V, $R_L = 50 \Omega$, All others open		4	13	μA
I_A	Receiver or transceiver with driver disabled input current	$V_A = 3.8 V, V_B = 1.2 V,$	0		32	μA
		$V_A = 0 V$ or $2.4 V, V_B = 1.2 V$	-20		20	μA
		$V_A = -1.4 V, V_B = 1.2 V$	-32		0	μA
I_B	Receiver or transceiver with driver disabled input current	$V_B = 3.8 V, V_A = 1.2 V$	0		32	μA
		$V_B = 0 V$ or $2.4 V, V_A = 1.2 V$	-20		20	μA
		$V_B = -1.4 V, V_A = 1.2 V$	-32		0	μA
I_{AB}	Receiver or transceiver with driver disabled differential input current ($I_A - I_B$)	$V_A = V_B, 1.4 \leq V_A \leq 3.8 V$	-4		4	μA
$I_{A(OFF)}$	Receiver or transceiver power-off input current	$V_A = 3.8 V, V_B = 1.2 V, 0 V \leq V_{CC} \leq 1.5 V$	0		32	μA
		$V_A = 0 V$ or $2.4 V, V_B = 1.2 V, 0 V \leq V_{CC} \leq 1.5 V$	-20		20	μA
		$V_A = -1.4 V, V_B = 1.2 V, 0 V \leq V_{CC} \leq 1.5 V$	-32		0	μA
$I_{B(OFF)}$	Receiver or transceiver power-off input current	$V_B = 3.8 V, V_A = 1.2 V,$ $0 V \leq V_{CC} \leq 1.5 V$	0		32	μA
		$V_B = 0 V$ or $2.4 V, V_A = 1.2 V,$ $0 V \leq V_{CC} \leq 1.5 V$	-20		20	μA
		$V_B = -1.4 V, V_A = 1.2 V,$ $0 V \leq V_{CC} \leq 1.5 V$	-32		0	μA
$I_{AB(OFF)}$	Receiver input or transceiver power-off differential input current ($I_A - I_B$)	$V_A = V_B, 0 V \leq V_{CC} \leq 1.5 V,$ $-1.4 \leq V_A \leq 3.8 V$	-4		4	μA

Driver Electrical Characteristics						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$ V_{AB} $	Differential output voltage magnitude	See Figure 1	480		650	mV
$\Delta V_{AB} $	Change in differential output voltage magnitude between logic states		-50		50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	See Figure 2	0.8		1.2	V
$\Delta V_{OS(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage				150	mV
$V_{A(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 6	0		VCC	V
$V_{B(OC)}$	Maximum steady-state open-circuit output voltage		0		VCC	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	See Figure 4			1.2 V_{SS}	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output		-0.2 V_{SS}			V
I_{IH}	High-level input current (D, DE)	$V_{IH} = 2\text{ V}$	0		10	μA
I_{IL}	Low-level input current (D, DE)	$V_{IL} = 0.8\text{ V}$	0		10	μA
$ I_{OS} $	Differential short-circuit output current magnitude	See Figure 3			75	mA
I_{OZ}	High-impedance state output current (driver only)	$-1.4\text{ V} \leq V_A \text{ or } V_B \leq 3.8\text{ V}$, Other output = 1.2 V	-32		32	μA

Driver Switching Characteristics							
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 4		2.8		ns	
t_{PHL}	Propagation delay time, high-to-low-level output				3.2		ns
t_r	Differential output signal rise time				1.6		ns

t_f	Differential output signal fall time			1.8		ns
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)			433		ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) ⁽³⁾	100 MHz clock input ⁽⁴⁾		1		ps
t_{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 5		4.5		ns
t_{PLZ}	Disable time, low-level-to-high-impedance output			3.2		ns
t_{PZH}	Enable time, high-impedance-to-high-level output			3.2		ns
t_{PZL}	Enable time, high-impedance-to-low-level output			5.0		ns

Receiver Electrical Characteristics						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IT+}	Positive-going differential input voltage threshold	See Figure 8 and Table 1 and Table 2			150	mV
V_{IT-}	Negative-going differential input voltage threshold		50			mV
V_{HYS}	Differential input voltage hysteresis, ($V_{IT+} - V_{IT-}$)			0		mV
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA			0.4	V
I_{IH}	High-level input current (RE)	$V_{IH} = 2$ V	-10		0	μ A
I_{IL}	Low-level input current (RE)	$V_{IL} = 0.8$ V	-10		0	μ A
C_A or C_B	Input capacitance	$V_I = 0.4 \sin(30E6\pi t) + 0.5$ V, ⁽²⁾ Other input at 1.2 V		7		pF
C_{AB}	Differential input capacitance	$V_{AB} = 0.4 \sin(30E6\pi t)$ V ⁽²⁾		7		pF
$C_{A/B}$	Input capacitance balance, (C_A/C_B)		0.99		1.01	

Receiver Switching Characteristics						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{pLH}	Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$, See Figure 9	2	4	6	ns
t_{pHL}	Propagation delay time, high-to-low-level output		2	4	6	ns
t_r	Output signal rise time			0.9	2.3	ns
t_f	Output signal fall time			0.8	2.3	ns
$t_{sk(p)}$	Pulse skew ($ t_{pHL} - t_{pLH} $)				100	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) ⁽³⁾	100 MHz clock input ⁽⁴⁾		1		ps
t_{pHZ}	Disable time, high-level-to-high-impedance output	See Figure 10		4.5		ns
t_{pLZ}	Disable time, low-level-to-high-impedance output			3.5		ns
t_{pZH}	Enable time, high-impedance-to-high-level output			7.5		ns
t_{pZL}	Enable time, high-impedance-to-low-level output			3.5		ns

Test Circuits, Configurations and Waveforms

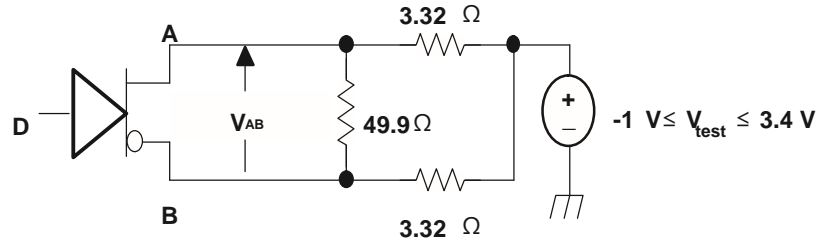


Figure 1. Differential Output Voltage Test Circuit

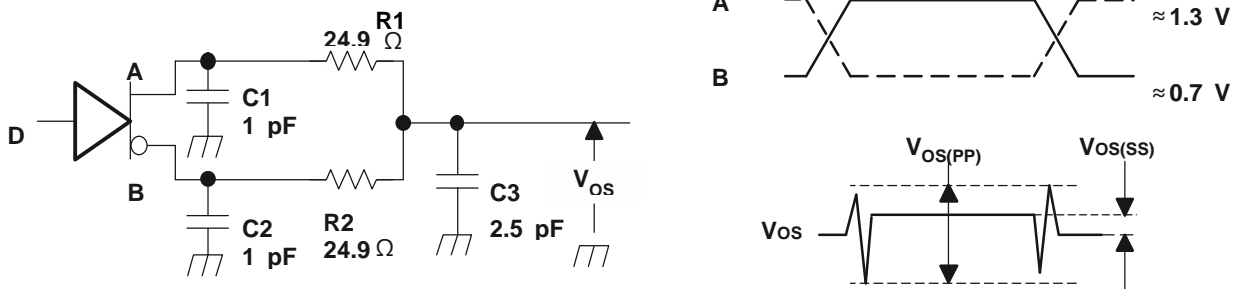


Figure 2. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

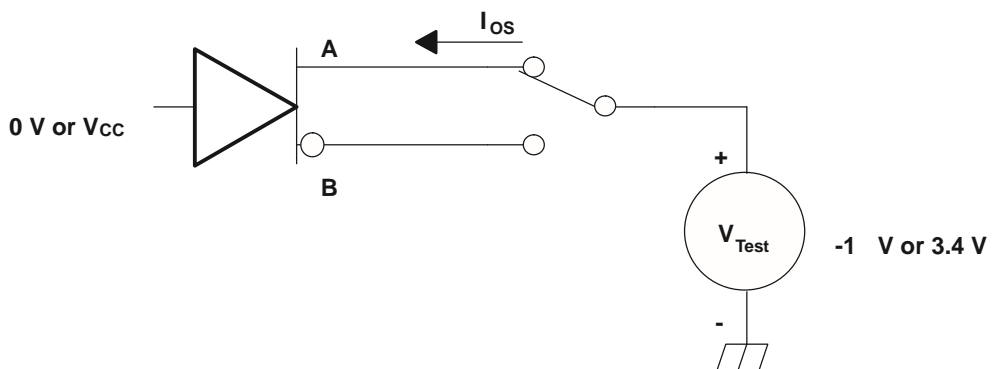


Figure 3. Driver Short-Circuit Test Circuit

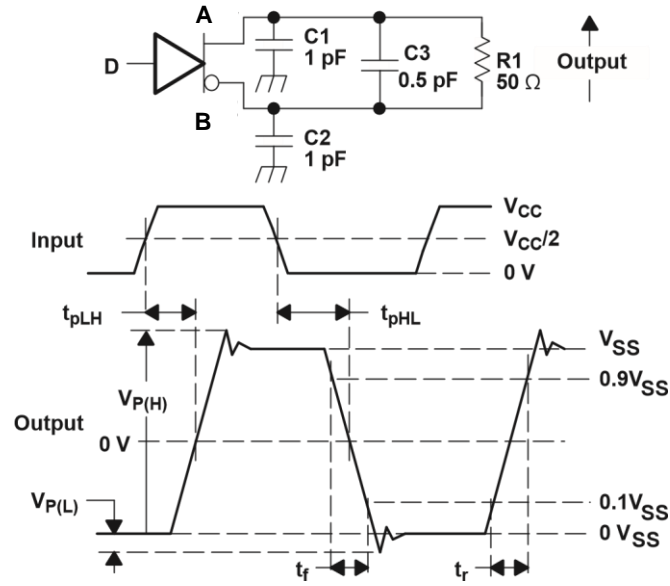


Figure 4. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

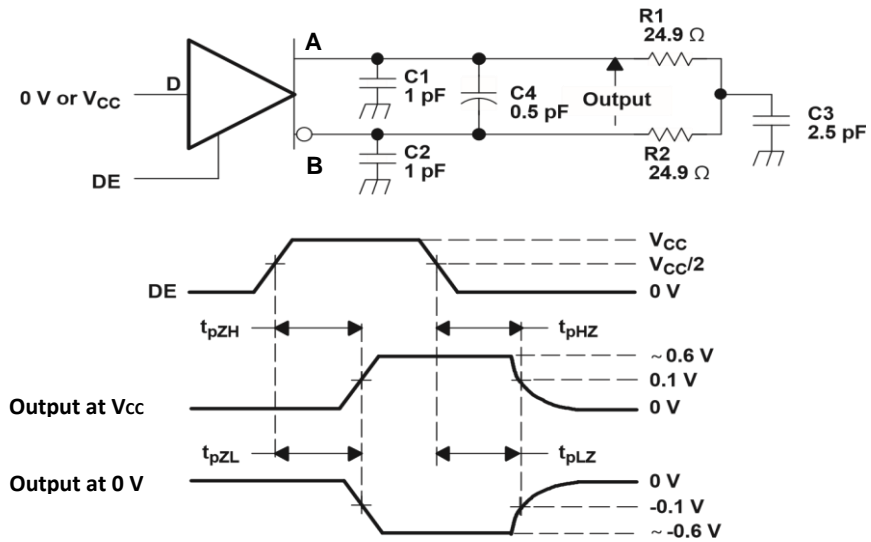


Figure 5. Driver Enable and Disable Time Circuit and Definitions

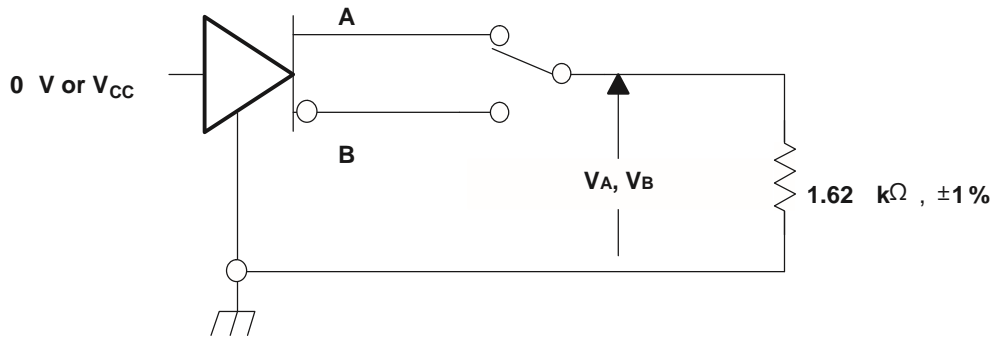


Figure 6. Maximum Steady State Output Voltage

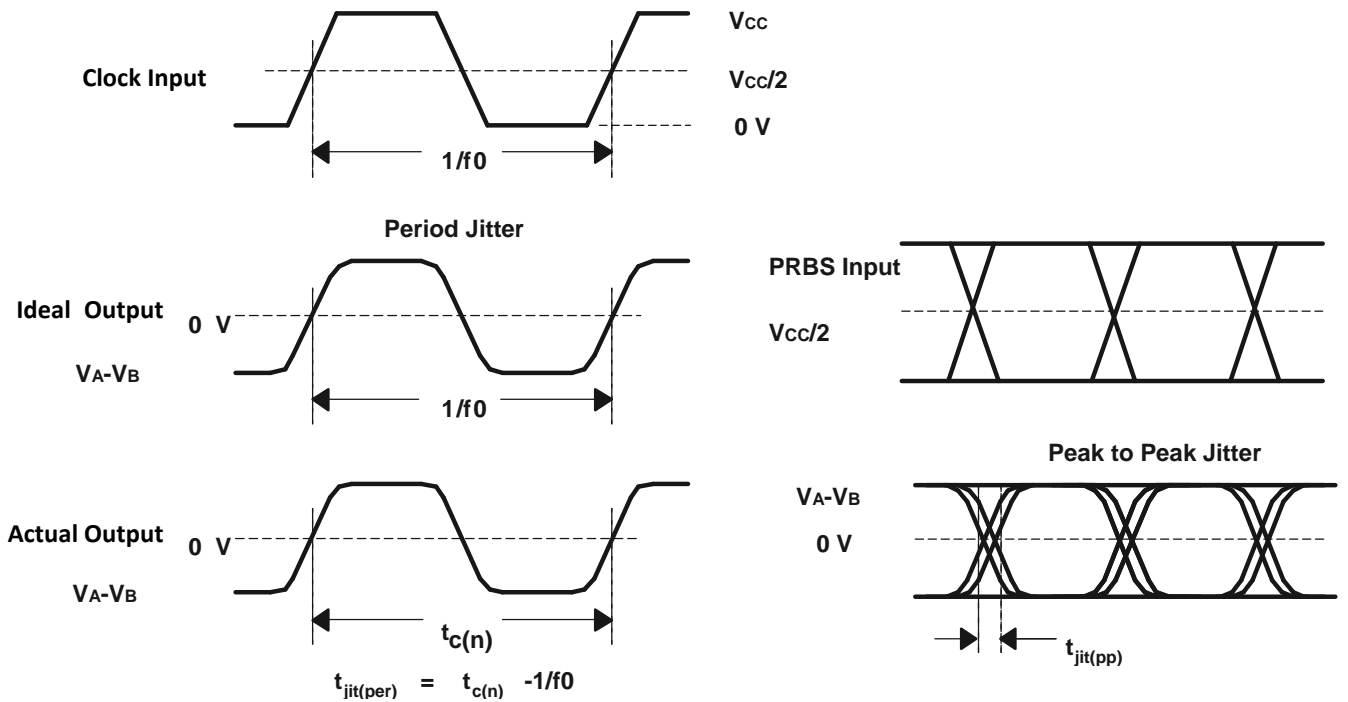


Figure 7. Driver Jitter Measurement Waveforms

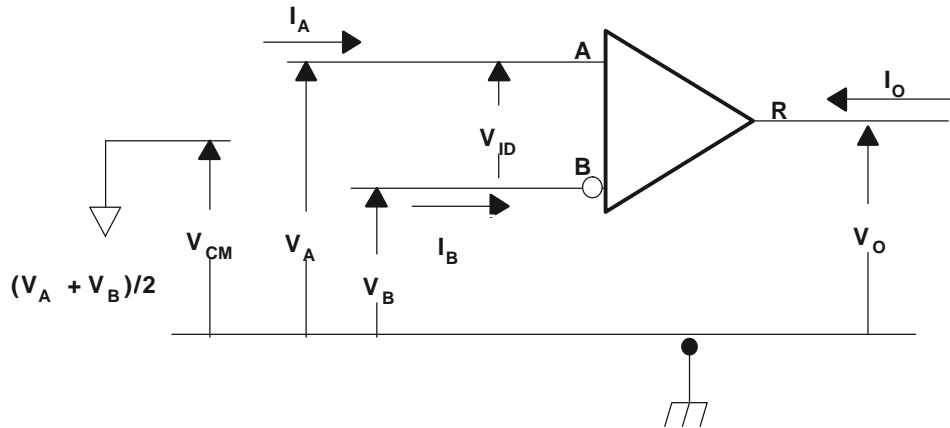


Figure 8. Receiver Voltage and Current Definitions

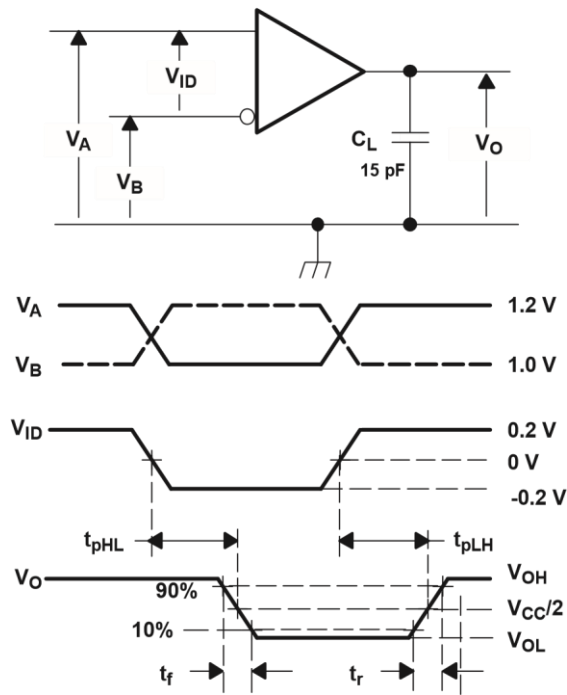


Figure 9. Receiver Timing Test Circuit and Waveforms

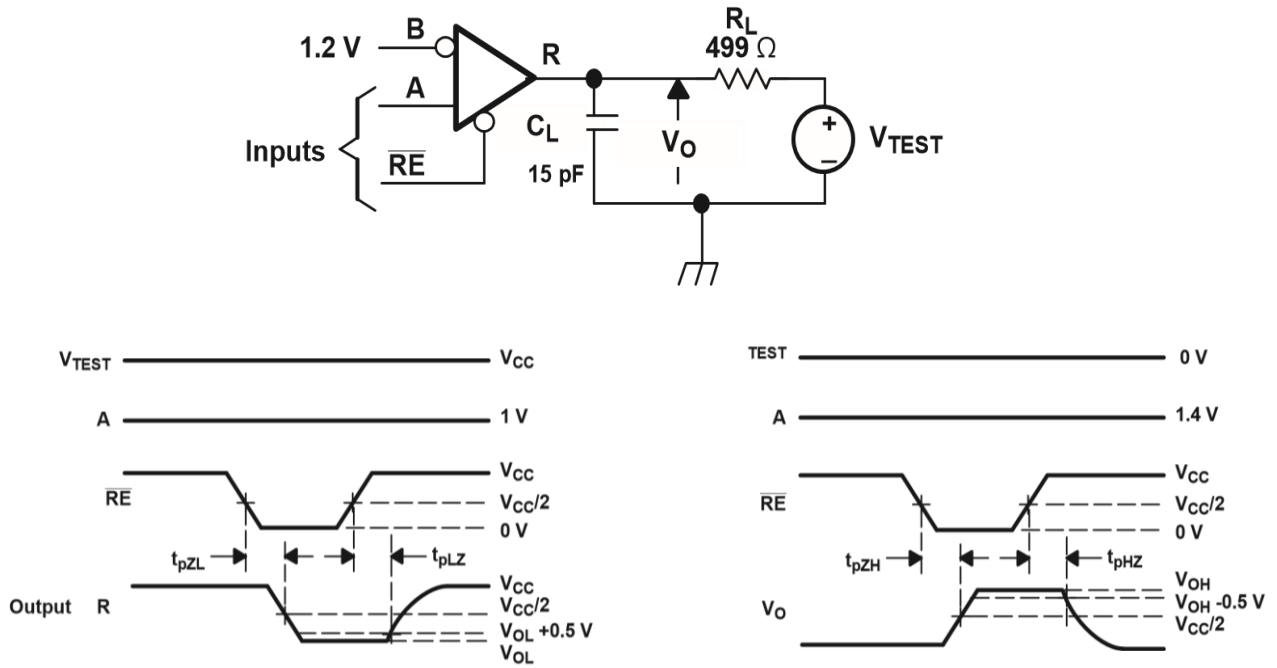


Figure 10. Receiver Enable/Disable Time Test Circuit and Waveforms

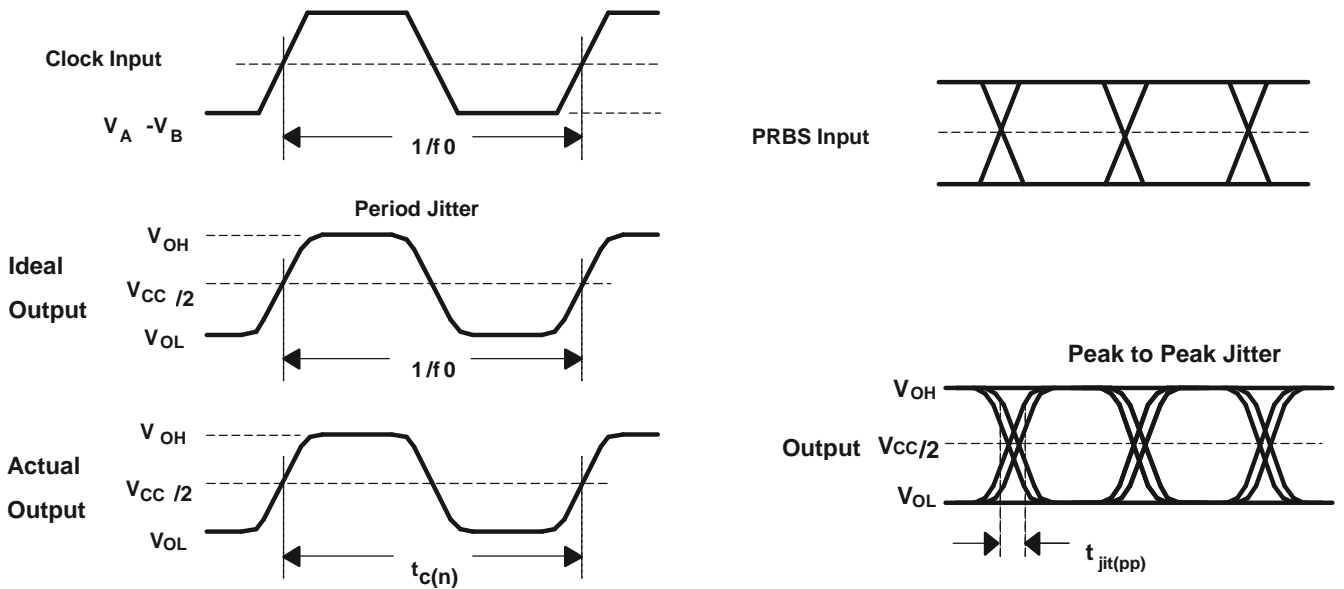
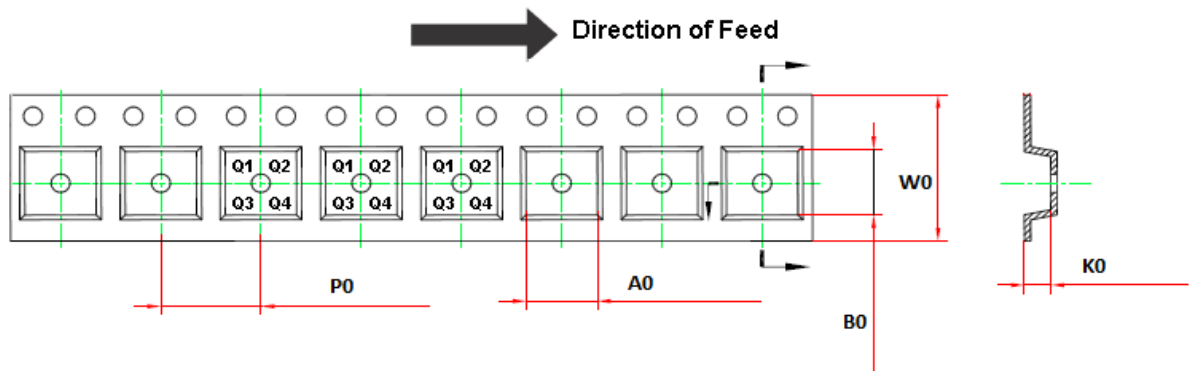
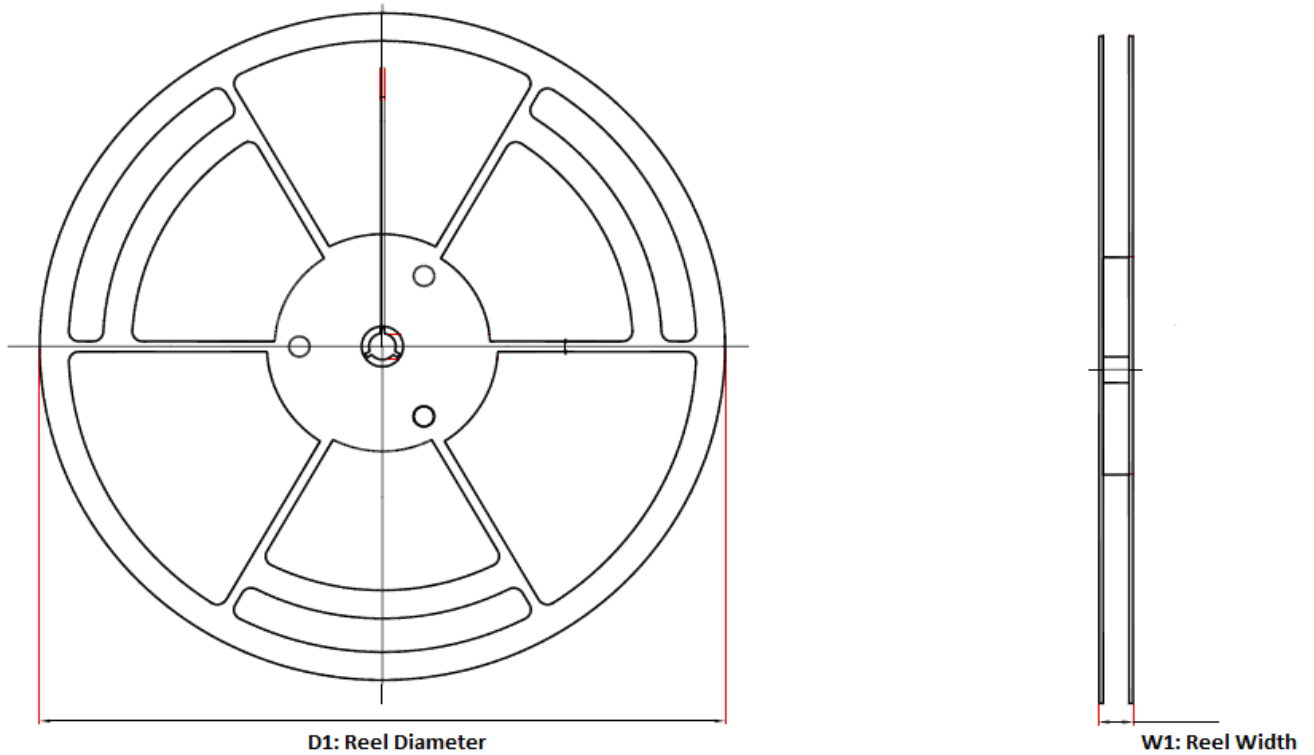


Figure 11. Receiver Jitter Measurement Waveforms

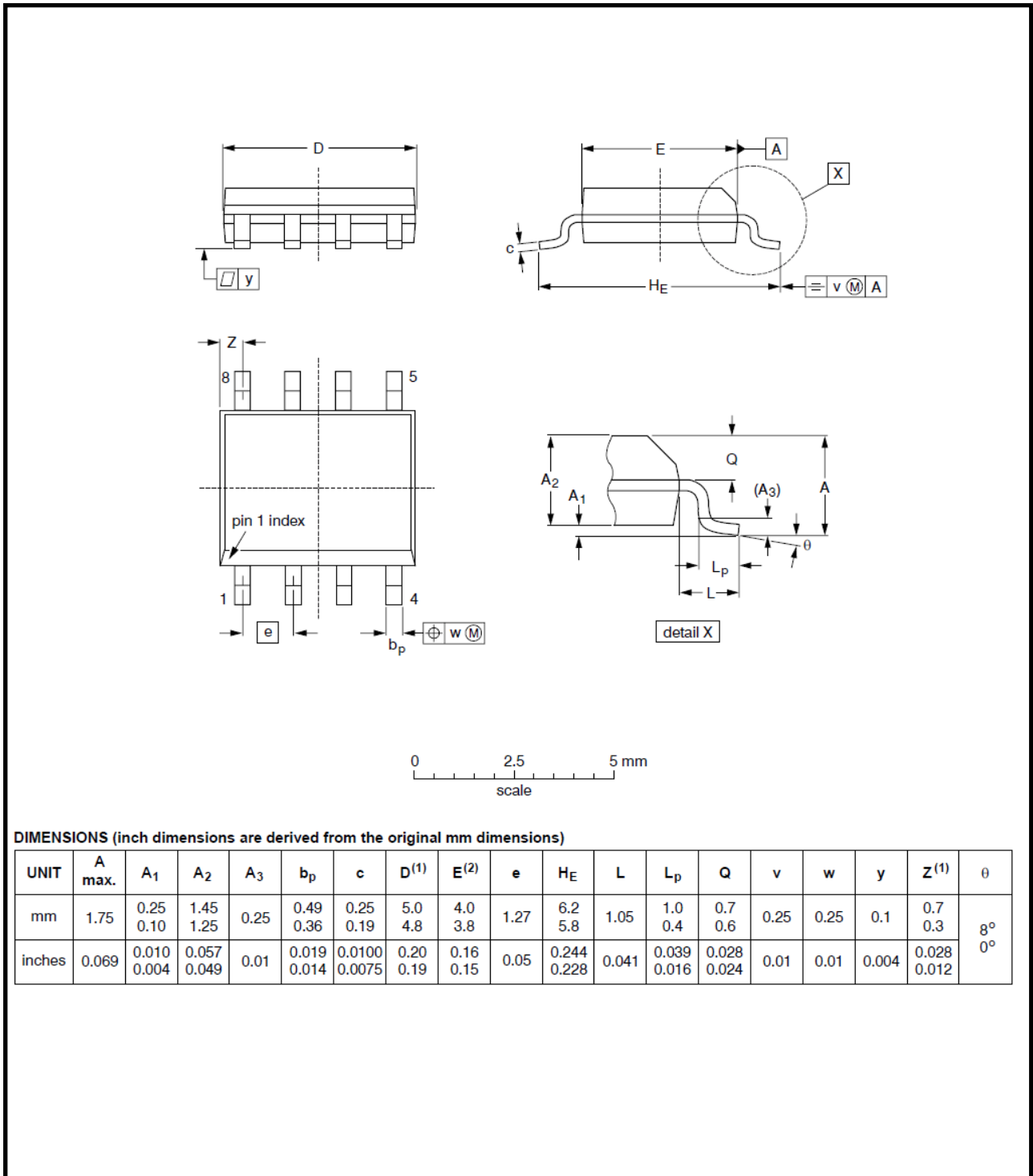
Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT9H221L1-SO1R	8-Pin SOP	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1

Package Outline Dimensions

SO1R (SOP8)



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	