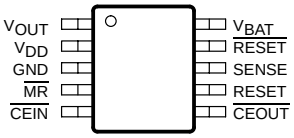
- **Supply Current of 40 μA (Max)**
- **Battery Supply Current of 100 nA (Max)**
- **Supply Voltage Supervision Range:**
  - **Adjustable**
  - **Other Versions Available on Request**
- **Backup-Battery Voltage Can Exceed $V_{DD}$**
- **Power-On Reset Generator With Fixed 100-ms Reset Delay Time**
- **Active-High and Active-Low Reset Output**
- **Chip-Enable Gating . . . 3 ns (at $V_{DD}$ = 5 V) Max Propagation Delay**
- **10-Pin MSOP Package**
- **Temperature Range . . . –40°C to 85°C**

## typical applications

- **Fax Machines**
- **Set-Top Boxes**
- **Advanced Voice Mail Systems**
- **Portable Battery Powered Equipment**
- **Computer Equipment**
- **Advanced Modems**
- **Automotive Systems**
- **Portable Long-Time Monitoring Equipment**
- **Point-of-Sale Equipment**

**MSOP (DGS) Package**
**(TOP VIEW)**




**ACTUAL SIZE**
**3,05 mm x 4,98 mm**

## description

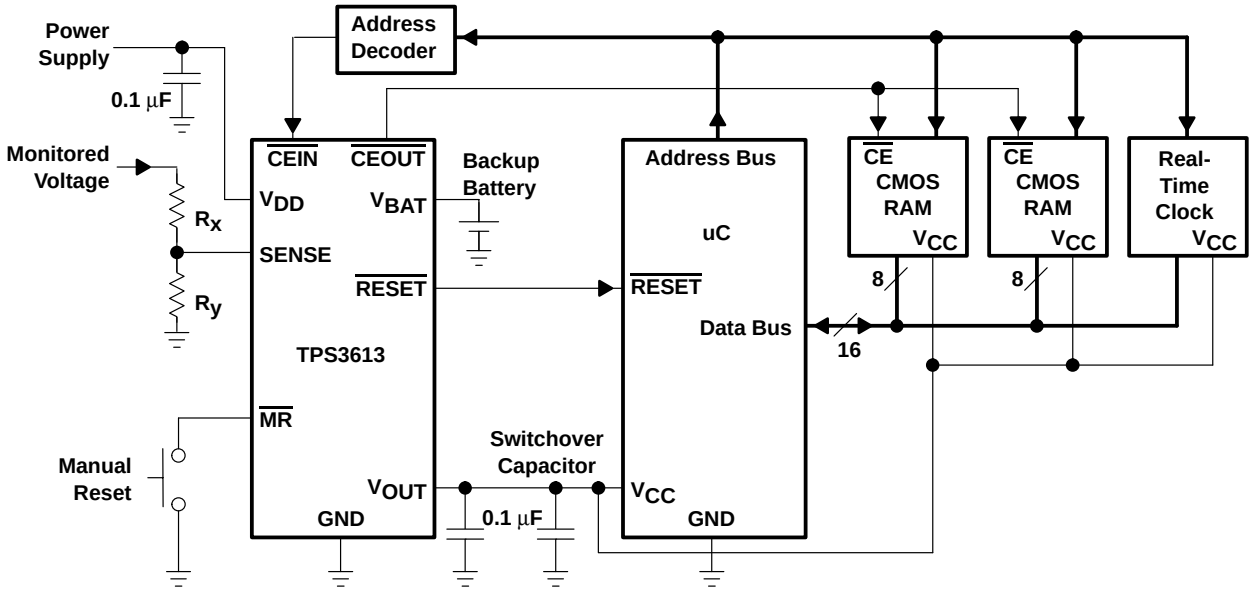
The TPS3613-01 supervisory circuit monitors and controls processor activity by providing backup-battery switchover for data retention of CMOS RAM.

During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage ($V_{DD}$ or $V_{BAT}$) becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors $V_{DD}$ and keeps $\overline{\text{RESET}}$ output active as long as $V_{DD}$ remains below the threshold voltage $V_{IT}$. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after $V_{DD}$ has risen above the threshold voltage $V_{IT}$.

When the supply voltage drops below the threshold voltage $V_{IT}$, the output becomes active (low) again.

The TPS3613-01 is available in a 10-pin MSOP package and is characterized for operation over a temperature range of –40°C to 85°C.

## typical operating circuit



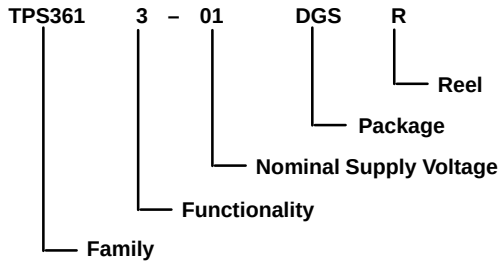

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**PACKAGE INFORMATION**

| $T_A$ | DEVICE NAME | MARKING |
|---|---|---|
| –40°C to 85°C | TPS3613–01DGSR† | AFK |

† The DGSR passive indicates tape and reel of 2500 parts.

## ordering information application specific versions



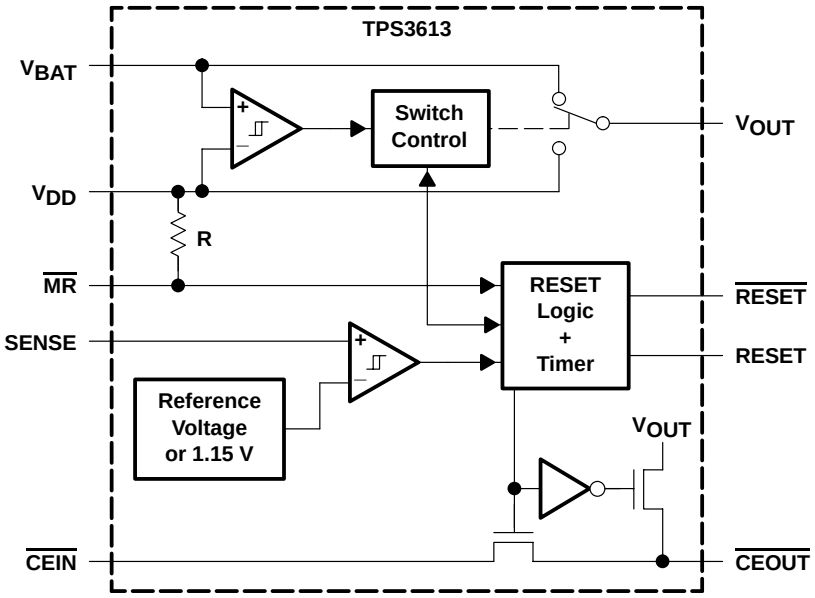

| DEVICE NAME | NOMINAL VOLTAGE‡, $V_{NOM}$ |
|---|---|
| TPS3613–01 DGS | Adjustable |

‡ For other threshold voltages, contact the local TI sales office for availability and lead-time.

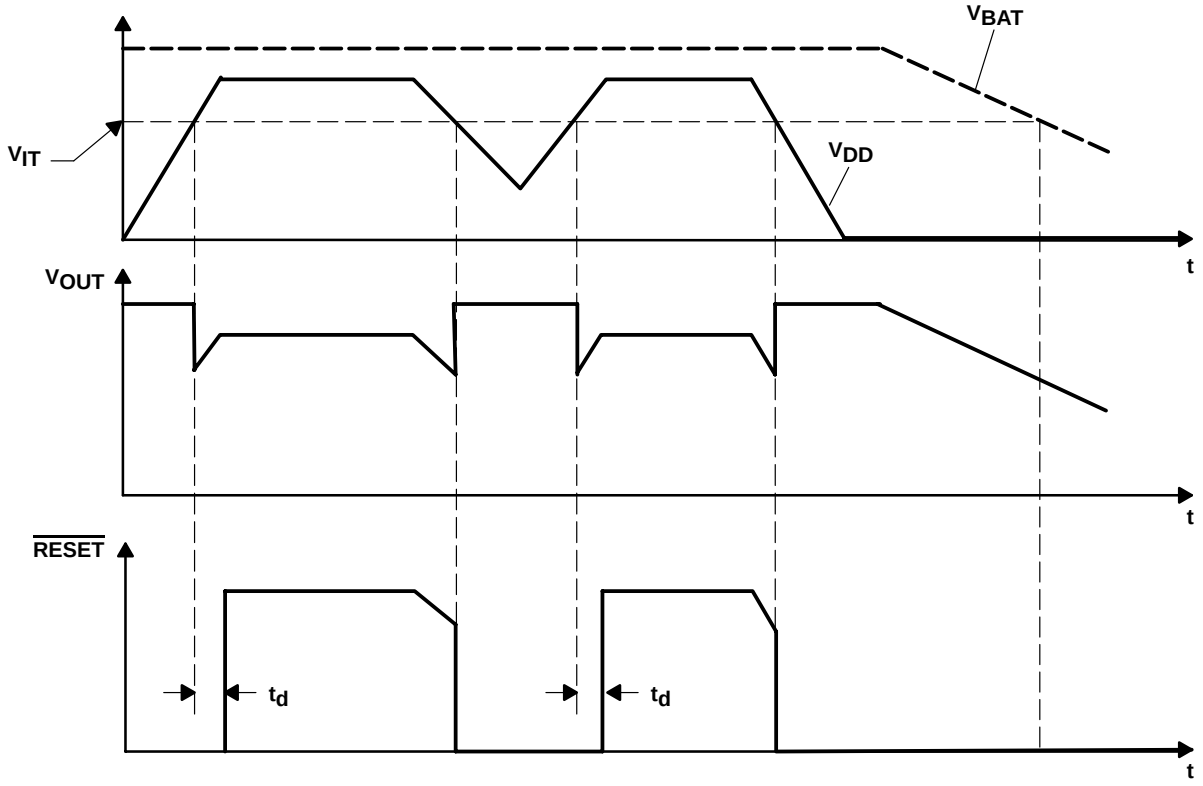
**FUNCTION TABLE**

| SENSE > $V_{IT}$ | $V_{DD}$ > $V_{BAT}$ | $\overline{MR}$ | $\overline{CEIN}$ | $V_{OUT}$ | $\overline{RESET}$ | RESET | $\overline{CEOUT}$ |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $V_{BAT}$ | 0 | 1 | DIS |
| 0 | 0 | 0 | 1 | $V_{BAT}$ | 0 | 1 | DIS |
| 0 | 0 | 1 | 0 | $V_{BAT}$ | 0 | 1 | DIS |
| 0 | 0 | 1 | 1 | $V_{BAT}$ | 0 | 1 | DIS |
| 0 | 1 | 0 | 0 | $V_{DD}$ | 0 | 1 | DIS |
| 0 | 1 | 0 | 1 | $V_{DD}$ | 0 | 1 | DIS |
| 0 | 1 | 1 | 0 | $V_{DD}$ | 0 | 1 | DIS |
| 0 | 1 | 1 | 1 | $V_{DD}$ | 0 | 1 | DIS |
| 1 | 0 | 0 | 0 | $V_{DD}$ | 0 | 1 | DIS |
| 1 | 0 | 0 | 1 | $V_{DD}$ | 0 | 1 | DIS |
| 1 | 0 | 1 | 0 | $V_{DD}$ | 1 | 0 | DIS |
| 1 | 0 | 1 | 1 | $V_{DD}$ | 1 | 0 | EN |
| 1 | 1 | 0 | 0 | $V_{DD}$ | 0 | 1 | DIS |
| 1 | 1 | 0 | 1 | $V_{DD}$ | 0 | 1 | DIS |
| 1 | 1 | 1 | 0 | $V_{DD}$ | 1 | 0 | DIS |
| 1 | 1 | 1 | 1 | $V_{DD}$ | 1 | 0 | EN |

## functional schematic




## timing diagram



### Terminal Functions

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $\overline{CEIN}$ | 5 | I | Chip-enable input |
| $\overline{CEOUT}$ | 6 | O | Chip-enable output |
| GND | 3 | I | Ground |
| $\overline{MR}$ | 4 | I | Manual reset input |
| RESET | 7 | O | Active-high reset output |
| $\overline{RESET}$ | 9 | O | Active-low reset output |
| SENSE | 8 | I | Adjustable sense input |
| $V_{BAT}$ | 10 | I | Backup-battery input |
| $V_{DD}$ | 2 | I | Input supply voltage |
| $V_{OUT}$ | 1 | O | Supply output |

## detailed description

### backup-battery switchover

In case of a brownout or power failure, it may be necessary to preserve the contents of RAM. If a backup battery is installed at $V_{BAT}$, the device automatically switches the connected RAM to backup power when $V_{DD}$ fails. In order to allow the backup battery (e.g., 3.6-V lithium cells) to have a higher voltage than $V_{DD}$, these supervisors do not connect $V_{BAT}$ to $V_{OUT}$ when $V_{BAT}$ is greater than $V_{DD}$. $V_{BAT}$ only connects to $V_{OUT}$ (through a 15-Ω switch) when $V_{DD}$ falls below $V_{IT}$ and $V_{BAT}$ is greater than $V_{DD}$. When $V_{DD}$ recovers, switchover is deferred either until $V_{DD}$ crosses $V_{BAT}$, or when $V_{DD}$ rises above the reset threshold $V_{IT}$. $V_{OUT}$ connects to $V_{DD}$ through a 1-Ω (max) PMOS switch when $V_{DD}$ crosses the reset threshold.

| $V_{DD}>V_{BAT}$ | $V_{DD}>V_{IT}$ | $V_{OUT}$ |
|---|---|---|
| 1 | 1 | $V_{DD}$ |
| 1 | 0 | $V_{DD}$ |
| 0 | 1 | $V_{DD}$ |
| 0 | 0 | $V_{BAT}$ |

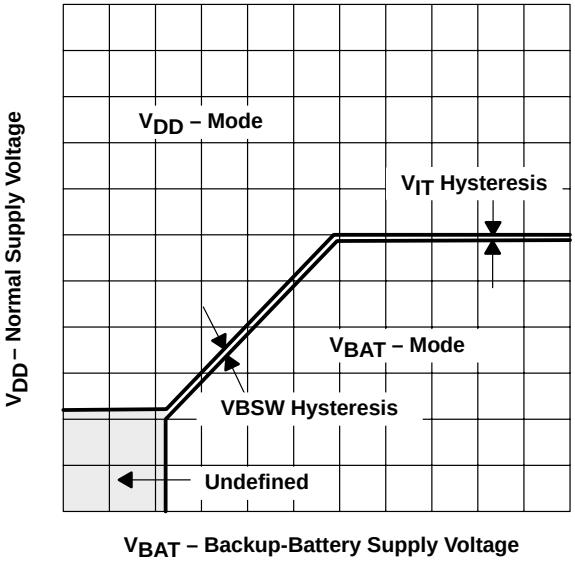



**Figure 1. $V_{DD}$ – $V_{BAT}$ Switchover**

## detailed description (continued)

### chip-enable signal gating

The internal gating of chip-enable (CE) signals prevents erroneous data from corrupting CMOS RAM during an under-voltage condition. The TPS3613 use a series transmission gate from $\overline{\text{CEIN}}$ to $\overline{\text{CEOUT}}$. During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from $\overline{\text{CEIN}}$ to $\overline{\text{CEOUT}}$ enables the TPS3613 device to be used with most processors.

The CE transmission gate is disabled and $\overline{\text{CEIN}}$ is high impedance (disable mode) while reset is asserted. During a power-down sequence when $V_{DD}$ crosses the reset threshold, the CE transmission gate is disabled and $\overline{\text{CEIN}}$ immediately becomes high impedance if the voltage at $\overline{\text{CEIN}}$ is high. If $\overline{\text{CEIN}}$ is low when reset is asserted, the CE transmission gate is disabled when $\overline{\text{CEIN}}$ goes high, or 15 μs after reset asserts, whichever occurs first. This allows the current write cycle to complete during power down. When the CE transmission gate is enabled, the impedance of $\overline{\text{CEIN}}$ appears as a resistor in series with the load at $\overline{\text{CEOUT}}$. The overall device propagation delay through the CE transmission gate depends on $V_{OUT}$, the source impedance of the drive connected to $\overline{\text{CEIN}}$, and the load at $\overline{\text{CEOUT}}$. To achieve minimum propagation delay, the capacitive load at $\overline{\text{CEOUT}}$ should be minimized, and a low-output-impedance driver is used.

In the disabled mode, the transmission gate is off and an active pullup connects $\overline{\text{CEOUT}}$ to $V_{OUT}$. This pullup turns off when the transmission gate is enabled.

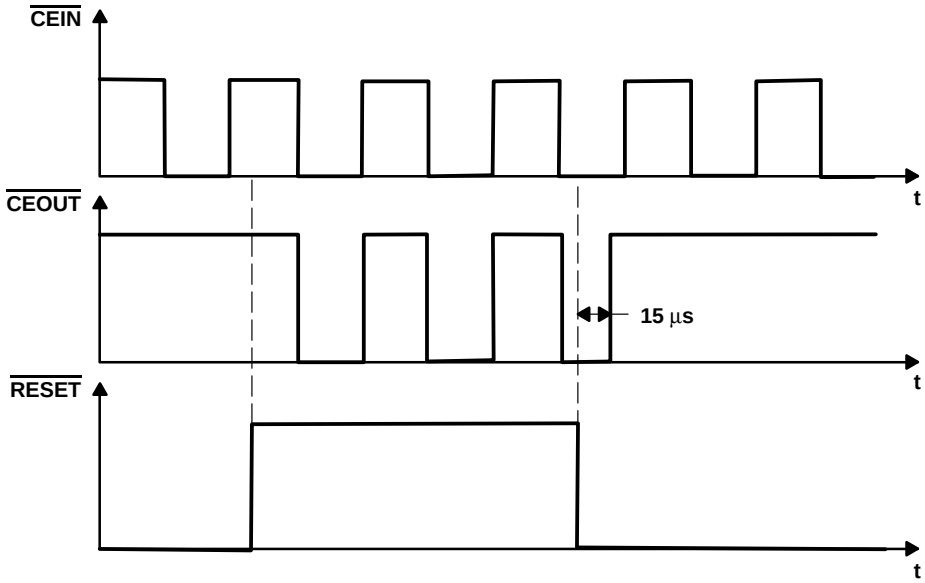



**Figure 2. Chip-Enable Timing**

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: $V_{DD}$ (see Note1) . . . . . 7 V
$\overline{MR}$ and SENSE pins (see Note 1) . . . . . –0.3 V to ($V_{DD}$ + 0.3 V)
Continuous output current at $V_{OUT}$: $I_O$ . . . . . 400 mA
All other pins, $I_O$ . . . . . ±10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, $T_A$ . . . . . –40°C to 85°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t=1000h continuously.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| DGS | 424 mW | 3.4 mW/°C | 271 mW | 220 mW |

### recommended operating conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{DD}$ | 1.65 | 5.5 | V |
| Battery supply voltage, $V_{BAT}$ | 1.5 | 5.5 | V |
| Input voltage, $V_I$ | 0 | $V_{DD}$ + 0.3 | V |
| High-level input voltage, $V_{IH}$ | 0.7 x $V_{DD}$ | | V |
| Low-level input voltage, $V_{IL}$ | | 0.3 x $V_{DD}$ | V |
| Continuous output current at $V_{OUT}$, $I_O$ | | 300 | mA |
| Input transition rise and fall rate at $\overline{MR}$, $\Delta t/\Delta V$ | | 100 | ns/V |
| Slew rate at $V_{DD}$ or $V_{bat}$ | | 1 | V/µs |
| Operating free-air temperature range, $T_A$ | –40 | 85 | °C |

## electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $\overline{\text{RESET}}$ | $V_{DD}$ = 1.8 V, $I_{OH}$ = –400 µA | $V_{DD}$ – 0.2 V | | | V |
| | | | $V_{DD}$ = 3.3 V, $I_{OH}$ = –2 mA<br>$V_{DD}$ = 5 V, $I_{OH}$ = –3 mA | $V_{DD}$ – 0.4 V | | | |
| | | RESET | $V_{DD}$ = 1.8 V, $I_{OH}$ = –20 µA | $V_{DD}$ – 0.3 V | | | |
| | | | $V_{DD}$ = 3.3 V, $I_{OH}$ = –80 µA<br>$V_{DD}$ = 5 V, $I_{OH}$ = –120 µA | $V_{DD}$ – 0.4 V | | | |
| | | $\overline{\text{CEOUT}}$ | $V_{OUT}$ = 1.8 V, $I_{OH}$ = –1 mA | $V_{OUT}$ – 0.2 V | | | |
| | | Enable mode<br>$\overline{\text{CEIN}}$ = $V_{OUT}$ | $V_{OUT}$ = 3.3 V, $I_{OH}$ = –2 mA<br>$V_{OUT}$ = 5 V, $I_{OH}$ = –5 mA | $V_{OUT}$ – 0.3 V | | | |
| | | $\overline{\text{CEOUT}}$<br>Disable mode | $V_{OUT}$ = 3.3 V, $I_{OH}$ = –0.5 mA | $V_{OUT}$ – 0.4 V | | | |
| $V_{OL}$ | Low-level output voltage | $\overline{\text{RESET}}$ | $V_{DD}$ = 1.8 V, $I_{OL}$ = 400 µA | | | 0.2 | V |
| | | RESET | $V_{DD}$ = 3.3 V, $I_{OL}$ = 2 mA<br>$V_{DD}$ = 5 V, $I_{OL}$ = 3 mA | | | 0.4 | |
| | | $\overline{\text{CEOUT}}$ | $V_{OUT}$ = 1.8 V, $I_{OL}$ = 1.0 mA | | | 0.2 | |
| | | Enable mode<br>$\overline{\text{CEIN}}$ = 0 V | $V_{OUT}$ = 3.3 V, $I_{OL}$ = 2 mA<br>$V_{OUT}$ = 5 V, $I_{OL}$ = 5 mA | | | 0.3 | |
| $V_{res}$ | Power-up reset voltage (see Note 2) | | $V_{DD}$ > 1.1 V or $V_{BAT}$ > 1.1 V, $I_{OL}$ = 20 µA | | | 0.4 | V |
| $V_{OUT}$ | Normal mode | | $I_O$ = 8.5 mA, $V_{DD}$ = 1.8 V, $V_{BAT}$ = 0 V | $V_{DD}$ – 50 mV | | | V |
| | | | $I_O$ = 125 mA, $V_{DD}$ = 3.3 V, $V_{BAT}$ = 0 V | $V_{DD}$ – 150 mV | | | |
| | | | $I_O$ = 200 mA, $V_{DD}$ = 5 V, $V_{BAT}$ = 0 V | $V_{DD}$ – 200 mV | | | |
| | Battery-backup mode | | $I_O$ = 0.5 mA, $V_{BAT}$ = 1.5 V, $V_{DD}$ = 0 V | $V_{BAT}$ – 20 mV | | | |
| | | | $I_O$ = 7.5 mA, $V_{BAT}$ = 3.3 V, $V_{DD}$ = 0 V | $V_{BAT}$ – 113 mV | | | |
| $R_{DS(on)}$ | $V_{DD}$ to $V_{OUT}$ on-resistance | | $V_{DD}$ = 5 V | | 0.6 | 1 | Ω |
| | $V_{BAT}$ to $V_{OUT}$ on-resistance | | $V_{BAT}$ = 3.3 V | | 8 | 15 | |
| $V_{IT}$ | Negative-going input threshold voltage (see Note 3) | | | 1.13 | 1.15 | 1.17 | V |
| $V_{hys}$ | Hysteresis | Sense | 1.1 V < $V_{IT}$ < 1.65 V | | 12 | | mV |
| | | $V_{BSW}$ (see Note 4) | $V_{DD}$ = 1.8 V | | 55 | | |
| $I_{IH}$ | High-level input current | $\overline{\text{MR}}$ | $\overline{\text{MR}}$ = 0.7 x $V_{DD}$, $V_{DD}$ = 5 V | –33 | | –76 | µA |
| $I_{IL}$ | Low-level input current | | $\overline{\text{MR}}$ = 0 V, $V_{DD}$ = 5 V | –110 | | –255 | |
| $I_I$ | Input current | SENSE | $V_{DD}$ = 1.15 V | –25 | | 25 | nA |
| $I_{DD}$ | $V_{DD}$ supply current | | $V_{OUT}$ = $V_{DD}$ | | | 40 | µA |
| | | | $V_{OUT}$ = $V_{BAT}$ | | | 40 | |
| $I_{BAT}$ | $V_{BAT}$ supply current | | $V_{OUT}$ = $V_{DD}$ | –0.1 | | 0.1 | µA |
| | | | $V_{OUT}$ = $V_{BAT}$ | | | 0.5 | |
| $I_{lkg}$ | $\overline{\text{CEIN}}$ leakage current | | Disable mode, $V_I$ < $V_{DD}$ | | | ±1 | µA |
| $C_i$ | Input capacitance | | $V_I$ = 0 V to 5 V | | 5 | | pF |

NOTES: 2. The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. $t_{r,(VDD)} \geq 15$ µs/V.
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near to the supply terminals.
4. For $V_{DD}$ < 1.6 V, $V_{OUT}$ switches to $V_{BAT}$ regardless of $V_{BAT}$

### timing requirements at $R_L$ = 1 MΩ, $C_L$ = 50 pF, $T_A$ = –40°C to 85°C

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_w$ | Pulse width | SENSE | $V_{IH} = V_{IT} + 0.2$ V, $V_{IL} = V_{IT} – 0.2$ V | 6 | | | µs |

### switching characteristics at $R_L$ = 1 MΩ, $C_L$= 50 pF, $T_A$ = –40°C to 85°C

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_d$ | Delay time | | $\overline{V_{SENSE}} \geq V_{IT} + 0.2$ V, $\overline{MR} \geq 0.7 \times V_{DD}$, See timing diagram | 60 | 100 | 140 | ms |
| $t_{PLH}$ | Propagation (delay) time, low-to-high-level output | 50% $\overline{\text{RESET}}$ to 50% $\overline{\text{CEOUT}}$ | $V_{OUT} = V_{IT}$ | | 15 | | µs |
| $t_{PHL}$ | Propagation (delay) time, high-to-low-level output | 50% $\overline{\text{CEIN}}$ to 50% $\overline{\text{CEOUT}}$, $C_L$ = 50 pF only (see Note 5) | $V_{DD}$ = 1.8 V | | 5 | 15 | ns |
| | | | $V_{DD}$ = 3.3 V | | 1.6 | 5 | |
| | | | $V_{DD}$ = 5 V | | 1 | 3 | |
| | | SENSE to $\overline{\text{RESET}}$ | $V_{IL} = V_{IT} – 0.2$ V, $V_{IH} = V_{IT} + 0.2$ V | | 2 | 5 | µs |
| | | $\overline{\text{MR}}$ to $\overline{\text{RESET}}$ | $V_{SENSE} \geq V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$ | | 0.1 | 1 | µs |
| | Transition time | $V_{DD}$ to $V_{BAT}$ | $V_{IH} = V_{BAT} + 0.2$ V, $V_{IL} = V_{BAT} – 0.2$ V, $V_{BAT} < V_{IT}$ | | | 3 | µs |

NOTE 5: Assured by design

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| $r_{DS(on)}$ | Static drain-source on-state resistance ($V_{DD}$ to $V_{OUT}$) | vs Output current | 3 |
| | Static drain-source on-state resistance ($V_{BAT}$ to $V_{OUT}$) | vs Output current | 4 |
| | Static drain-source on-state resistance ($\overline{CEIN}$ to $\overline{CEOUT}$) | vs Input voltage at $\overline{CEIN}$ | 5 |
| $I_{DD}$ | Supply current | vs Supply voltage | 6 |
| $V_{IT}$ | Input threshold voltage at $\overline{RESET}$ | vs Free-air temperature | 7 |
| $V_{OH}$ | High-level output voltage at $\overline{RESET}$ | vs High-level output current | 8, 9 |
| | High-level output voltage at $\overline{CEOUT}$ | | 10, 11, 12, 13 |
| $V_{OL}$ | Low-level output voltage at $\overline{RESET}$ | vs Low-level output current | 14, 15 |
| | Low-level output voltage at $\overline{CEOUT}$ | vs Low-level output current | 16, 17 |

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE ($V_{DD}$ to $V_{OUT}$) vs OUTPUT CURRENT**

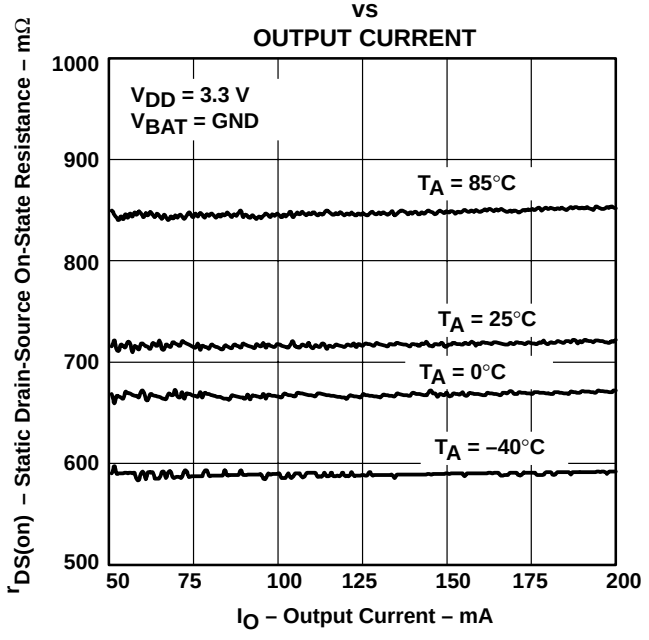



Figure 3

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE ($V_{BAT}$ to $V_{OUT}$) vs OUTPUT CURRENT**

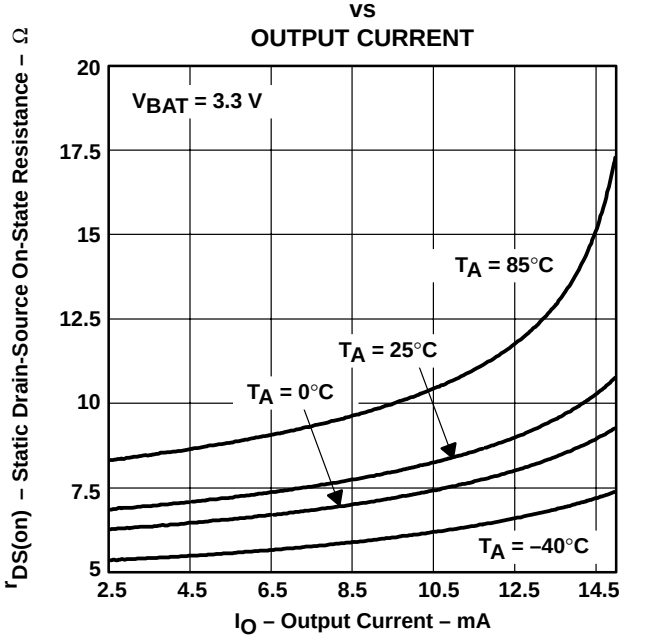



Figure 4

## TYPICAL CHARACTERISTICS

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE ($\overline{CEIN}$ to $\overline{CEOUT}$) vs INPUT VOLTAGE AT $\overline{CEIN}$**

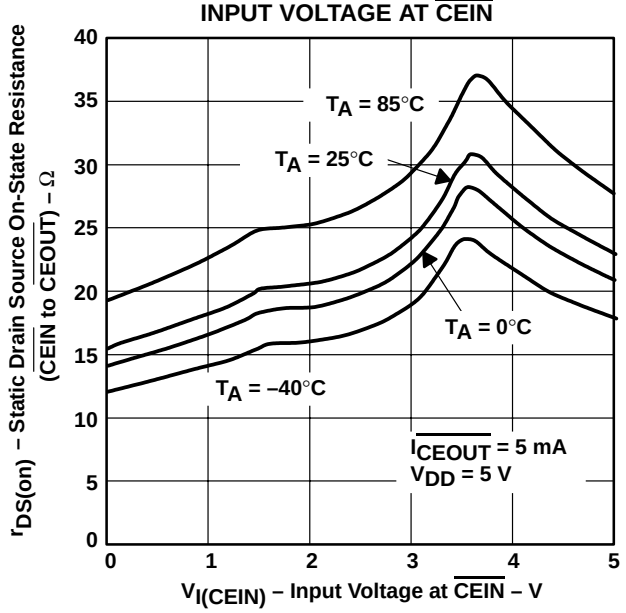



Figure 5

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

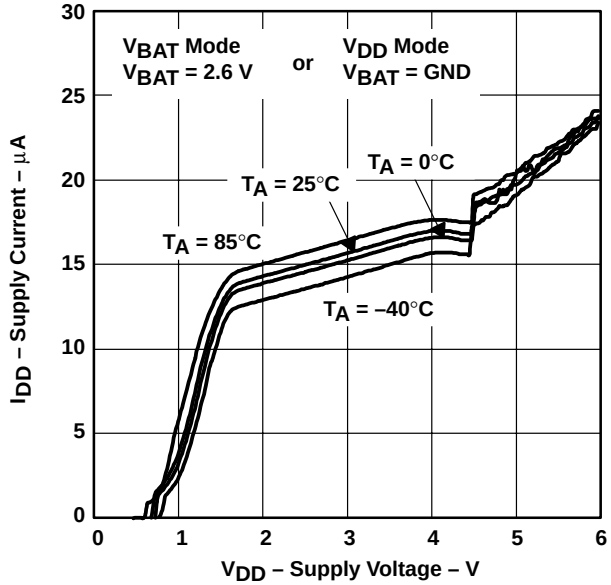



Figure 6

**INPUT THRESHOLD VOLTAGE AT $\overline{RESET}$ vs FREE-AIR TEMPERATURE**

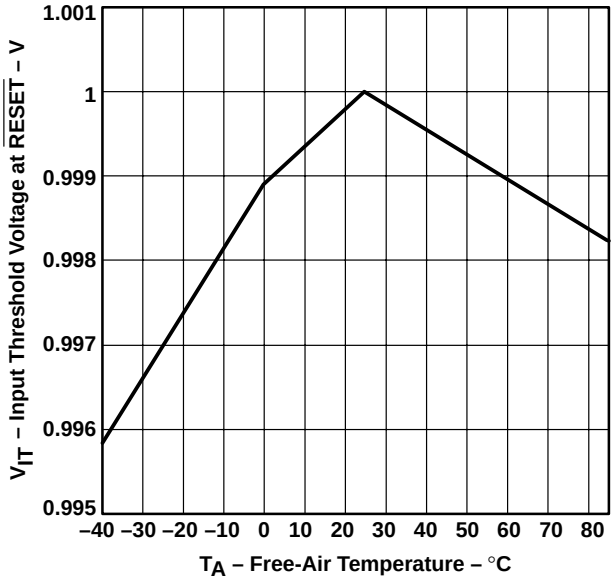



Figure 7

## TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$
vs
HIGH-LEVEL OUTPUT CURRENT

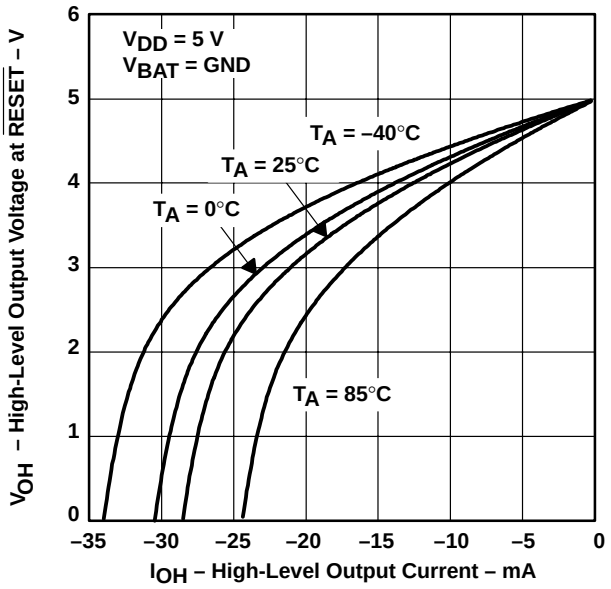



Figure 8

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$
vs
HIGH-LEVEL OUTPUT CURRENT

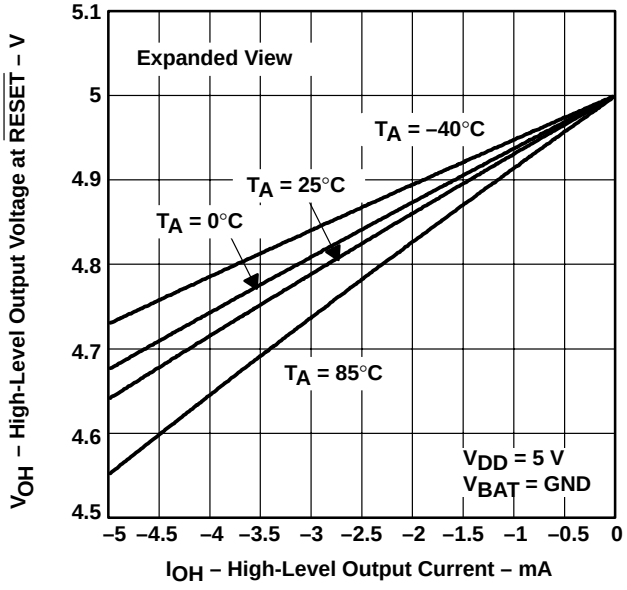



Figure 9

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{CEOUT}}$
vs
HIGH-LEVEL OUTPUT CURRENT

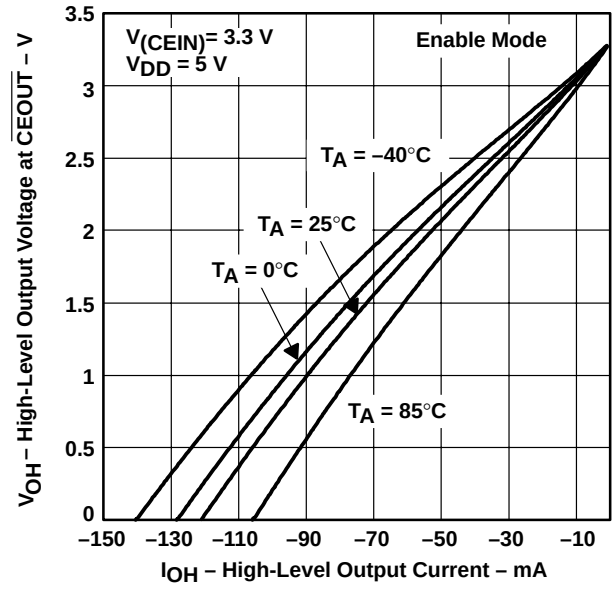



Figure 10

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{CEOUT}}$
vs
HIGH-LEVEL OUTPUT CURRENT

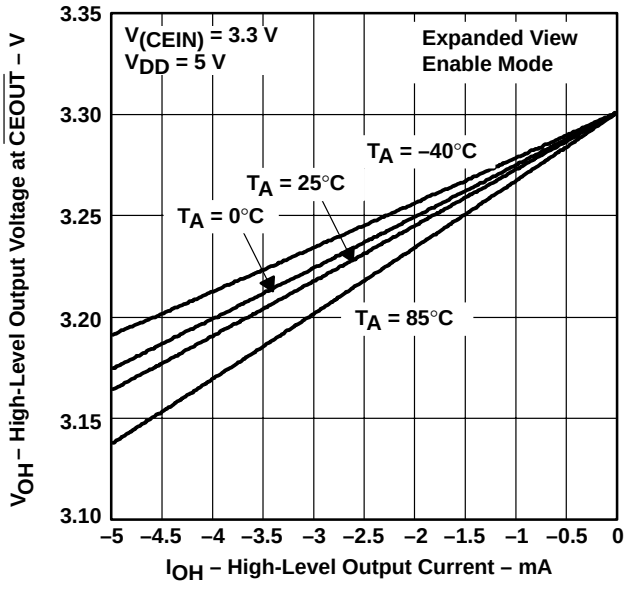



Figure 11

## TYPICAL CHARACTERISTICS

**HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{CEOUT}}$ vs HIGH-LEVEL OUTPUT CURRENT**

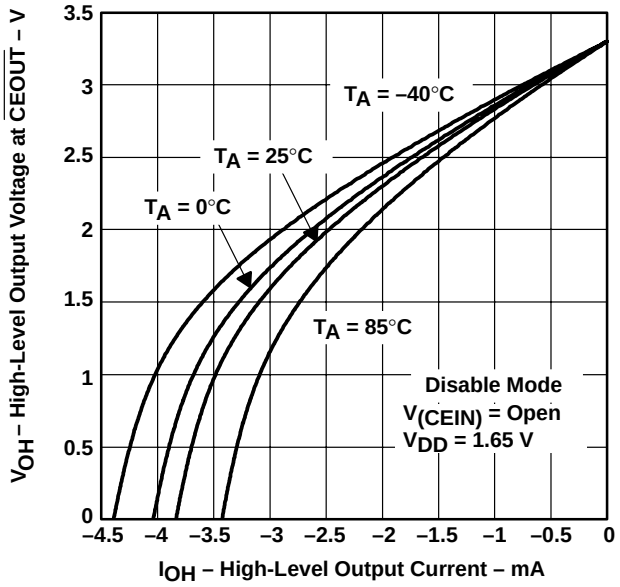



Figure 12

**HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{CEOUT}}$ vs HIGH-LEVEL OUTPUT CURRENT**

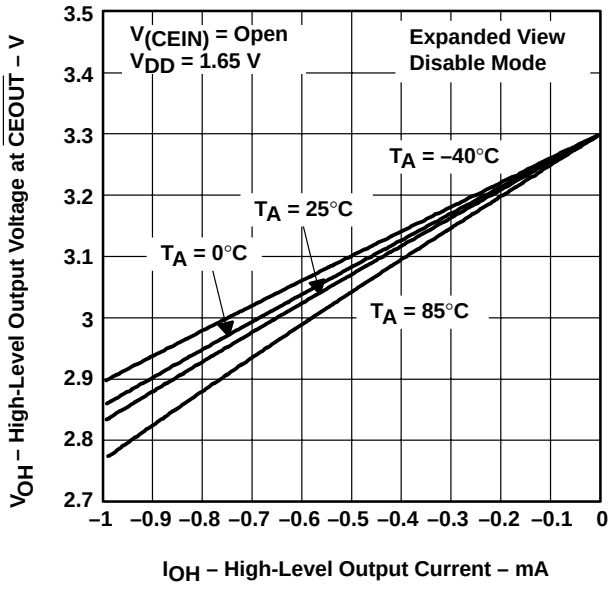



Figure 13

**LOW-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$ vs LOW-LEVEL OUTPUT CURRENT**

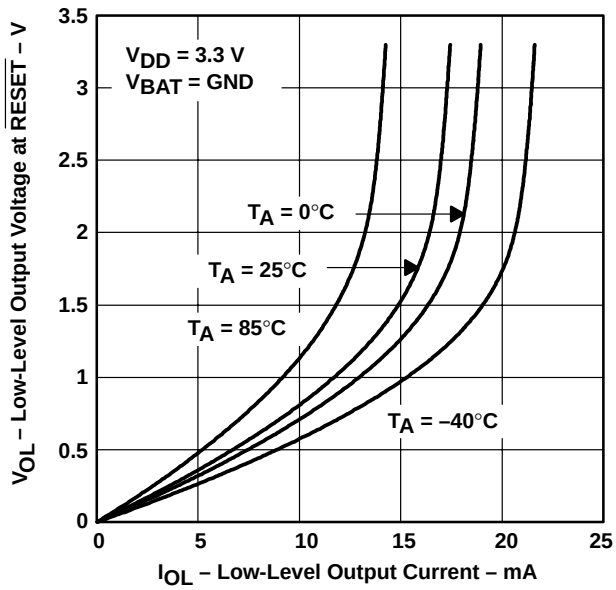



Figure 14

**LOW-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$ vs LOW-LEVEL OUTPUT CURRENT**

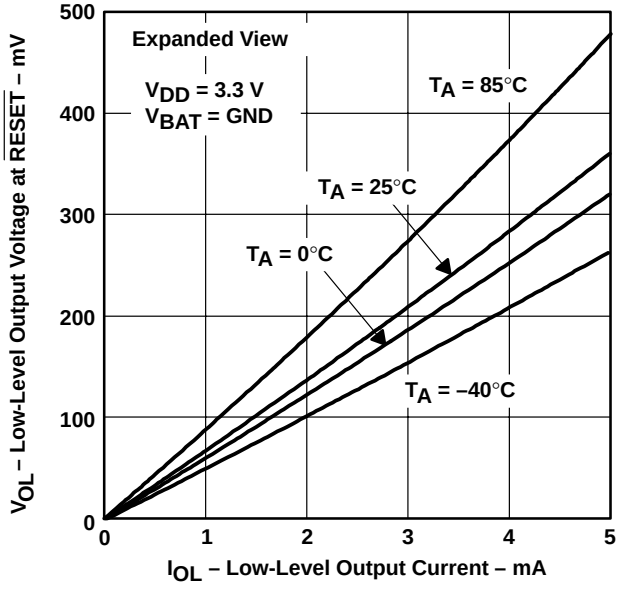



Figure 15

## TYPICAL CHARACTERISTICS

**LOW-LEVEL OUTPUT VOLTAGE AT $\overline{\text{CEOUT}}$ vs LOW-LEVEL OUTPUT CURRENT**

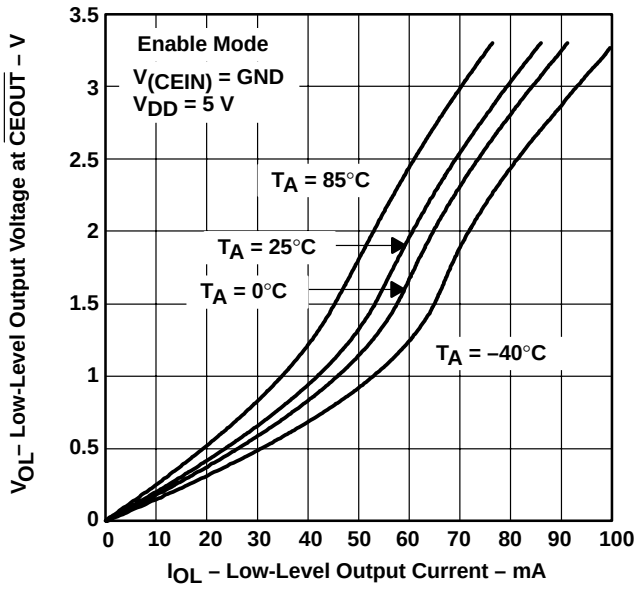



Figure 16

**LOW-LEVEL OUTPUT VOLTAGE AT $\overline{\text{CEOUT}}$ vs LOW-LEVEL OUTPUT CURRENT**

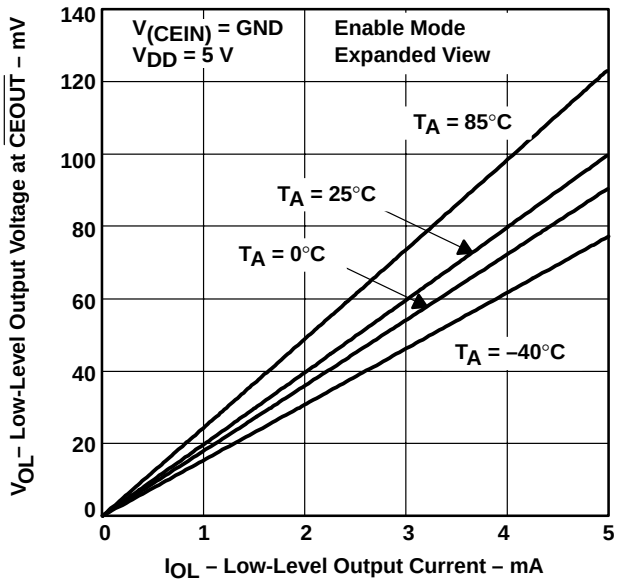
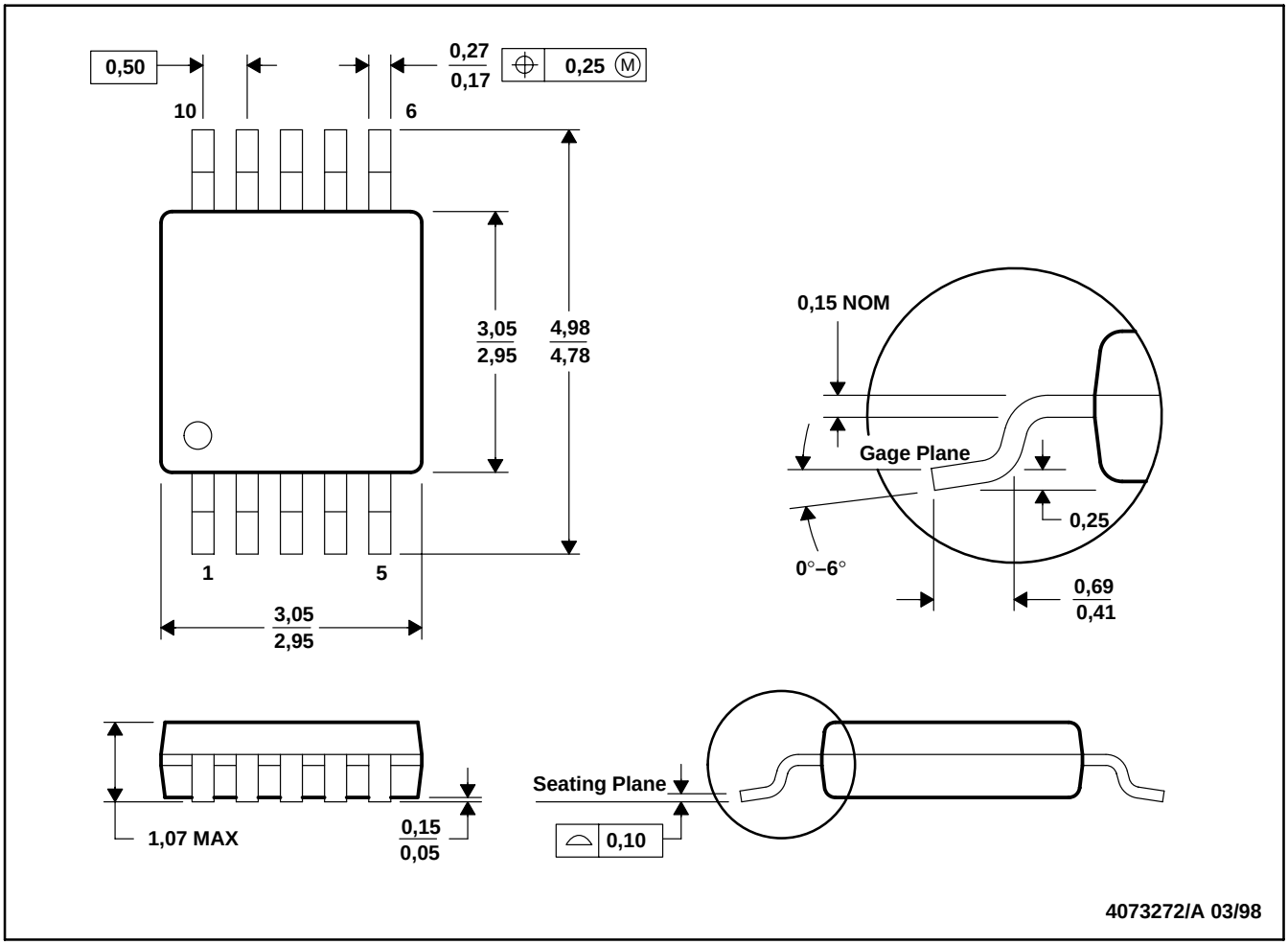



Figure 17

## MECHANICAL DATA

**DGS (S-PDSO-G10)** **PLASTIC SMALL-OUTLINE PACKAGE**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265