LM9036 Ultra-Low Quiescent Current Voltage Regulator

Check for Samples: LM9036

## FEATURES

- **Ultra low Ground Pin Current (I_{GND} ≤ 25µA for I_{OUT} = 0.1mA)**
- **Fixed 5V, 3.3V, 50mA Output**
- **Output Tolerance ±5% Over Line, Load, and Temperature**
- **Dropout Voltage Typically 200mV @ I_{OUT} = 50mA**
- **−45V Reverse Transient Protection**
- **Internal Short Circuit Current Limit**
- **Internal Thermal Shutdown Protection**
- **40V Operating Voltage Limit**

DESCRIPTION

The LM9036 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 25µA Ground Pin current at a 0.1mA load, the LM9036 is ideally suited for automotive and other battery operated systems. The LM9036 retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery protection, and thermal shutdown. The LM9036 has a 40V maximum operating voltage limit, a −40°C to +125°C operating temperature range, and ±5% output voltage tolerance over the entire output current, input voltage, and temperature range.
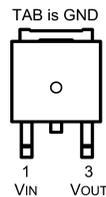
Typical Application
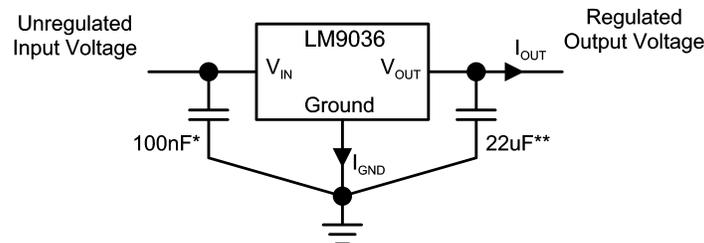
* Required if regulator is located more than 2″ from power supply filter capacitor.
** Required for stability. Must be rated over intended operating temperature range. Effective series resistance (ESR) is critical, see Electrical Characteristics. Locate capacitor as close as possible to the regulator output and ground pins. Capacitance may be increased without bound.
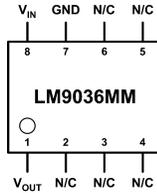
Connection Diagram

Figure 1. PFM
Top View
Order Number LM9036DT-5.0, LM9036DTX-5.0,
LM9036DT-3.3, LM9036DTX-3.3
See NS Package Number NDP0003B

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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```
          VIN  GND  N/C  N/C                              VIN  GND  GND  N/C
          8    7    6    5                                8    7    6    5

              LM9036MM                                        LM9036M
          ○                                              ○
          1    2    3    4                                1    2    3    4

          VOUT N/C  N/C  N/C                              VOUT GND  GND  N/C
```

Figure 2. 8 Lead VSSOP
Top View
LM9036MM-3.3, , LM9036MMX-3.3, LM9036MM-5.0,
LM9036MMX-5.0
See NS Package Number DGK
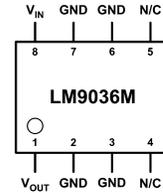
Figure 3. 8 Lead SOIC
Top View
LM9036M-3.3, LM9036MX-3.3, LM9036M-5.0,
LM9036MX-5.0
See NS Package Number D

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Input Voltage (Survival)	+55V, −45V
ESD Susceptibility[3]	±1.9kV
Power Dissipation[4]	Internally limited
Junction Temperature (T_{Jmax})	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model, 100pF discharge through a 1.5kΩ resistor.
(4) The maximum power dissipation is a function of T_{Jmax}, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{Jmax} − T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM9036 will go into thermal shutdown.

Operating Ratings

Operating Temperature Range	−40°C to +125°C
Maximum Input Voltage (Operational)	40V
SOIC-8 (D) θ_{JA}[1]	140°C/W
PFM (NDP0003B) θ_{JA}[1]	125°C/W
PFM (NDP0003B) θ_{JA}[2]	50°C/W
PFM (NDP0003B) θ_{JC}[1]	11°C/W
MSO-8 (DGK) θ_{JA}[1]	200°C/W

(1) Worst case (Free Air) per EIA / JESD51-3.
(2) Typical θ_{JA} with 1 square inch of 2oz copper pad area directly under the ground tab.

Product Folder Links: *LM9036*

Electrical Characteristics - LM9036-5.0

V_{IN} = 14V, I_{OUT} = 10 mA, T_J = 25°C, unless otherwise specified. **Boldface** limits apply over entire operating temperature range

Parameter	Conditions	Min (1)	Typical (2)	Max (1)	Units
Output Voltage (V_{OUT})		4.80	5.00	5.20	V
	5.5V ≤ V_{IN} ≤ 26V, 0.1mA ≤ I_{OUT} ≤ 50mA (3)	**4.75**	**5.00**	**5.25**	
Quiescent Current (I_{GND})	I_{OUT} = 0.1mA, 8V ≤ V_{IN} ≤ 24V		20	25	μA
	I_{OUT} = 1mA, 8V ≤ V_{IN} ≤ 24V		50	100	
	I_{OUT} = 10mA, 8V ≤ V_{IN} ≤ 24V		0.3	0.5	mA
	I_{OUT} = 50mA, 8V ≤ V_{IN} ≤ 24V		2.0	2.5	
Line Regulation (Δ V_{OUT})	6V ≤ V_{IN} ≤ 40V, I_{OUT} = 1mA		10	30	mV
Load Regulation (Δ V_{OUT})	0.1mA ≤ I_{OUT} ≤ 5mA		10	30	mV
	5mA ≤ I_{OUT} ≤ 50mA		10	30	mV
Dropout Voltage (Δ V_{OUT})	I_{OUT} = 0.1mA		0.05	0.10	V
	I_{OUT} = 50mA		0.20	0.40	V
Short Circuit Current (I_{SC})	V_{OUT} = 0V	65	120	250	mA
Ripple Rejection (PSRR)	V_{ripple} = 1V_{rms}, F_{ripple} = 120Hz	−40	−60		dB
Output Bypass Capacitance (C_{OUT})	0.3Ω ≤ ESR ≤ 8Ω 0.1mA ≤ I_{OUT} ≤ 50mA	10	22		μF

(1) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level) and 100% tested.
(2) Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.
(3) To ensure constant junction temperature, pulse testing is used.
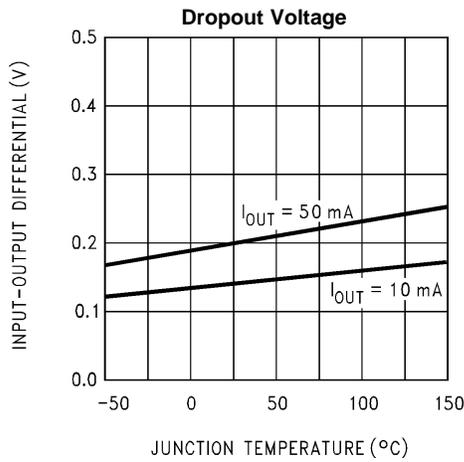
Electrical Characteristics - LM9036-3.3

V_{IN} = 14V, I_{OUT} = 10 mA, T_J = 25°C, unless otherwise specified. **Boldface** limits apply over entire operating temperature range

Parameter	Conditions	Min (1)	Typical (2)	Max (1)	Units
Output Voltage (V_{OUT})		3.168	3.30	3.432	V
	5.5V ≤ V_{IN} ≤ 26V, 0.1mA ≤ I_{OUT} ≤ 50mA (3)	**3.135**	**3.30**	**3.465**	
Quiescent Current (I_{GND})	I_{OUT} = 0.1mA, 8V ≤ V_{IN} ≤ 24V		20	25	μA
	I_{OUT} = 1mA, 8V ≤ V_{IN} ≤ 24V		50	100	
	I_{OUT} = 10mA, 8V ≤ V_{IN} ≤ 24V		0.3	0.5	mA
	I_{OUT} = 50mA, 8V ≤ V_{IN} ≤ 24V		2.0	2.5	
Line Regulation (Δ V_{OUT})	6V ≤ V_{IN} ≤ 40V, I_{OUT} = 1mA		10	30	mV
Load Regulation (Δ V_{OUT})	0.1mA ≤ I_{OUT} ≤ 5mA		10	30	mV
	5mA ≤ I_{OUT} ≤ 50mA		10	30	mV
Dropout Voltage (Δ V_{OUT})	I_{OUT} = 0.1mA		0.05	0.10	V
	I_{OUT} = 50mA		0.20	0.40	V
Short Circuit Current (I_{SC})	V_{OUT} = 0V	65	120	250	mA
Ripple Rejection (PSRR)	V_{ripple} = 1V_{rms}, F_{ripple} = 120Hz	−40	−60		dB
Output Bypass Capacitance (C_{OUT})	0.3Ω ≤ ESR ≤ 8Ω 0.1mA ≤ I_{OUT} ≤ 50mA	22	33		μF

(1) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level) and 100% tested.
(2) Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.
(3) To ensure constant junction temperature, pulse testing is used.

LM9036
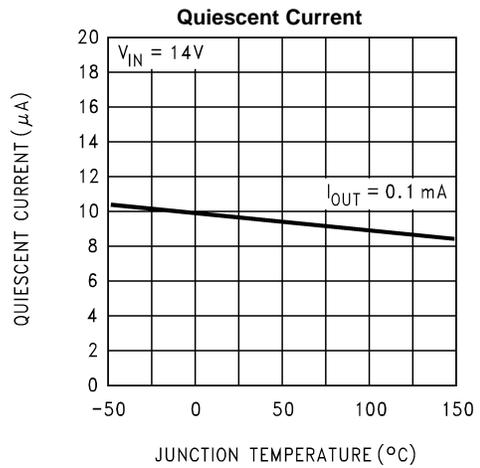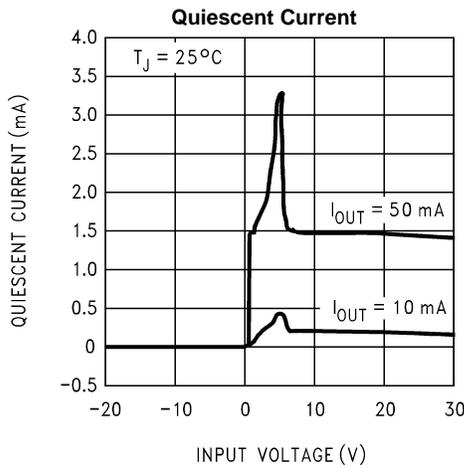
Typical Performance Characteristics

Dropout Voltage

Figure 4.

Quiescent Current

Figure 5.

Quiescent Current

Figure 6.

Quiescent Current

Figure 7.

Peak Output Current

Figure 8.

Product Folder Links: *LM9036*
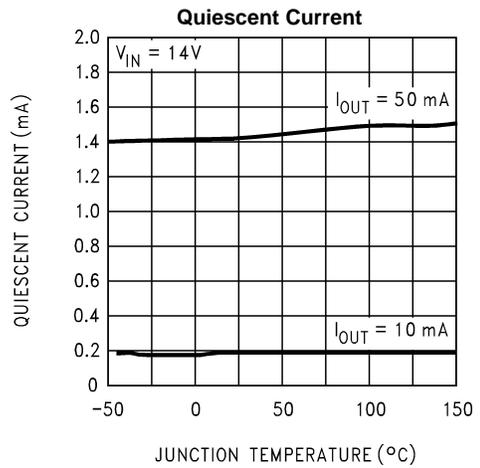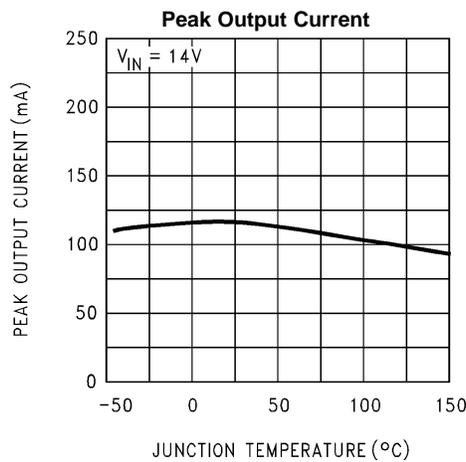
APPLICATIONS INFORMATION

Unlike other PNP low dropout regulators, the LM9036 remains fully operational to 40V. Owing to power dissipation characteristics of the package, full output current cannot be ensured for all combinations of ambient temperature and input voltage.

The junction to ambient thermal resistance θ_{JA} rating has two distinct components: the junction to case thermal resistance rating θ_{JC}; and the case to ambient thermal resistance rating θ_{CA}. The relationship is defined as: $\theta_{JA} = \theta_{JC} + \theta_{CA}$.

On the PFM package the ground tab is thermally connected to the backside of the die. Adding 1 square inch of 2 oz. copper pad area directly under the ground tab will improve the θ_{JA} rating to approximately 50°C/W.

While the LM9036 has an internally set thermal shutdown point of typically 150°C, this is intended as a safety feature only. Continuous operation near the thermal shutdown temperature should be avoided as it may have a negative affect on the life of the device.

Using the θ_{JA} for a LM9036DT mounted on a circuit board as defined at, see[1], and using the formula for maximum allowable dissipation given in, see[2], for an ambient temperature (T_A) of +85°C, we find that $P_{DMAX} =$ 1.3W. Including the small contribution of the quiescent current I_Q to the total power dissipation, the maximum input voltage (while still delivering 50mA output current) is 29.5V. The LM9036DT will go into thermal shutdown when attempting to deliver the full output current of 50mA, with an ambient temperature of +85°C, and the input voltage is greater than 29.5V. Similarly, with an ambient temperature of 25°C the $P_{DMAX} = 2.5$W, and the LM9036DT can deliver the full output current of 50mA with an input voltage of up to 40V.

While the LM9036 maintains regulation to 55V, it will not withstand a short circuit above 40V because of safe operating area limitations in the internal PNP pass device. Above 55V the LM9036 will break down with catastrophic effects on the regulator and possibly the load as well. Do not use this device in a design where the input operating voltage may exceed 40V, or where transients are likely to exceed 55V.

(1) Typical θ_{JA} with 1 square inch of 2oz copper pad area directly under the ground tab.
(2) The maximum power dissipation is a function of T_{Jmax}, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM9036 will go into thermal shutdown.

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E   **Page**

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Product Folder Links: *LM9036*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM9036DT-5.0/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LM9036D T-5.0	Samples
LM9036DTX-5.0/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LM9036D T-5.0	Samples
LM9036M-3.3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM903 6M-3	Samples
LM9036M-5.0	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	LM903 6M-5	
LM9036M-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM903 6M-5	Samples
LM9036MM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	KDB	Samples
LM9036MM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	KDA	Samples
LM9036MX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM903 6M-3	Samples
LM9036MX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM903 6M-5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM9036DTX-5.0/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LM9036MM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036MM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036MX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM9036MX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS
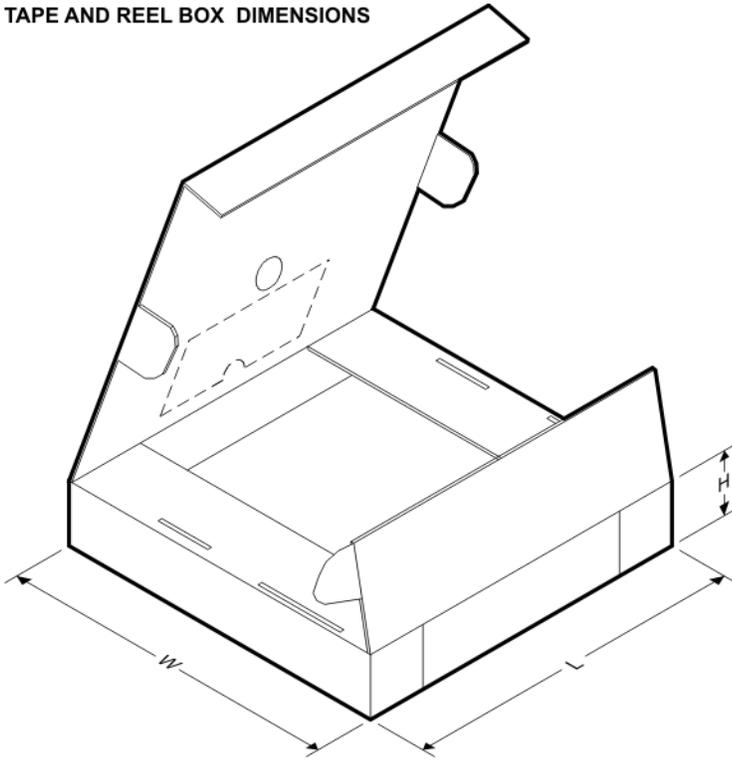
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM9036DTX-5.0/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LM9036MM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM9036MM-5.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM9036MX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM9036MX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

10.42
9.40

B

6.22
5.97

1.27
0.88

A

(2.345)

1

2.285

2

4.57

(2.5)

5.46
4.96

6.73
6.35

3

3X 0.88
0.64

1.02
0.64

PKG
℄

OPTIONAL

⊕ 0.25 Ⓜ C A B

8°
TOP & BOTTOM

8°

1.14
0.89

2.55 MAX

C

0.17

0.60
0.46

0.88
0.46

SEATING PLANE

0.51 MIN

4.32 MIN

3

2

4

1
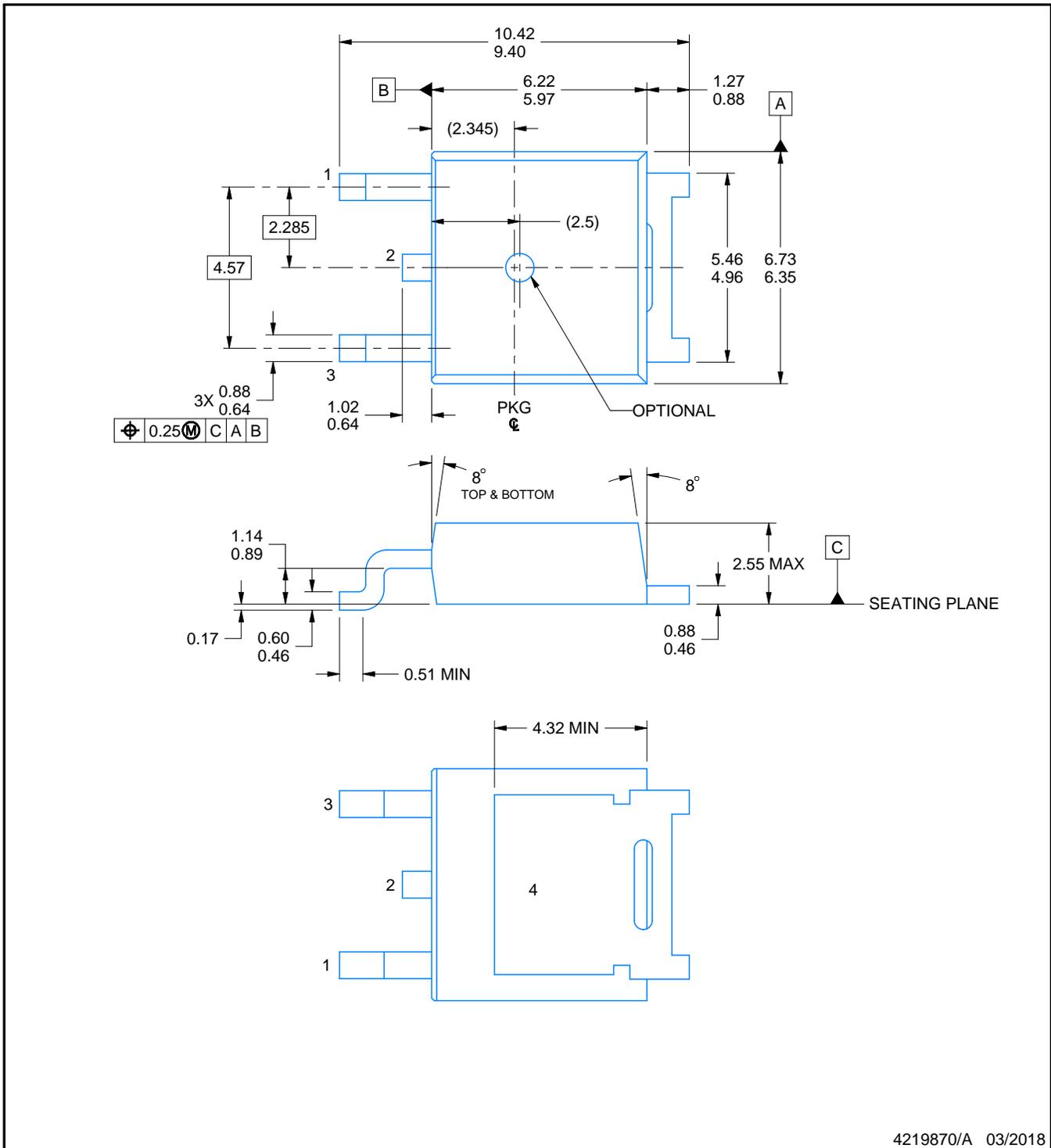
4219870/A 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-252.

SEE SOLDER MASK
DETAIL

2X (2.15)

2X (1.3)

1

(4.57)

3

(R0.05) TYP

(4.38)

(2.285)

(5.7)

4

SYMM

(5.5)

PKG
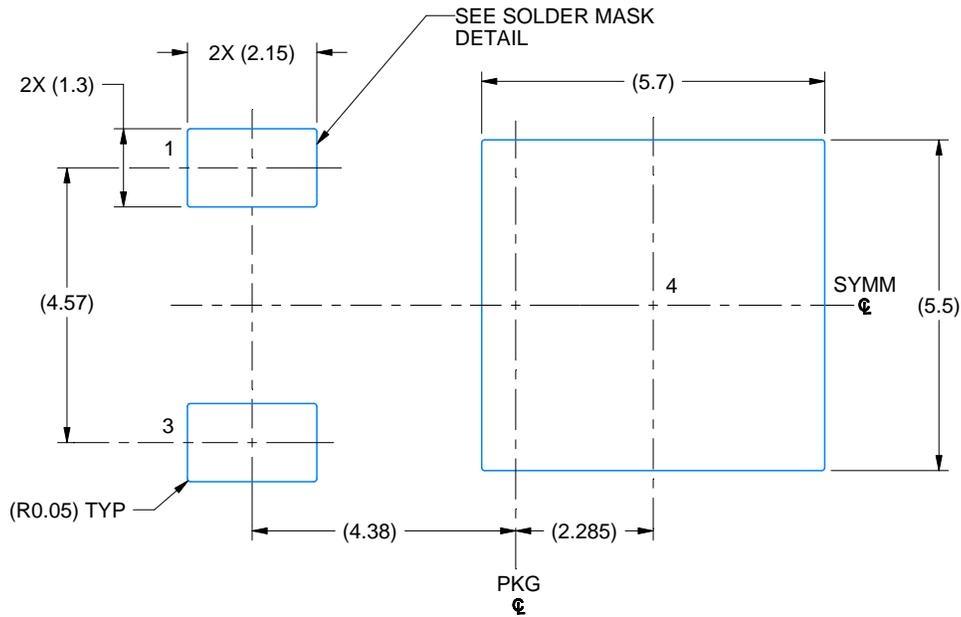
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

0.07 MAX
ALL AROUND

METAL EDGE

EXPOSED
METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

EXPOSED
METAL

SOLDER MASK
OPENING

SOLDER MASK DEFINED
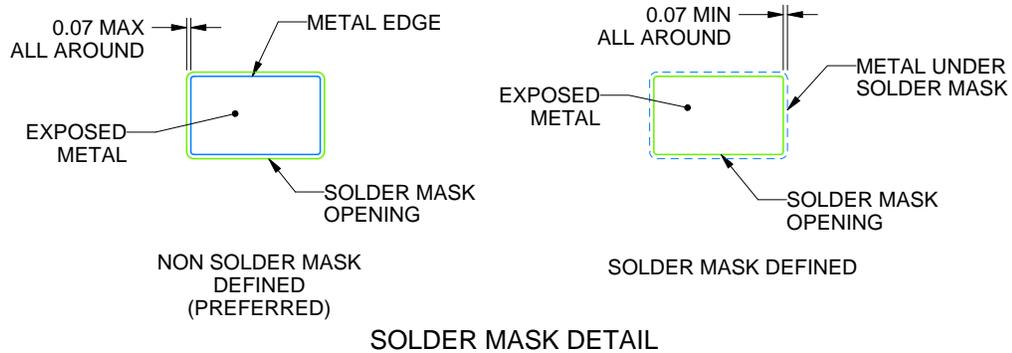
SOLDER MASK DETAIL

4219870/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
5. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

2X (2.15)

2X (1.3)

(0.26)

(1.35) TYP

(R0.05) TYP

(1.32) TYP

(4.57)

(4.38)

16X (1.12)

16X (1.15)

PKG
₡
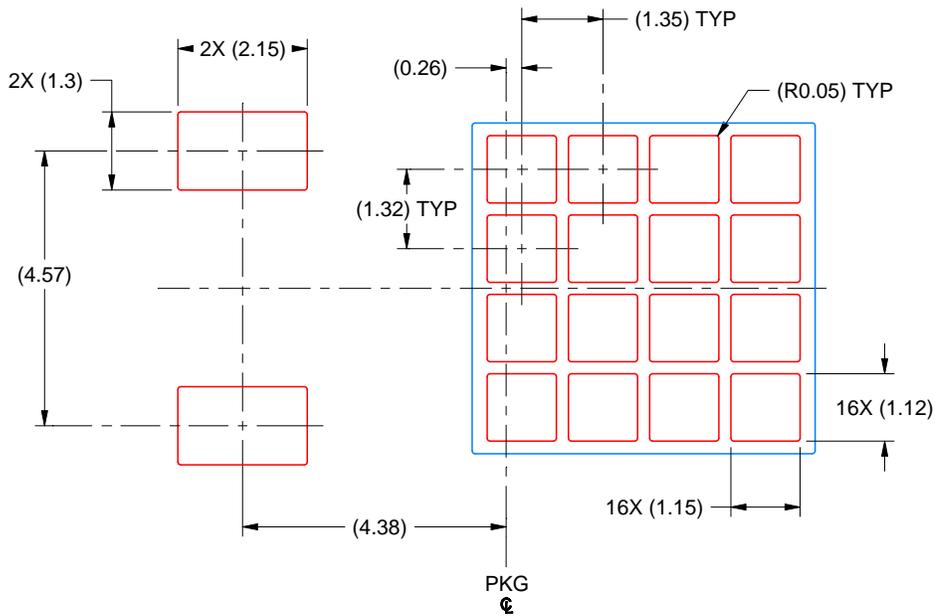
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 8X

4219870/A   03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

0.197 (5,00)
0.189 (4,80)
C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   D

Pin 1
Index Area

1   4

0.050 (1,27)   0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/M   06/11
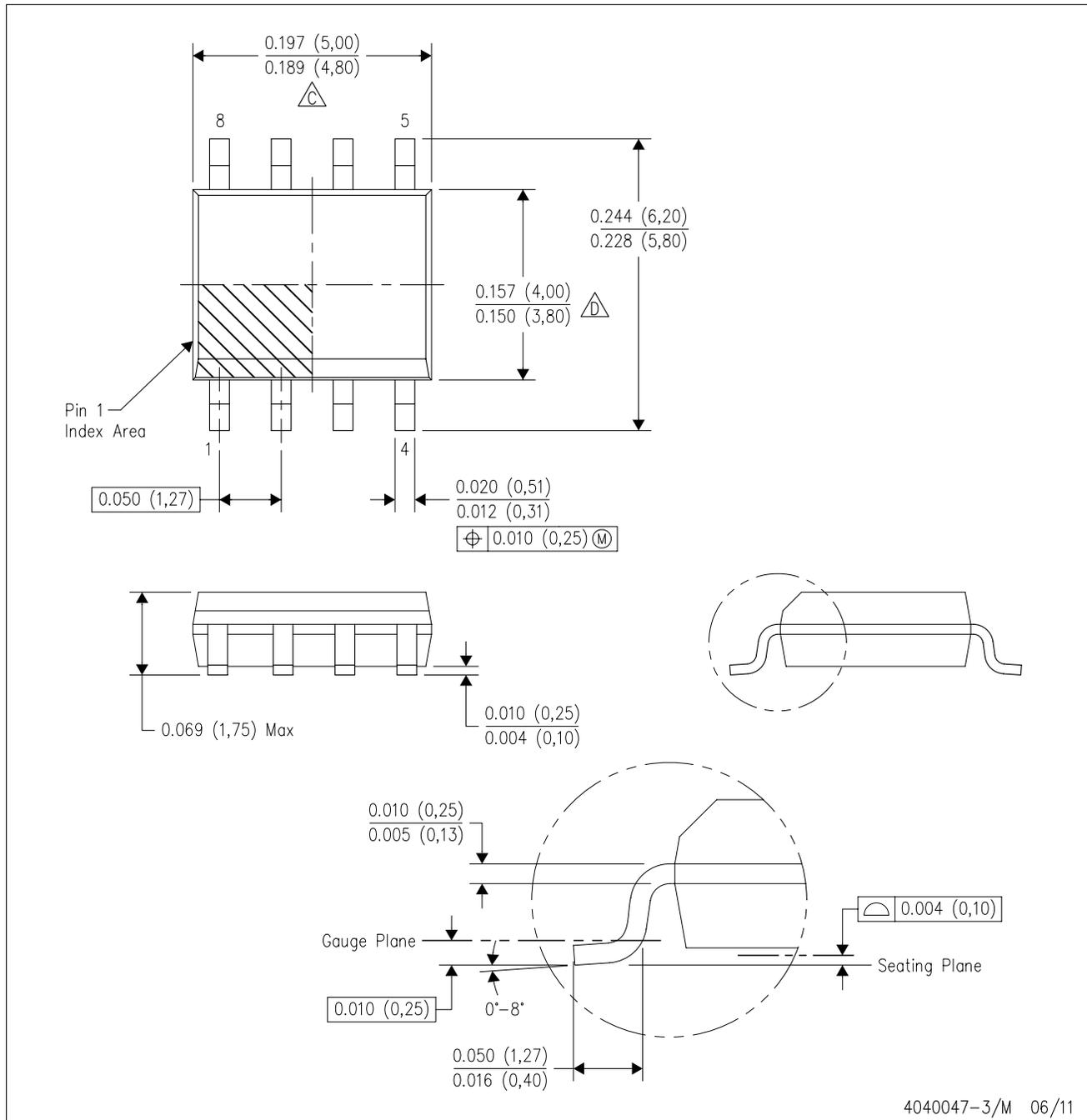
NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AA.
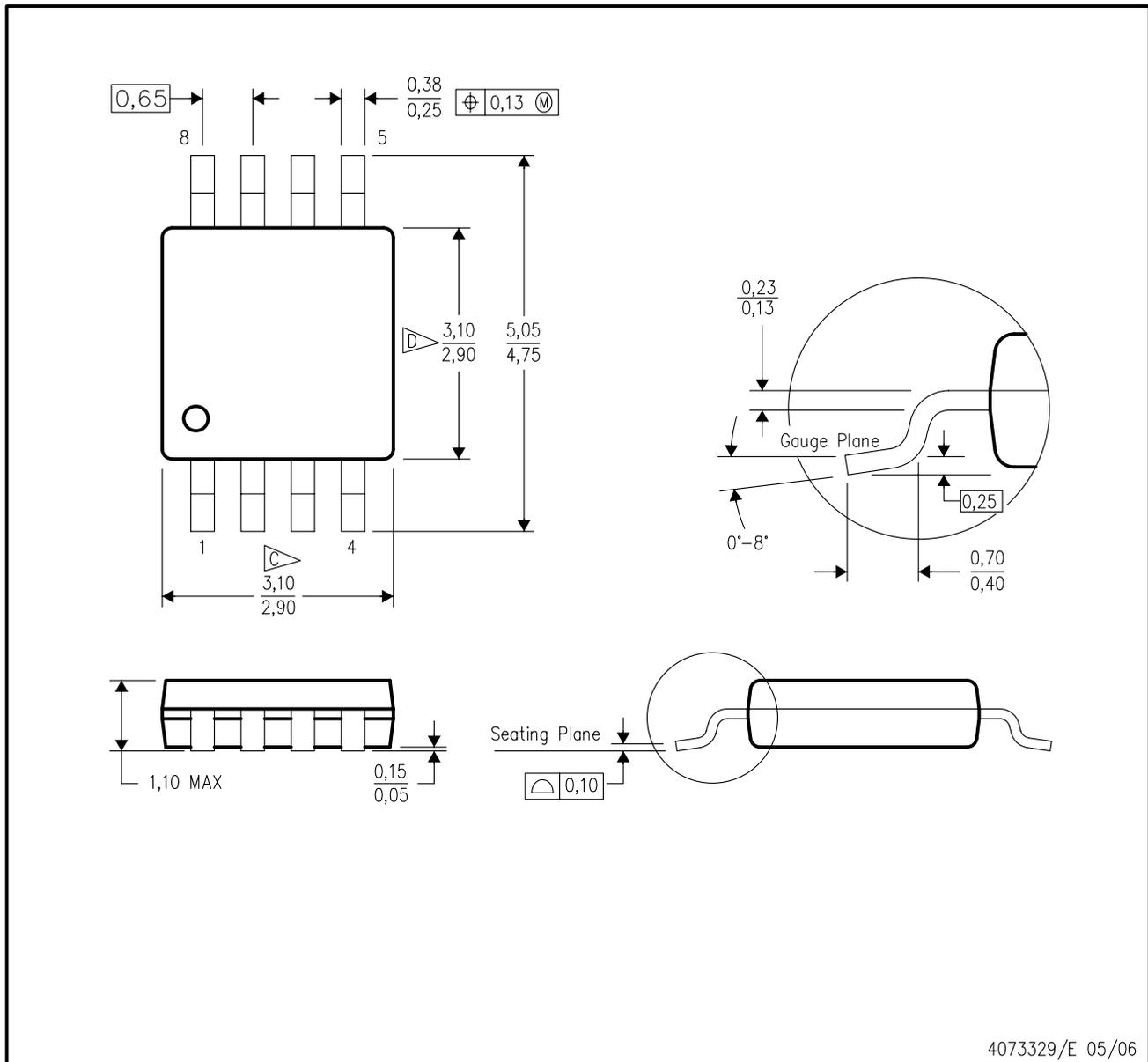
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DGK (S−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE

0,65

8   5

0,38
0,25   ⊕ 0,13 Ⓜ

3,10
2,90

5,05
4,75

1   4

C
3,10
2,90

0,23
0,13

Gauge Plane

0°−8°

0,25

0,70
0,40

1,10 MAX

0,15
0,05

Seating Plane

0,10

4073329/E 05/06

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.15 per end.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
         E.   Falls within JEDEC MO−187 variation AA, except interlead flash.
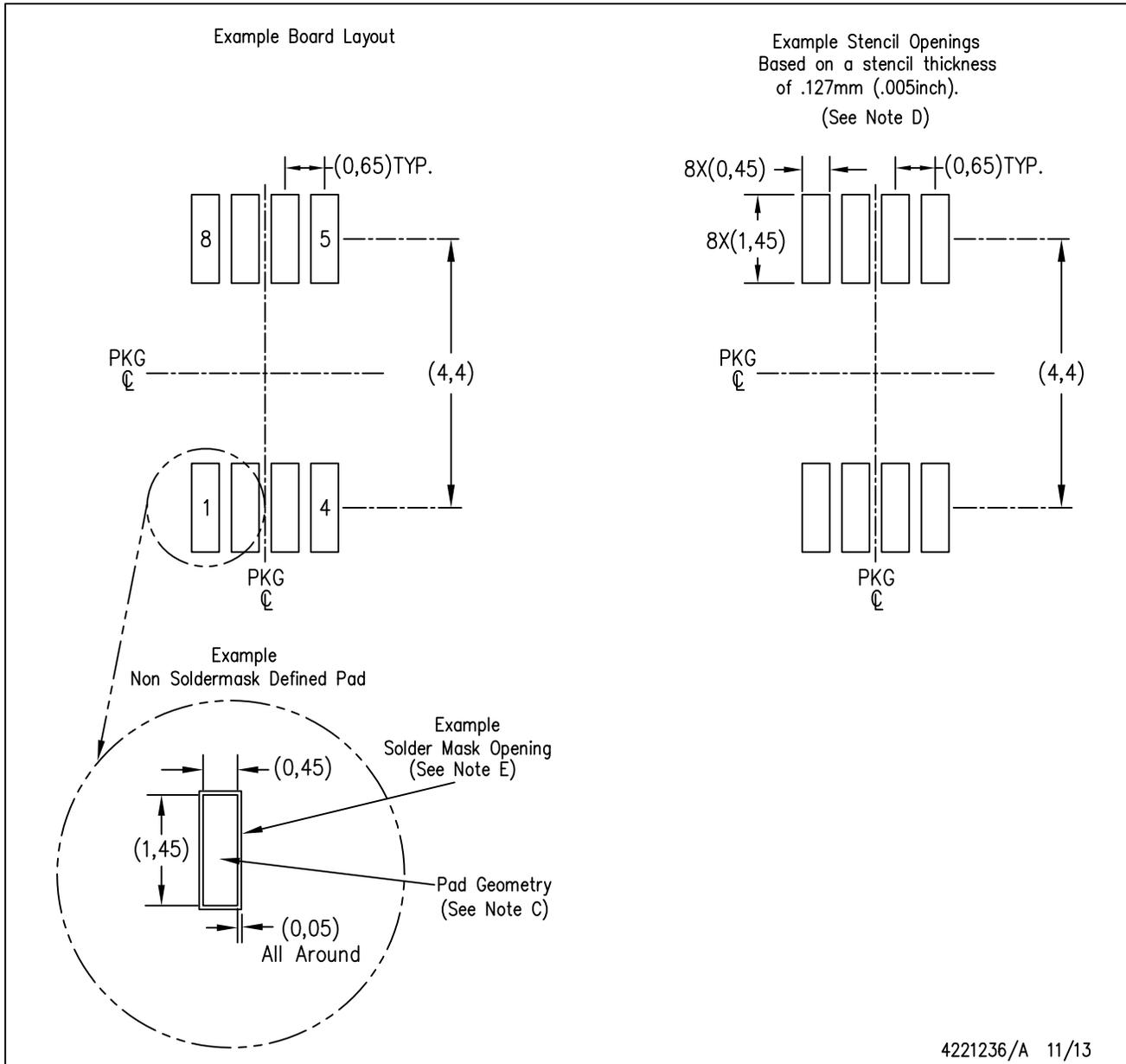
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DGK (S–PDSO–G8)   PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

|←→|(0,65)TYP.

8 [ ] [ ] 5 ─ ─ ─ ─

PKG
Ⅎ ─ ─ ─ ─   (4,4)

1 [ ] [ ] 4 ─ ─ ─ ─

PKG
Ⅎ

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

←(0,45)

(1,45)

─Pad Geometry
(See Note C)

←(0,05)
All Around

Example Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
(See Note D)

8X(0,45) →| |←→|(0,65)TYP.

8X(1,45)

PKG
Ⅎ ─ ─ ─ ─   (4,4)

PKG
Ⅎ

4221236/A 11/13

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate designs.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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IMPORTANT NOTICE