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TEXAS
INSTRUMENTS

TS5A9411

SCDS241B −MAY 2008−REVISED DECEMBER 2016

TS5A9411 10-Ω 1:2 SPDT Analog Switch
Single-Channel 2:1 Multiplexer and Demultiplexer

1 Features

- Specified Break-Before-Make Switching
- Low ON-State Resistance
  (10-Ω Maximum at V_{CC} = 5 V)
- Low Power Consumption
- TTL- and CMOS-Compatible Control Input
- Low Input and Output Capacitance
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion
- 2.25-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA
  Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model
    (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Control Inputs Are 5.5-V Tolerant

2 Applications

- Cell Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample-and-Hold Circuits

3 Description

The TS5A9411 device is a bidirectional, single-pole double-throw (SPDT) analog switch that is designed to operate from 2.25 V to 5.5 V. The device offers low ON-state resistance, low leakage, and low power with a break-before-make feature. These features make this device suitable for portable and battery-powered applications.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A9411	SOT (6)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (July 2008) to Revision B**   **Page**

- Added *Device Information* table, *Pin Configuration and Functions* section, *Specifications* section, *ESD Ratings* table, *Recommended Operating Conditions* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

- Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the data sheet 1

- Deleted *Summary of Characteristics* table 1

- Moved ON-state switch current and ON-state peak switch current From: *Absolute Maximum Ratings* table To: *Recommended Operating Conditions* table.. 4

- Added *Thermal Information* table 4

- Changed Package thermal impedance, $R_{\theta JA}$, value in *Thermal Information* table From: 259°C/W To: 346.7°C/W 4

- Deleted *Charge Injection vs V_{COM}* graph from *Typical Characteristics* 7

- Changed graph title From: OFF Isolation vs Crosstalk (V_{CC} = 3 V) To: Crosstalk and Insertion Loss vs Frequency (V_{CC} = 3 V) in *Typical Characteristics*.. 7

- Changed V+ to V_{CC} and IN to V_{IN} on all images in *Parameter Measurement Information*.. 8

Product Folder Links: *TS5A9411*

5 Pin Configuration and Functions

DCK Package
6-Pin SOT
Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COM	5	I/O	Common signal path
GND	3	—	Digital ground
IN	1	I	Digital control input. High = COM connected to NO; Low = COM connected to NC.
NC	4	I/O	Normally closed signal path
NO	6	I/O	Normally open signal path
VCC	2	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
Supply voltage	–0.3	6	V
Analog voltage[3]	–0.3	V_{CC} + 0.3	V
Digital input voltage	–0.5	V_{CC} + 0.3	V
Analog port diode current (V_{NC}, V_{NO}, V_{COM} < 0)	–50		mA
Digital input clamp current (V_I < 0)	–50		mA
Continuous current through VCC		100	mA
Continuous current through GND	–100		mA
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) This value is limited to 5.5 V (maximum).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Product Folder Links: *TS5A9411*

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.25	5.5	V
V_{NO}		NC	0	V_{CC}	
V_{NC}	Analog voltage	NO	0	V_{CC}	V
V_{COM}		COM	0	V_{CC}	
V_I	Digital input voltage		0	5.5	V
	ON-state switch current (V_{NO}, V_{NC}, V_{COM} = 0 to V_{CC})		−50	50	mA
	ON-state peak switch current (V_{NO}, V_{NC}, V_{COM} = 0 to V_{CC})[1]		−200	200	mA

(1) Pulse at 1-ms duration < 10% duty cycle

6.4 Thermal Information

	THERMAL METRIC[1]	TS5A9411 DCK (SOT) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	346.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	163.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	154.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	153.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: 5-V Supply

V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
r_{ON}	ON-state resistance	V_{NO} or V_{NC} = 3 V, V_{CC} = 4.5 V, I_{COM} = −10 mA, Switch ON, see Figure 5	T_A = 25°C		5.3	9	Ω
			−40°C ≤ T_A ≤ 85°C			10	
Δr_{ON}	ON-state resistance match between channels	V_{NO} or V_{NC} = 3 V, V_{CC} = 4.5 V, I_{COM} = −10 mA, Switch ON, see Figure 5	T_A = 25°C		0.03	0.3	Ω
			−40°C ≤ T_A ≤ 85°C			0.3	
$r_{ON(FLAT)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, V_{CC} = 4.5 V, I_{COM} = −10 mA, Switch ON, see Figure 5			2		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 1 V and V_{COM} = 1 V to 4.5 V, or V_{NC} or V_{NO} = 4.5 V and V_{COM} = 1 V; V_{CC} = 5.5 V, Switch OFF, see Figure 6	T_A = 25°C	−500		500	pA
			−40°C ≤ T_A ≤ 85°C	−3		3	nA
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 1 V and V_{COM} = 1 V, or V_{NC} or V_{NO} = 4.5 V and V_{COM} = 4.5 V; V_{CC} = 5.5 V, Switch ON, see Figure 7	T_A = 25°C	−500		500	pA
			−40°C ≤ T_A ≤ 85°C	−3		3	nA
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 1 V or 4.5 V, V_{CC} = 5.5 V, Switch ON, see Figure 7	T_A = 25°C	−500		500	pA
			−40°C ≤ T_A ≤ 85°C	−3		3	nA
DIGITAL INPUT (IN)[1]							
V_{IH}	Input logic high	−40°C ≤ T_A ≤ 85°C	4.5 V ≤ V_{CC} ≤ 5.5 V	2.4		5.5	V
			V_{CC} = 4.5 V	2		5.5	
V_{IL}	Input logic low	4.5 V ≤ V_{CC} ≤ 5.5 V, −40°C ≤ T_A ≤ 85°C		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0, V_{CC} = 5.5 V	T_A = 25°C	−0.05		0.05	μA
			−40°C ≤ T_A ≤ 85°C	−0.05		0.05	
DYNAMIC							
t_{ON}	Turnon time	V_{COM} = 3 V, R_L = 300 Ω, C_L = 35 pF, see Figure 9	V_{CC} = 5 V, T_A = 25°C			9	ns
			4.5 V ≤ V_{CC} ≤ 5.5 V, −40°C ≤ T_A ≤ 85°C			10	

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Electrical Characteristics: 5-V Supply (continued)

V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{OFF}	Turnoff time	V_{COM} = 3 V, R_L = 300 Ω, C_L = 35 pF, see Figure 9	V_{CC} = 5 V, T_A = 25°C			7	ns
			4.5 V ≤ V_{CC} ≤ 5.5 V, −40°C ≤ T_A ≤ 85°C			7.5	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = 3 V, R_L = 300 Ω, C_L = 35 pF, see Figure 10	T_A = 25°C		1		ns
			−40°C ≤ T_A ≤ 85°C		0.9		
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, see Figure 14			12.5		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or GND, f = 1 MHz, Switch OFF, see Figure 8			3.5		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_{CC} or GND, f = 1 MHz, see Figure 8			8.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, f = 1 MHz, Switch ON, see Figure 8			8.5		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND, f = 1 MHz, see Figure 8			25		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON, see Figure 11			100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, Switch OFF, see Figure 12			−84		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, Switch ON, see Figure 13			−85		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF, f = 20 Hz to 20 kHz, see Figure 15			0.03%		
SUPPLY							
I_{CC}	Positive supply current	V_I = V_{CC} or GND, V_{CC} = 5.5 V, Switch ON or OFF	T_A = 25°C		0.01		µA
			−40°C ≤ T_A ≤ 85°C			0.5	

6.6 Electrical Characteristics: 3-V Supply

V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
r_{ON}	ON-state resistance	V_{NO} or V_{NC} = 1.5 V, V_{CC} = 2.7 V, I_{COM} = −10 mA, Switch ON, see Figure 5	T_A = 25°C		11.5	15	Ω
			−40°C ≤ T_A ≤ 85°C			20	
Δr_{ON}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.5 V, V_{CC} = 2.7 V, I_{COM} = −10 mA, Switch ON, see Figure 5	T_A = 25°C		0.05	0.3	Ω
			−40°C ≤ T_A ≤ 85°C			0.3	
$r_{ON(FLAT)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = −10 mA, Switch ON, see Figure 5			2		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 1 V and V_{COM} = 1 V to 3 V, or V_{NC} or V_{NO} = 3 V and V_{COM} = 1 V; V_{CC} = 3.3 V, Switch OFF, see Figure 6	T_A = 25°C	−400		400	pA
			−40°C ≤ T_A ≤ 85°C	−2		2	nA
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 1 V and V_{COM} = 1 V, or V_{NC} or V_{NO} = 3 V and V_{COM} = 3 V; V_{CC} = 3.3 V, Switch ON, see Figure 7	T_A = 25°C	−400		400	pA
			−40°C ≤ T_A ≤ 85°C	−2		2	nA
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 1 V or 3 V, V_{CC} = 3.3 V, Switch ON, see Figure 7	T_A = 25°C	−400		400	pA
			−40°C ≤ T_A ≤ 85°C	−2		2	nA
DIGITAL INPUT (IN)[1]							
V_{IH}	Input logic high	−40°C ≤ T_A ≤ 85°C		2		5.5	V
V_{IL}	Input logic low	−40°C ≤ T_A ≤ 85°C		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0, V_{CC} = 3.6 V	T_A = 25°C	−0.05		0.05	µA
			−40°C ≤ T_A ≤ 85°C	−0.05		0.05	
DYNAMIC							
t_{ON}	Turnon time	V_{COM} = 3 V, R_L = 300 Ω, C_L = 35 pF, see Figure 9	V_{CC} = 3.3 V, T_A = 25°C			13	ns
			2.7 V ≤ V_{CC} ≤ 3.3 V, −40°C ≤ T_A ≤ 85°C			15	
t_{OFF}	Turnoff time	V_{COM} = 3 V, R_L = 300 Ω, C_L = 35 pF, see Figure 9	V_{CC} = 3.3 V, T_A = 25°C			7.5	ns
			2.7 V ≤ V_{CC} ≤ 3.3 V, −40°C ≤ T_A ≤ 85°C			8.5	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = 3 V, R_L = 300 Ω, V_{CC} = 3.3 V, C_L = 35 pF, see Figure 10	T_A = 25°C		1		ns
			−40°C ≤ T_A ≤ 85°C		0.9		
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, see Figure 14			6		pC

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Electrical Characteristics: 3-V Supply (continued)

V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$C_{NC\,(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or GND, f = 1 MHz, Switch OFF, see Figure 8			3.5		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_{CC} or GND, f = 1 MHz, Switch OFF, see Figure 8			8.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, f = 1 MHz, Switch OFF, see Figure 8			8.5		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND, f = 1 MHz, see Figure 8			2.5		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON, see Figure 11			100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz, Switch OFF, see Figure 12			−84		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz, Switch ON, see Figure 13			−85		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF, f = 20 Hz to 20 kHz, see Figure 15			0.09%		
SUPPLY							
I_{CC}	Positive supply current	V_I = V_{CC} or GND, V_{CC} = 3.6 V, Switch ON or OFF	T_A = 25°C		0.01		μA
			−40°C ≤ T_A ≤ 85°C			0.5	

6.7 Electrical Characteristics: 2.5-V Supply

V_{CC} = 2.5 V, T_A = 25°C (unless otherwise noted)

| PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
r_{ON}	ON-state resistance	V_{NO} or V_{NC} = 1 V, V_{CC} = 2.25 V, I_{COM} = −10 mA, Switch ON, see Figure 5	T_A = 25°C		15	25	Ω
			−40°C ≤ T_A ≤ 85°C			28	
Δr_{ON}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1 V, V_{CC} = 2.25 V, I_{COM} = −10 mA, Switch ON, see Figure 5	T_A = 25°C		0.06	0.3	Ω
			−40°C ≤ T_A ≤ 85°C			0.3	
$r_{ON(FLAT)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, V_{CC} = 2.25 V, I_{COM} = −10 mA, Switch ON, see Figure 5			4		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 1.5 V and V_{COM} = 0.5 V to 1.5 V, or V_{NC} or V_{NO} = 1.5 V and V_{COM} = 1.5 V; V_{CC} = 2.75 V, Switch OFF, see Figure 6	T_A = 25°C	−300		300	pA
			−40°C ≤ T_A ≤ 85°C	−1		1	nA
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 1.5 V and V_{COM} = 0.5 V to 1.5 V, or V_{NC} or V_{NO} = 1.5 V and V_{COM} = 1.5 V; V_{CC} = 2.75 V, Switch ON, see Figure 7	T_A = 25°C	−300		300	pA
			−40°C ≤ T_A ≤ 85°C	−1		1	nA
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0.5 V or 1.5 V, V_{CC} = 2.75 V, Switch ON, see Figure 7	T_A = 25°C	−300		300	pA
			−40°C ≤ T_A ≤ 85°C	−1		1	nA
DIGITAL INPUT (IN)[1]							
V_{IH}	Input logic high		−40°C ≤ T_A ≤ 85°C	2		5.5	V
V_{IL}	Input logic low		−40°C ≤ T_A ≤ 85°C	0		0.4	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0 V, V_{CC} = 2.75 V	T_A = 25°C	−0.05		0.05	μA
			−40°C ≤ T_A ≤ 85°C	−0.05		0.05	
DYNAMIC							
t_{ON}	Turnon time	V_{COM} = 2 V, R_L = 300 Ω, C_L = 35 pF, see Figure 9	V_{CC} = 2.5 V, T_A = 25°C			18	ns
			2.25 V ≤ V_{CC} ≤ 2.75 V, −40°C ≤ T_A ≤ 85°C			20	
t_{OFF}	Turnoff time	V_{COM} = 2 V, R_L = 300 Ω, C_L = 35 pF, see Figure 9	V_{CC} = 2.5 V, T_A = 25°C			8	ns
			2.25 V ≤ V_{CC} ≤ 2.75 V, −40°C ≤ T_A ≤ 85°C			9.5	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = 2 V, R_L = 300 Ω, C_L = 35 pF, see Figure 10	T_A = 25°C	1			ns
			−40°C ≤ T_A ≤ 85°C	0.9			
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, see Figure 14			4.5		pC
$C_{NC\,(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_{CC} or GND, f = 1 MHz, Switch OFF, see Figure 8			3.5		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_{CC} or GND, f = 1 MHz, Switch OFF, see Figure 8			8.5		pF

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Product Folder Links: *TS5A9411*

Electrical Characteristics: 2.5-V Supply (continued)

V_{CC} = 2.5 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, f = 1 MHz, Switch OFF, see Figure 8			8.5		pF
C_i	Digital input capacitance	V_I = V_{CC} or GND, f = 1 MHz, see Figure 8			2.5		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON, see Figure 11			100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz, Switch OFF, see Figure 12			–84		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz, Switch ON, see Figure 13			–84		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF, f = 20 Hz to 20 kHz, see Figure 15			0.15%		
SUPPLY							
I_{CC}	Positive supply current	V_I = V_{CC} or GND, V_{CC} = 2.75 V, Switch ON or OFF	T_A = 25°C		0.01		μA
			–40°C ≤ T_A ≤ 85°C			0.5	

6.8 Typical Characteristics
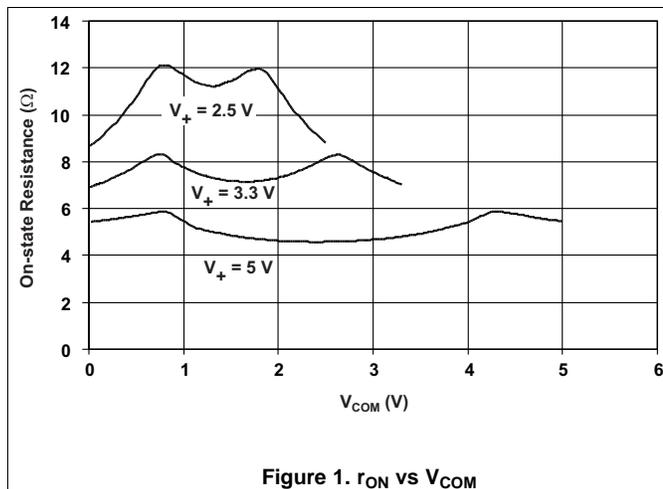
Figure 1. r_{ON} vs V_{COM}
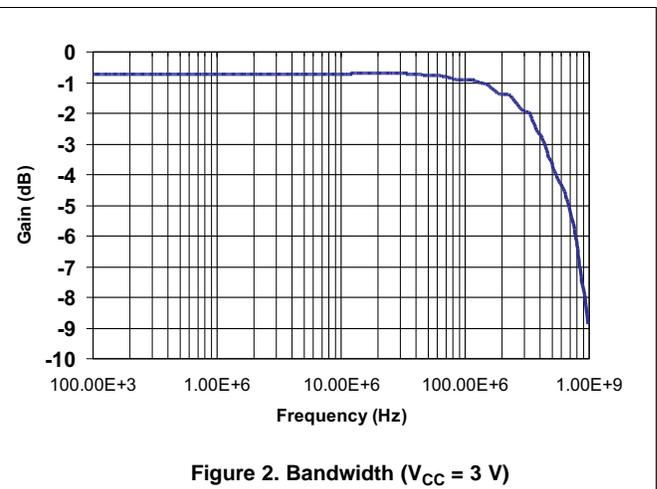
Figure 2. Bandwidth (V_{CC} = 3 V)
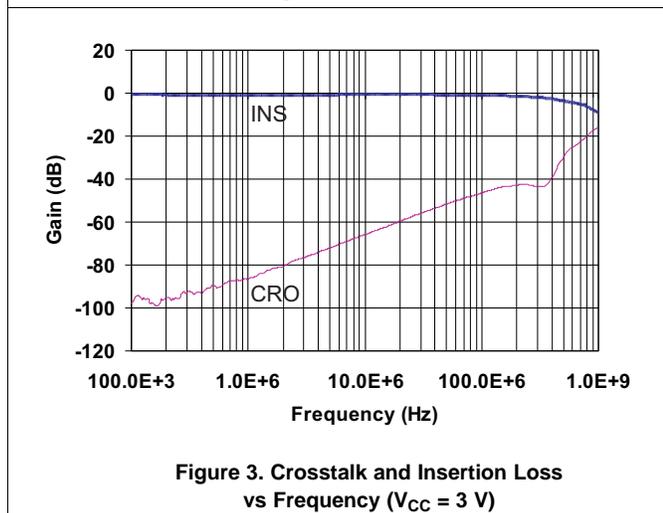
Figure 3. Crosstalk and Insertion Loss
vs Frequency (V_{CC} = 3 V)
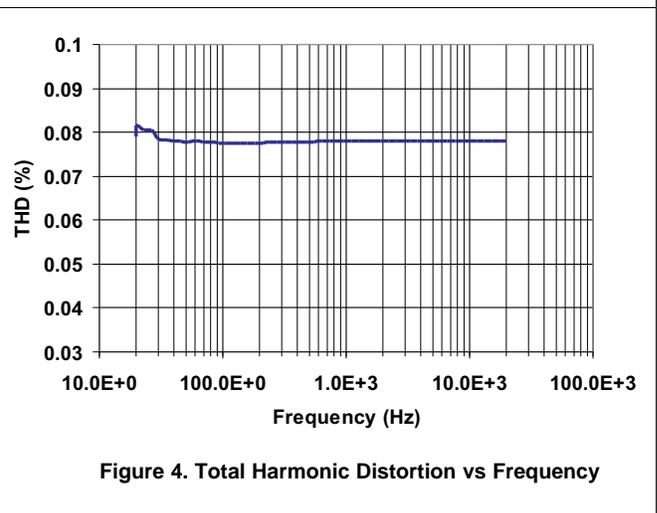
Figure 4. Total Harmonic Distortion vs Frequency

Product Folder Links: TS5A9411

7 Parameter Measurement Information

Figure 5. ON-State Resistance

$$r_{ON} = \frac{V_{COM} - V_{NO} \text{ or } V_{NC}}{I_{COM}}$$

Channel ON

$V_{IN} = V_{IH} \text{ or } V_{IL}$

Figure 5. ON-State Resistance

OFF-State Leakage Current
Channel OFF
$V_{IN} = V_{IH} \text{ or } V_{IL}$

$I_{NC(OFF)}, I_{NC(PWROFF)}, I_{NO(OFF)}, I_{NO(PWROFF)}, I_{COM(OFF)}, I_{COM(PWROFF)}$
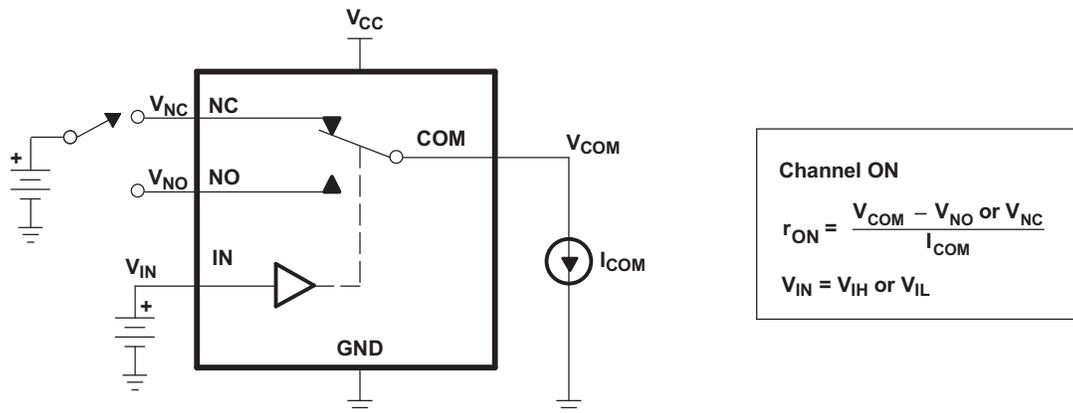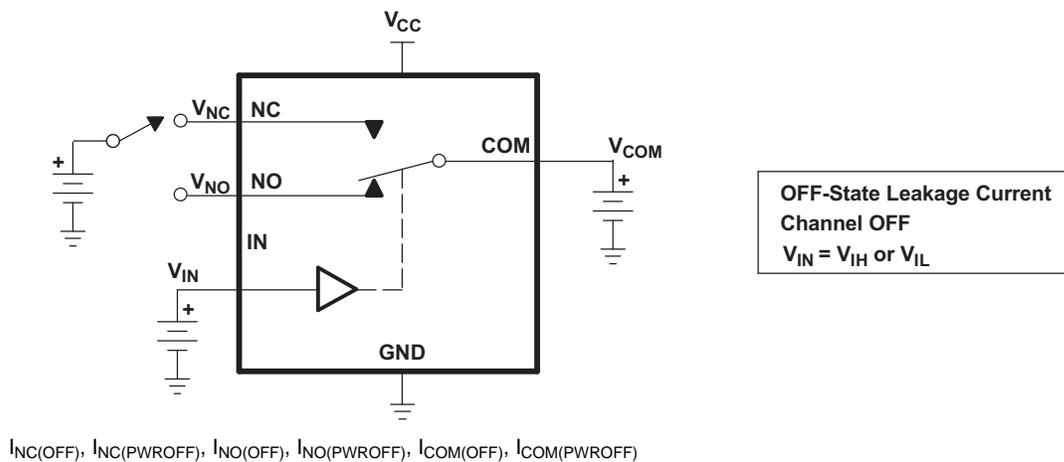
Figure 6. OFF-State Leakage Current

ON-State Leakage Current
Channel ON
$V_{IN} = V_{IH} \text{ or } V_{IL}$

$I_{COM(ON)}, I_{NC(ON)}, I_{NO(ON)}$
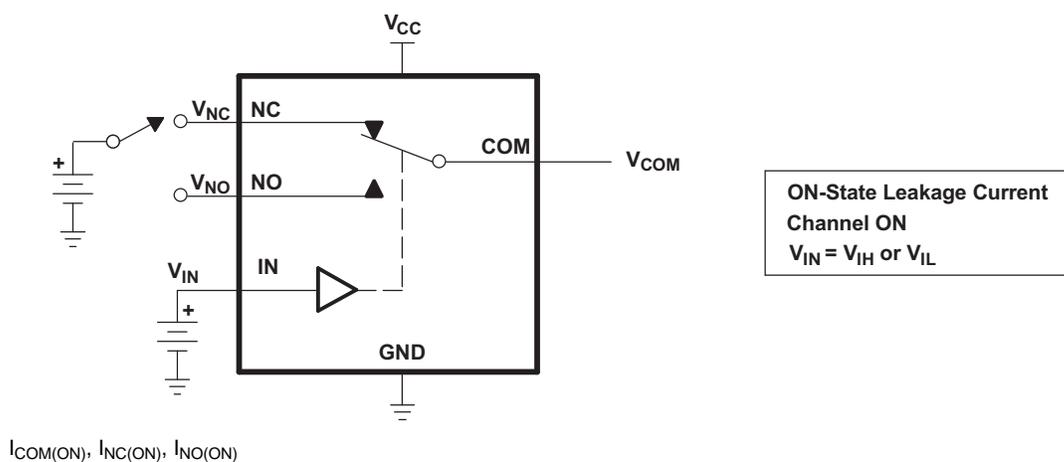
Figure 7. ON-State Leakage Current

Parameter Measurement Information (continued)
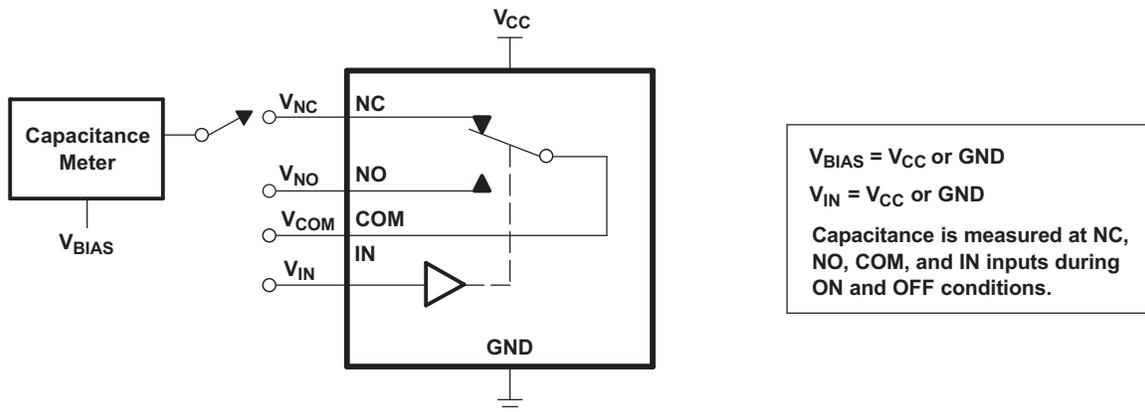
C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$

Figure 8. Capacitance
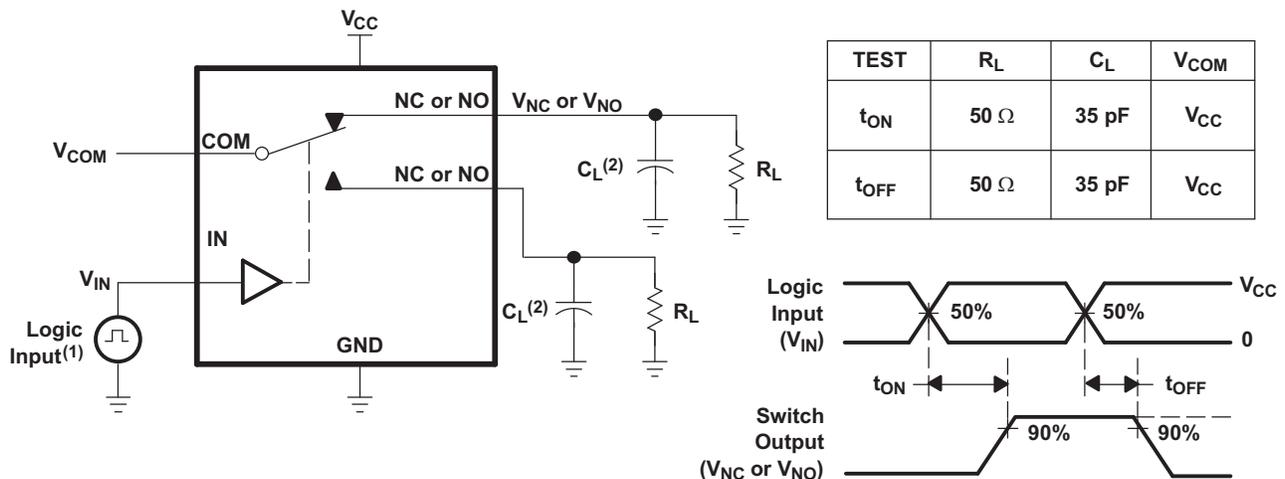
TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_{CC}
t_{OFF}	50 Ω	35 pF	V_{CC}

(1) All input pulses are supplied by generators having the following characteristics:
- PRR ≤ 10 MHz
- Z_O = 50 Ω
- t_r < 5 ns
- t_f < 5 ns

(2) C_L includes probe and jig capacitance.

Figure 9. Turnon and Turnoff Time

Product Folder Links: *TS5A9411*
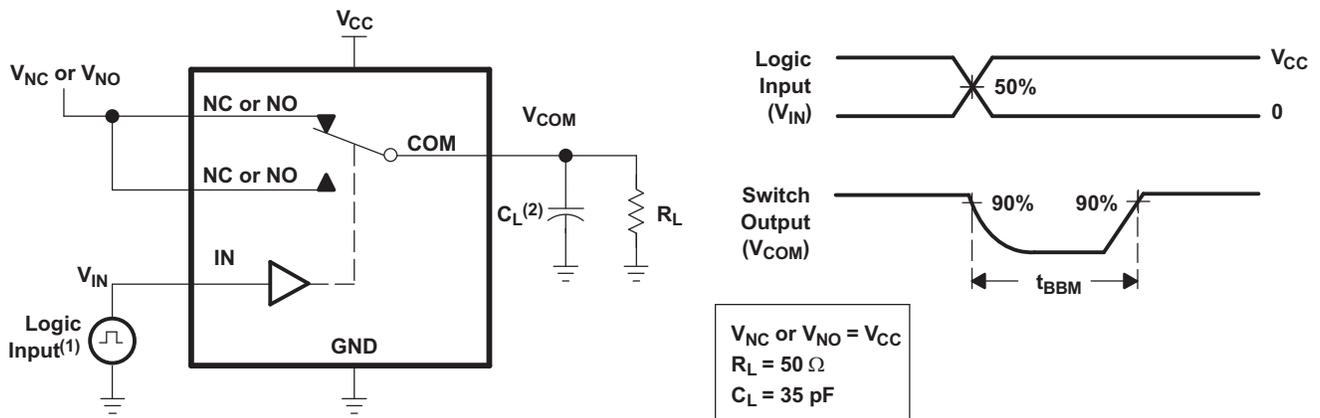
Parameter Measurement Information (continued)

(1) All input pulses are supplied by generators having the following characteristics:
- PRR ≤ 10 MHz
- Z_O = 50 Ω
- t_r < 5 ns
- t_f < 5 ns

(2) C_L includes probe and jig capacitance.

Figure 10. Break-Before-Make Time
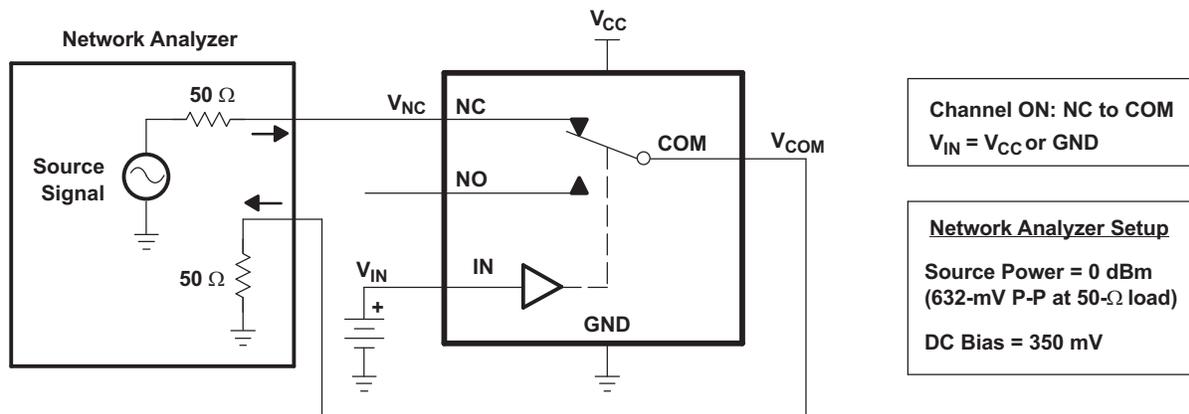
Figure 11. Bandwidth
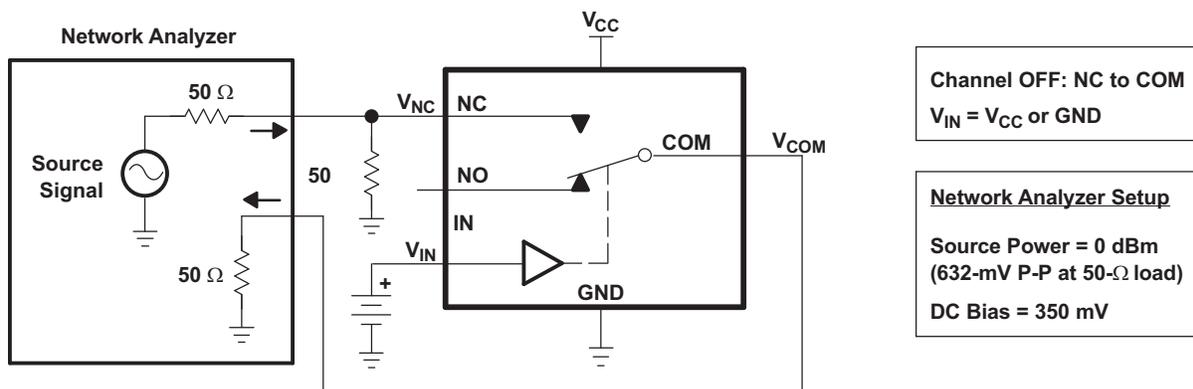
Figure 12. OFF Isolation

Parameter Measurement Information (continued)
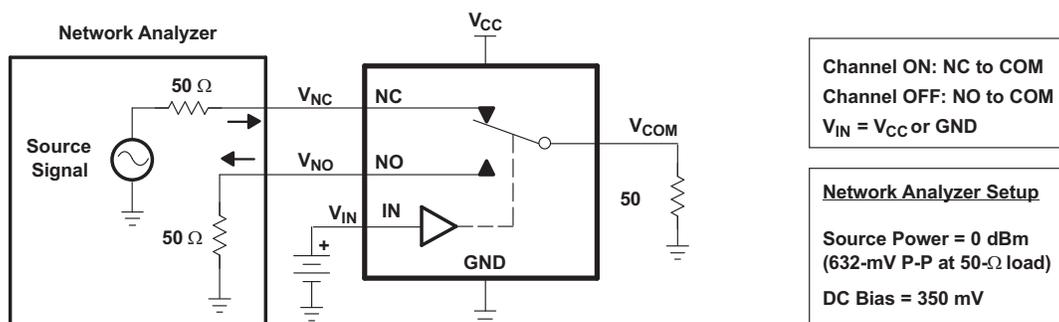
Figure 13. Crosstalk
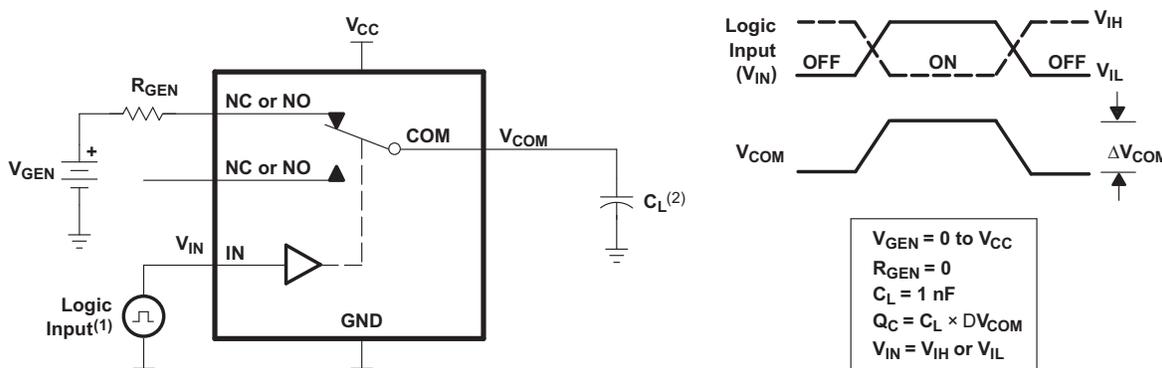
(1) All input pulses are supplied by generators having the following characteristics:
- PRR ≤ 10 MHz
- Z_O = 50 Ω
- t_r < 5 ns
- t_f < 5 ns

(2) C_L includes probe and jig capacitance.

Figure 14. Charge Injection
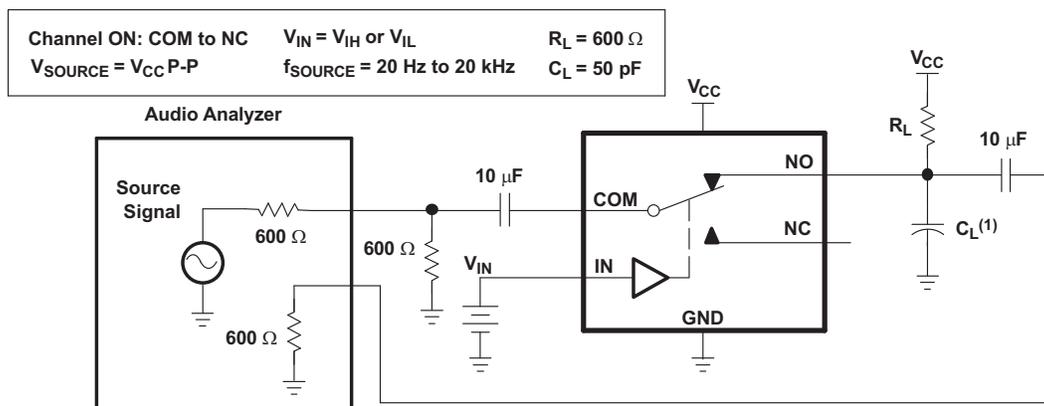
(1) C_L includes probe and jig capacitance.

Figure 15. Total Harmonic Distortion

Product Folder Links: *TS5A9411*

8 Detailed Description

8.1 Overview

The TS5A9411 device is a 1:2 or single-pole-double-throw (SPDT) solid-state analog switch. The TS5A9411, like all analog switches, is bidirectional. When powered on, each COM pin is connected to the NC pin or NO pin depending on the status of the IN pin. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO. The TS5A9411 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram
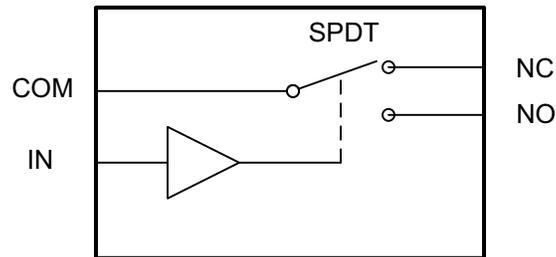
8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A9411 make this switch an excellent choice for analog signals that require minimal distortion. The 2.25-V to 5.5-V operation allows compatibility with more voltage nodes, and the bidirectional I/Os can pass analog signals from 0 V to V_{CC} with low distortion.

8.4 Device Functional Modes

Table 1 lists the functional modes of the TS5A9411. If IN pin is low, COM is connected to NC. If IN is high, COM is connected to NO.

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

Product Folder Links: *TS5A9411*

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs. The device is used in systems where multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application
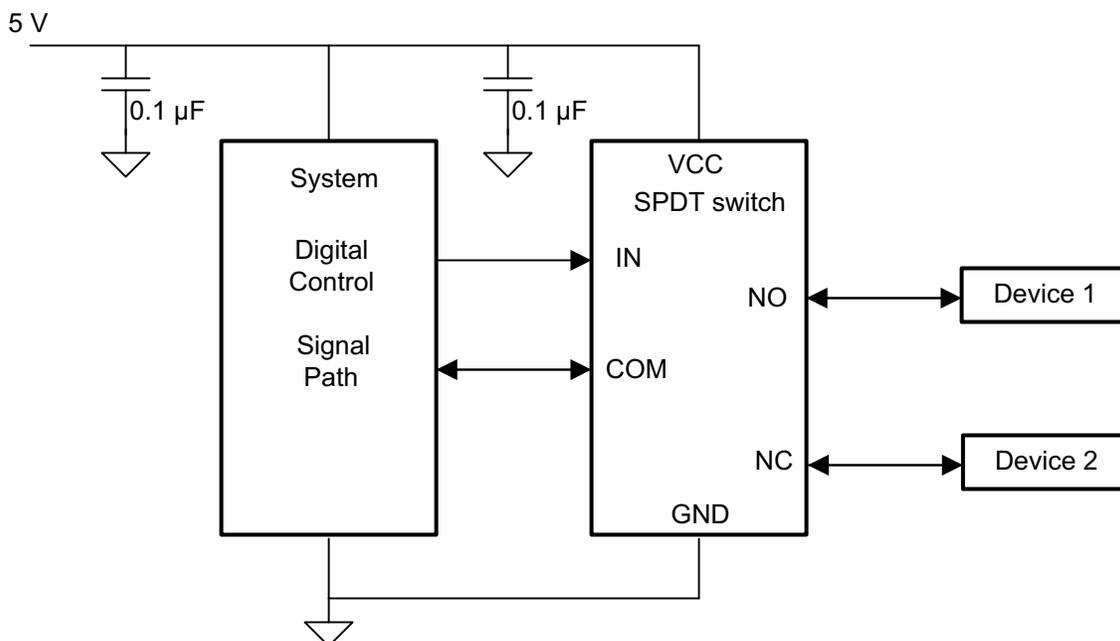
Figure 16. Typical Application Diagram

9.2.1 Design Requirements

Pull the digitally controlled input select pin (IN) to V_{CC} or GND to avoid unwanted switch states that could result if the logic control pin is left floating.

9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the input or output signal swing of the device is dependant of the supply voltage (V_{CC}).

Typical Application (continued)

9.2.3 Application Curve
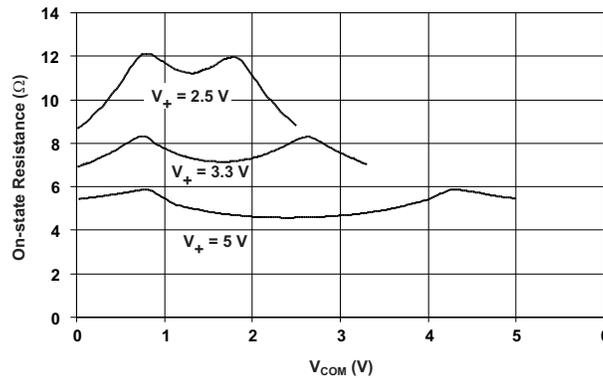
Figure 17. r_{ON} vs V_{COM}

10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC on first, followed by NO, NC, or COM pins.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components. A 0.1-µF capacitor, connected from VCC to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

TI recommends placing a bypass capacitor as close to the supply pins (VCC and –VCC) as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum. Minimize trace lengths and vias on the signal paths to preserve signal integrity.

11.2 Layout Example
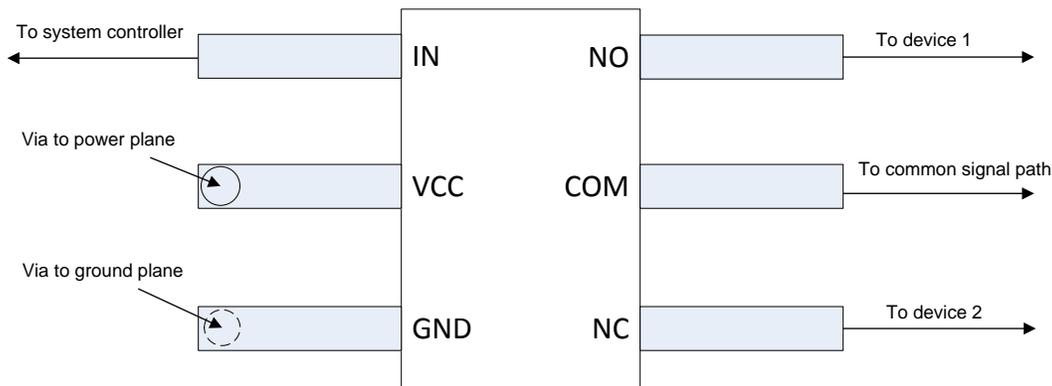
Figure 18. Layout Recommendation

Product Folder Links: *TS5A9411*

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is −3 dB below the DC gain.
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF.
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF.
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON.
C_I	Capacitance of control input (IN).
I_{CC}	Static power-supply current with the control (IN) pin at V_{CC} or GND.
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open.
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition ($V_{CC} = 0$).
I_{IH}, I_{IL}	Leakage current measured at the control input (IN).
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions.
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open.
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions.
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open.
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
Δr_{ON}	Difference of r_{ON} between channels in a specific device.
r_{ON}	Resistance between COM and NC or COM and NO ports when the channel is ON.
$r_{ON(FLAT)}$	Difference of r_{ON} in a channel over the specified range of conditions.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
t_{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
t_{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is

Device Support (continued)

defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.

V_{COM} Voltage at COM.

V_I Voltage at the control input (IN).

V_{IH} Minimum input voltage for logic high for the control input (IN).

V_{IL} Maximum input voltage for logic low for the control input (IN).

V_{NC} Voltage at NC.

V_{NO} Voltage at NO.

X_{TALK} Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *TS5A9411*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A9411DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F ~ 32R) (32H ~ 32P)	Samples
TS5A9411DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F ~ 32R) (32H ~ 32P)	Samples
TS5A9411DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F ~ 32R) 32H	Samples
TS5A9411DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F ~ 32R) 32H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
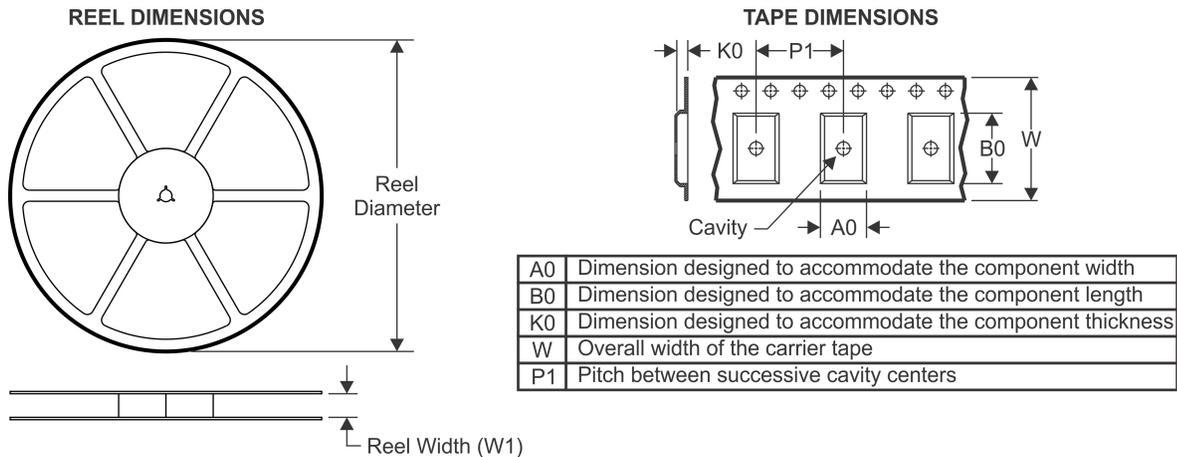
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
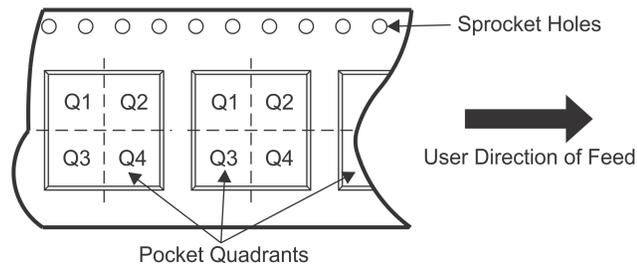
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A9411DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TS5A9411DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS
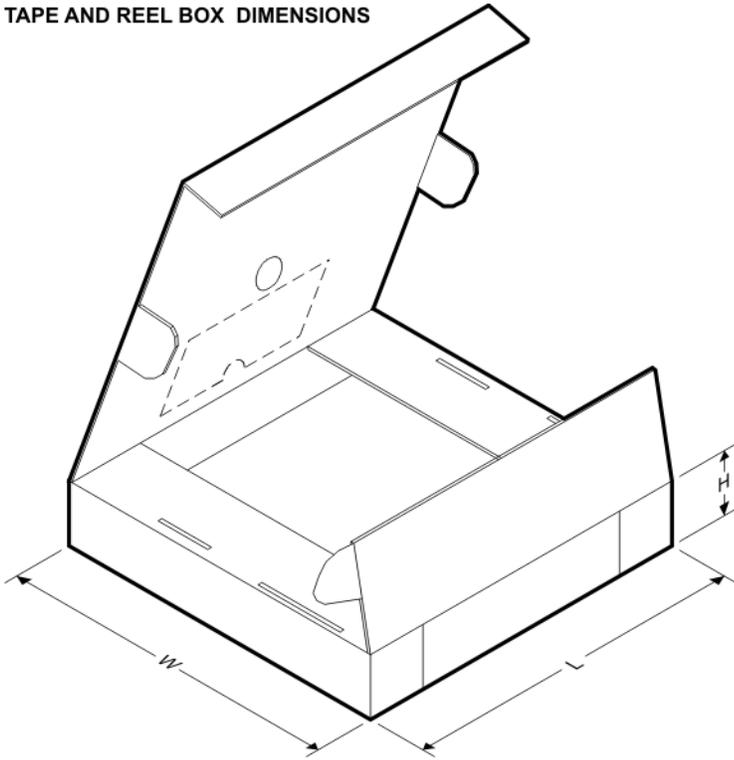
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A9411DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
TS5A9411DCKT	SC70	DCK	6	250	202.0	201.0	28.0

DCK (R−PDSO−G6)   PLASTIC SMALL−OUTLINE PACKAGE
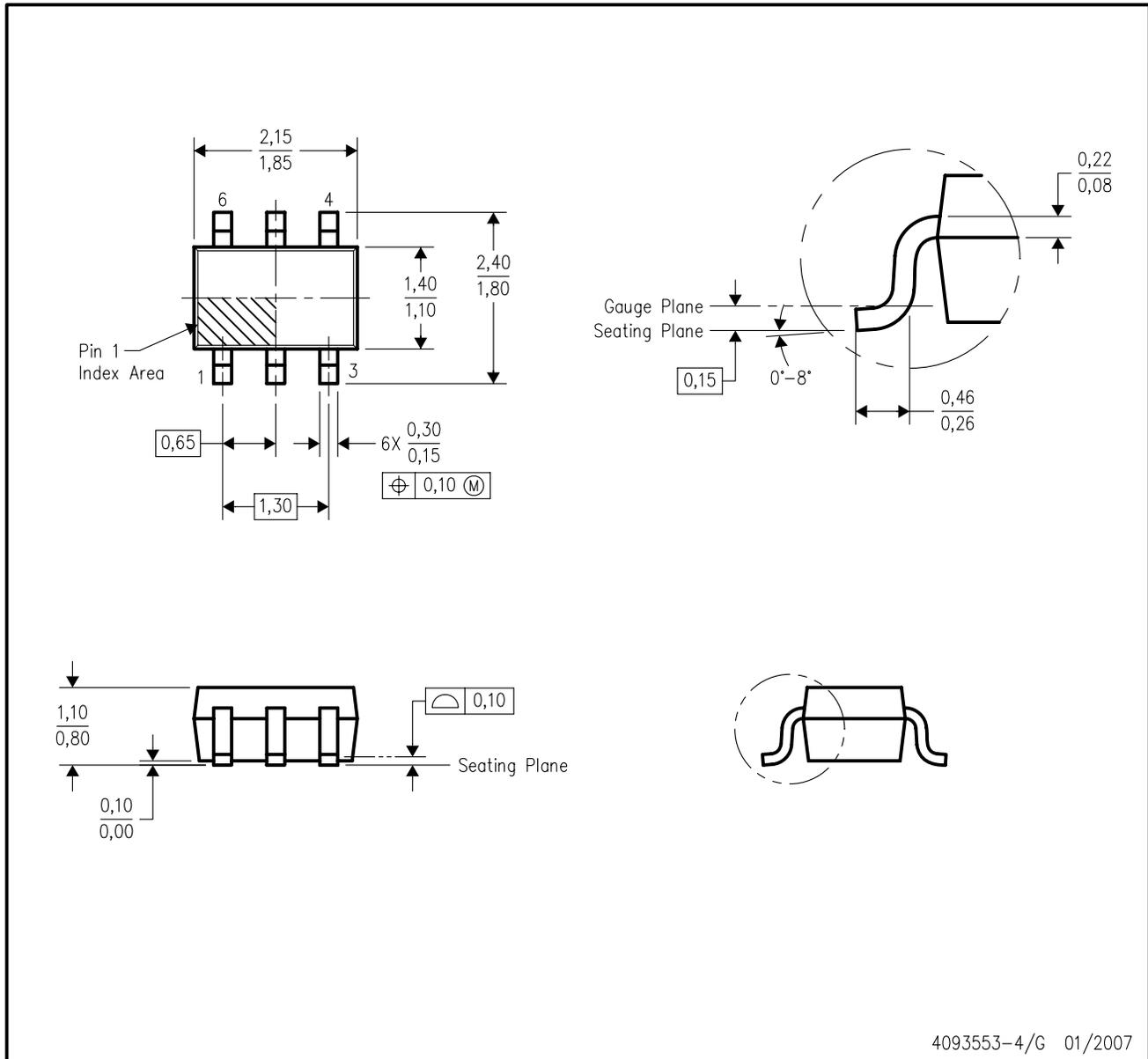
$\frac{2,15}{1,85}$

6   4

$\frac{1,40}{1,10}$

$\frac{2,40}{1,80}$

Pin 1
Index Area

1   3

0,65

6X $\frac{0,30}{0,15}$

1,30

⊕ | 0,10 Ⓜ

$\frac{0,22}{0,08}$

Gauge Plane
Seating Plane

0,15   0°−8°

$\frac{0,46}{0,26}$

$\frac{1,10}{0,80}$

⌒ | 0,10

Seating Plane

$\frac{0,10}{0,00}$

4093553−4/G   01/2007

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO−203 variation AB.
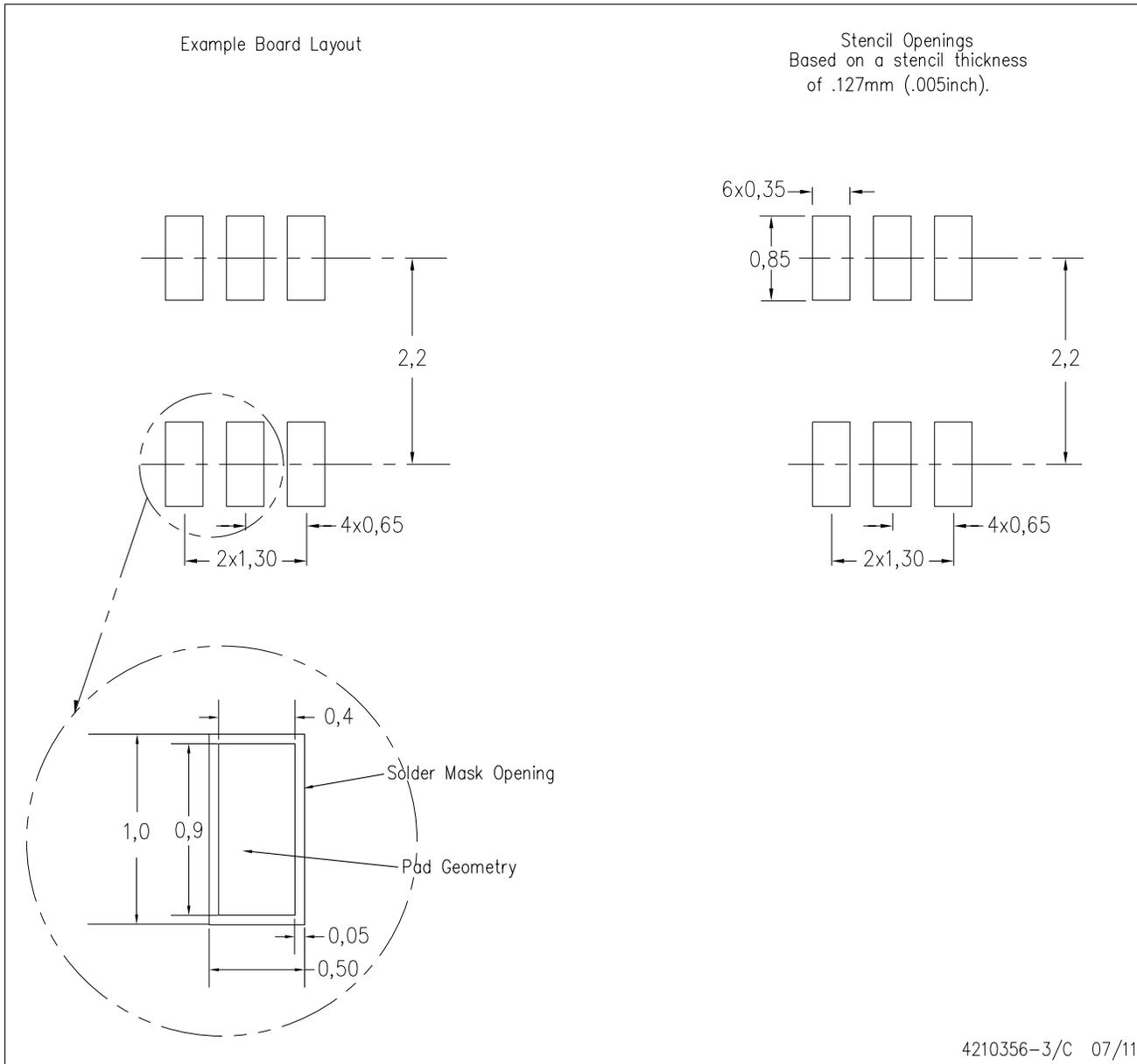
TEXAS
INSTRUMENTS
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DCK (R−PDSO−G6)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

4x0,65

2x1,30

4x0,65

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−3/C 07/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D. Publication IPC−7351 is recommended for alternate designs.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
             metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

IMPORTANT NOTICE