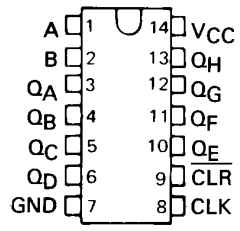
# SN54164, SN54LS164, SN74164, SN74LS164
# 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

MARCH 1974 – REVISED MARCH 1988

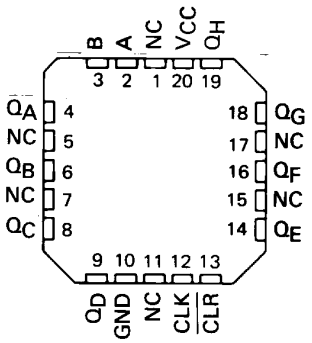
- **Gated Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Asynchronous Clear**

| TYPE | TYPICAL MAXIMUM CLOCK FREQUENCY | TYPICAL POWER DISSIPATION |
|---|---|---|
| '164 | 36 MHz | 21 mW per bit |
| 'LS164 | 36 MHz | 10 mW per bit |

SN54164, SN54LS164 . . . J OR W PACKAGE
SN74164 . . . N PACKAGE
SN74LS164 . . . D OR N PACKAGE
(TOP VIEW)




SN54LS164 . . . FK PACKAGE
(TOP VIEW)




NC – No internal connection

## description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup-time requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

The SN54164 and SN54LS164 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74164 and SN74LS164 are characterized for operation from 0°C to 70°C.

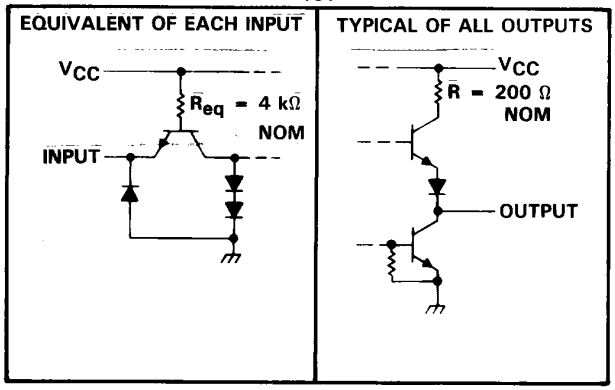
FUNCTION TABLE

| INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| CLEAR | CLOCK | A | B | $Q_A$ | $Q_B$ | ... | $Q_H$ |
| L | X | X | X | L | L | | L |
| H | L | X | X | $Q_{A0}$ | $Q_{B0}$ | | $Q_{H0}$ |
| H | ↑ | H | H | H | $Q_{An}$ | | $Q_{Gn}$ |
| H | ↑ | L | X | L | $Q_{An}$ | | $Q_{Gn}$ |
| H | ↑ | X | L | L | $Q_{An}$ | | $Q_{Gn}$ |

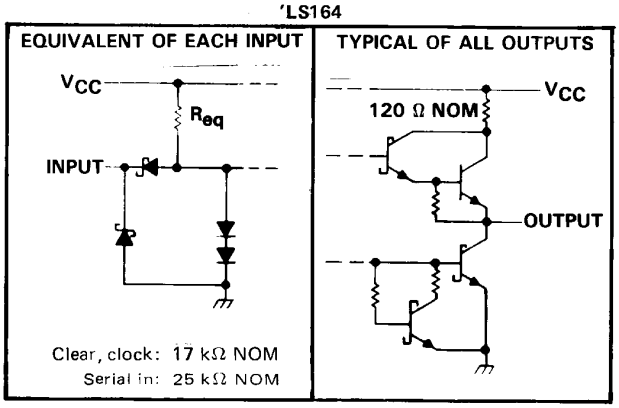
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
$Q_{A0}$, $Q_{B0}$, $Q_{H0}$ = the level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady-state input conditions were established.
$Q_{An}$, $Q_{Gn}$ = the level of $Q_A$ or $Q_G$ before the most-recent ↑ transition of the clock; indicates a one-bit shift.

## schematics of inputs and outputs

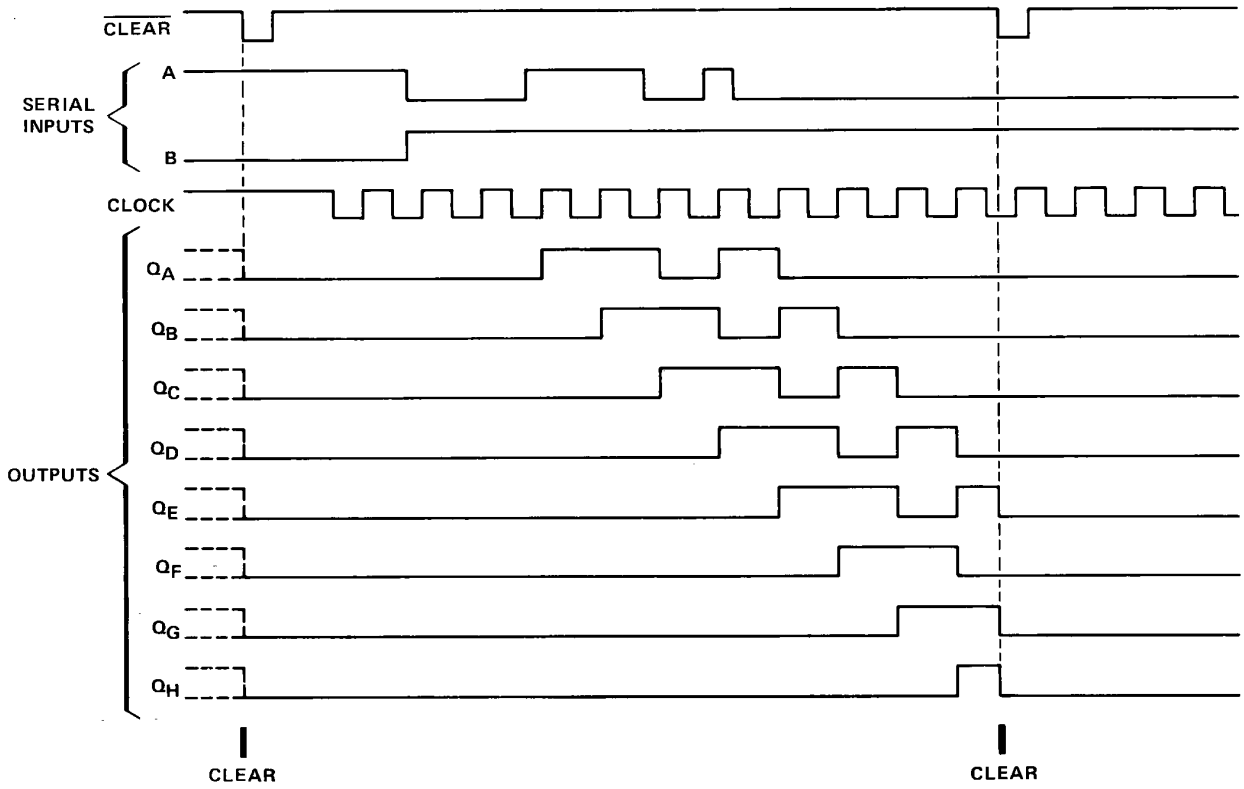
'164



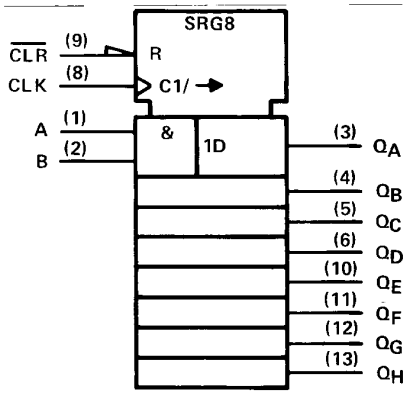

'LS164



typical clear, shift, and clear sequences

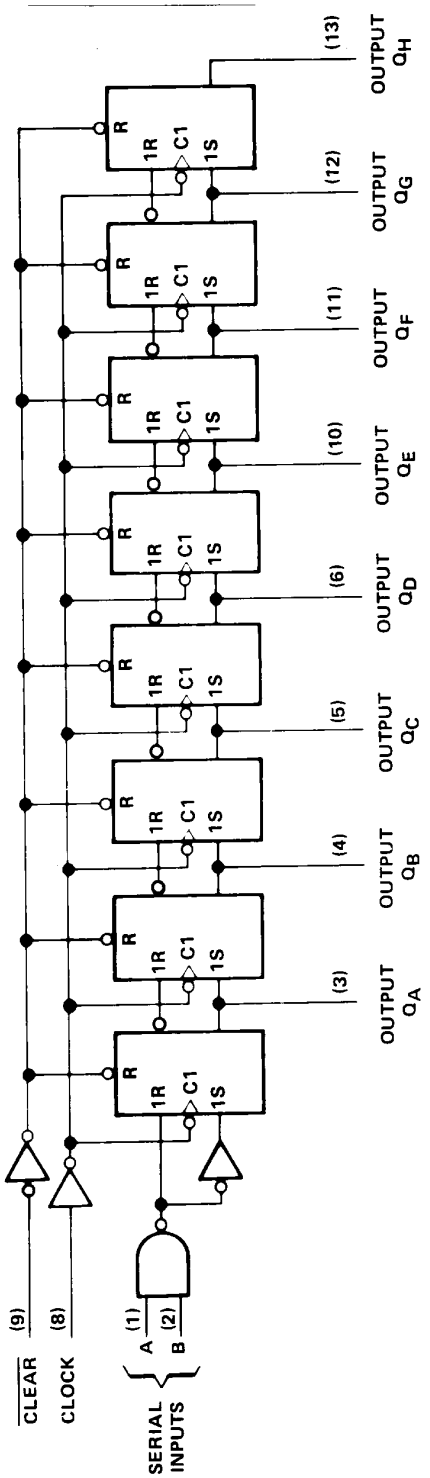



logic symbol†




†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

**logic diagram (positive logic)**




Pin numbers shown are for D, J, N, and W packages.

## absolute maximum ratings over oprating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54164 . . . . . −55°C to 125°C
SN74164 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | SN54164 | | | SN74164 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | −400 | | | −400 | μA |
| Low-level output current, $I_{OL}$ | | | 8 | | | 8 | mA |
| Clock frequency, $f_{clock}$ | 0 | | 25 | 0 | | 25 | MHz |
| Width of clock or clear input pulse, $t_w$ | 20 | | | 20 | | | ns |
| Data setup time, $t_{su}$ (see Figure 1) | 15 | | | 15 | | | ns |
| Data setup time, $t_{su}$ (Clear Inactive) (see Figure 1) | 20 | | | 20 | | | ns |
| Data hold time, $t_h$ (see Figure 1) | 5 | | | 5 | | | ns |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54164 | | | SN74164 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −400 μA | | 2.4 | 3.2 | | 2.4 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 8 mA | | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V, | | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | mA |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | | −10 | | −27.5 | −9 | | −27.5 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | $V_{I(clock)}$ = 0.4 V | | 30 | | | 30 | | mA |
| | | | $V_{I(clock)}$ = 2.4 V | | 37 | 54 | | 37 | 54 | |

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than two outputs should be shorted at a time.
NOTE 2: $I_{CC}$ is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | $R_L$ = 800 Ω, See Figure 1 | $C_L$ = 15 pF | 25 | 36 | | MHz |
| $t_{PHL}$ | Propagation delay time, high-to-low-level Q outputs from clear input | | $C_L$ = 15 pF | | 24 | 36 | ns |
| | | | $C_L$ = 50 pF | | 28 | 42 | |
| $t_{PLH}$ | Propagation delay time, low-to-high-level Q outputs from clock input | | $C_L$ = 15 pF | 8 | 17 | 27 | ns |
| | | | $C_L$ = 50 pF | 10 | 20 | 30 | |
| $t_{PHL}$ | Propagation delay time, high-to-low-level Q outputs from the clock input | | $C_L$ = 15 pF | 10 | 21 | 32 | ns |
| | | | $C_L$ = 50 pF | 10 | 25 | 37 | |





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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS164 . . . . . −55°C to 125°C
SN74LS164 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

| | | SN54LS164 | | | SN74LS164 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | 4 | | | 8 | mA |
| $f_{clock}$ | Clock frequency | 0 | | 25 | 0 | | 25 | MHz |
| $t_w$ | Width of clock or clear input pulse | 20 | | | 20 | | | ns |
| $t_{su}$ | Data setup time (See Figure 1) | 15 | | | 15 | | | ns |
| $t_{su}$ | Clear inactive setup time (See Figure 1) | 20 | | | 20 | | | ns |
| $t_h$ | Data hold time (See Figure 1) | 5 | | | 5 | | | ns |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

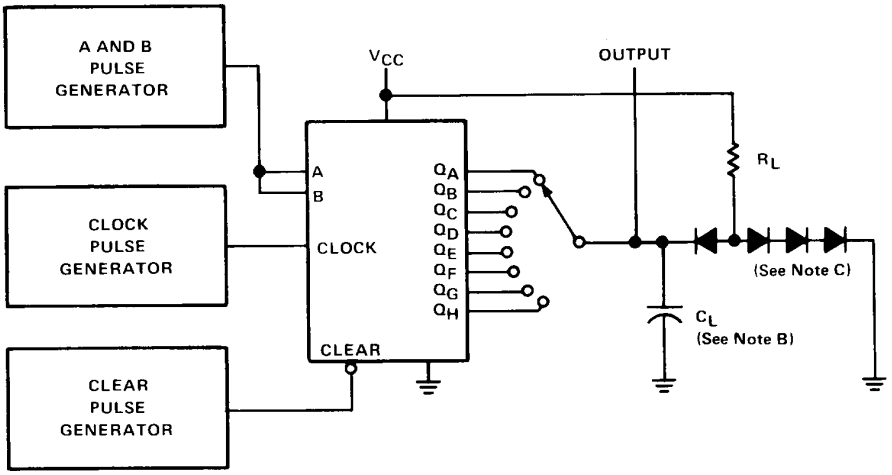
| PARAMETER | TEST CONDITIONS† | | SN54LS164 | | | SN74LS164 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX, $I_{OH}$ = −0.4 mA | | 2.5 | 3.5 | | 2.7 | 3.5 | | V |
| $V_{OL}$ | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | $V_{CC}$ = MAX, $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | 20 | | | 20 | | μA |
| $I_{IL}$ | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| $I_{OS}$ | $V_{CC}$ = MAX | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | $V_{CC}$ = MAX, See Note 3 | | | 16 | 27 | | 16 | 27 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 3: $I_{CC}$ is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied to clear.

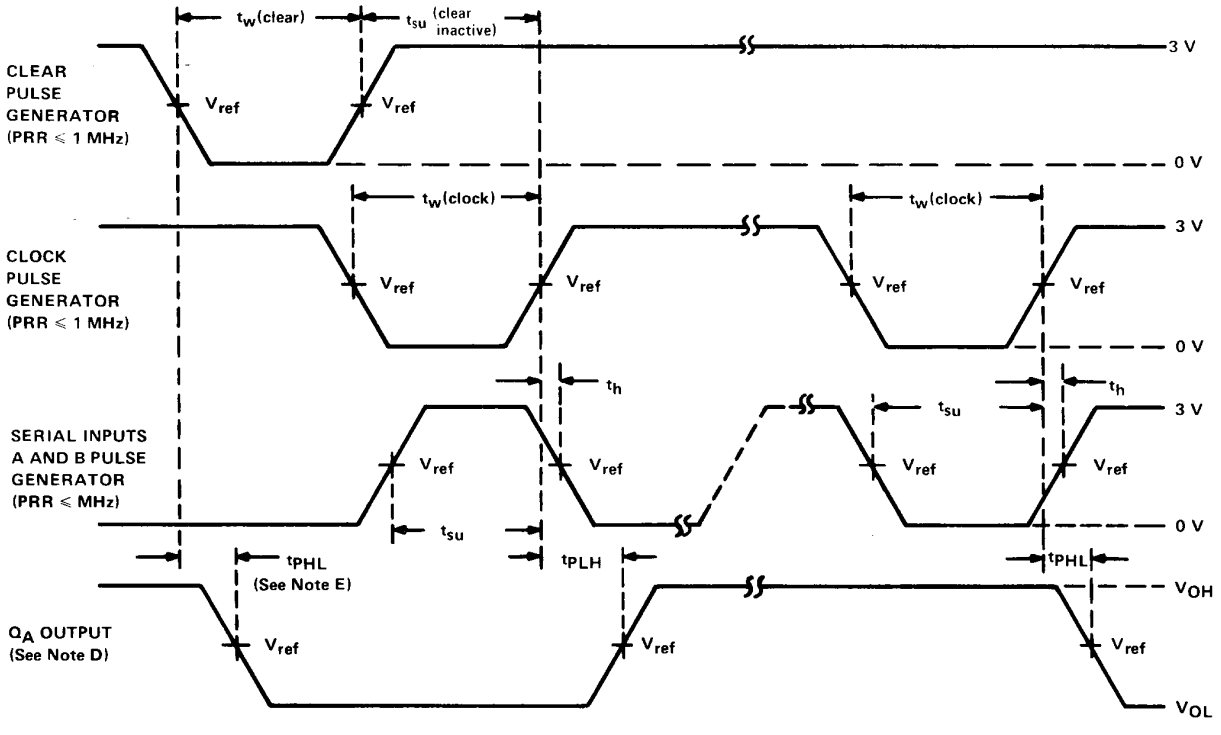
### switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | $R_L$ = 2 kΩ, $C_L$ = 15 pF, See Figure 1 | 25 | 36 | | MHz |
| $t_{PHL}$ | Propagation delay time, high-to-low-level Q outputs from clear input | | | 24 | 36 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level Q outputs from clock input | | | 17 | 27 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level Q outputs from clock input | | | 21 | 32 | ns |

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for '164, $t_r \leq 10$ ns, $t_f \leq 10$ ns; and for 'LS164, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
B. $C_L$ includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. $Q_A$ output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measurement of $t_{PHL}$ from the clear input.
F. For '164, $V_{ref}$ = 1.5 V; for 'LS164, $V_{ref}$ = 1.3 V.

FIGURE 1–SWITCHING TIMES



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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| JM38510/30605B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 30605B2A | Samples |
| JM38510/30605BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605BCA | Samples |
| JM38510/30605BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605BCA | Samples |
| JM38510/30605BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605BDA | Samples |
| JM38510/30605BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605BDA | Samples |
| JM38510/30605SCA | ACTIVE | CDIP | J | 14 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605SCA | Samples |
| JM38510/30605SCA | ACTIVE | CDIP | J | 14 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605SCA | Samples |
| JM38510/30605SDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605SDA | Samples |
| JM38510/30605SDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605SDA | Samples |
| M38510/30605B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 30605B2A | Samples |
| M38510/30605B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 30605B2A | Samples |
| M38510/30605BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605BCA | Samples |
| M38510/30605BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605BCA | Samples |
| M38510/30605BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605BDA | Samples |
| M38510/30605BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605BDA | Samples |
| M38510/30605SCA | ACTIVE | CDIP | J | 14 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605SCA | Samples |
| M38510/30605SCA | ACTIVE | CDIP | J | 14 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605SCA | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M38510/30605SDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605SDA | Samples |
| M38510/30605SDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30605SDA | Samples |
| SN54LS164J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS164J | Samples |
| SN54LS164J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS164J | Samples |
| SN74LS164D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS164 | Samples |
| SN74LS164D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS164 | Samples |
| SN74LS164DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS164 | Samples |
| SN74LS164DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS164 | Samples |
| SN74LS164DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS164 | Samples |
| SN74LS164DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS164 | Samples |
| SN74LS164DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS164 | Samples |
| SN74LS164DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS164 | Samples |
| SN74LS164N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS164N | Samples |
| SN74LS164N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS164N | Samples |
| SN74LS164NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS164N | Samples |
| SN74LS164NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS164N | Samples |
| SN74LS164NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS164 | Samples |
| SN74LS164NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS164 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS164NSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS164 | Samples |
| SN74LS164NSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS164 | Samples |
| SNJ54LS164FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54LS 164FK | Samples |
| SNJ54LS164FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54LS 164FK | Samples |
| SNJ54LS164J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS164J | Samples |
| SNJ54LS164J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS164J | Samples |
| SNJ54LS164W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS164W | Samples |
| SNJ54LS164W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS164W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN54LS164, SN54LS164-SP, SN74LS164 :**

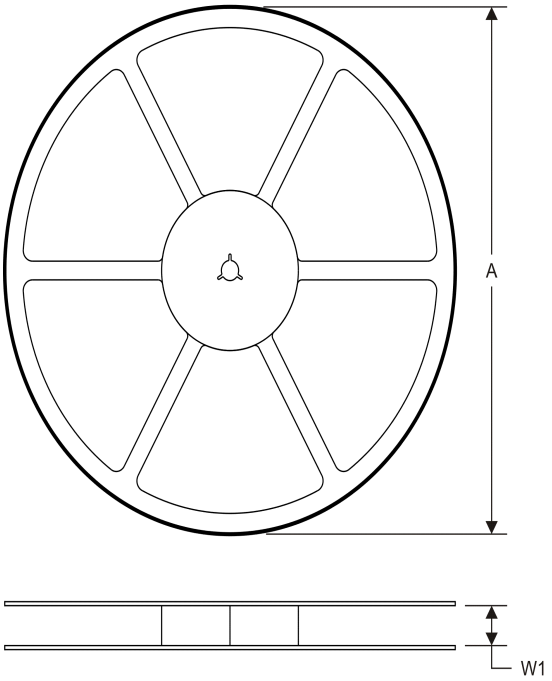
- Catalog: SN74LS164, SN54LS164
- Military: SN54LS164
- Space: SN54LS164-SP

NOTE: Qualified Version Definitions:

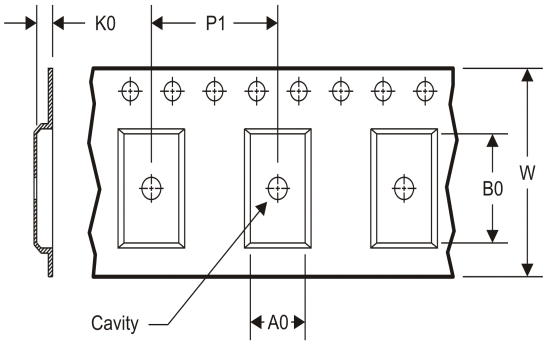
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



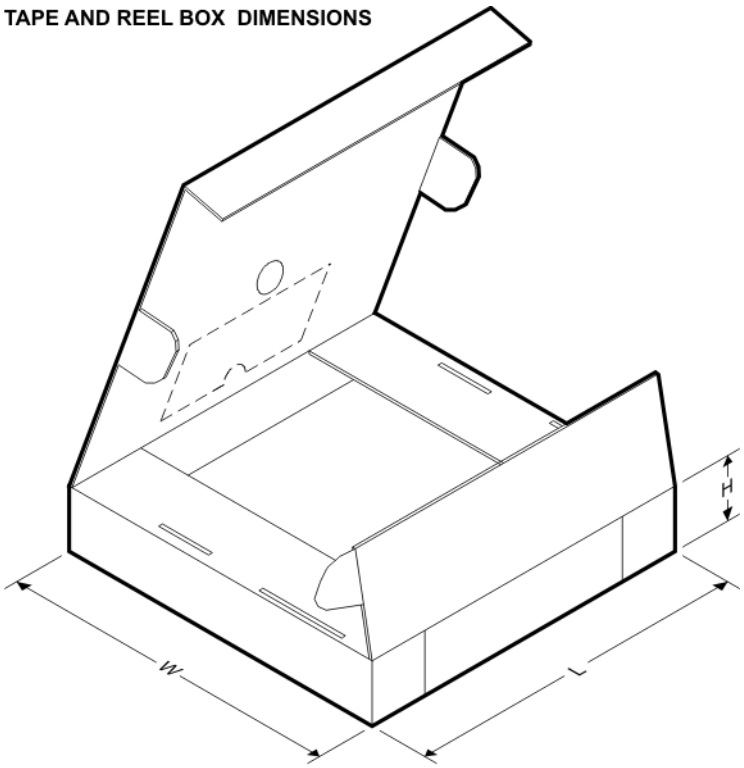

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS164DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS164NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

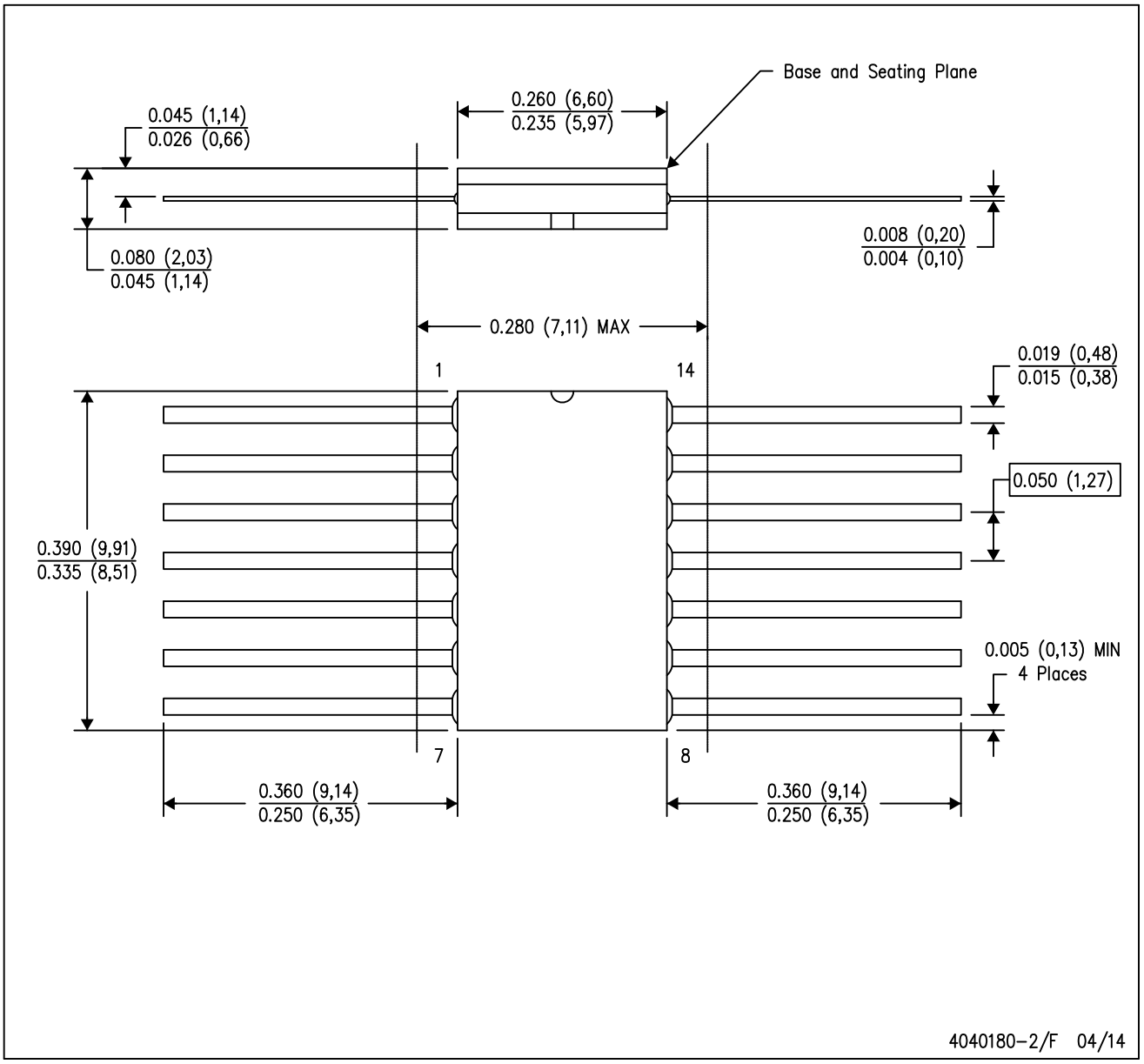
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LS164DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74LS164NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

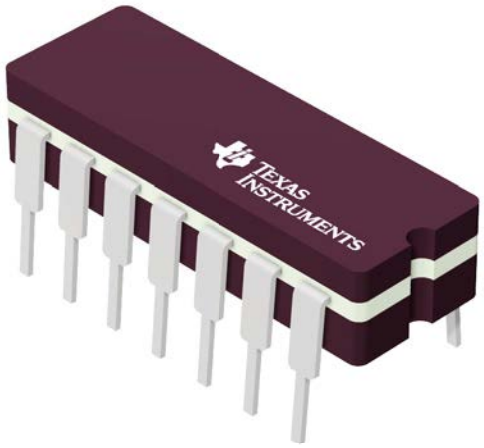



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

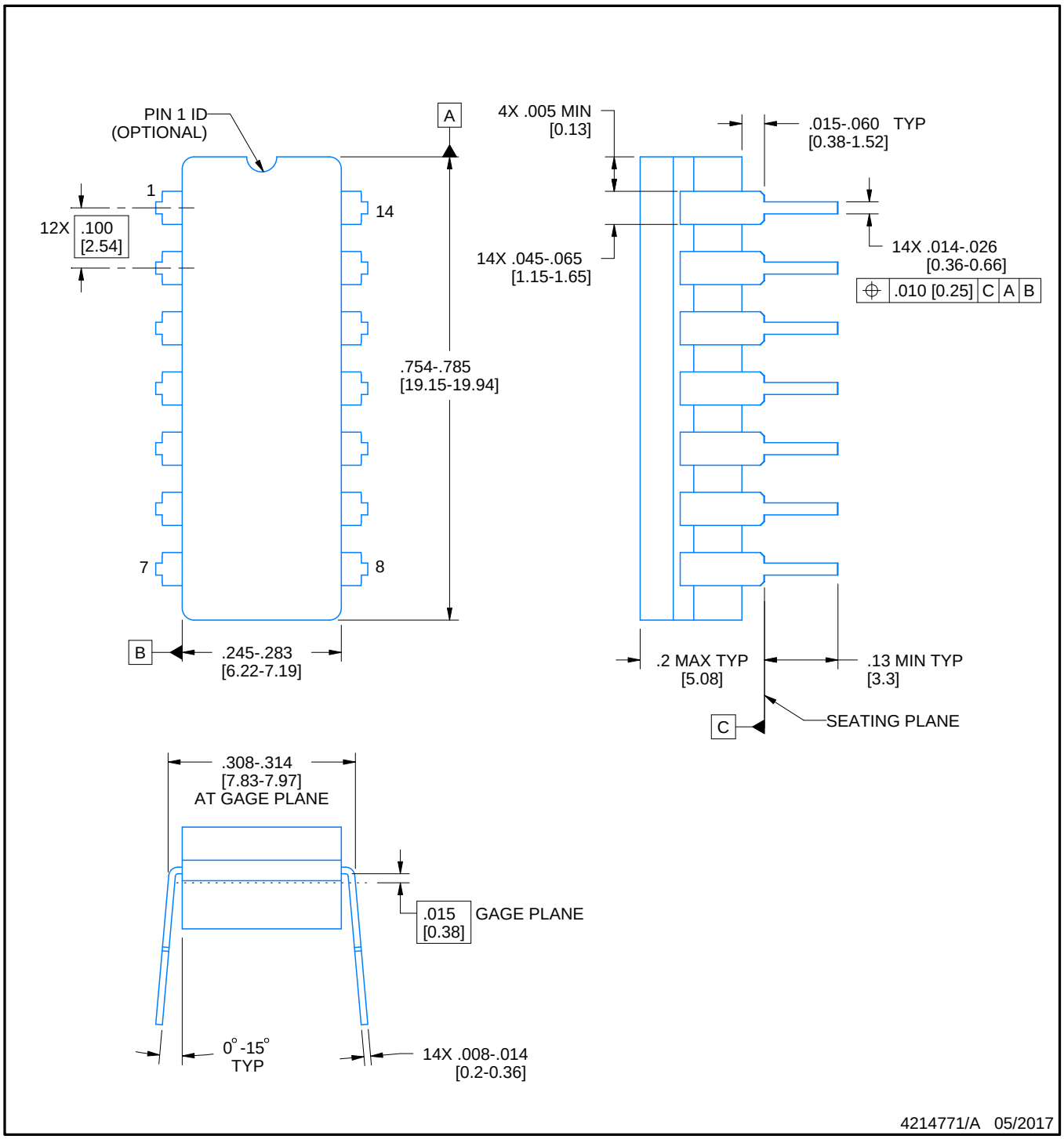
4040083-5/G

# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

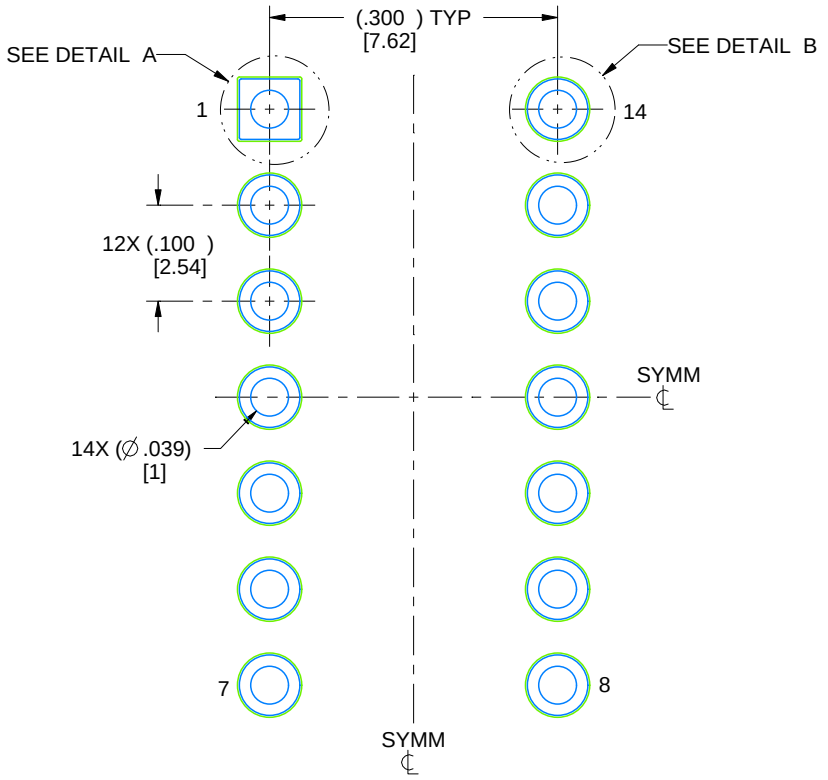
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

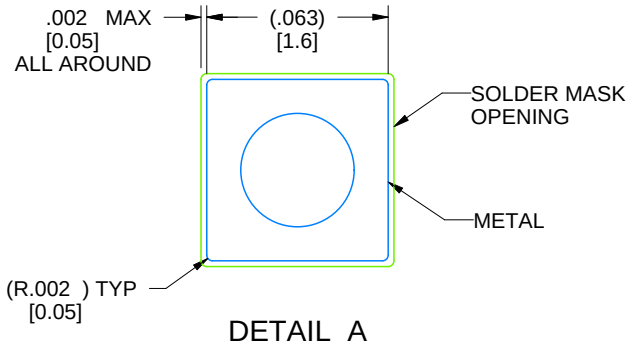
## J0014A

## CDIP - 5.08 mm max height

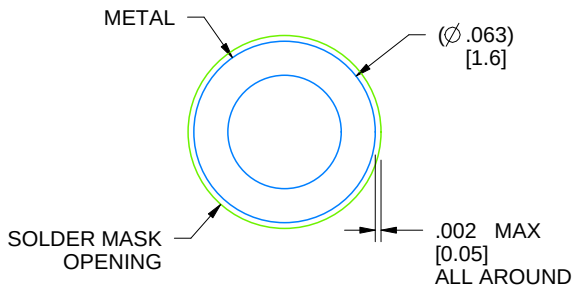
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



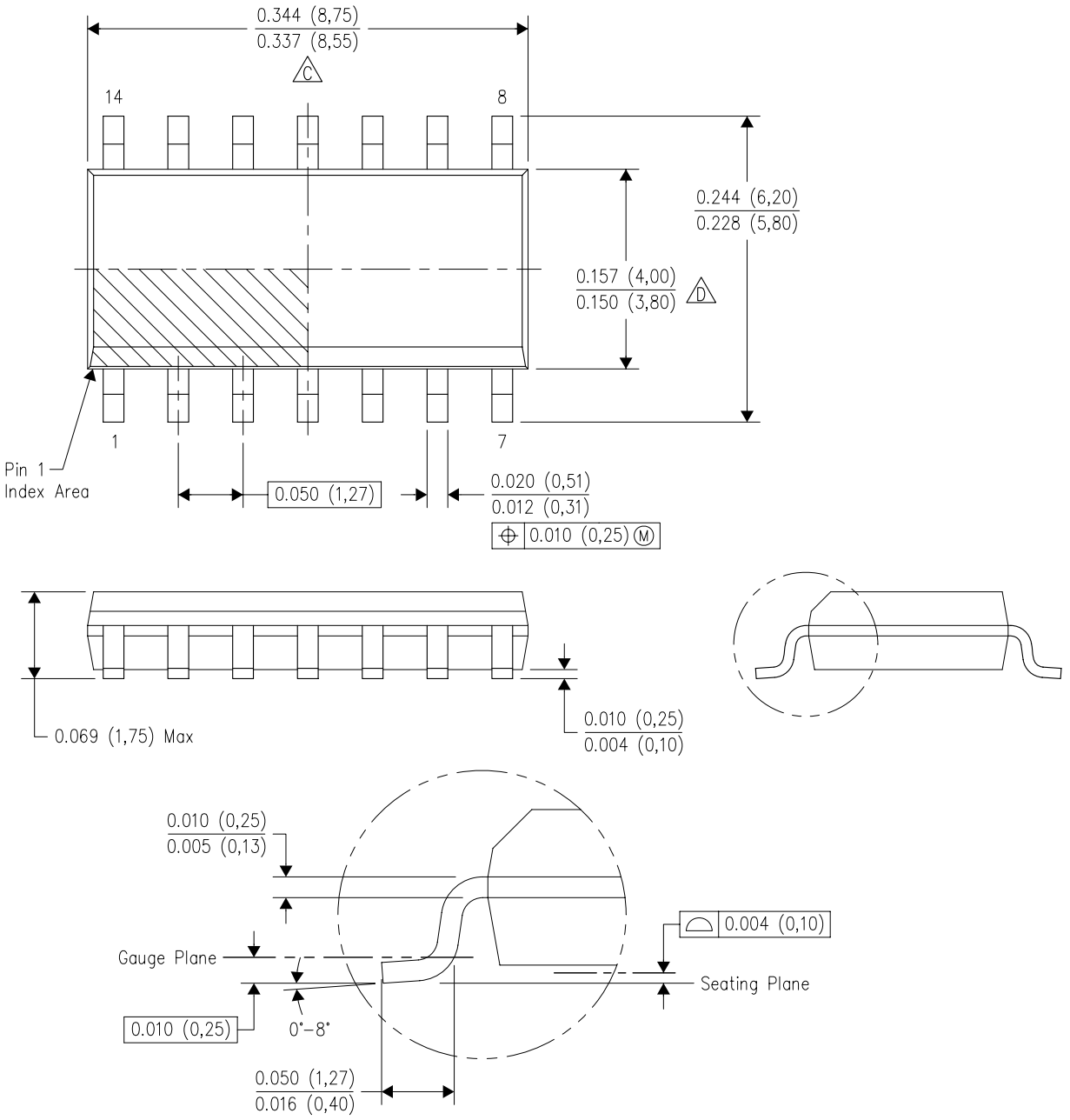

DETAIL A
SCALE: 15X




DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

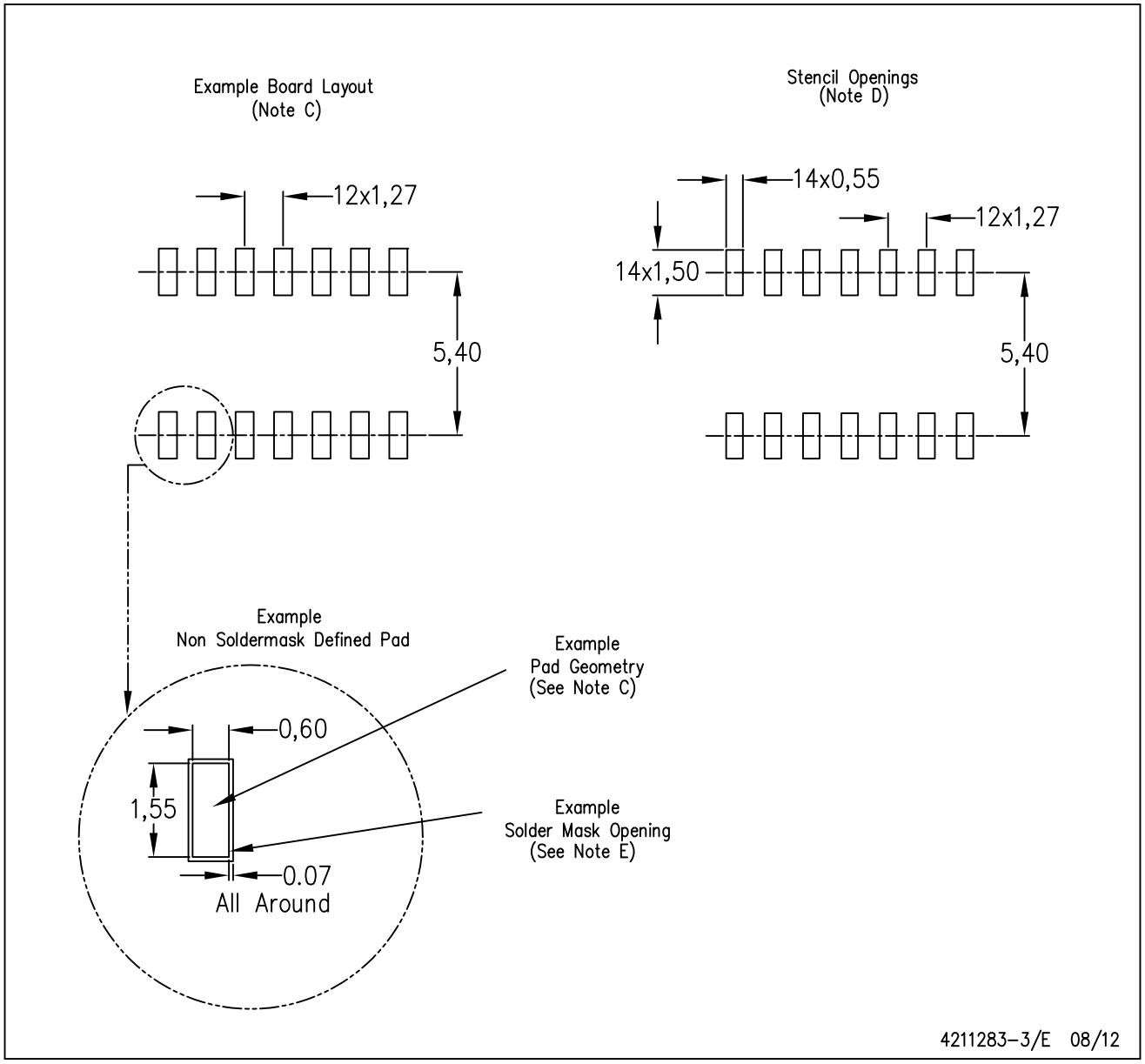
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

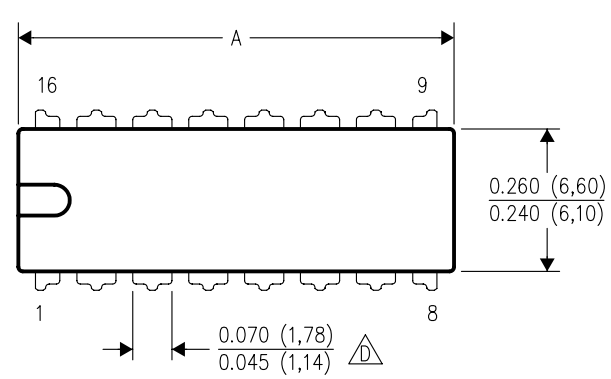



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

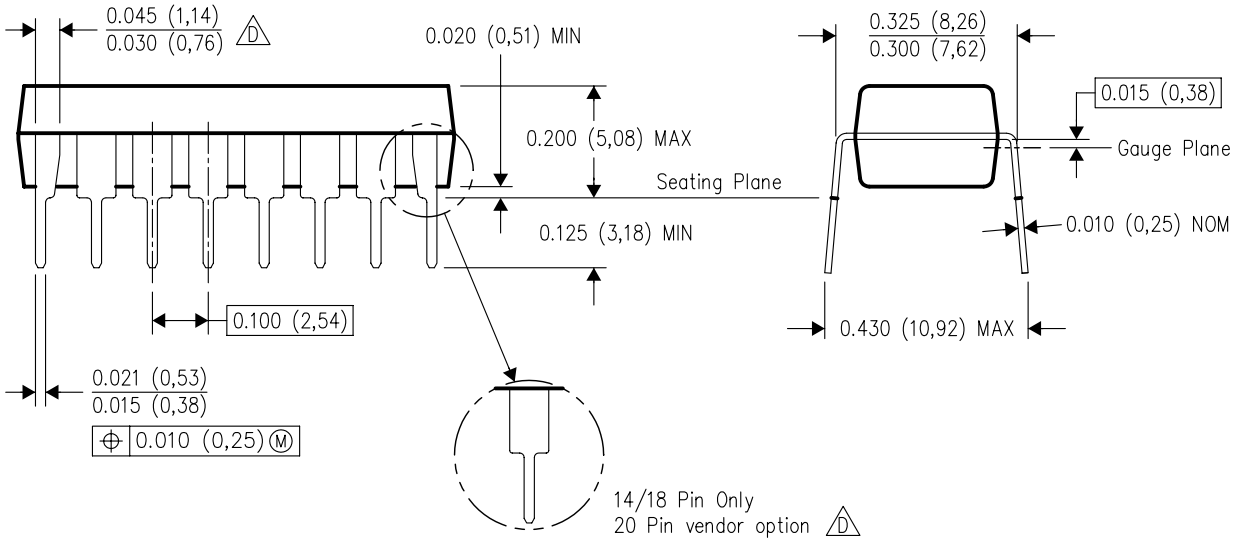
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

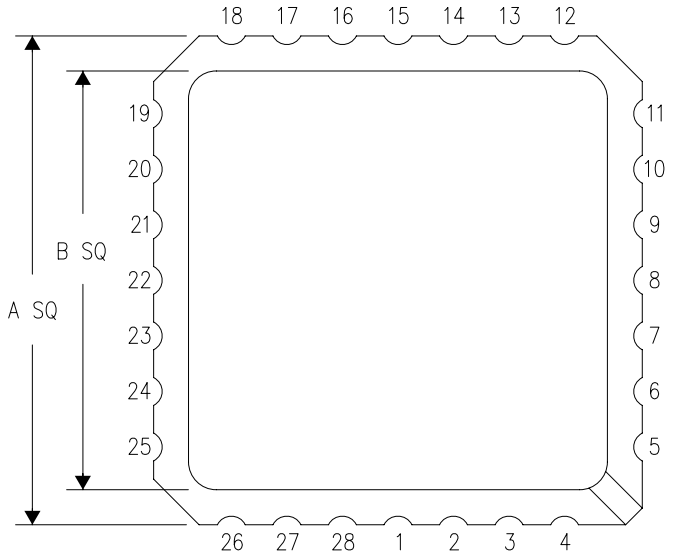



4040049/E 12/2002

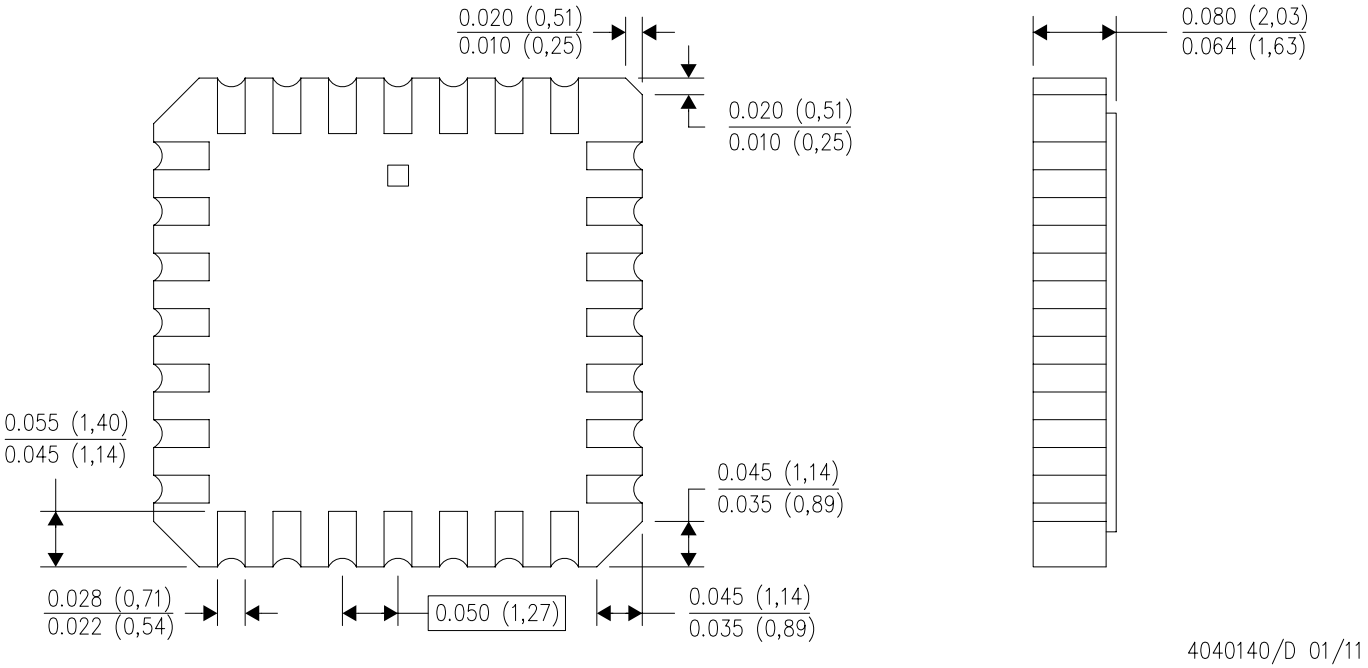
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



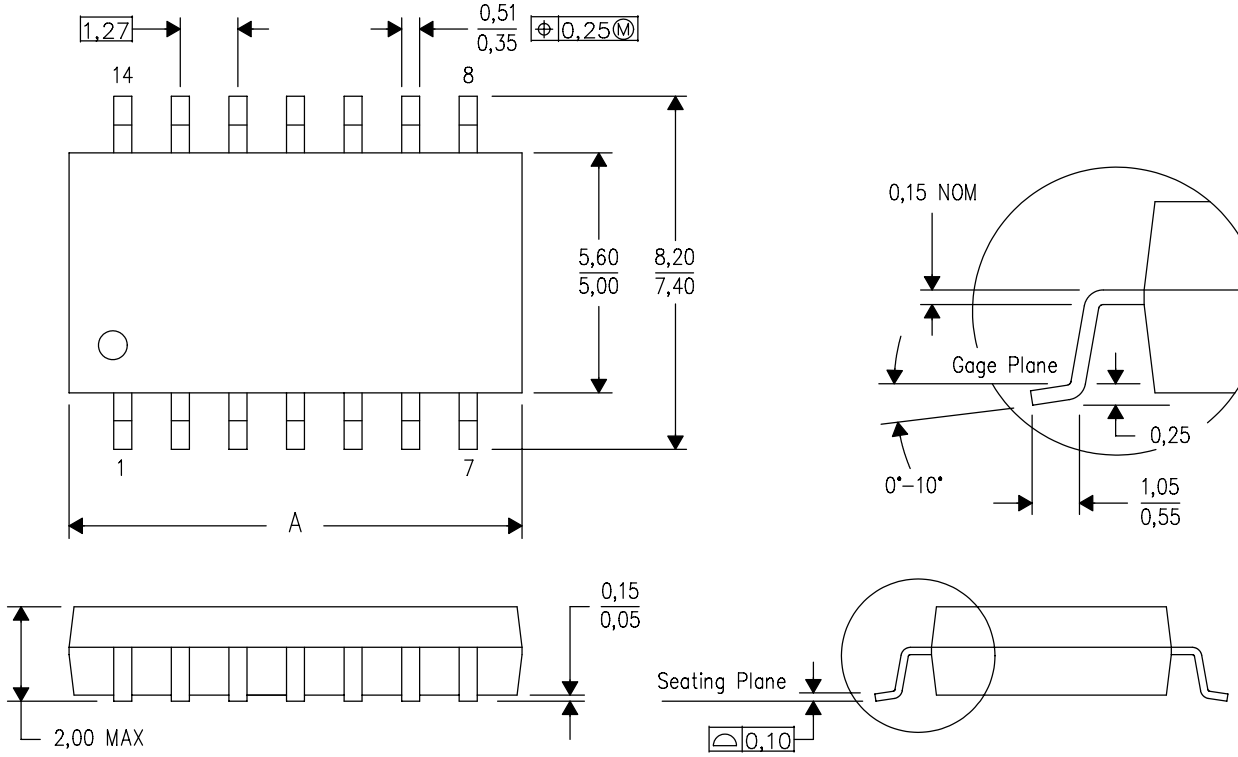

4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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