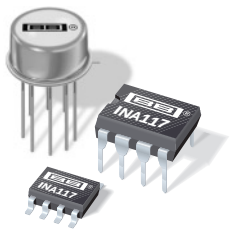
Burr-Brown Products
from Texas Instruments

INA117



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High Common-Mode Voltage DIFFERENCE AMPLIFIER

FEATURES

- **COMMON-MODE INPUT RANGE: ±200V (V_S = ±15V)**
- **PROTECTED INPUTS: ±500V Common-Mode ±500V Differential**
- **UNITY GAIN: 0.02% Gain Error max**
- **NONLINEARITY: 0.001% max**
- **CMRR: 86dB min**

APPLICATIONS

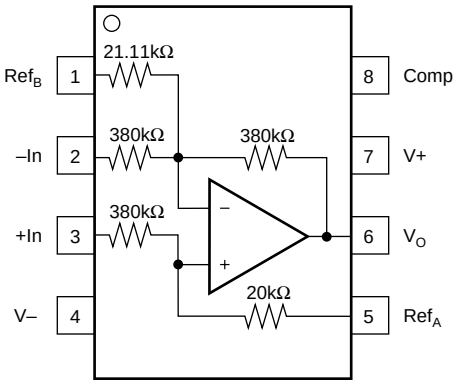
- **CURRENT MONITOR**
- **BATTERY CELL-VOLTAGE MONITOR**
- **GROUND BREAKER**
- **INPUT PROTECTION**
- **SIGNAL ACQUISITION IN NOISY ENVIRONMENTS**
- **FACTORY AUTOMATION**

DESCRIPTION

The INA117 is a precision unity-gain difference amplifier with very high common-mode input voltage range. It is a single monolithic IC consisting of a precision op amp and integrated thin-film resistor network. It can accurately measure small differential voltages in the presence of common-mode signals up to ±200V. The INA117 inputs are protected from momentary common-mode or differential overloads up to ±500V.

In many applications, where galvanic isolation is not essential, the INA117 can replace isolation amplifiers. This can eliminate costly isolated input-side power supplies and their associated ripple, noise and quiescent current. The INA117's 0.001% nonlinearity and 200kHz bandwidth are superior to those of conventional isolation amplifiers.

The INA117 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range. The metal TO-99 models are available specified for the –40°C to +85°C and –55°C to +125°C temperature range.



TEXAS INSTRUMENTS

Printed in U.S.A. December, 2000

SPECIFICATIONS

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

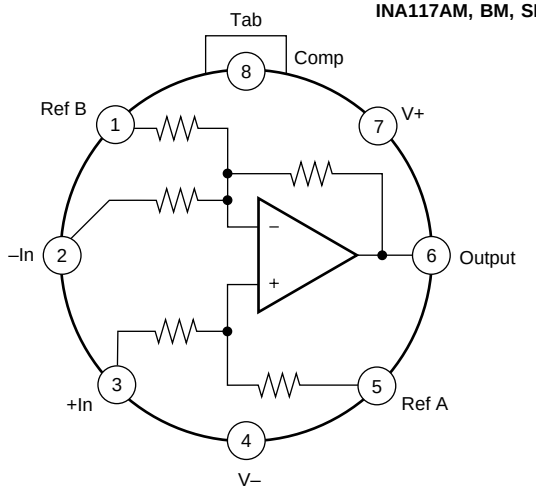
PARAMETER	CONDITIONS	INA117AM, SM			INA117BM			INA117P, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Initial (1)			1			*			*		V/V
Error			0.01	0.05		*	0.02		*	*	%
vs Temperature			2	10			*		*		ppm/°C
Nonlinearity (2)			0.0002	0.001		*	*		*	*	%
OUTPUT											
Rated Voltage	I_O = +20mA, –5mA	10	12		*	*		*	*		V
Rated Current	V_O = 10V	+20, –5			*			*			mA
Impedance			0.01			*			*		Ω
Current Limit	To Common		+49, –13			*			*		mA
Capacitive Load	Stable Operation		1000			*			*		pF
INPUT											
Impedance	Differential		800			*			*		kΩ
	Common-Mode		400			*			*		kΩ
Voltage Range	Differential	±10				*			*		V
	Common-Mode, Continuous	±200			*			*			V
Common-Mode Rejection (3)											
DC		70	80		86	94		*	*		dB
AC, 60Hz	V_{CM} = 400Vp-p	66	80		66	94		*	*		dB
vs Temperature, DC	T_A = T_{MIN} to T_{MAX}										
AM, BM, P, KU		66	75		80	90			*		dB
SM		60	75								dB
OFFSET VOLTAGE	RTO (4)										
Initial			120	1000		*	1000		*	*	µV
KU Grade (SO-8 Package)									600	2000	µV
vs Temperature	T_A = T_{MIN} to T_{MAX}		8.5	40		*	40		*		µV/°C
vs Supply	V_S = ±5V to ±18V	74	90		80	*	*	*	*		dB
vs Time			200			*			*		µV/mo
OUTPUT NOISE VOLTAGE	RTO (5)										
f_B = 0.01Hz to 10Hz			25			*			*		µVp-p
f_B = 10kHz			550			*			*		nV/√Hz
DYNAMIC RESPONSE											
Gain Bandwidth, –3dB			200			*			*		kHz
Full Power Bandwidth	V_O = 20Vp-p	30			*			*			kHz
Slew Rate		2	2.6		*	*		*	*		V/µs
Settling Time: 0.1%	V_O = 10V Step		6.5			*			*		µs
0.01%	V_O = 10V Step		10			*			*		µs
0.01%	V_{CM} = 10V Step, V_{DIFF} = 0V		4.5			*			*		µs
POWER SUPPLY											
Rated			±15			*			*		V
Voltage Range	Derated Performance	±5		±18	*		*	*		*	V
Quiescent Current	V_O = 0V		1.5	2		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: AM, BM, P, KU		–25		+85	*		*	–40		+85	°C
SM		–55		+125							°C
Operation		–55		+125	*		*	–40		+85	°C
Storage		–65		+150	*		*	–55		+125	°C

*Specification same as for INA117AM.

NOTES: (1) Connected as difference amplifier (see Figure 1). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) With zero source impedance (see discussion of common-mode rejection in Application Information section). (4) Includes effects of amplifier's input bias and offset currents. (5) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

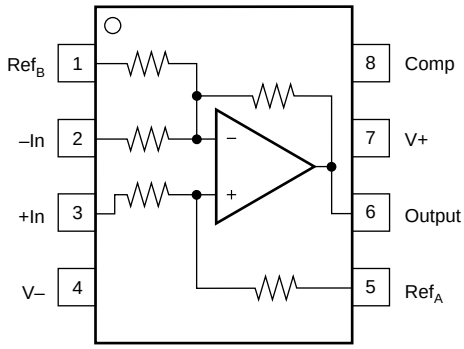
PIN CONFIGURATION

Top View **TO-99**
INA117AM, BM, SM



Case internally connected to V–. Make no connection.

Top View **DIP/SO**
INA117P, KU



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Input Voltage Range, Continuous	±200V
Common-Mode and Differential, 10s	±500V
Operating Temperature	
M Metal TO-99	–55 to +125°C
P Plastic DIP and U SO-8	–40 to +85°C
Storage Temperature	
M Package	–65 to +150°C
P Plastic DIP and U SO-8	–55 to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Common	Continuous

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

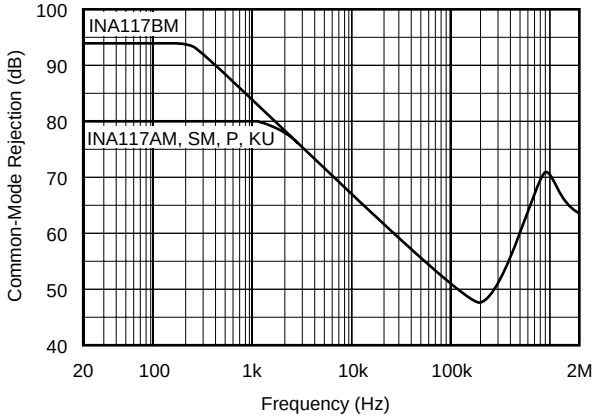
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
INA117P	DIP-8	006	–40°C to +85°C	INA117P	INA117P	Rails
INA117KU	SO-8 Surface-Mount	182	"	INA117KU	INA117KU	Rails
"	"	"	"	"	INA117KU/2K5	Tape and Reel
INA117AM	TO-99 Metal	001	–25°C to +85°C	INA117AM	INA117AM	Rails
INA117BM	"	"	"	INA117BM	INA117BM	Rails
INA117SM	"	"	–55°C to +125°C	INA117SM	INA117SM	Rails

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "INA117KU/2K5" will get a single 2500-piece Tape and Reel.

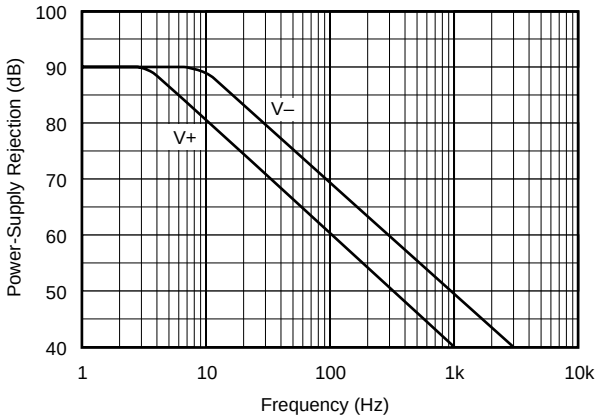
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

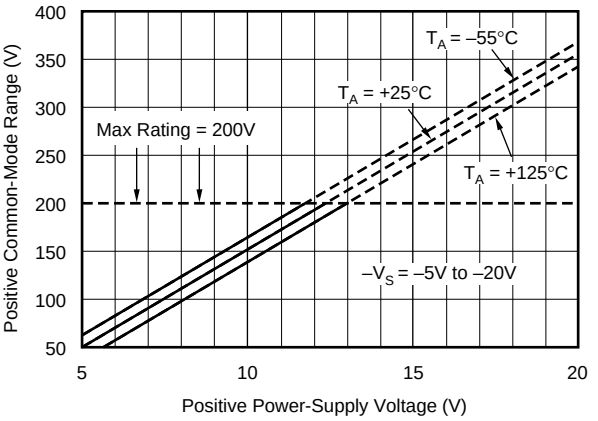
COMMON-MODE REJECTION vs FREQUENCY



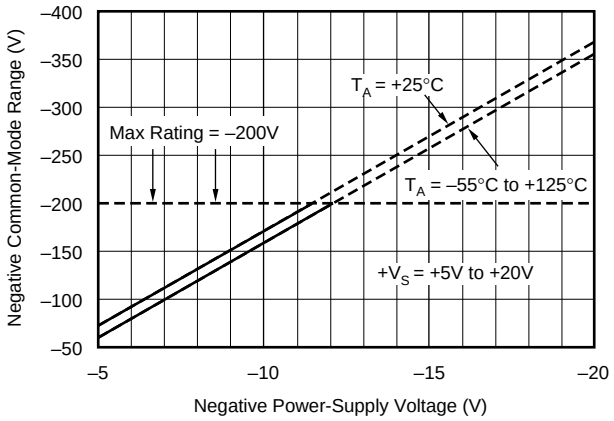
POWER-SUPPLY REJECTION vs FREQUENCY



POSITIVE COMMON-MODE VOLTAGE RANGE
vs POSITIVE POWER-SUPPLY VOLTAGE



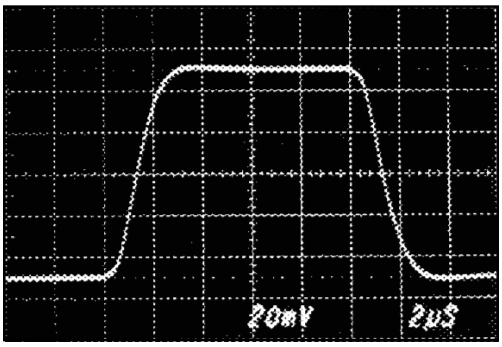
NEGATIVE COMMON-MODE VOLTAGE RANGE
vs NEGATIVE POWER-SUPPLY VOLTAGE



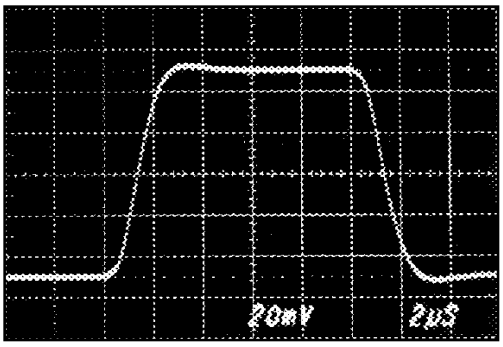
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

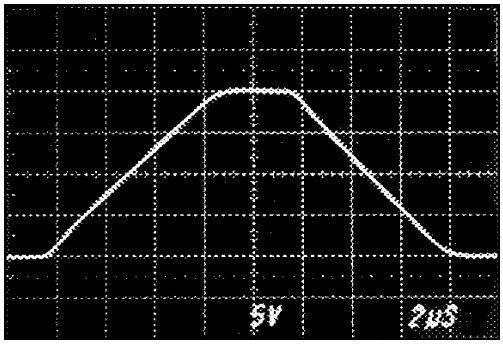
SMALL SIGNAL STEP RESPONSE
C_L = 0



SMALL SIGNAL STEP RESPONSE
C_L = 1000pF



LARGE SIGNAL STEP RESPONSE



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation.

Applications with noisy or high-impedance power-supply lines may require decoupling capacitors close to the device pins.

The output voltage is equal to the differential input voltage between pins 2 and 3. The common mode input voltage is rejected.

Internal circuitry connected to the compensation pin 8 cancels the parasitic distributed capacitance between the feedback resistor, R_2, and the IC substrate. For specified dynamic performance, pin 8 should be grounded or connected through a 0.1µF capacitor to an AC ground such as V+.

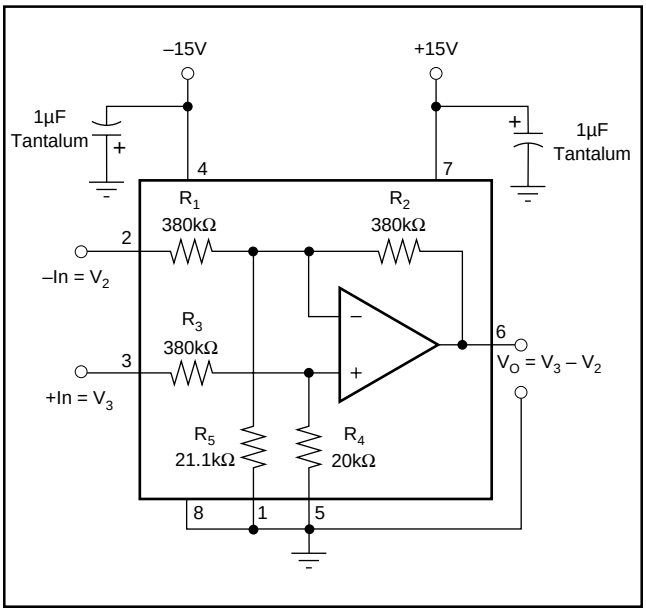


FIGURE 1. Basic Power and Signal Connections.

COMMON-MODE REJECTION

Common-mode rejection (CMR) of the INA117 is dependent on the input resistor network, which is laser-trimmed for accurate ratio matching. To maintain high CMR, it is important to have low source impedances driving the two inputs. A 75Ω resistance in series with pin 2 or 3 will decrease CMR from 86dB to 72dB.

Resistance in series with the reference pins will also degrade CMR. A 4Ω resistance in series with pin 1 or 5 will decrease CMRR from 86dB to 72dB.

Most applications do not require trimming. Figures 2 and 3 show optional circuits that may be used for trimming offset voltage and common-mode rejection.

TRANSFER FUNCTION

Most applications use the INA117 as a simple unity-gain difference amplifier. The transfer function is:

$$V_O = V_3 - V_2$$

V_3 and V_2 are the voltages at pins 3 and 2.

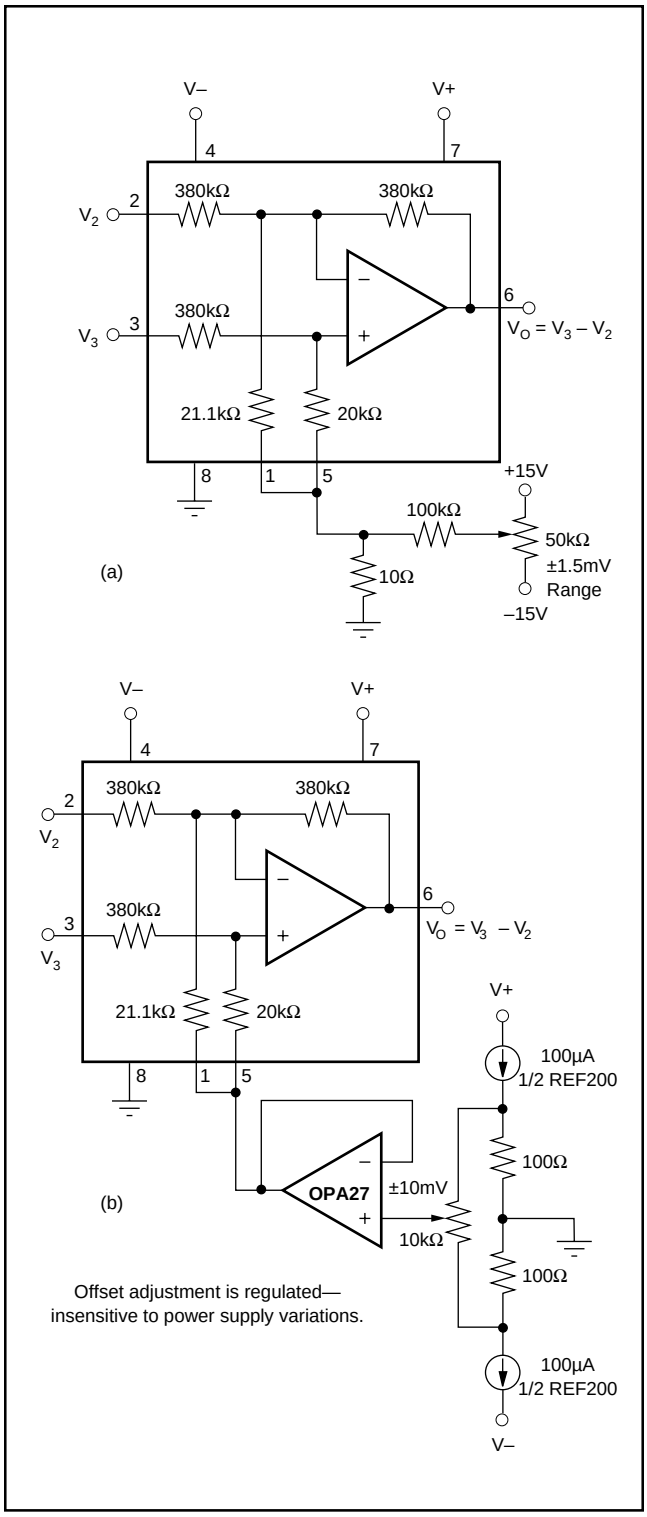


FIGURE 2. Offset Voltage Trim Circuits.

Some applications, however, apply voltages to the reference terminals (pins 1 and 5). A more complete transfer function is:

$$V_O = V_3 - V_2 + 19 \bullet V_5 - 18 \bullet V_1$$

V_5 and V_1 are the voltages at pins 5 and 1.

MEASURING CURRENT

The INA117 can be used to measure a current by sensing the voltage drop across a series resistor, R_S. Figure 4 shows the INA117 used to measure the supply currents of a device under test. The circuit in Figure 5 measures the output current of a power supply. If the power supply has a sense connection, it can be connected to the output side of R_S to eliminate the voltage-drop error. Another common application is current-to-voltage conversion, as shown in Figure 6.

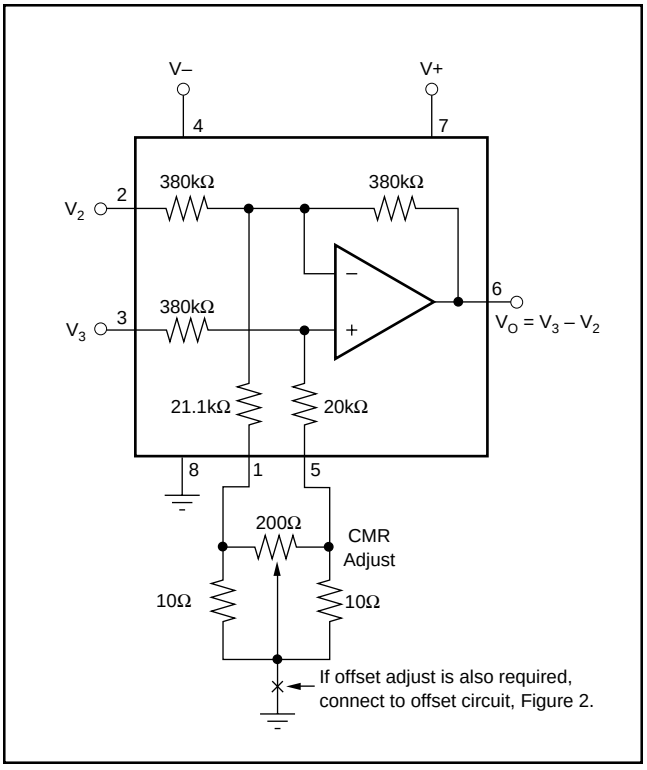


FIGURE 3. CMR Trim Circuit.

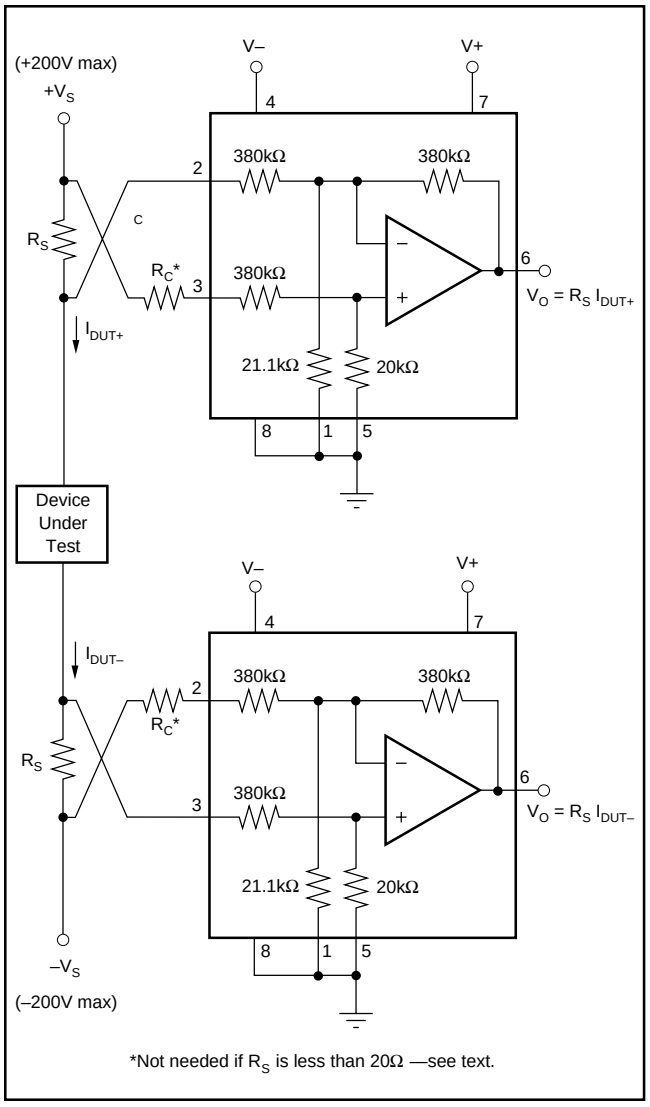


FIGURE 4. Measuring Supply Currents of Device Under Test.

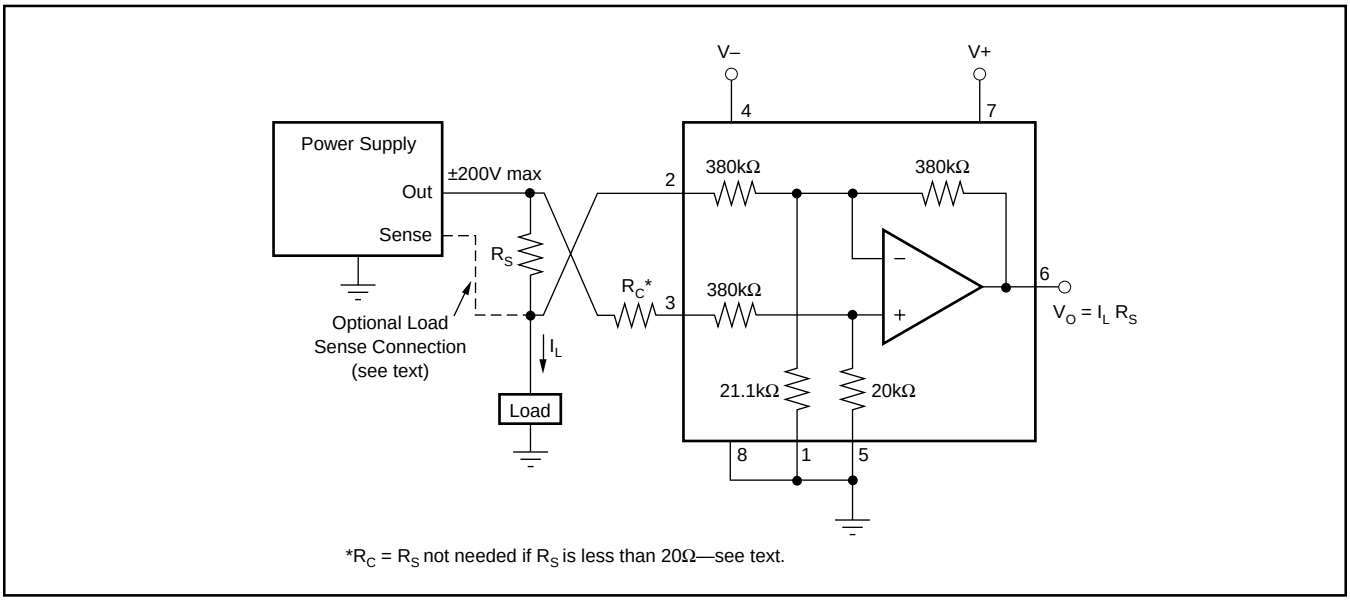


FIGURE 5. Measuring Power Supply Output Current.

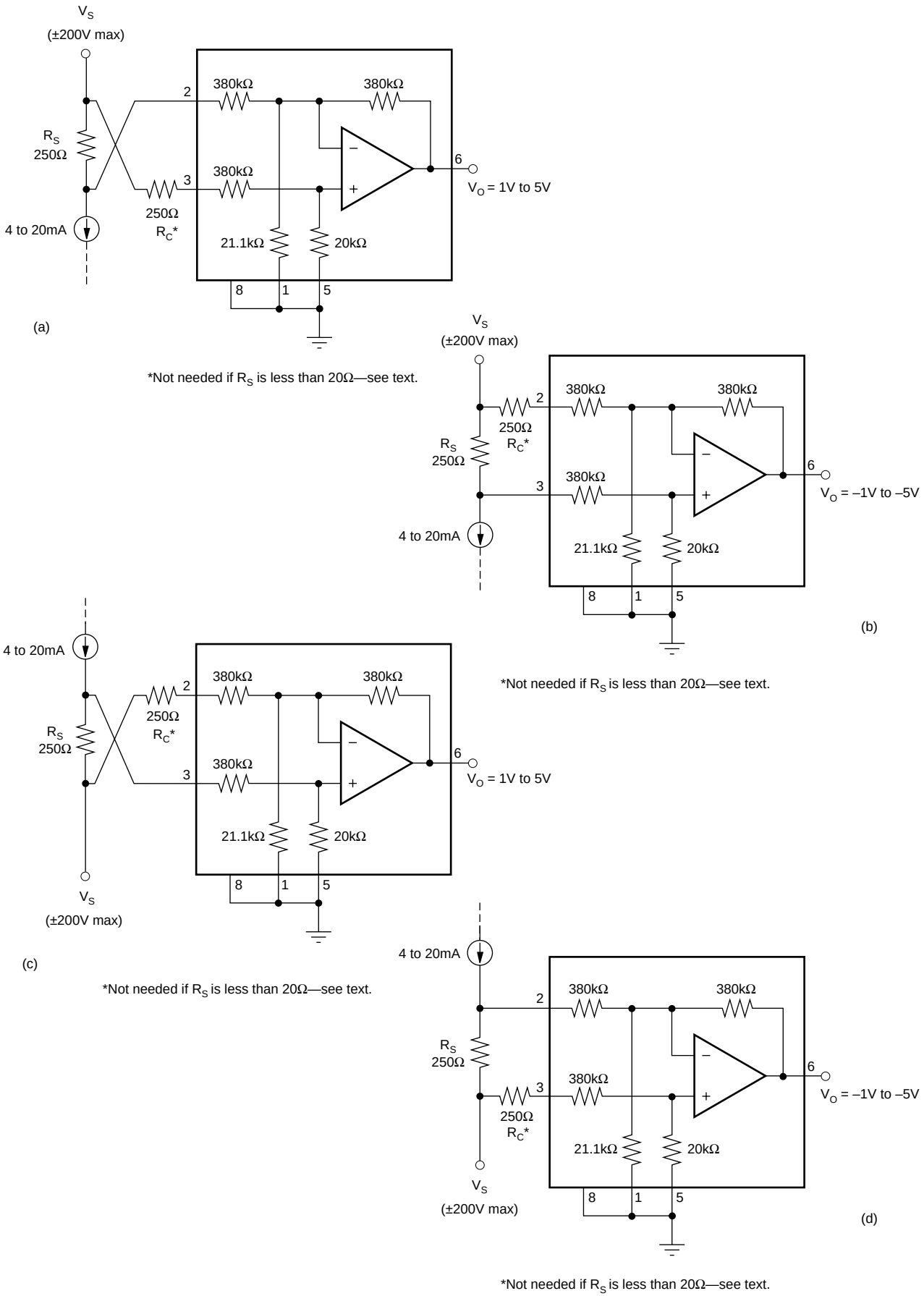


FIGURE 6. Current to Voltage Converter.

In all cases, the sense resistor imbalances the input resistor matching of the INA117, degrading its CMR. Also, the input impedance of the INA117 loads R_S, causing gain error in the voltage-to-current conversion. Both of these errors can be easily corrected.

The CMR error can be corrected with the addition of a compensation resistor, R_C, equal in value to R_S as shown in Figures 4, 5, and 6. If R_S is less than 20Ω, the degradation in CMR is negligible and R_C can be omitted. If R_S is larger than approximately 2kΩ, trimming R_C may be required to achieve greater than 86dB CMR. This is because the actual INA117 input impedances have 1% typical mismatch.

If R_S is more than approximately 100Ω, the gain error will be greater than the 0.02% specification of the INA117. This gain error can be corrected by slightly increasing the value of R_S. The corrected value, R_S', can be calculated by:

$$R_S' = \frac{R_S \bullet 380k\Omega}{380k\Omega - R_S}$$

Example: For a 1V/mA transfer function, the nominal, uncorrected value for R_S would be 1kΩ. A slightly larger value, R_S' = 1002.6Ω, compensates for the gain error due to loading.

The 380kΩ term in the equation for R_S' has a tolerance of ±25%, so sense resistors above approximately 400Ω may require trimming to achieve gain accuracy better than 0.02%.

Of course, if a buffer amplifier is added as shown in Figure 7, both inputs see a low source impedance, and the sense resistor is not loaded. As a result, there is no gain error or CMR degradation. The buffer amplifier can operate as a unity gain buffer or as an amplifier with non-inverting gain. Gain added ahead of the INA117 improves both CMR and signal-to-noise. Added gain also allows a lower voltage drop across the sense resistor. The OPA1013 is a good choice for the buffer amplifier since both its input and output can swing close to its negative power supply.

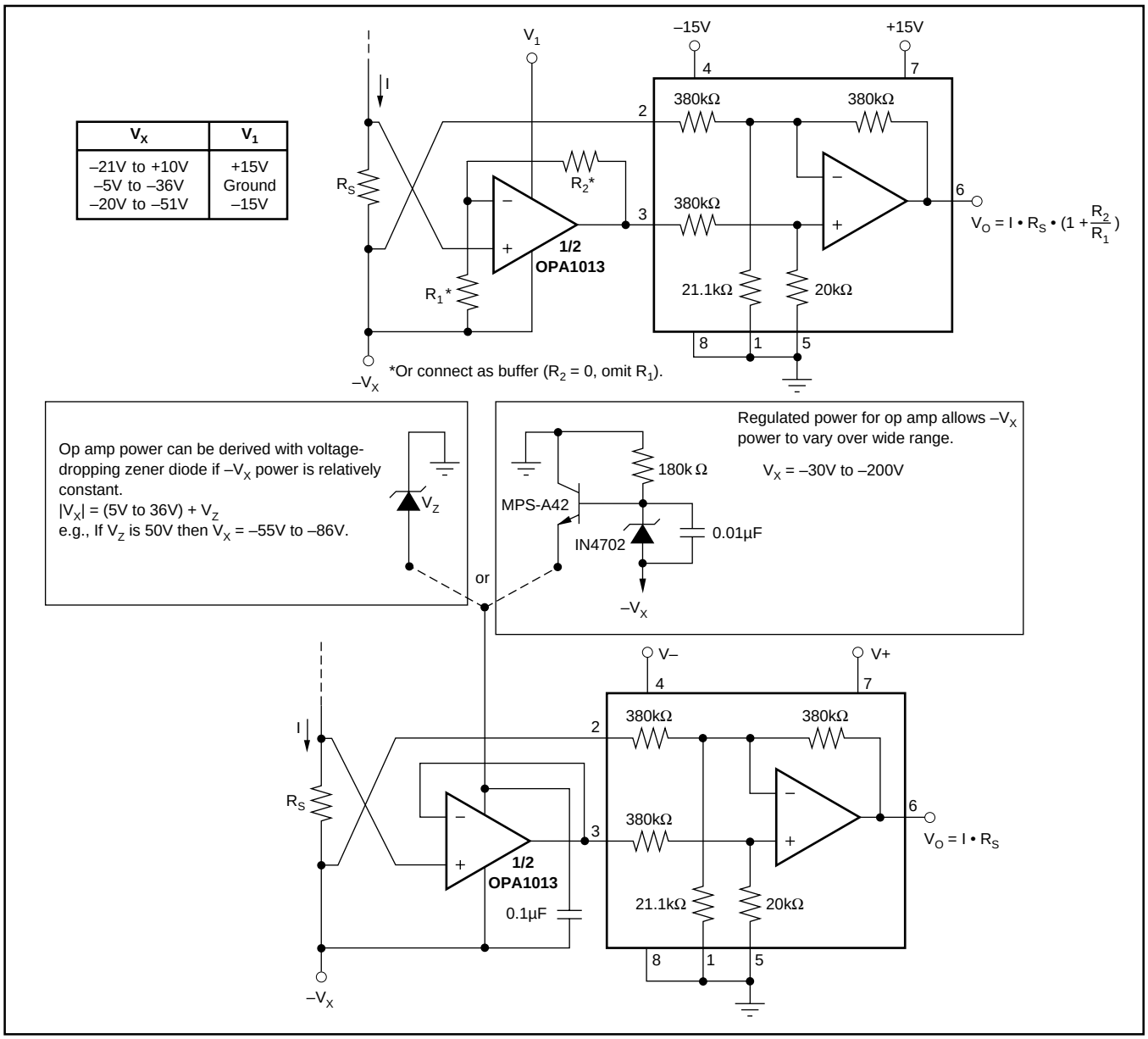


FIGURE 7. Current Sensing with Input Buffer.

Figure 8 shows very high input impedance buffer used to measure low leakage currents. Here, the buffer op amp is powered with an isolated, split-voltage power supply. Using an isolated power supply allows full ±200V common-mode input range.

NOISE PERFORMANCE

The noise performance of the INA117 is dominated by the internal resistor network. The thermal or Johnson noise of these resistors produces approximately 550nV/$\sqrt{\text{Hz}}$ noise. The internal op amp contributes virtually no excess noise at frequencies above 100Hz.

Many applications may be satisfied with less than the full 200kHz bandwidth of the INA117. In these cases, the noise can be reduced with a low-pass filter on the output. The two-pole filter shown in Figure 9 limits bandwidth to 1kHz and reduces noise by more than 15:1. Since the INA117 has a 1/f noise corner frequency of approximately 100Hz, a cutoff frequency below 100Hz will not further reduce noise.

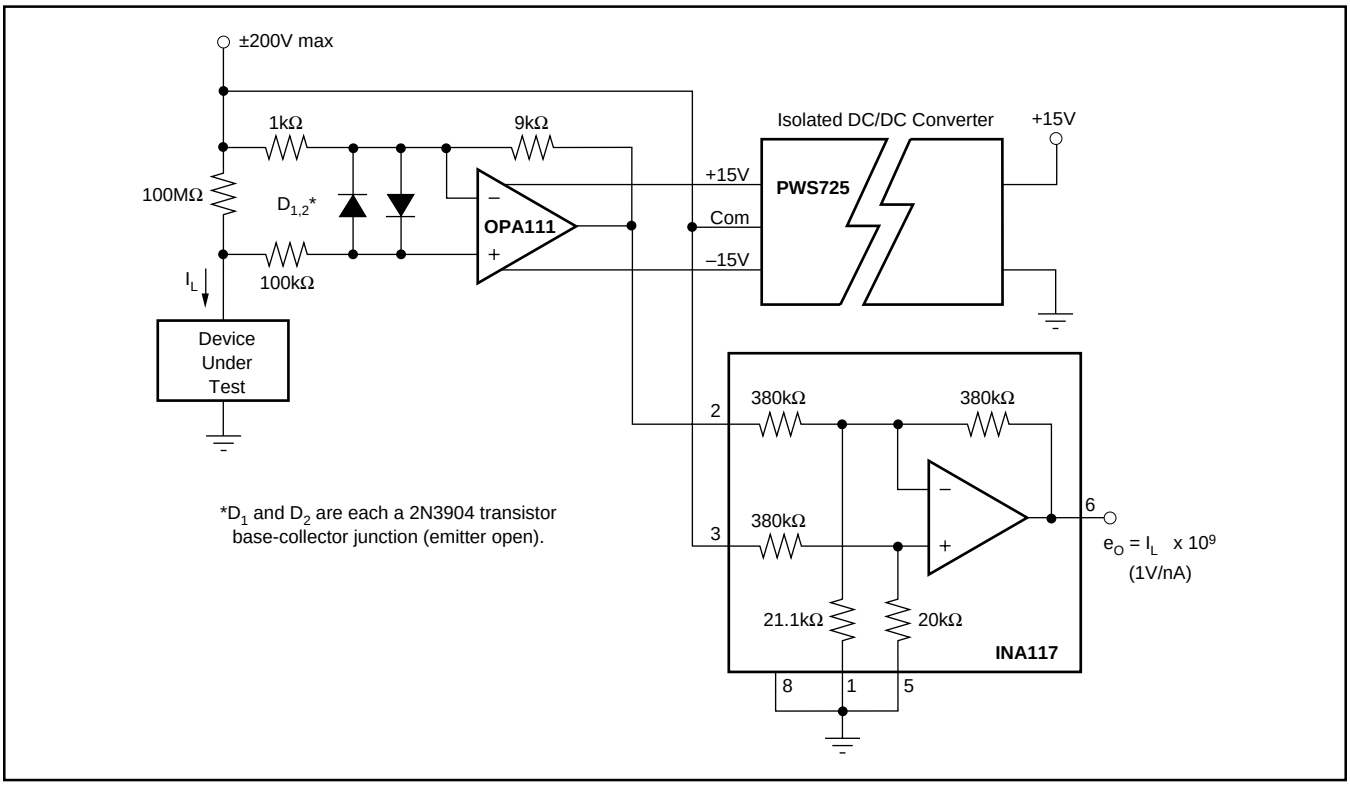
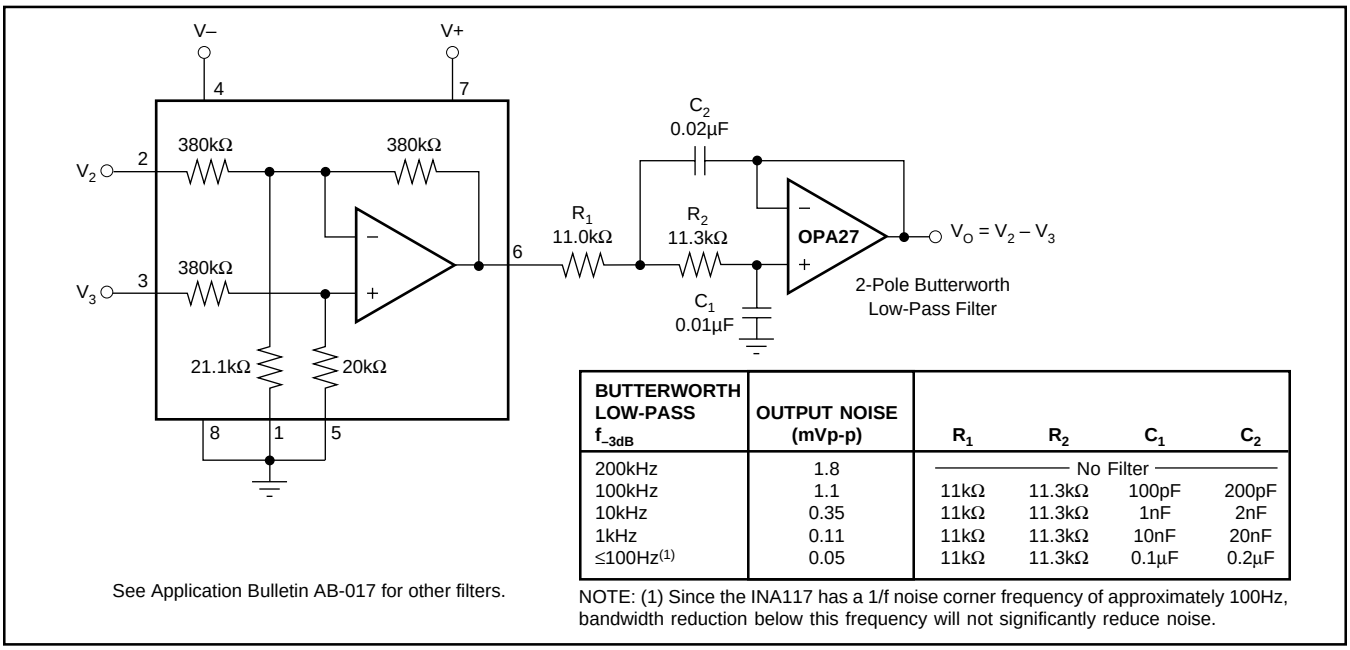


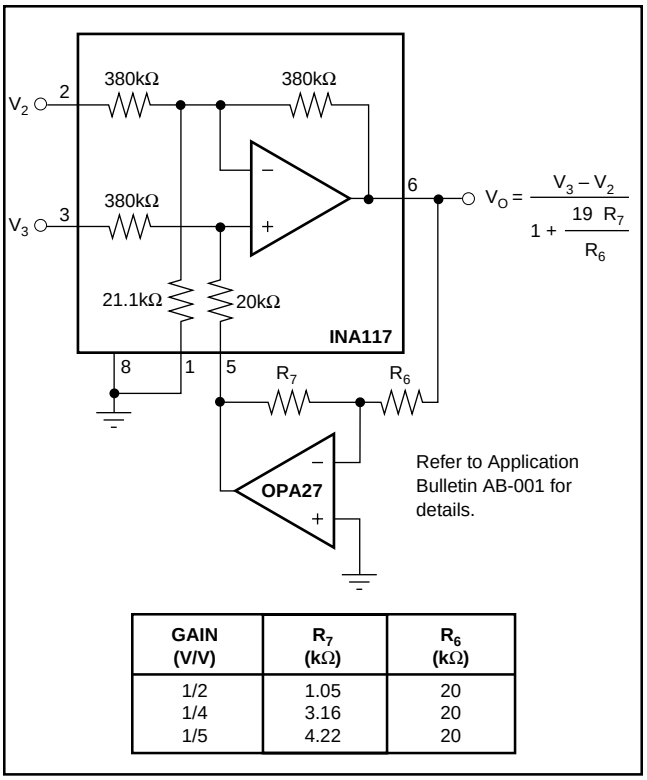
FIGURE 8. Leakage Current Measurement Circuit.



BUTTERWORTH LOW-PASS f_{-3dB}	OUTPUT NOISE (mVp-p)	R_1	R_2	C_1	C_2
200kHz	1.8	No Filter			
100kHz	1.1	11kΩ	11.3kΩ	100pF	200pF
10kHz	0.35	11kΩ	11.3kΩ	1nF	2nF
1kHz	0.11	11kΩ	11.3kΩ	10nF	20nF
≤100Hz(1)	0.05	11kΩ	11.3kΩ	0.1µF	0.2µF

NOTE: (1) Since the INA117 has a 1/f noise corner frequency of approximately 100Hz, bandwidth reduction below this frequency will not significantly reduce noise.

FIGURE 9. Output Filter for Noise Reduction.



GAIN (V/V)	R_7 (kΩ)	R_6 (kΩ)
1/2	1.05	20
1/4	3.16	20
1/5	4.22	20

FIGURE 10. Reducing Differential Gain.

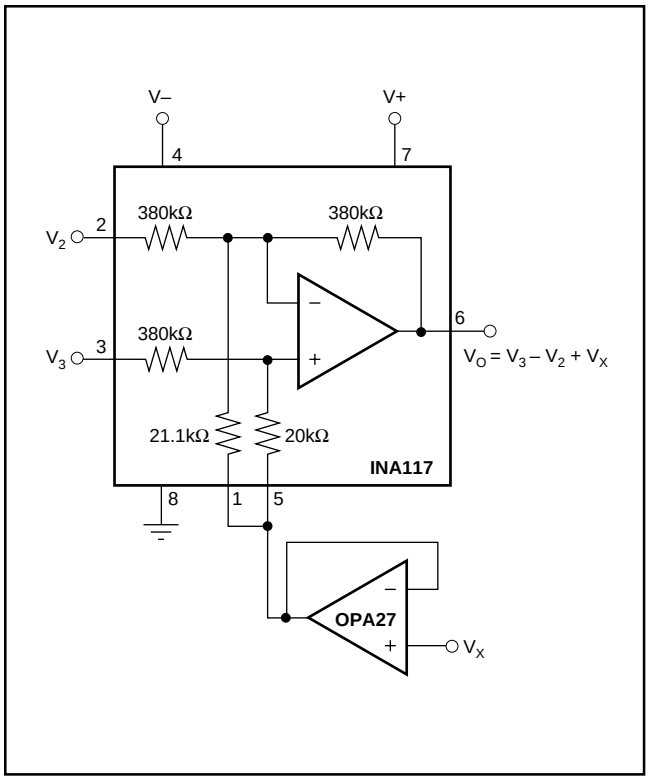


FIGURE 11. Summing V_X in Output.

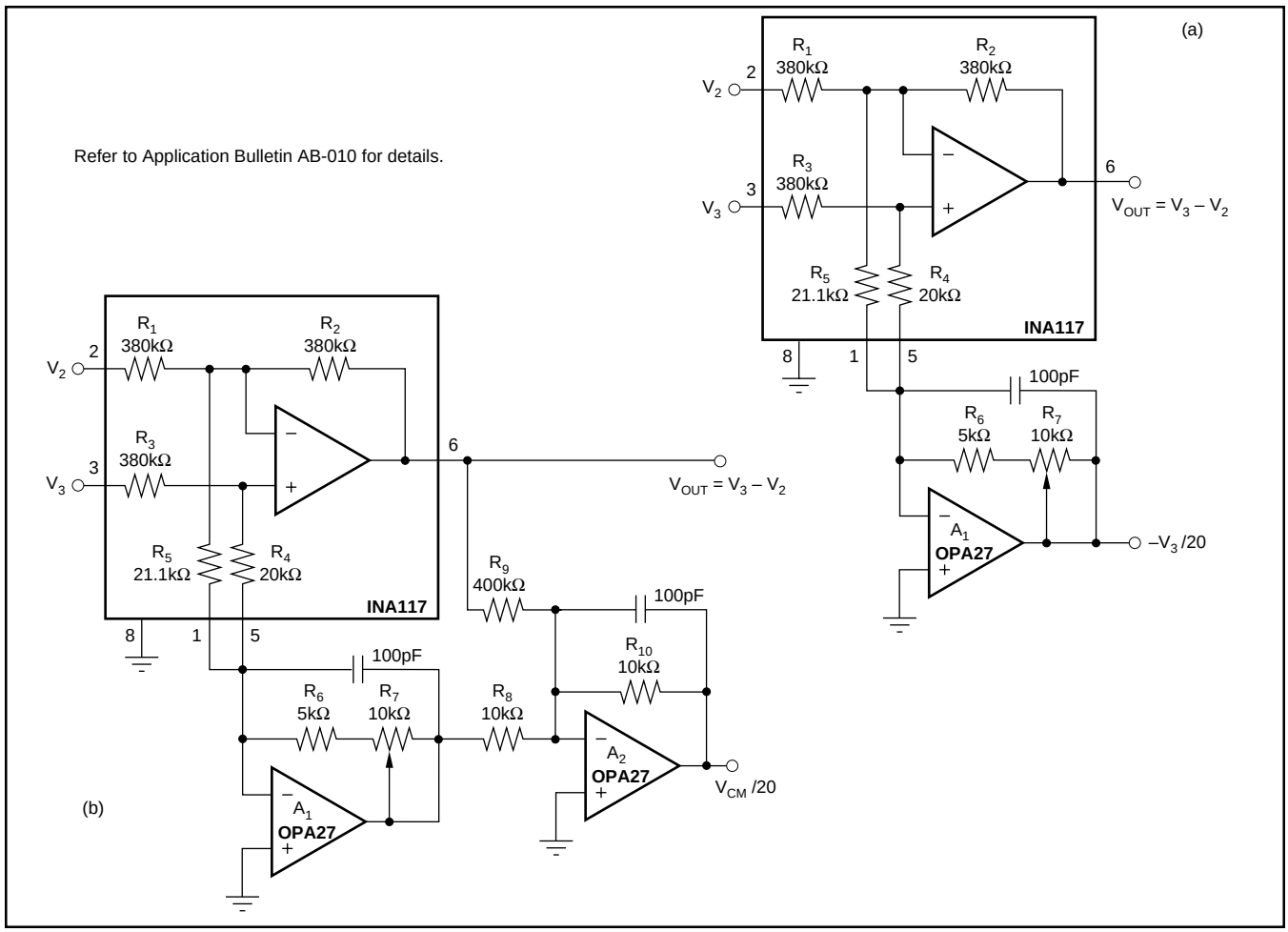


FIGURE 12. Common-Mode Voltage Monitoring.

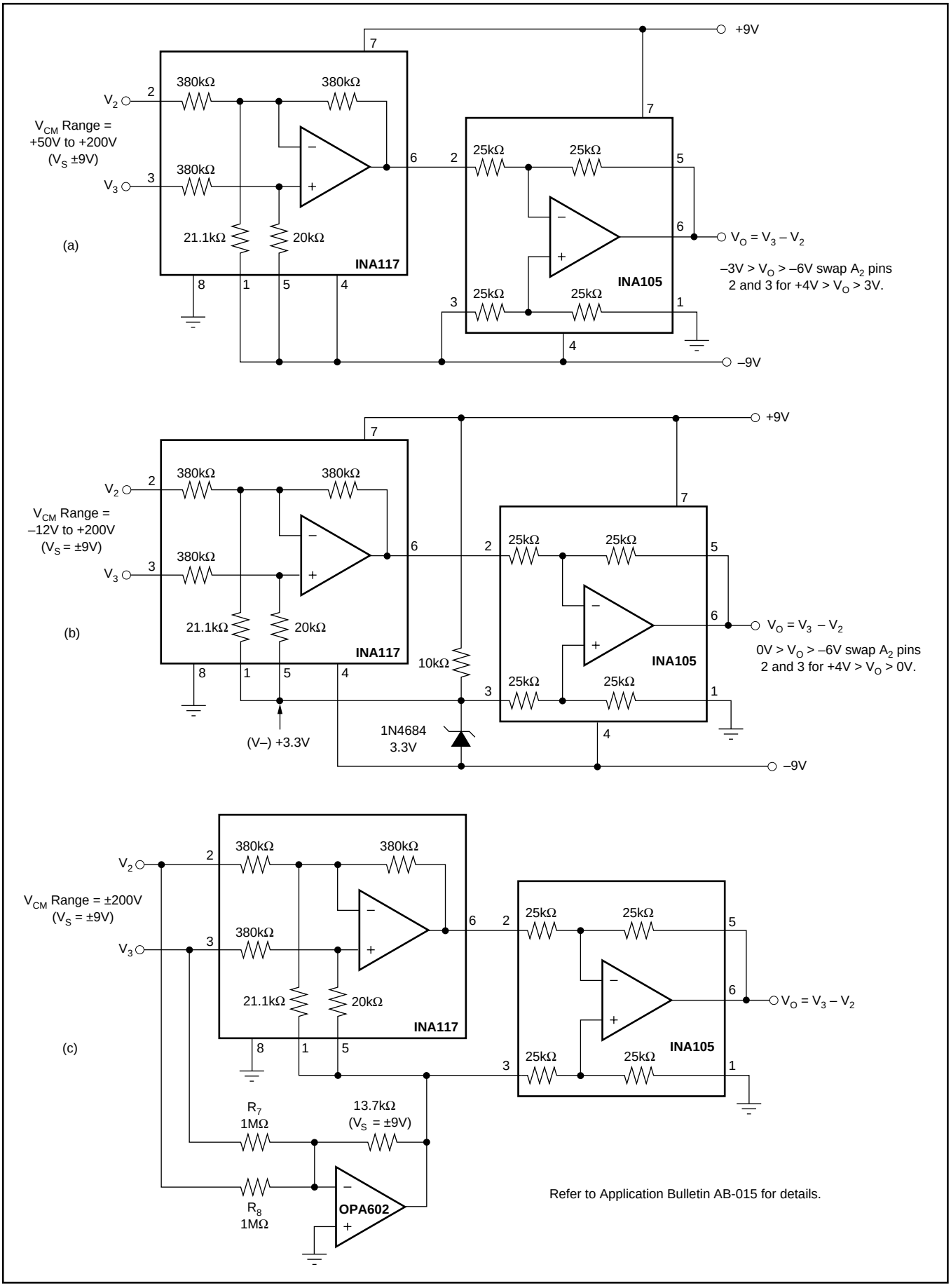


FIGURE 13. Offsetting or Boosting Common-Mode Voltage Range for Reduced Power-Supply Voltage Operation.

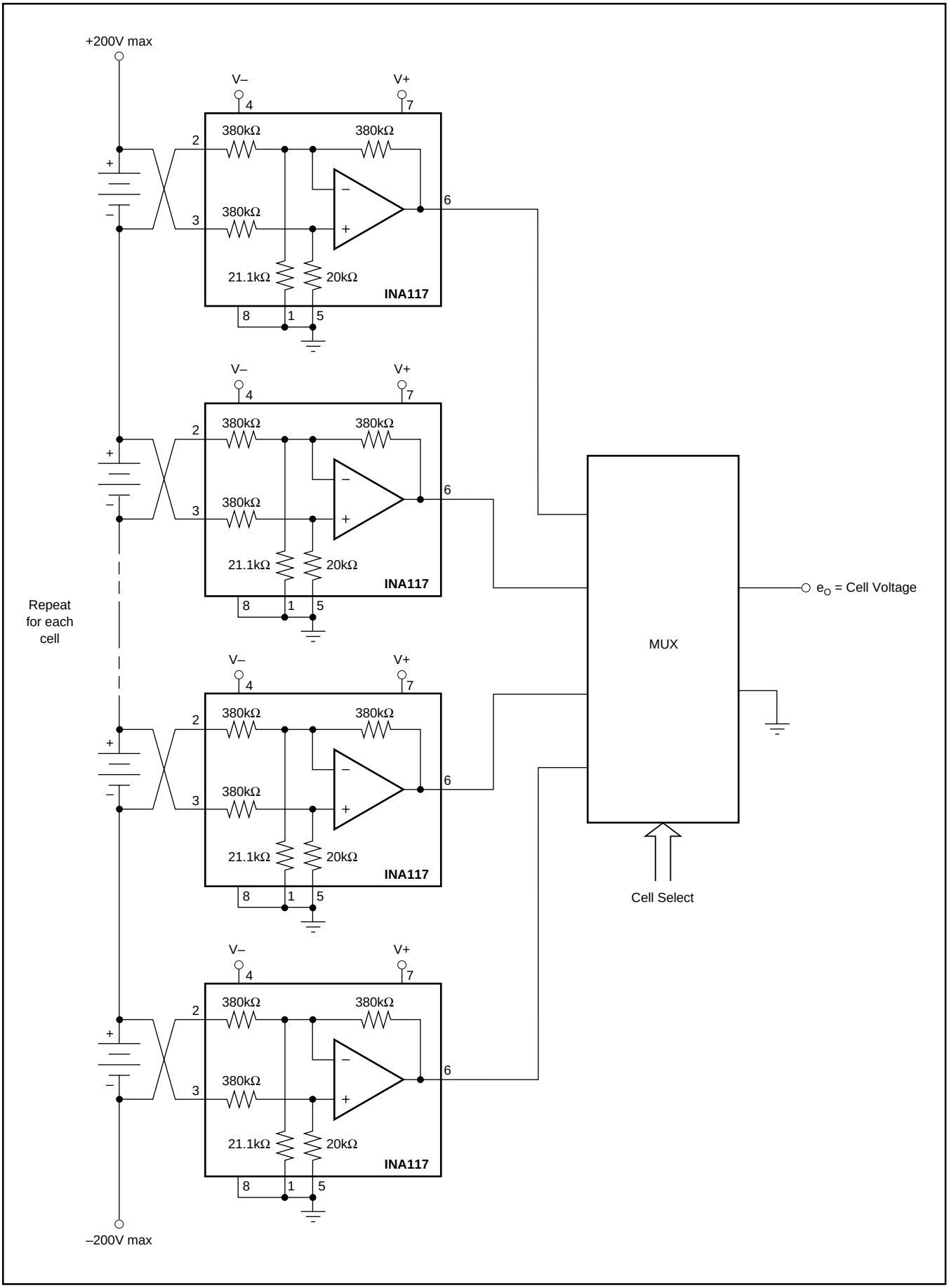


FIGURE 14. Battery Cell Voltage Monitor.

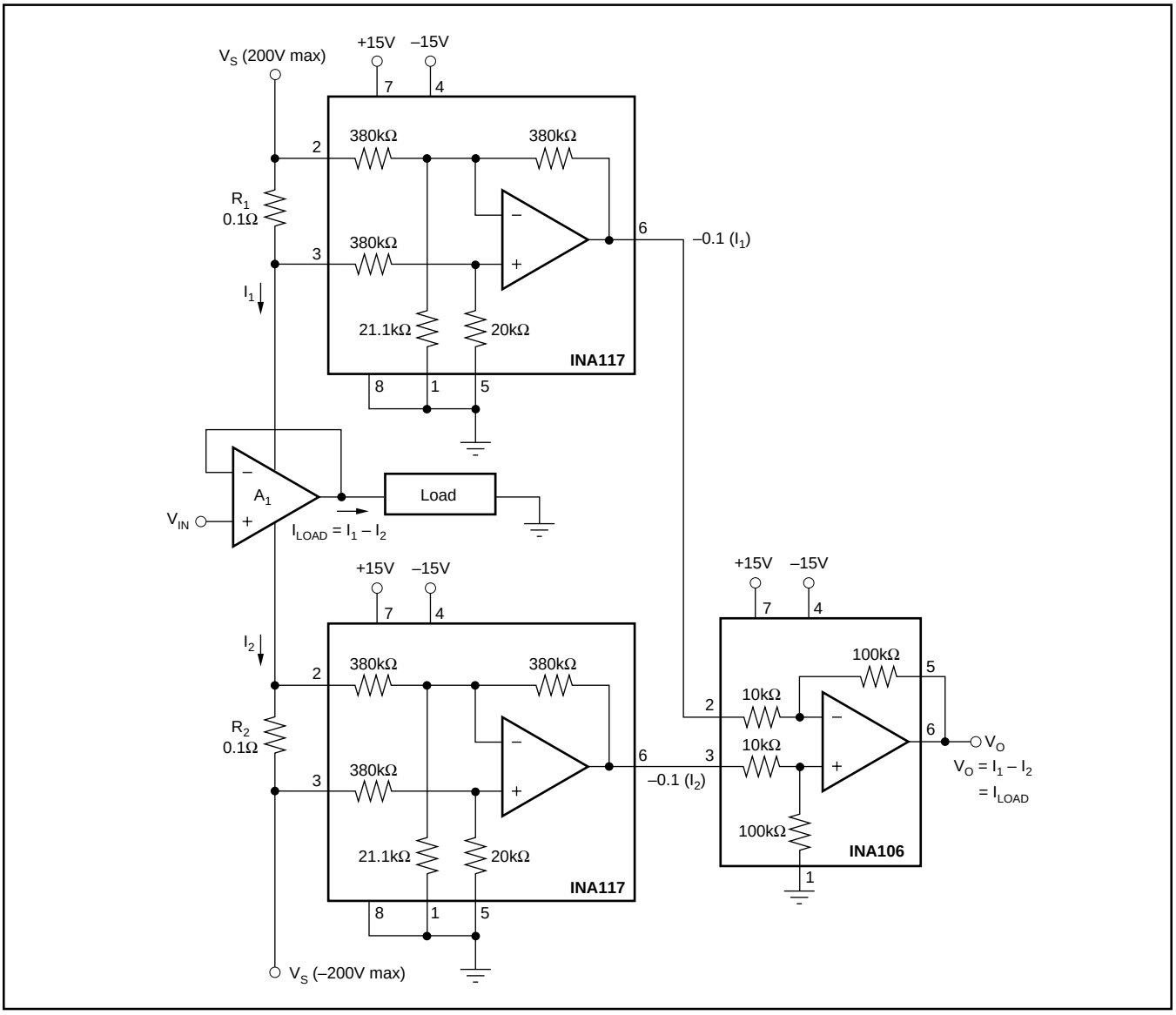


FIGURE 15. Measuring Amplifier Load Current.

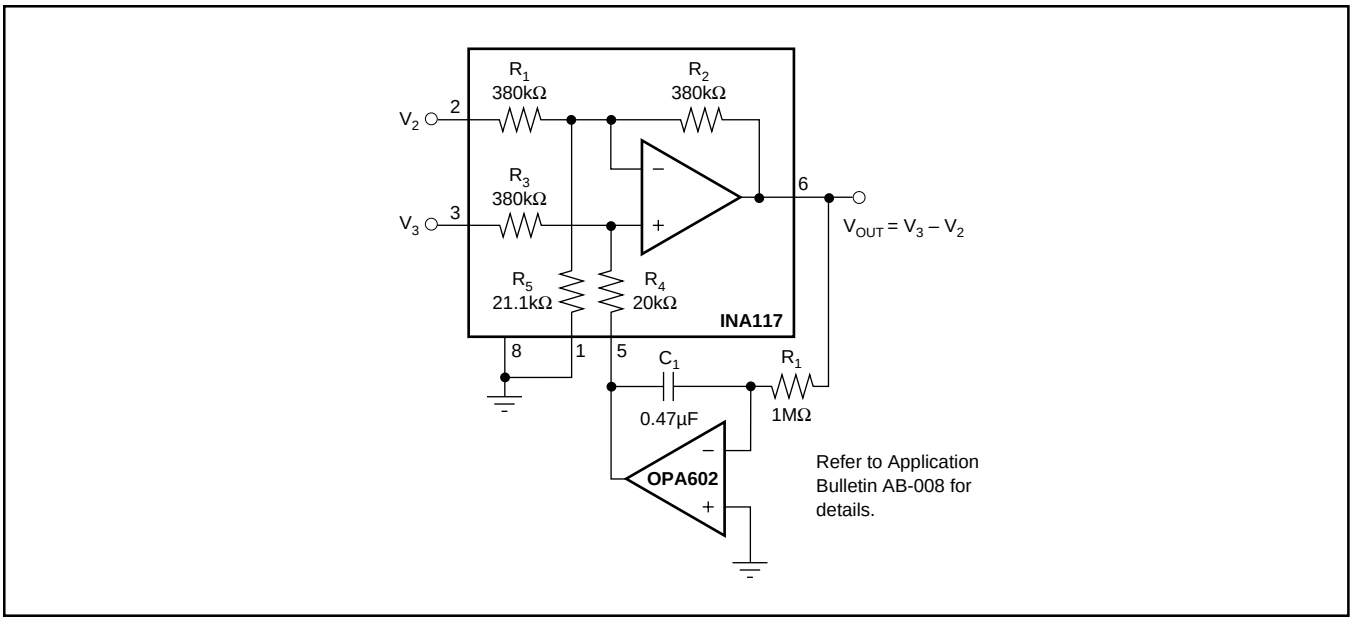


FIGURE 16. AC-Coupled INA117.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA117AM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		INA117AM	
INA117BM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		INA117BM	
INA117KU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA 117KU 2	Samples
INA117KU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		INA 117KU 2	Samples
INA117KU/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		INA 117KU 2	Samples
INA117KUG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA 117KU 2	Samples
INA117P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA117P	Samples
INA117PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA117P	Samples
INA117SM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		INA117SM	
INA117SMQ	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		INA117SMQ	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

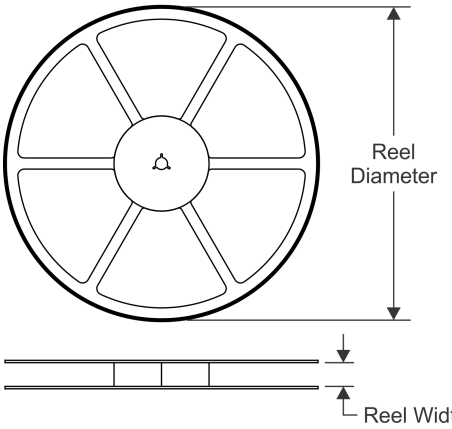
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

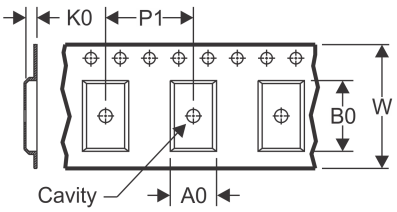
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

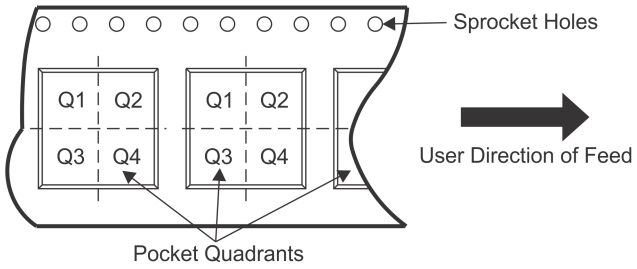


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

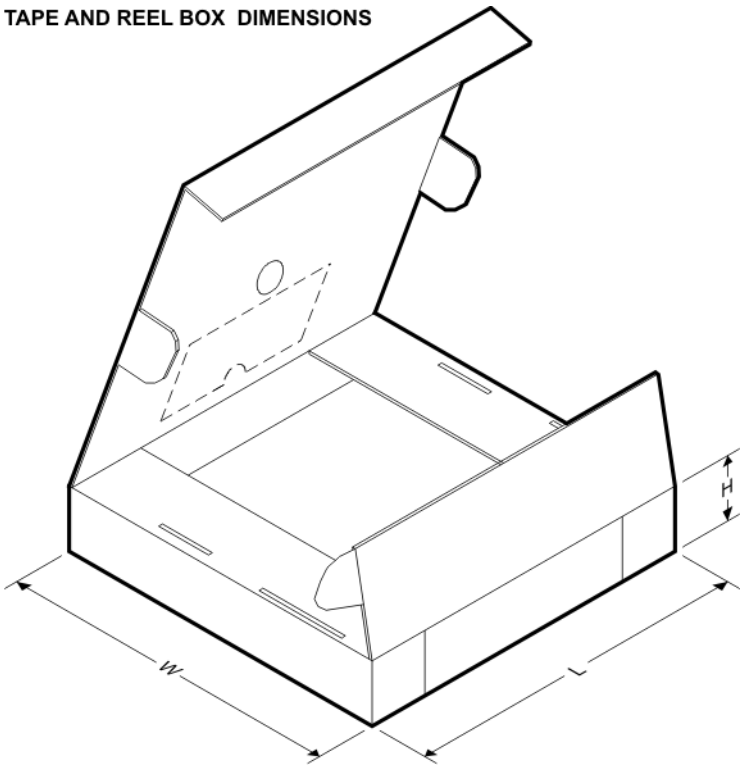
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA117KU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA117KU/2K5	SOIC	D	8	2500	367.0	367.0	35.0

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