Wideband, Low Distortion, Unity-Gain Stable, Voltage-Feedback OPERATIONAL AMPLIFIER

Check for Samples: OPA842

FEATURES

- **UNITY-GAIN BANDWIDTH: 400MHz**
- **GAIN-BANDWIDTH PRODUCT: 200MHz**
- **LOW INPUT VOLTAGE NOISE: 2.6nV/√Hz**
- **VERY LOW DISTORTION: –93dBc (5MHz)**
- **HIGH OPEN-LOOP GAIN: 110dB**
- **FAST 12-BIT SETTLING: 22ns (0.01%)**
- **LOW DC VOLTAGE OFFSET: 300μV Typical**
- **PROFESSIONAL LEVEL DIFF GAIN/PHASE ERROR: 0.003%/0.008°**

APPLICATIONS

- **ADC/DAC BUFFER DRIVER**
- **LOW DISTORTION IF AMPLIFIER**
- **ACTIVE FILTER CONFIGURATION**
- **LOW-NOISE DIFFERENTIAL RECEIVER**
- **HIGH-RESOLUTION IMAGING**
- **TEST INSTRUMENTATION**
- **PROFESSIONAL AUDIO**
- **OPA642 UPGRADE**

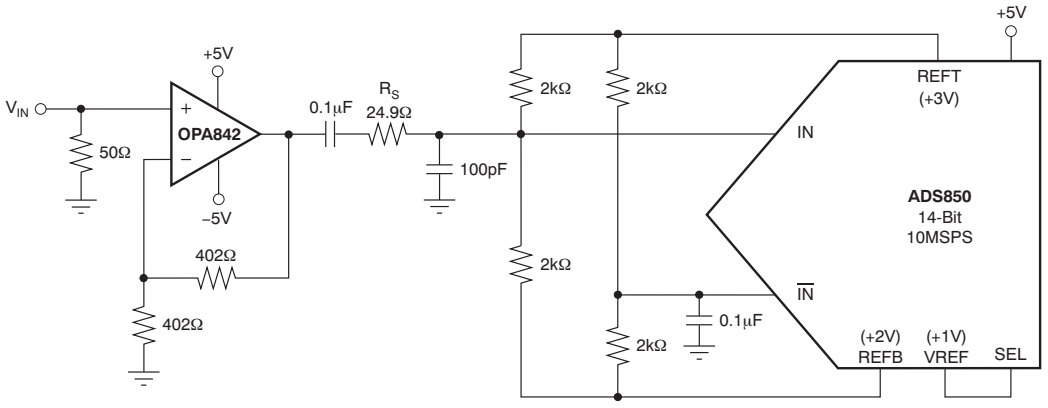
DESCRIPTION

The OPA842 provides a level of speed and dynamic range previously unattainable in a monolithic op amp. Using unity-gain stable, voltage-feedback architecture with two internal gain stages, the OPA842 achieves exceptionally low harmonic distortion over a wide frequency range. The *classic* differential input provides all the familiar benefits of precision op amps, such as bias current cancellation and very low inverting current noise compared with wideband current differential gain/phase performance, low-voltage noise, and high output current drive make the OPA842 ideal for most high dynamic range applications.

Unity-gain stability makes the OPA842 particularly suitable for low-gain differential amplifiers, transimpedance amplifiers, gain of +2 video line drivers, wideband integrators, and low-distortion analog-to-digital converter (ADC) buffers. Where higher gain or even lower harmonic distortion is required, consider the OPA843—a higher-gain bandwidth and lower-noise version of the OPA842.

OPA842 RELATED PRODUCTS

SINGLES	INPUT NOISE VOLTAGE (nV/√Hz)	GAIN-BANDWIDTH PRODUCT (MHz)
OPA843	2.0	800
OPA846	1.1	2500
OPA847	0.8	3700



AC-Coupled to 14-Bit ADS850 Interface

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA842	SO-8	D	-40°C to +85°C	OPA842	OPA842ID	Rails, 100
					OPA842IDR	Tape and Reel, 2500
OPA842	SOT23-5	DBV	-40°C to +85°C	OAQI	OPA842IDBVT	Tape and Reel, 250
					OPA842IDBVR	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see device product folder at www.ti.com.

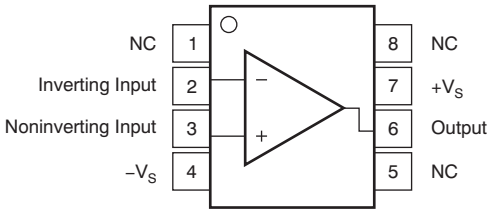
ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		OPA842	UNIT
Power Supply		±6.5	V_{DC}
Internal Power Dissipation		See Thermal Analysis	
Differential Input Voltage		±1.2	V
Input Voltage Range		$\pm V_S$	V
Storage Temperature Range (T_{stg}): D, DBV		–65 to +125	°C
Junction Temperature (T_J)		+175	°C
ESD Ratings	Human Body Model (HBM)	2000	V
	Charge Device Model (CDM)	1500	V
	Machine Model (MM)	200	V

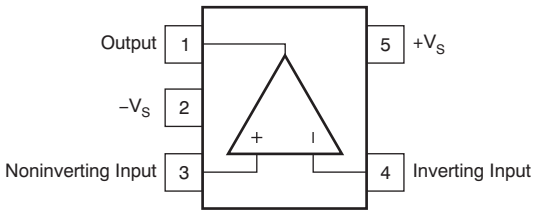
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

D PACKAGE
SO-8
(TOP VIEW)



NC = No connection.

DRB PACKAGE
SOT23-5
(TOP VIEW)



Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are tested at **+25°C**. At T_A = +25°C, V_S = ±5V, R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted. See Figure 37 for ac performance.

PARAMETER	TEST CONDITIONS	OPA842ID, IDBV						TEST LEVELS(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to +70°C(3)	-40°C to +85°C(3)	UNIT	MIN/ MAX	
AC Performance (see Figure 37)								
Closed-Loop Bandwidth (V_O = 100mV_{PP})	G = +1, R_F = 25Ω	350				MHz	typ	C
	G = +2	150	105	101	100	MHz	min	B
	G = +5	45	30	29	29	MHz	min	B
	G = +10	21	15	14	14	MHz	min	B
Gain-Bandwidth Product		200	136	135	135	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +2, R_L = 100Ω, V_O = 100mV_{PP}	56				MHz	typ	C
	G = +1, R_L = 100Ω, R_F = 25Ω	105				MHz	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2V_{PP}							
second-Harmonic	R_L = 100Ω	–80	–78	–77	–76	dBc	max	B
	R_L = 500Ω	–94	–92	–91	–90	dBc	max	B
third-Harmonic	R_L = 100Ω	–97	–96	–95	–94	dBc	max	B
	R_L = 500Ω	–93	–91	–90	–90	dBc	max	B
Two-Tone, Third-Order Intercept	G = +2, f = 10MHz	44				dBm	typ	C
Input Voltage Noise	f > 1MHz	2.6	2.8	3.0	3.1	nV/√Hz	max	B
Input Current Noise	f > 1MHz	2.7	2.8	2.9	3.0	pA/√Hz	max	B
Rise and Fall Time	0.2V Step	2.3	3.3	3.4	3.5	ns	max	B
Slew Rate	2V Step	400	300	250	225	V/µs	min	B
Settling Time to 0.01%	2V Step	22				ns	typ	C
Settling Time to 0.1%	2V Step	15	19.6	20.3	21.3	ns	max	B
Settling Time to 1.0%	2V Step	9	10.2	11.3	12.5	ns	max	B
Differential Gain	G = +2, NTSC, R_L = 150Ω	0.003				%	typ	C
Differential Phase	G = +2, NTSC, R_L = 150Ω	0.008				degrees	typ	C
DC PERFORMANCE(4)								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V	110	**100**	96	92	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±0.30	**±1.2**	±1.4	±1.5	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±4	±4	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	–20	**–35**	–36	–37	µA	max	A
Input Bias Current Drift	V_{CM} = 0V			25	25	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±0.35	**±1.0**	±1.15	±1.17	µA	max	A
Input Offset Current Drift	V_{CM} = 0V			±2	±2	nA/°C	max	B
INPUT								
Common-Mode Input Range(5) (CMIR)		±3.2	**±3.0**	±2.9	±2.8	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±1V, Input-Referred	95	**85**	84	82	dB	min	A
Input Impedance								
Differential Mode	V_{CM} = 0V	14 || 1				kΩ || pF	typ	C
Common-Mode	V_{CM} = 0V	3.1 || 1.2				MΩ || pF	typ	C

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Junction temperature = ambient temperature for +25°C specifications.
(3) Junction temperature = ambient at low temperature limits; junction temperature = ambient +23°C at high temperature limit for over-temperature min/max specifications.
(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

Boldface limits are tested at **+25°C**. At T_A = +25°C, V_S = ±5V, R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted. See Figure 37 for ac performance.

PARAMETER	TEST CONDITIONS	OPA842ID, IDBV						TEST LEVELS[1]
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[2]	0°C to +70°C[3]	-40°C to +85°C[3]	UNIT	MIN/ MAX	
OUTPUT								
Output Voltage Swing	R_L > 1kΩ, Positive Output	3.2	**3.0**	±2.9	±2.8	V	min	A
	R_L > 1kΩ, Negative Output	–3.7	**–3.5**	–3.4	–3.3	V	min	A
	R_L = 100Ω, Positive Output	3.0	**2.8**	2.7	2.6	V	min	A
	R_L = 100Ω, Negative Output	–3.5	**–3.3**	–3.2	–3.1	V	min	A
Current Output, Sourcing	V_O = 0V	±100	**±90**	±85	±80	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 1kHz	0.00038				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage			**±6**	±6	±6	V	min	A
Minimum Operating Voltage		±3.5				V	typ	C
Maximum Quiescent Current	V_S = ±5V	20.2	**20.8**	22.2	22.5	mA	max	A
Minimum Quiescent Current	V_S = ±5V	20.2	**19.6**	19.1	18.3	mA	min	A
Power-Supply Rejection Ratio (+PSRR, –PSRR)	$\|V_S\|$ = 4.5V to 5.5V, Input-Referred	100	**90**	88	85	dB	min	A
THERMAL CHARACTERISTICS								
Specified Operating Range: D, DBV		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient	—				—	—	—
D SO-8		125				°C/W	typ	C
DBV SOT23		150				°C/W	typ	C

TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE

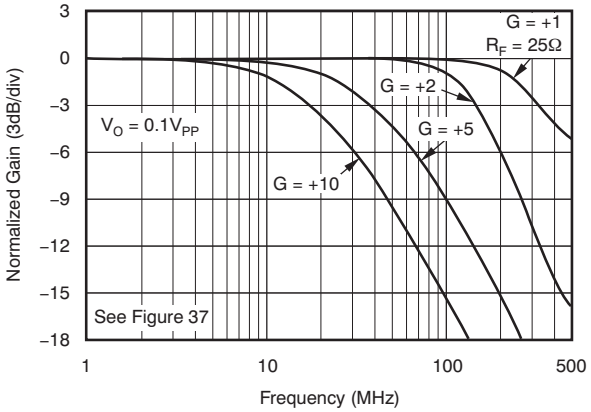


Figure 1.

INVERTING SMALL−SIGNAL FREQUENCY RESPONSE

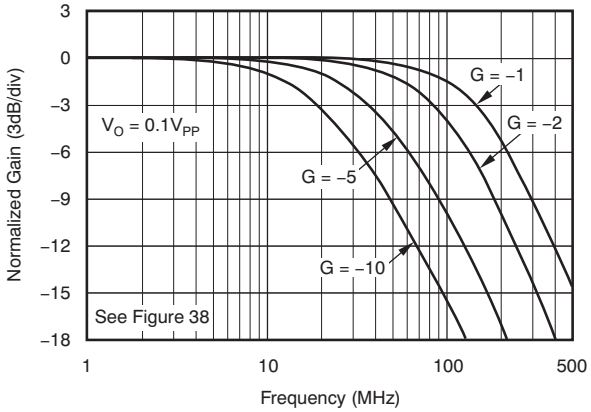


Figure 2.

NONINVERTING LARGE−SIGNAL FREQUENCY RESPONSE

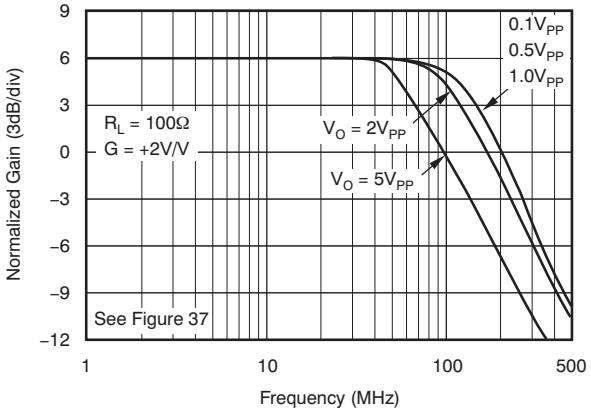


Figure 3.

INVERTING LARGE−SIGNAL FREQUENCY RESPONSE

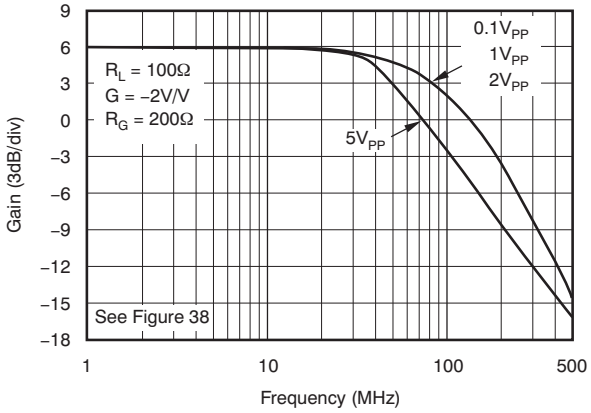


Figure 4.

NONINVERTING PULSE RESPONSE

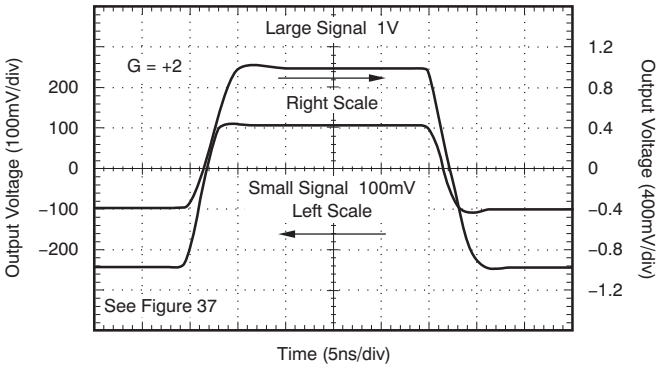


Figure 5.

INVERTING PULSE RESPONSE

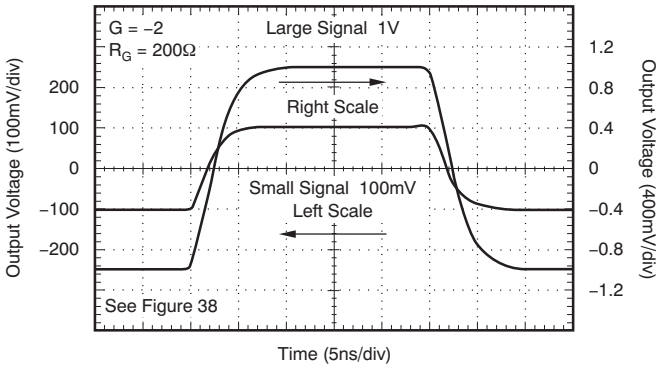


Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

5MHz HARMONIC DISTORTION vs LOAD RESISTANCE

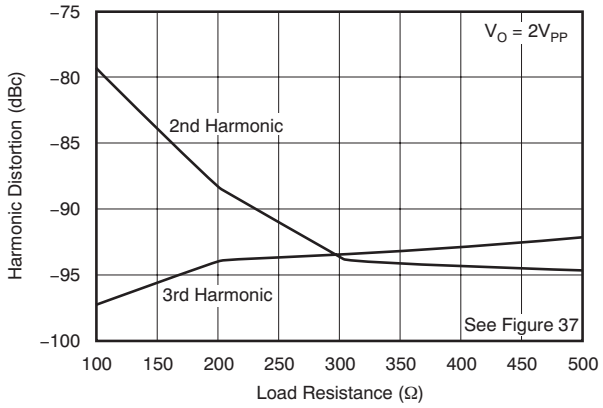


Figure 7.

1MHz HARMONIC DISTORTION vs LOAD RESISTANCE

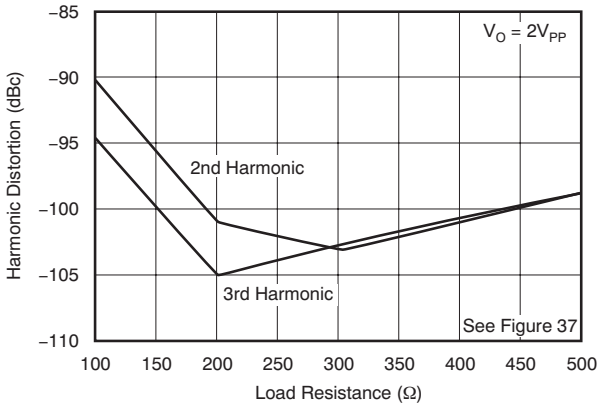


Figure 8.

HARMONIC DISTORTION vs FREQUENCY

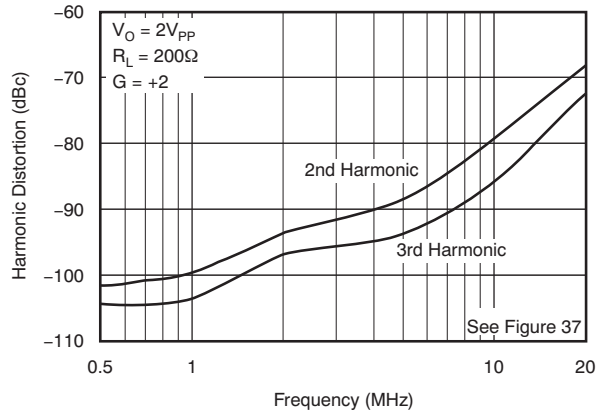


Figure 9.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

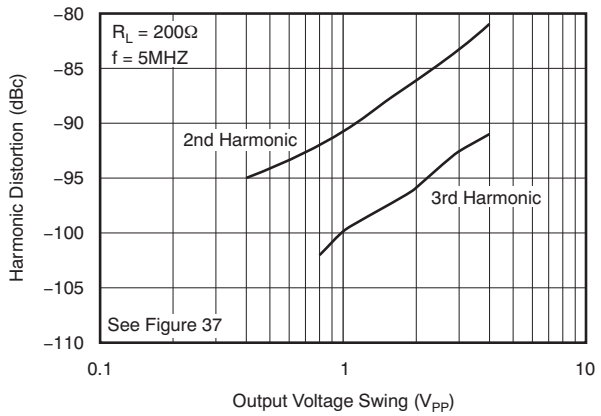


Figure 10.

HARMONIC DISTORTION vs NONINVERTING GAIN

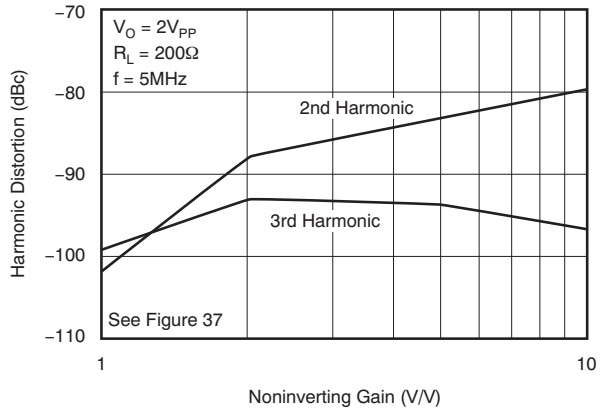


Figure 11.

HARMONIC DISTORTION vs INVERTING GAIN

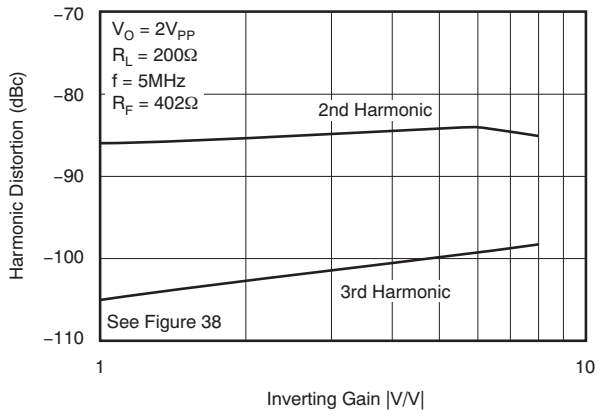


Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

INPUT VOLTAGE AND CURRENT NOISE

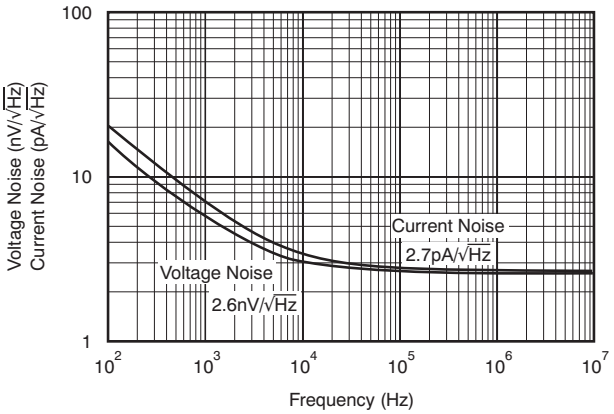


Figure 13.

TWO−TONE, THIRD−ORDER INTERMODULATION INTERCEPT

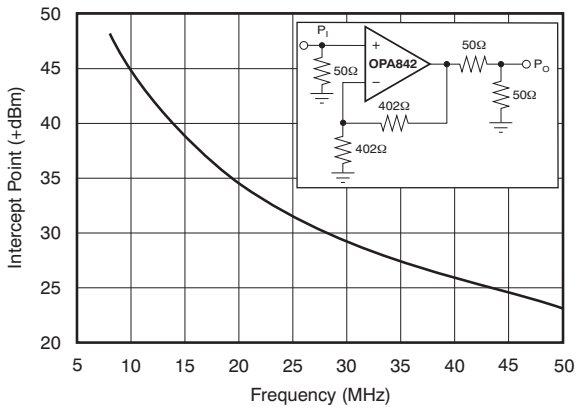


Figure 14.

RECOMMENDED R_S vs CAPACITIVE LOAD

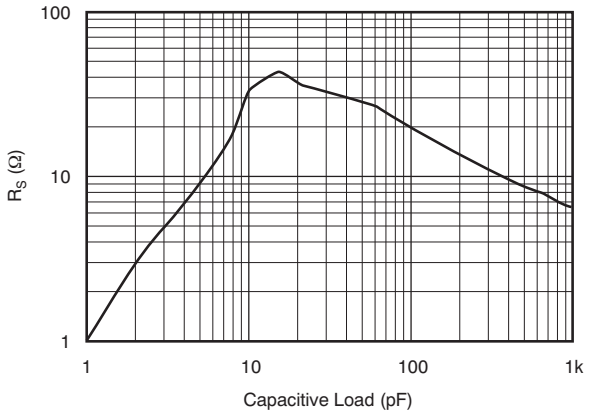


Figure 15.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

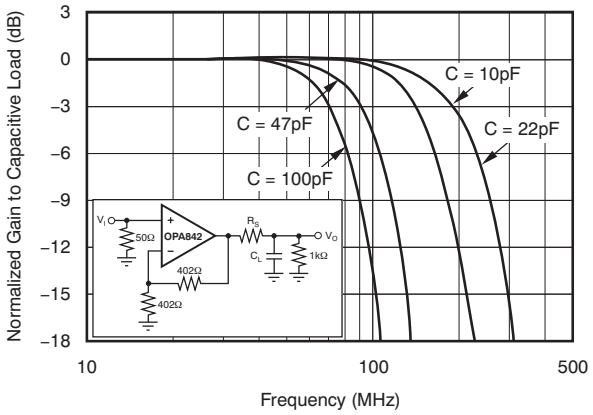


Figure 16.

GAIN = +1 FLATNESS

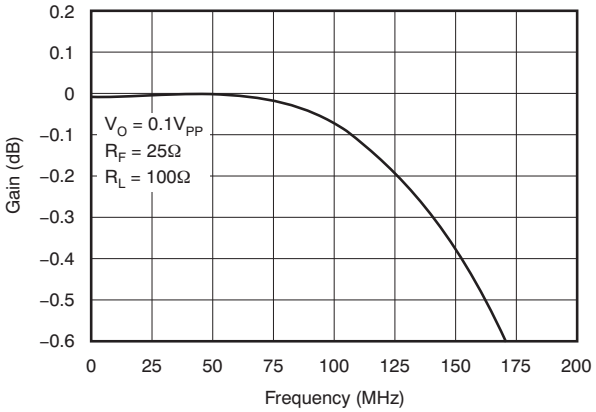


Figure 17.

PULSE RESPONSE G = +1

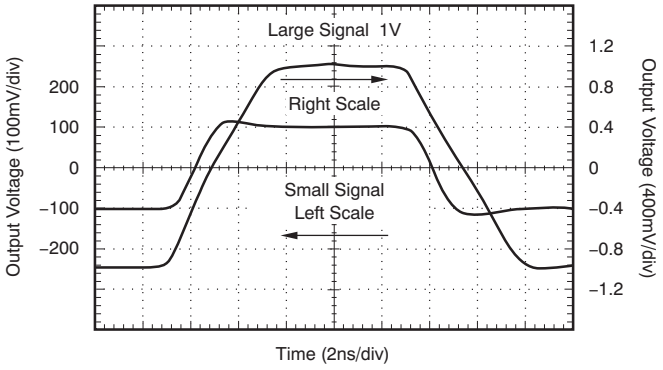


Figure 18.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

COMMON−MODE REJECTION RATIO AND POWER−SUPPLY REJECTION RATIO vs FREQUENCY

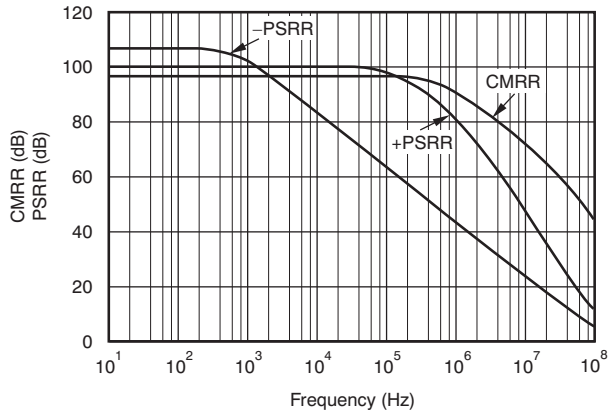


Figure 19.

OPEN−LOOP GAIN AND PHASE

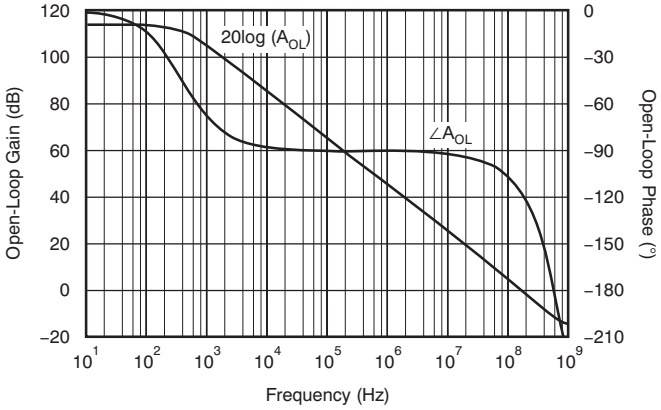


Figure 20.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

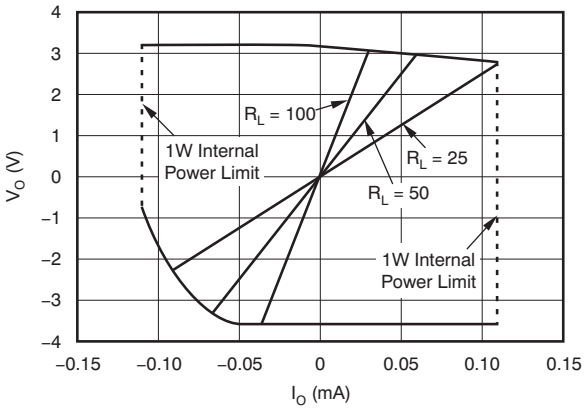


Figure 21.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

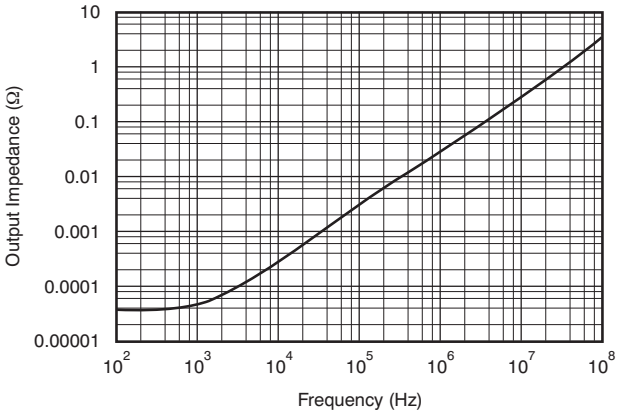


Figure 22.

NONINVERTING OVERDRIVE RECOVERY

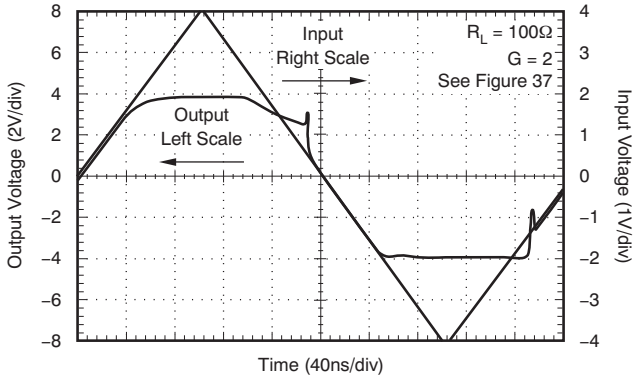


Figure 23.

INVERTING OVERDRIVE RECOVERY

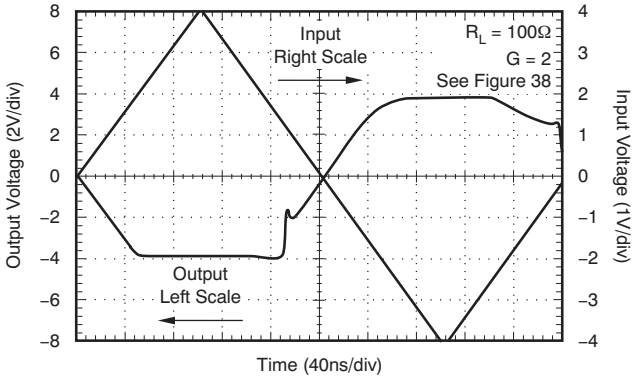


Figure 24.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

SETTLING TIME

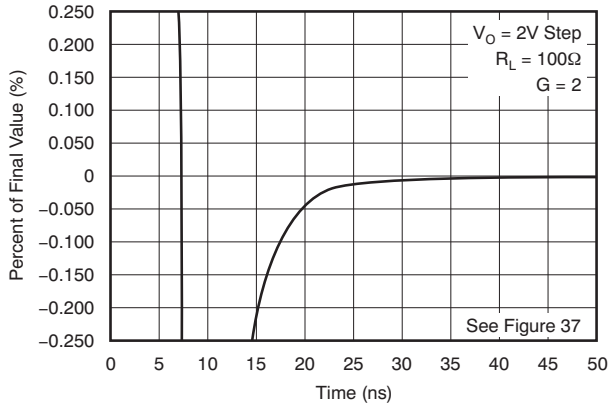


Figure 25.

VIDEO DIFFERENTIAL GAIN/DIFFERENTIAL PHASE

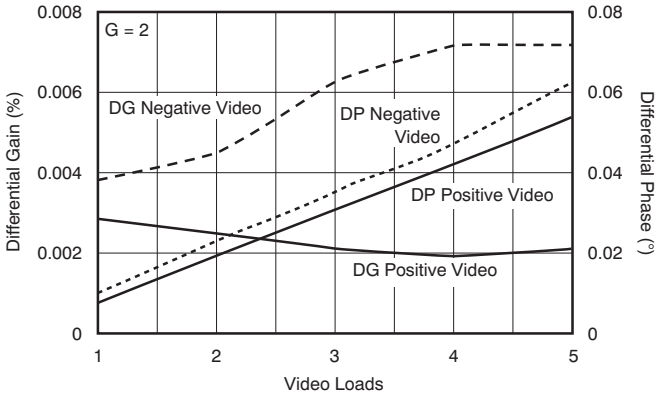


Figure 26.

TYPICAL DC DRIFT OVER TEMPERATURE

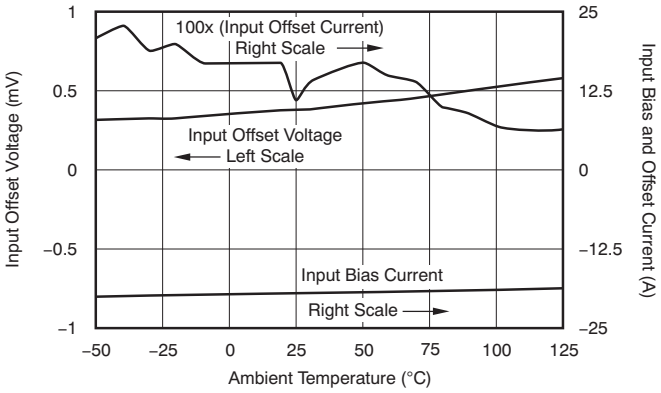


Figure 27.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

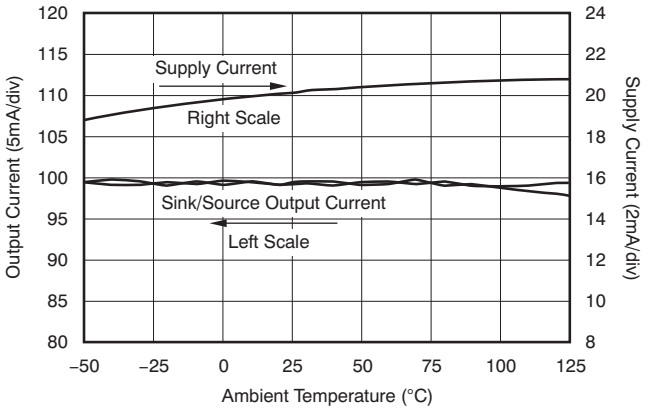


Figure 28.

COMMON-MODE INPUT RANGE AND OUTPUT SWING vs SUPPLY VOLTAGE

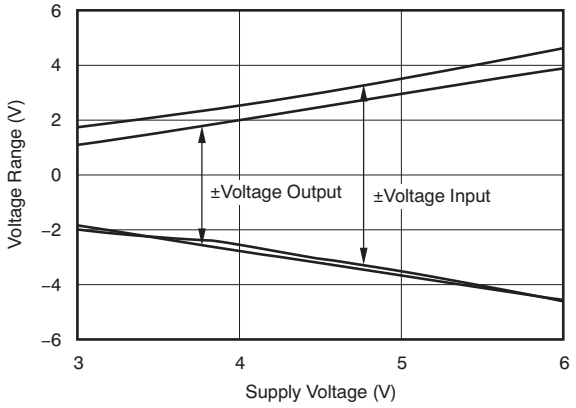


Figure 29.

COMMON-MODE AND DIFFERENTIAL INPUT IMPEDANCE

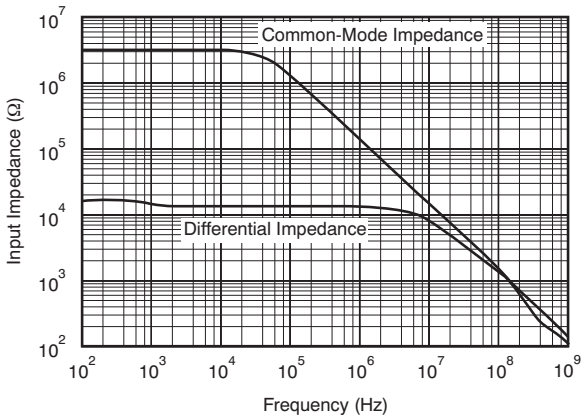


Figure 30.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

DIFFERENTIAL PERFORMANCE TEST CIRCUIT

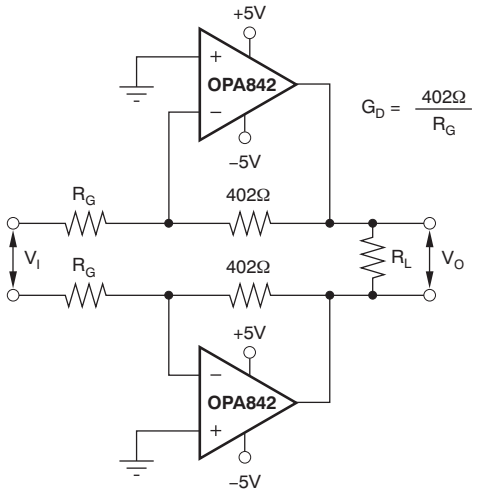


Figure 31.

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

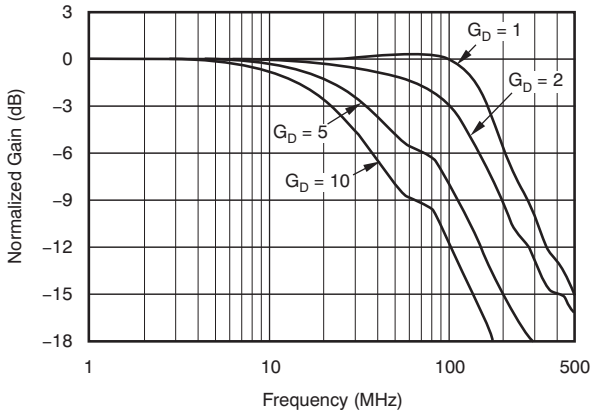


Figure 32.

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

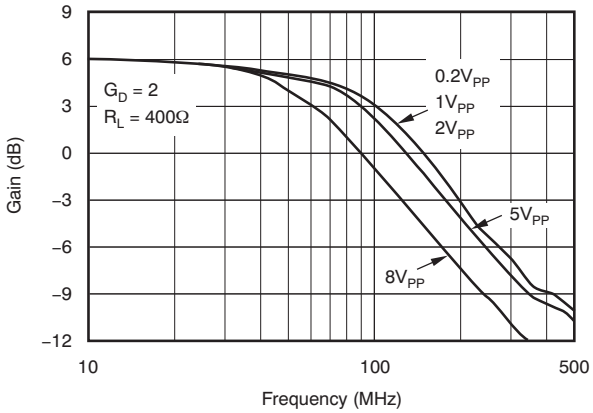


Figure 33.

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

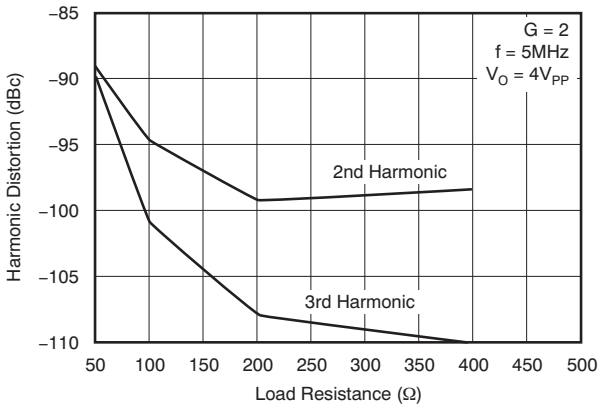


Figure 34.

DIFFERENTIAL DISTORTION vs FREQUENCY

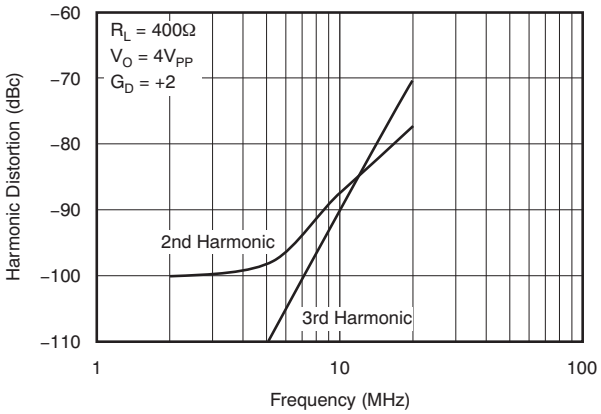


Figure 35.

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

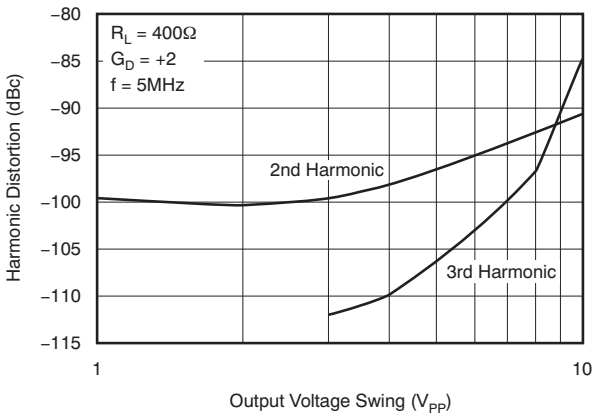


Figure 36.

APPLICATION INFORMATION

WIDEBAND CURRENT FEEDBACK OPERATION

The OPA842 combination of speed and dynamic range is easily achieved in a wide variety of application circuits, providing that simple principles of good design practice are observed. For example, good power-supply decoupling, as shown in Figure 37, is essential to achieve the lowest possible harmonic distortion and smooth frequency response.

Proper printed circuit board (PCB) layout and careful component selection will maximize the performance of the OPA842 in all applications, as discussed in the following sections of this data sheet.

Figure 37 shows the gain of +2 configuration used as the basis for most of the Typical Characteristics. Most of the curves were characterized using signal sources with 50Ω driving impedance and with measurement equipment presenting 50Ω load impedance. In Figure 37, the 50Ω shunt resistor at the V_I terminal matches the source impedance of the test generator while the 50Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet specifications refer to the voltage swing at the output pin (V_O in Figure 37). The 100Ω load, combined with the 804Ω total feedback network load, presents the OPA842 with an effective load of approximately 90Ω in Figure 37.

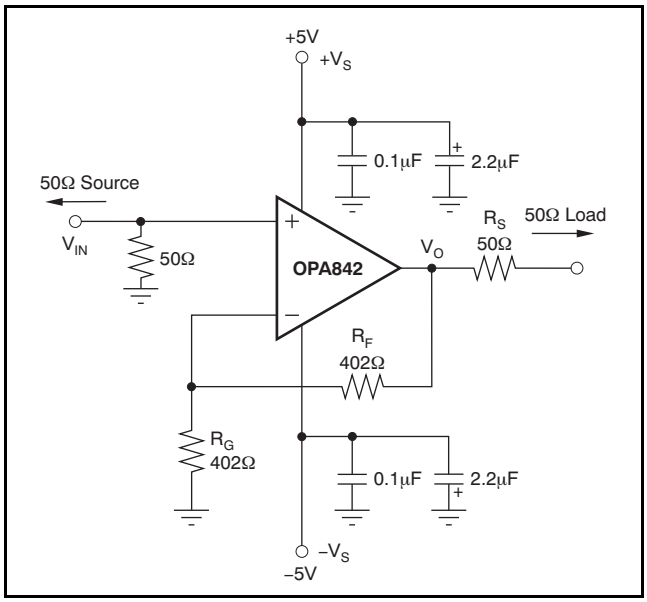


Figure 37. Gain of +2, High-Frequency Application and Characterization Circuit

WIDEBAND INVERTING OPERATION

Operating the OPA842 as an inverting amplifier has several benefits and is particularly useful when a matched 50Ω source and input impedance is required. Figure 38 shows the inverting gain of –2 circuit used as the basis of the inverting mode Typical Characteristics.

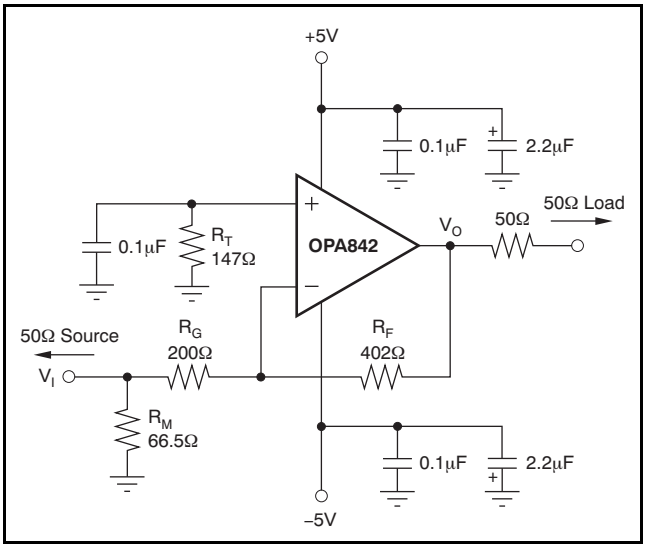


Figure 38. Inverting G = –2 Specifications and Test Circuit

In the inverting case, just the feedback resistor appears as part of the total output load in parallel with the actual load. For the 100Ω load used in the Typical Characteristics, this gives a total load of 80Ω in this inverting configuration. The gain resistor is set to get the desired gain (in this case, 200Ω for a gain of –2) while an additional input matching resistor (R_M) can be used to set the total input impedance equal to the source if desired. In this case, R_M = 66.5Ω in parallel with the 200Ω gain setting resistor gives a matched input impedance of 50Ω. This matching is only needed when the input needs to be matched to a source impedance, as in the characterization testing done using the circuit of Figure 38. The OPA842 offers extremely good dc accuracy as well as low noise and distortion. To take full advantage of that dc precision, the total dc impedance looking out of each of the input nodes must be matched to get bias current cancellation. For the circuit of Figure 38, this requires the 147Ω resistor shown to ground on the noninverting input. The calculation for this resistor includes a dc-coupled 50Ω source impedance along

with R_G and R_M. Although this resistor will provide cancellation for the bias current, it must be well-decoupled (0.1μF in Figure 38) to filter the noise contribution of the resistor and the input current noise.

As the required R_G resistor approaches 50Ω at higher gains, the bandwidth for the circuit in Figure 38 will far exceed the bandwidth at that same gain magnitude for the noninverting circuit of Figure 37. This occurs due to the lower noise gain for the circuit of Figure 38 when the 50Ω source impedance is included in the analysis. For instance, at a signal gain of –8 (R_G = 50Ω, R_M = open, R_F = 402Ω) the noise gain for the circuit of Figure 38 will be 1 + 402Ω/(50Ω + 50Ω) = 5 due to the addition of the 50Ω source in the noise gain equation. This gives considerable higher bandwidth than the noninverting gain of +8. Using the 200MHz gain bandwidth product for the OPA842, an inverting gain of –8 from a 50Ω source to a 50Ω R_G will give approximately 40MHz bandwidth, whereas the noninverting gain of +8 will give 25MHz.

BUFFERING HIGH-PERFORMANCE ADCs

To achieve full performance from a high dynamic range ADC, considerable care must be exercised in the design of the input amplifier interface circuit. The example circuit on the front page shows a typical ac-coupled interface to a very high dynamic range converter. This ac-coupled example allows the OPA842 to be operated using a signal range that swings symmetrically around ground (0V). The $2V_{PP}$ swing is then level-shifted through the blocking capacitor to a midscale reference level, which is created by a well-decoupled resistive divider off the converter internal reference voltages. To have a negligible effect on the rated spurious-free dynamic range (SFDR) of the converter, the amplifier SFDR should be at least 10dB greater than the converter. The OPA842 has no effect on the rated distortion of the ADS850, given its 82dB SFDR at $2V_{PP}$, 5MHz. The greater than 92dB SFDR for the OPA842 in this configuration will not degrade the converter.

Successful application of the OPA842 for ADC driving requires careful selection of the series resistor at the amplifier output, along with the additional shunt capacitor at the ADC input. To some extent, selection of this RC network will be determined empirically for each model of the converter. Many high-performance CMOS ADCs, like the ADS850, perform better with the shunt capacitor at the input pin. This capacitor provides low source impedance for the transient currents produced by the sampling process. Improved SFDR is often obtained by adding this external capacitor, whose value is often recommended in this converter data sheet. The external capacitor, in combination with the built-in capacitance of the ADC input, presents a significant capacitive load to the OPA842. Without a series isolation resistor, an undesirable peaking or loss of stability in the amplifier may result.

Since the dc bias current of the CMOS ADC input is negligible, the resistor has no effect on overall gain or offset accuracy. Refer to the Typical Characteristic graph, *R_S vs Capacitive Load* (Figure 15) to obtain a good starting value for the series resistor. This will ensure flat frequency response to the ADC input. Increasing the external capacitor value will allow the series resistor to be reduced. Intentionally bandlimiting using this RC network can also be used to limit noise at the converter input.

VIDEO LINE DRIVING

Most video distribution systems are designed with 75Ω series resistors to drive a matched 75Ω cable. In order to deliver a net gain of 1 to the 75Ω matched load, the amplifier is typically set up for a voltage gain of +2, compensating for the 6dB attenuation of the voltage divider formed by the series and shunt 75Ω resistors at either end of the cable.

The circuit of Figure 37 applies to this requirement if all references to 50Ω resistors are replaced by 75Ω values. Often, the amplifier gain is further increased to 2.2, which recovers the additional dc loss of a typical long cable run. This change would require the gain resistor (R_G) in Figure 37 to be reduced from 402Ω to 335Ω. In either case, both the gain flatness and the differential gain/phase performance of the OPA842 will provide exceptional results in video distribution applications. Differential gain and phase measure the change in overall small-signal gain and phase for the color sub-carrier frequency (3.58MHz in NTSC systems) versus changes in the large-signal output level (which represents luminance information in a composite video signal). The OPA842, with the typical 150Ω load of a single matched video cable, shows less than 0.01%/0.01° differential gain/phase errors over the standard luminance range for a positive video (negative sync) signal. Similar performance would be observed for negative video signals.

SINGLE OP AMP DIFFERENTIAL AMPLIFIER

The voltage-feedback architecture of the OPA842, with its high Common-Mode Rejection Ratio (CMRR), will provide exceptional performance in differential amplifier configurations. Figure 39 shows a typical configuration. The starting point for this design is the selection of the R_F value in the range of 200Ω to 2kΩ. Lower values reduce the required R_G, increasing the load on the V_2 source and on the OPA842 output. Higher values increase output noise and exacerbate the effects of parasitic board and device capacitances. Following the selection of R_F, R_G must be set to achieve the desired inverting gain for V_2. Remember that the bandwidth will be set approximately by the Gain Bandwidth Product (GBP) divided by the noise gain ($1 + R_F/R_G$). For accurate differential operation (that is, good CMRR), the ratio R_2/R_1 must be set equal to R_F/R_G.

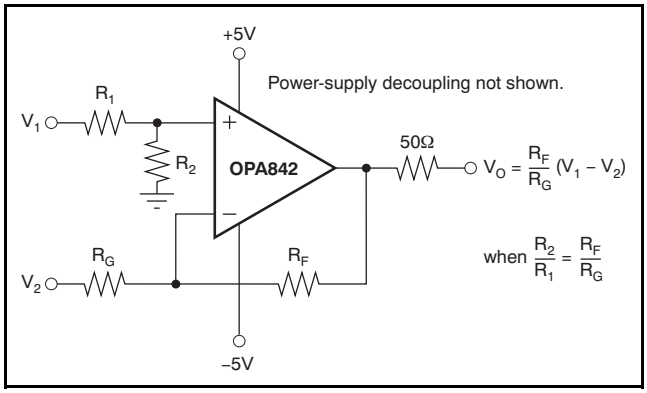


Figure 39. High-Speed, Single Differential Amplifier

Usually, it is best to set the absolute values of R_2 and R_1 equal to R_F and R_G, respectively; this equalizes the divider resistances and cancels the effect of input bias currents. However, it is sometimes useful to scale the values of R_2 and R_1 in order to adjust the loading on the driving source V_1. In most cases, the achievable low-frequency CMRR will be limited by the accuracy of the resistor values. The 85dB CMRR of the OPA842 itself will not determine the overall circuit CMRR unless the resistor ratios are matched to better than 0.003%. If it is necessary to trim the CMRR, then R_2 is the suggested adjustment point.

THREE OP AMP DIFFERENCING (Instrumentation Topology)

The primary drawback of the single op amp differential amplifier is its relatively low input impedance. Where high impedance is required at the differential input, a standard instrumentation amplifier (INA) topology may be built using the OPA842 as the differencing stage. Figure 40 shows an example of this, in which the two input amplifiers are packaged together as a dual voltage-feedback op amp, the OPA2822. This approach saves board space, cost, and power compared to using two additional OPA842 devices, and still achieves very good noise and distortion performance due to the moderate loading on the input amplifiers.

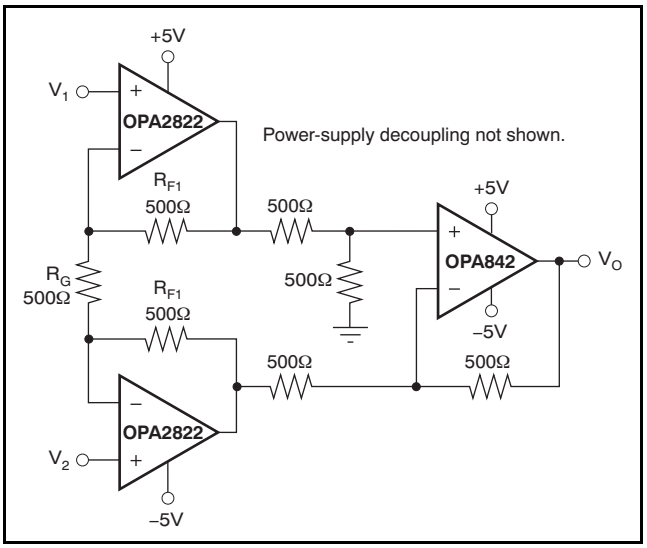


Figure 40. Wideband Three-Op Amp Differencing Amplifier

In this circuit, the common-mode gain to the output is always 1, due to the four matched 500Ω resistors, whereas the differential gain is set by ($1 + 2R_{F1}/R_G$), which is equal to 2 using the values in Figure 40. The differential to single-ended conversion is still performed by the OPA842 output stage. The high-impedance inputs allow the V_1 and V_2 sources to be terminated or impedance matched as required. If the V_1 and V_2 inputs are already truly differential, such as the output from a signal transformer, then a single matching termination resistor may be used between them. Remember, however, that a defined dc signal path must always exist for the V_1 and V_2 inputs; for the transformer case, a center-tapped secondary connected to ground would provide an optimum dc operating point.

DAC TRANSIMPEDANCE AMPLIFIER

High-frequency digital-to-analog converters (DACs) require a low-distortion output amplifier to retain the SFDR performance into real-world loads. A single-ended output drive implementation is shown in Figure 41. In this circuit, only one side of the complementary output drive signal is used. The diagram shows the signal output current connected into the virtual ground-summing junction of the OPA842, which is set up as a transimpedance stage or I-V converter. The unused current output of the DAC is connected to ground. If the DAC requires its outputs terminated to a compliance voltage other than ground for operation, then the appropriate voltage level may be applied to the noninverting input of the OPA842.

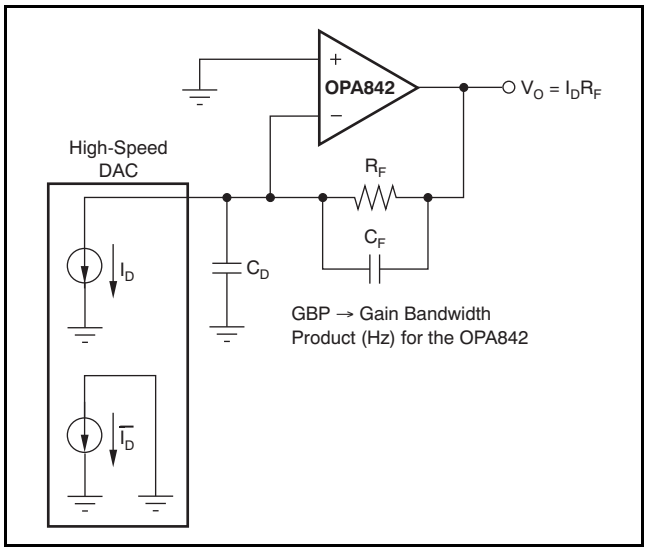


Figure 41. Wideband, Low-Distortion DAC Transimpedance Amplifier

The dc gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance will produce a zero in the noise gain for the OPA842 that may cause peaking in the closed-loop frequency response. CF is added across RF to compensate for this noise-gain peaking. To achieve a flat transimpedance frequency response, this pole in the feedback network should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (1)$$

which will give a corner frequency (f_{-3dB}) of approximately:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \quad (2)$$

ACTIVE FILTERS

Most active filter topologies will have exceptional performance using the broad bandwidth and unity-gain stability of the OPA842. Topologies employing capacitive feedback require a unity-gain stable, voltage-feedback op amp. Sallen-Key filters simply use the op amp as a noninverting gain stage inside an RC network. Either current- or voltage-feedback op amps may be used in Sallen-Key implementations.

See Figure 42 for an example Sallen-Key low-pass filter, in which the OPA842 is set up to deliver a low-frequency gain of +2. The filter component values have been selected to achieve a maximally flat Butterworth response with a 5MHz, –3dB bandwidth. The resistor values have been slightly adjusted to compensate for the effects of the 150MHz bandwidth provided by the OPA842 in this configuration. This filter may be combined with the ADC driver suggestions to provide moderate (two-pole) Nyquist filtering, limiting noise, and out-of-band harmonics into the input of an ADC. This filter will deliver the exceptionally low harmonic distortion required by high SFDR ADCs such as the ADS850 (14-bit, 10MSPS, 82dB SFDR).

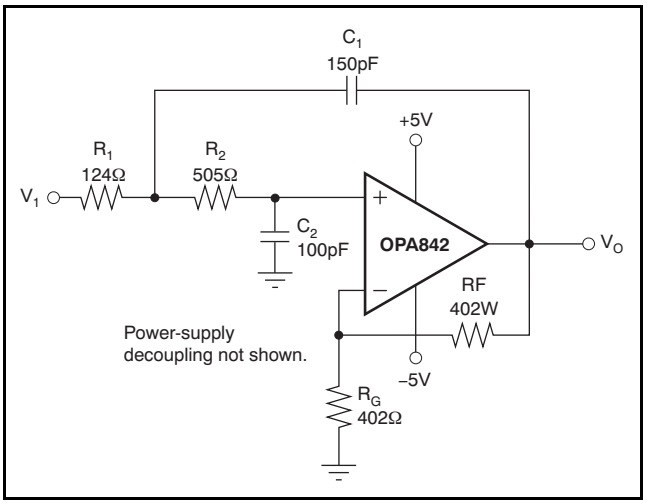


Figure 42. 5MHz Butterworth Low-Pass Active Filter

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA842 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA842ID	SO-8	DEM-OPA-SO-1A	SBOU009
OPA842IDBV	SOT23-5	DEM-OPA-SOT-1A	SBOU010

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA842 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA842 and its circuit designs. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA842 is available through the TI web page (www.ti.com). The applications group is also available for design assistance. These models predict typical small-signal ac, transient steps, dc performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the Electrical Characteristics of the data sheet. These models do not attempt to distinguish between the package types in the small-signal ac performance.

OPERATING SUGGESTIONS

OPTIMIZING RESISTOR VALUES

Since the OPA842 is a unity-gain stable, voltage-feedback op amp, a wide range of resistor values may be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a noninverting unity-gain follower application, the feedback connection should be made with a 25Ω resistor—not a direct short. This will isolate the inverting input capacitance from the output pin and improve the frequency response flatness. Usually, the feedback resistor value should be between 200Ω and 1kΩ. Below 200Ω, the feedback network will present additional output loading which can degrade the harmonic distortion performance of the OPA842. Above 1kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor may cause unintentional band limiting in the amplifier response.

A good rule of thumb is to target the parallel combination of R_F and R_G (see Figure 37) to be less than about 200Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding $R_F \parallel R_G <$ 200Ω will keep this pole above 400MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

In the inverting configuration, an additional design consideration must be noted. R_G becomes the input resistor and therefore the load impedance to the driving source. If impedance matching is desired, R_G may be set equal to the required termination value. However, at low inverting gains, the resultant feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2 with a 50Ω input matching resistor (equal to R_G) would require a 100Ω feedback resistor, which would contribute to output loading in parallel with the external load. In such a case, it would be preferable to increase both the R_F and R_G values, and then achieve the input matching impedance with a third resistor to ground (see Figure 38). The total input impedance becomes the parallel combination of R_G and the additional shunt resistor.

BANDWIDTH vs GAIN

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the GBP shown in the specifications. Ideally, dividing GBP by the noninverting signal gain (also called the *Noise Gain*, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90 degrees, as it does in high-gain configurations. At low signal gains, most amplifiers will exhibit a more complex response with lower phase margin. The OPA842 is optimized to give a maximally flat second-order Butterworth response in a gain of 2. In this configuration, the OPA842 has approximately 60 degrees of phase margin and will show a typical –3dB bandwidth of 150MHz. When the phase margin is 60 degrees, the closed-loop bandwidth is approximately $\sqrt{2}$ greater

than the value predicted by dividing GBP by the noise gain. Increasing the gain will cause the phase margin to approach 90 degrees and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the 21MHz bandwidth shown in the Electrical Characteristics agrees with that predicted using the simple formula and the typical GBP of 200MHz.

OUTPUT DRIVE CAPABILITY

The OPA842 has been optimized to drive the demanding load of a doubly-terminated transmission line. When a 50Ω line is driven, a series 50Ω into the cable and a terminating 50Ω load at the end of the cable are used. Under these conditions, the cable impedance will appear resistive over a wide frequency range, and the total effective load on the OPA842 is 100Ω in parallel with the resistance of the feedback network. The Electrical Characteristics show a +2.8V/–3.3V swing into this load—which will then be reduced to a +1.4V/–1.65V swing at the termination resistor. The ±90mA output drive over temperature provides adequate current drive margin for this load. Higher voltage swings (and lower distortion) are achievable when driving higher impedance loads.

A single video load typically appears as a 150Ω load (using standard 75Ω cables) to the driving amplifier. The OPA842 provides adequate voltage and current drive to support up to three parallel video loads (50Ω total load) for an NTSC signal. With only one load, the OPA842 achieves an exceptionally low 0.003%/0.008° dG/dP error.

DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. A high-speed, high open-loop gain amplifier like the OPA842 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. In simple terms, the capacitive load reacts with the open-loop output resistance of the amplifier to introduce an additional pole into the loop and thereby decrease the phase margin. This issue has become a popular topic of application notes and articles, and several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S *vs Capacitive Load* (see Figure 15) and the resulting frequency response at the load. The criterion for setting the recommended resistor is maximum bandwidth, flat frequency response at the load. Since there is now a passive low-pass filter between the output pin and the load capacitance, the response at the output pin itself is typically somewhat peaked, and becomes flat after the roll-off action of the RC network. This is not a concern in most applications, but can cause clipping if the desired signal swing at the load is very close to the amplifier's swing limit. Such clipping would be most likely to occur in pulse response applications where the frequency peaking is manifested as an overshoot in the step response.

Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA842. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA842 output pin (see Board Layout section).

DISTORTION PERFORMANCE

The OPA842 is capable of delivering an exceptionally low distortion signal at high frequencies and low gains. The distortion plots in the Typical Characteristics show the typical distortion under a wide variety of conditions. Most of these plots are limited to 100dB dynamic range. The OPA842 distortion does not rise above –100dBc until either the signal level exceeds 0.5V and/or the fundamental frequency exceeds 500kHz. Distortion in the audio band is ≤ –120dBc. Generally, until the fundamental signal reaches very high frequencies or powers, the second-harmonic will dominate the distortion with a negligible third-harmonic component. Focusing then on the second-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network— in the noninverting configuration this is the sum of $R_F + R_G$, whereas in the inverting configuration this is just R_F (see Figure 37). Increasing the output voltage swing increases harmonic distortion directly. Increasing the signal gain will also increase the second-harmonic distortion. Again, a 6dB increase in gain will increase the second- and third-harmonics by 6dB even with a constant output power and frequency. Finally, the distortion increases as the fundamental frequency increases due to the roll off in the loop gain with frequency. Conversely, the distortion will improve going to lower frequencies down to the dominant open-loop pole at

approximately 600Hz. Starting from the –100dBc second-harmonic for $2V_{PP}$ into 200Ω, G = +2 distortion at 1MHz (from the Typical Characteristics), the second-harmonic distortion at 20kHz should be approximately:

–100dB – 20log (1MHz/20kHz) = –134dBc

The OPA842 has an extremely low third-order harmonic distortion. This also gives an exceptionally good two-tone, third-order intermodulation intercept, as shown in the Typical Characteristics. This intercept curve is defined at the 50Ω load when driven through a 50Ω-matching resistor to allow direct comparisons to RF MMIC devices. This network attenuates the voltage swing from the output pin to the load by 6dB. If the OPA842 drives directly into the input of a high-impedance device, such as an ADC, this 6dB attenuation is not taken. Under these conditions, the intercept will increase by a minimum 6dBm. The intercept is used to predict the intermodulation spurious for two closely spaced frequencies. If the two test frequencies, f_1 and f_2, are specified in terms of average and delta frequency, $f_O = (f1 + f2)/2$ and $\Delta f = |f_2 - f_1|/2$, the two thirdorder, close-in spurious tones will appear at $f_O \pm (3 \bullet \Delta f)$. The difference between the two equal test-tone power levels and these intermodulation spurious power levels is given by $2 \bullet (IM_3 - P_O)$, where IM_3 is the intercept taken from the Typical Characteristic curve and P_O is the power level in dBm at the 50Ω load for one of the two closely-spaced test frequencies. For instance, at 10MHz, the OPA842 at a gain of +2 has an intercept of 45dBm at a matched 50Ω load. If the full envelope of the two frequencies needs to be $2V_{PP}$, this requires each tone to be 4dBm. The third-order intermodulation spurious tones will then be $2 \bullet (45 - 4) = 82$dBc below the test-tone power level (–80dBm). If this same $2V_{PP}$ two-tone envelope were delivered directly into the input of an ADC without the matching loss or loading of the 50Ω network, the intercept would increase to at least 51dBm. With the same signal and gain conditions driving directly into a light load, the spurious tones will then be at least $2 \bullet (51 - 4) = 94$dBc below the $1V_{PP}$ test-tone signal levels.

NOISE PERFORMANCE

The OPA842 complements its ultralow harmonic distortion with low input noise terms. Both the input-referred voltage noise and the two input-referred current noise terms combine to give a low output noise under a wide variety of operating conditions. Figure 43 shows the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

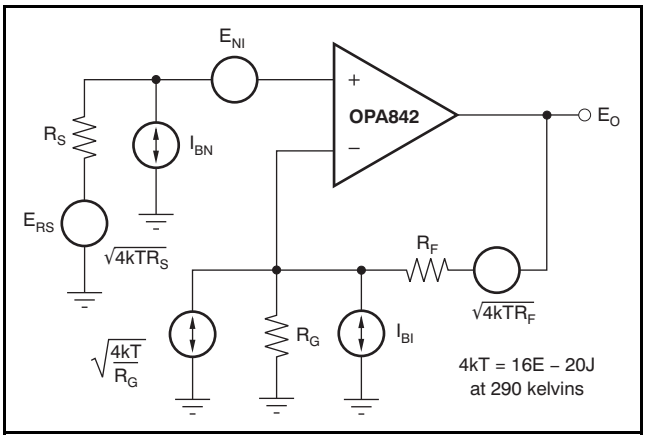


Figure 43. Op Amp Noise Analysis Model

The total output spot noise voltage is computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, then taking the square root to get back to a spot noise voltage. Equation 3 shows the general form for this output noise voltage using the terms presented in Figure 43.

$$E_O = \sqrt{\left(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right)NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (3)$$

Dividing this expression by the noise gain [$NG = (1 + R_F/R_G)$] will give the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 4.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (4)$$

Evaluating these two equations for the OPA842 circuit presented in Figure 37 will give a total output spot noise voltage of 6.6nV/√Hz and an equivalent input spot noise voltage of 3.3nV/√Hz.

Narrow band communications systems are more commonly concerned with the noise figure for the amplifier. The total input referred voltage noise expression (see Equation 4), may be used to calculate the noise figure. Equation 5 shows this noise figure expression using the NG of Equation 4 for the noninverting configuration where the input terminating resistor, R_T, has been set to match the source impedance, R_S (see Figure 37).

kT = 4E – 21J at 290 kelvins

$$NF = 10\log\left(2 + \frac{E_N^2}{kTR_S}\right) \quad (5)$$

Evaluating Equation 5 for the circuit of Figure 37 gives a noise figure = 17.6dB.

DC OFFSET CONTROL

The OPA842 can provide excellent dc signal accuracy due to its high open-loop gain, high common-mode rejection, high power-supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of this low input offset voltage, careful attention to input bias current cancellation is also required. The high-speed input stage for the OPA842 has a relatively high input bias current (20μA typ into the pins) but with a very close match between the two input currents—typically 0.35μA input offset current. The total output offset voltage may be considerably reduced by matching the source impedances looking out of the two inputs. For example, one way to add bias current cancellation to the circuit of Figure 37 would be to insert a 175Ω series resistor into the noninverting input from the 50Ω terminating resistor. When the 50Ω source resistor is dc-coupled, this will increase the source impedance for the noninverting input bias current to 200Ω. Since this is now equal to the impedance looking out of the inverting input (R_F || R_G), the circuit will cancel the gains for the bias currents to the output leaving only the offset current times the feedback resistor as a residual dc error term at the output. Using a 402Ω feedback resistor, this output error will now be less than 1μA • 402Ω = 0.4mV at +25°C.

THERMAL ANALYSIS

The OPA842 will not require heat sinking or airflow in most applications. Maximum desired junction temperature would set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. PDL will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_{S2}/(4 \bullet R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA842IDBV (SOT23-5 package) in the circuit of Figure 37 operating at the maximum specified ambient temperature of +85°C.

$P_D = 10V \bullet 22.5mA + 5^2/[4 \bullet (100\Omega \parallel 800\Omega)] = 291mW$

Maximum $T_J = +85°C + (0.29W \bullet (150°C/W) = 129°C$

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier such as the OPA842 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25in., or 0.635cm) from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA842. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wire-wound type resistors in a highfrequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values

can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values greater than 1.5kΩ, this parasitic capacitance can add a pole and/or a zero below 500MHz that can affect circuit operation. Keep resistor values as low as possible consistent with load-driving considerations. It has been suggested here that a good starting point for design would be to set $R_G \parallel R_F \leq 200\Omega$. Doing this will automatically keep the resistor noise terms low, and minimize the effect of the parasitic capacitance.

d) Connections to other wideband devices on the board may be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load* (Figure 15). Low parasitic capacitive loads (less than 5pF) may not need an R_S since the OPA842 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA842 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of *R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA842 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA842 onto the board.

INPUT AND ESD PROTECTION

The OPA842 is built using a very high speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 44.

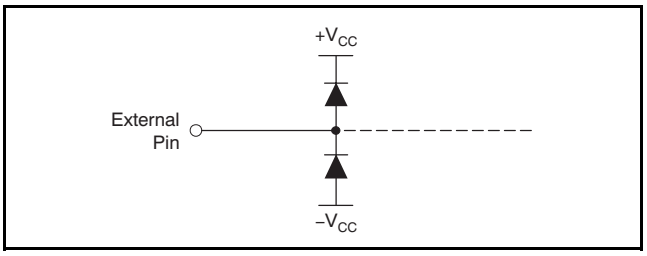


Figure 44. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA842), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response. Figure 45 shows an example protection circuit for I/O voltages that may exceed the supplies.

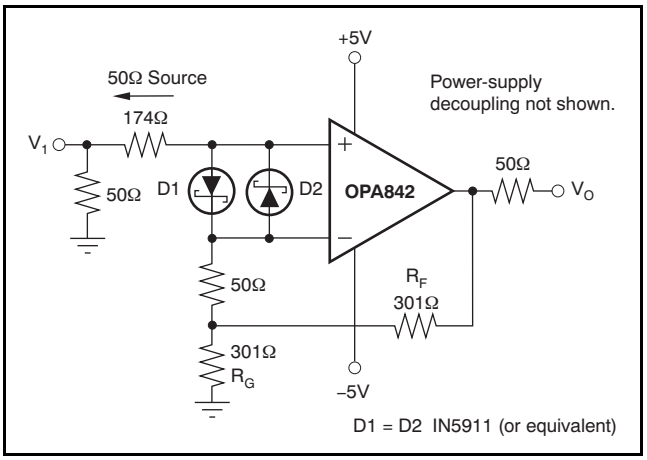


Figure 45. Gain of +2 with Input Protection

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December, 2008) to Revision D **Page**

- Updated document format to current standards 1
- Deleted *lead temperature* specifications from Absolute Maximum Ratings table 2
- Added minimum operating voltage specification to *Electrical Characteristics* table 4

Changes from Revision B (March, 2006) to Revision C **Page**

- Changed minimum storage temperature range from −40°C to −65°C 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA842ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 842	Samples
OPA842IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OAQI	Samples
OPA842IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OAQI	Samples
OPA842IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OAQI	Samples
OPA842IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OAQI	Samples
OPA842IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 842	Samples
OPA842IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 842	Samples
OPA842IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 842	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

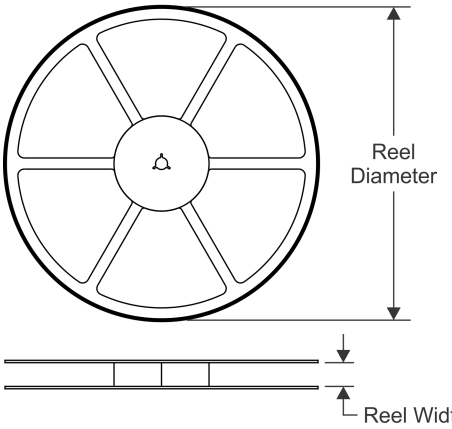
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

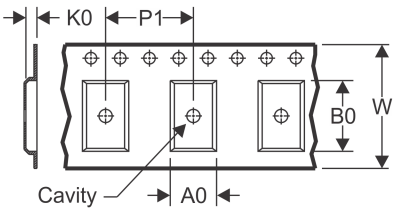
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

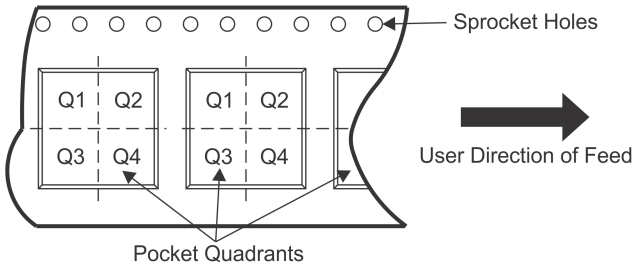


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

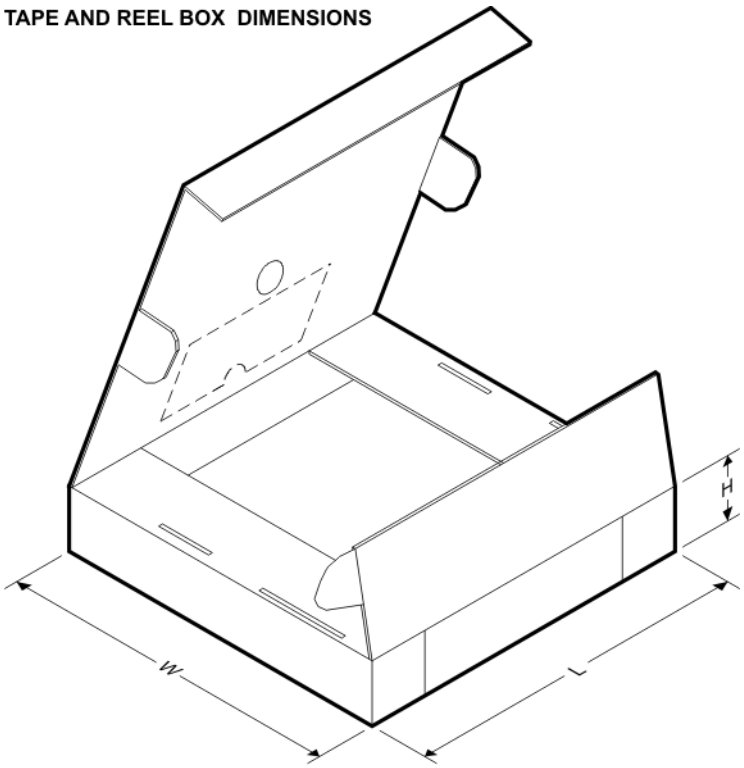
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA842IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

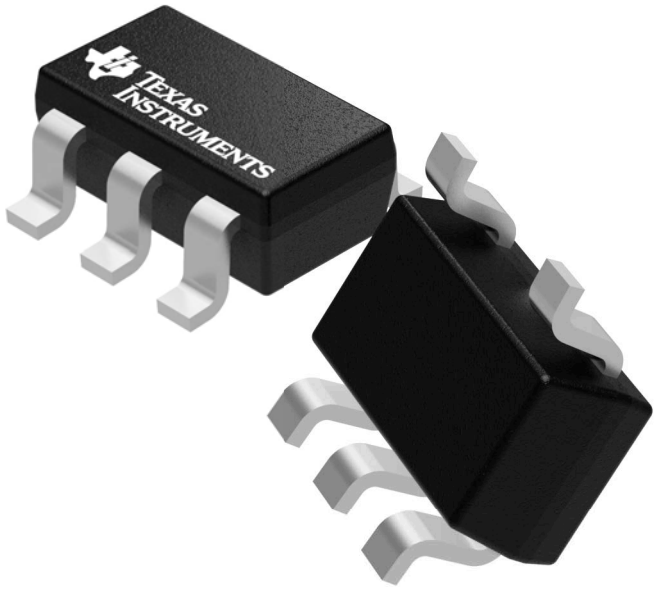


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA842IDR	SOIC	D	8	2500	367.0	367.0	35.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



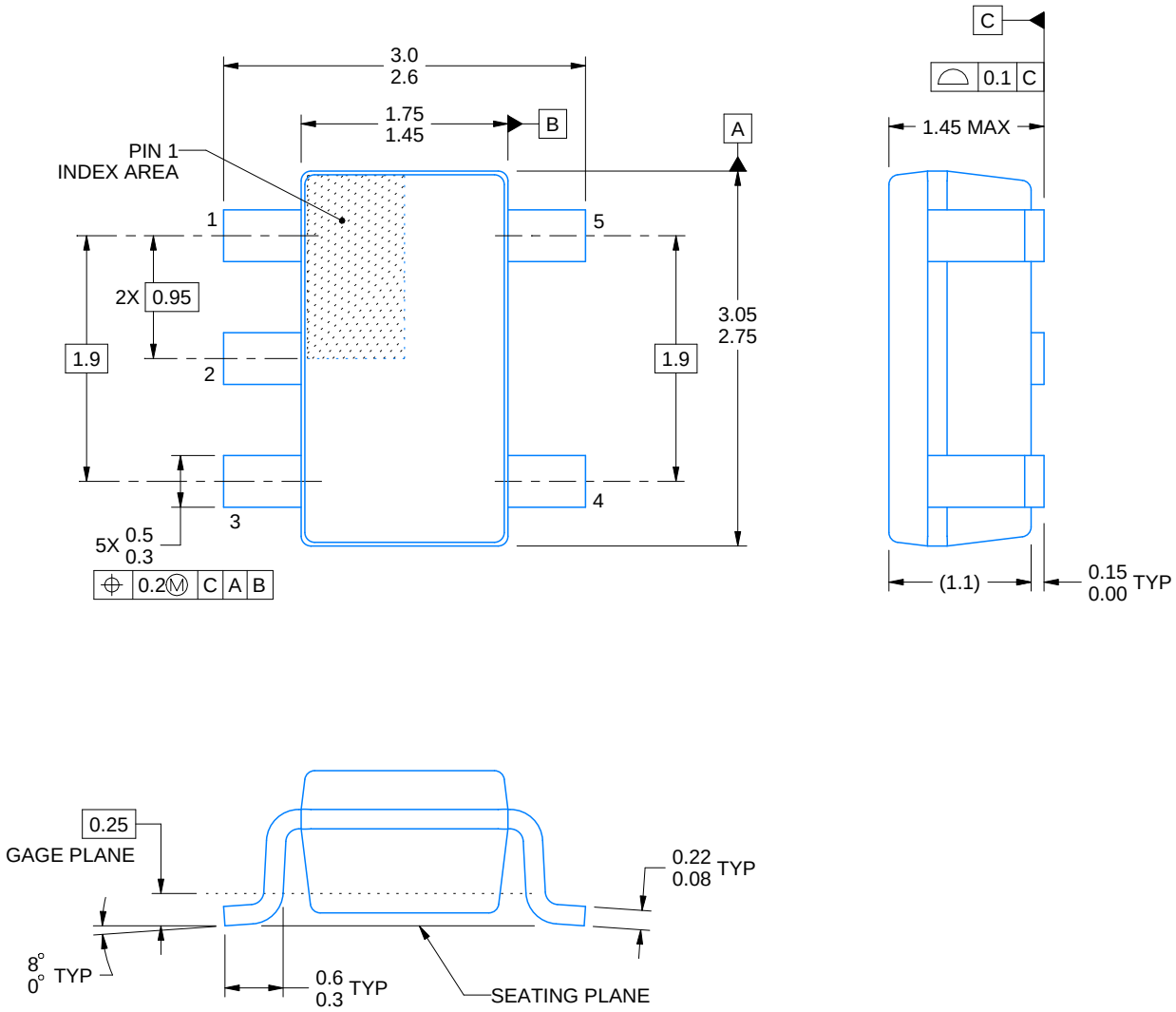
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

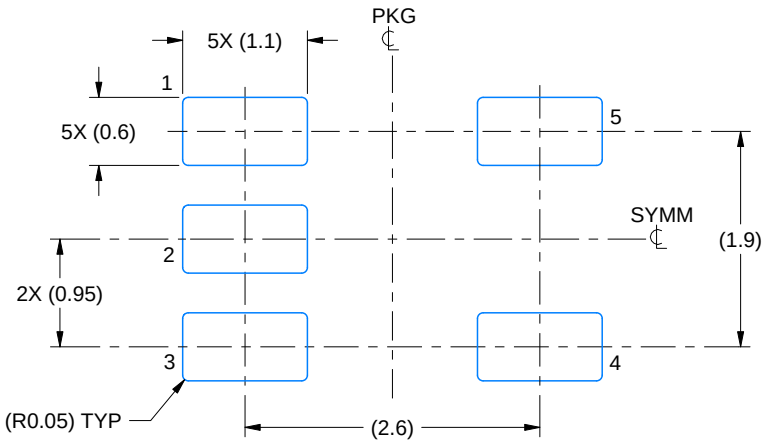
SMALL OUTLINE TRANSISTOR



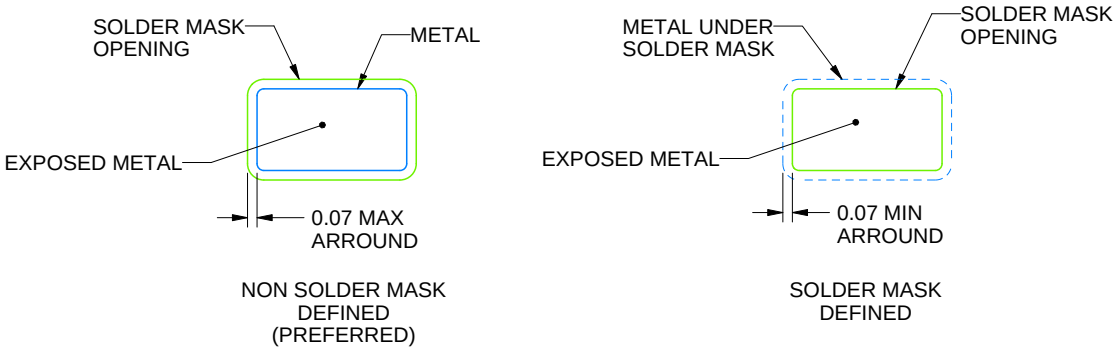
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

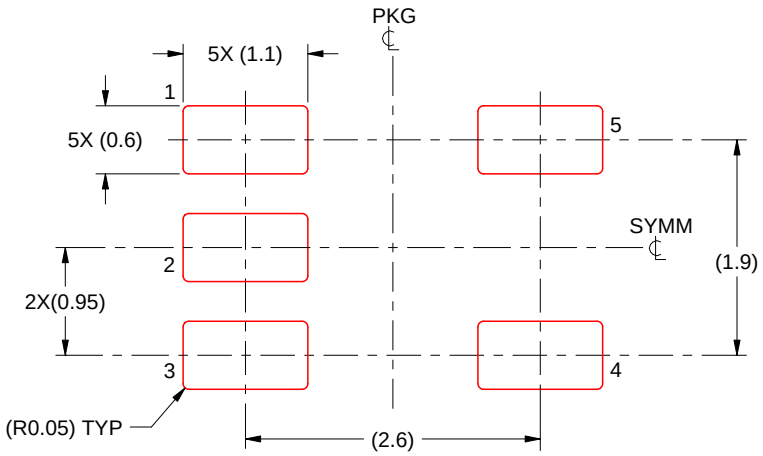


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

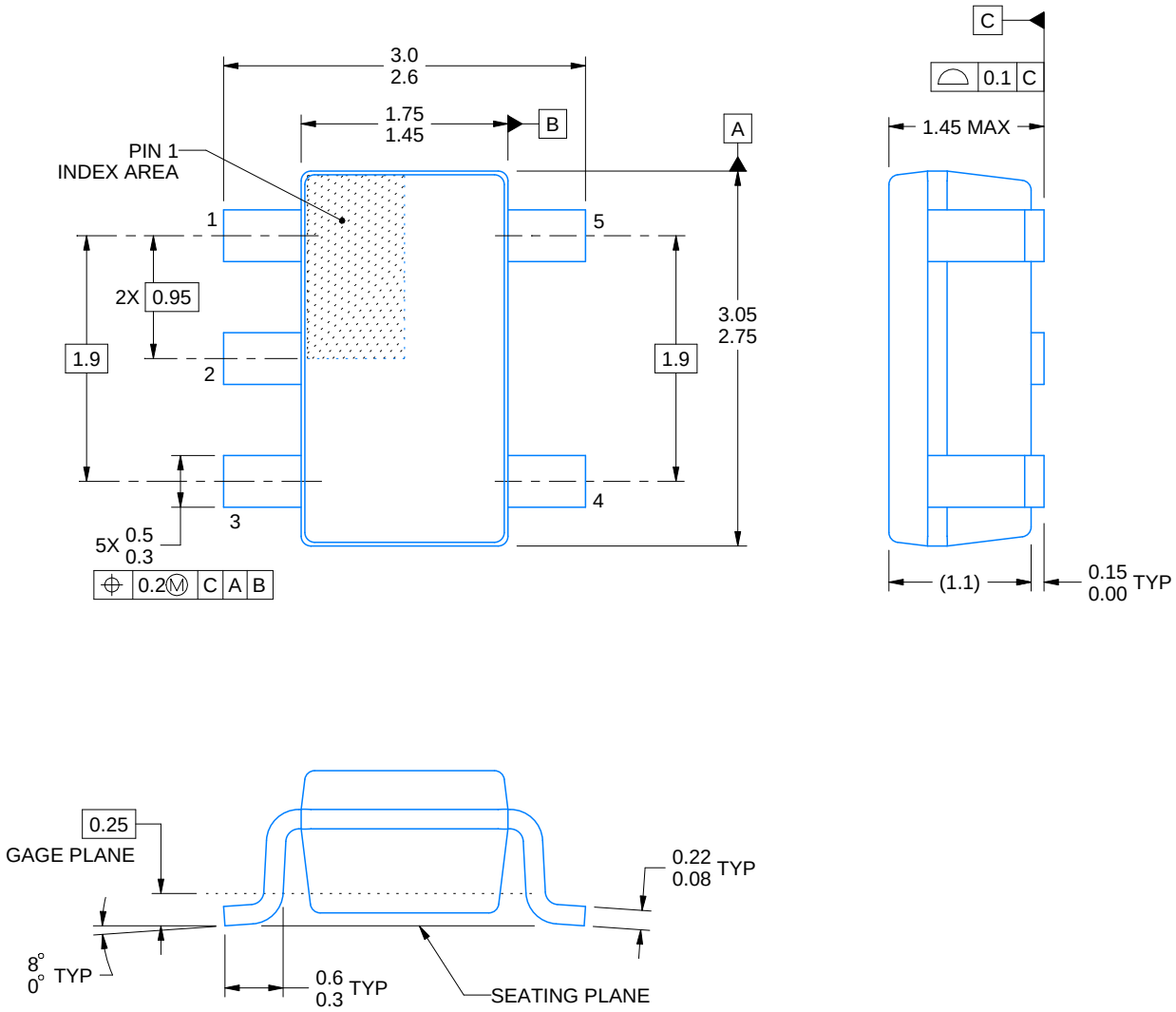
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

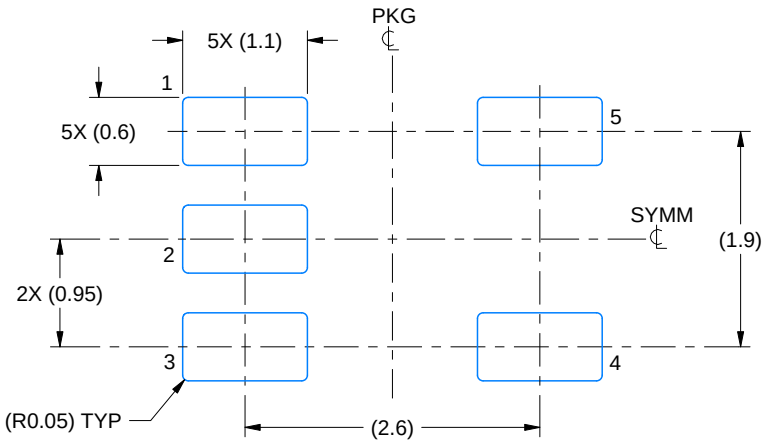
SMALL OUTLINE TRANSISTOR



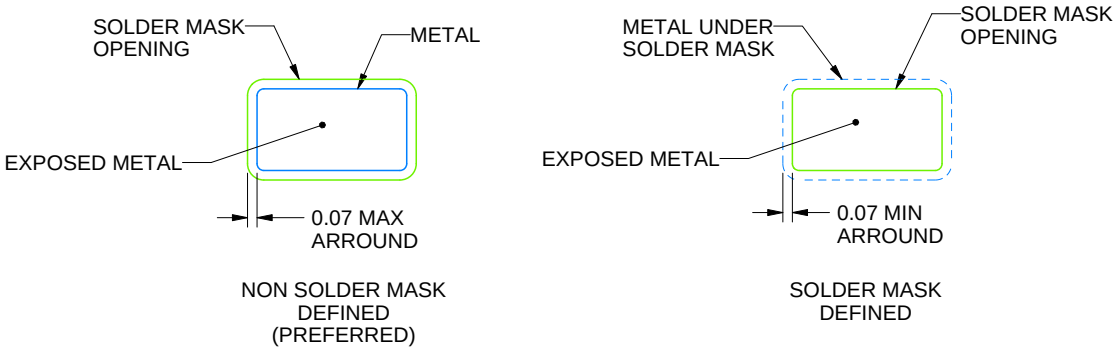
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

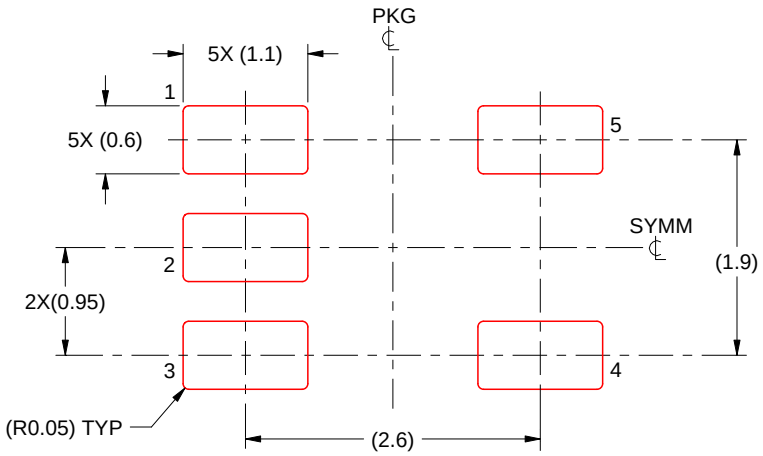


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



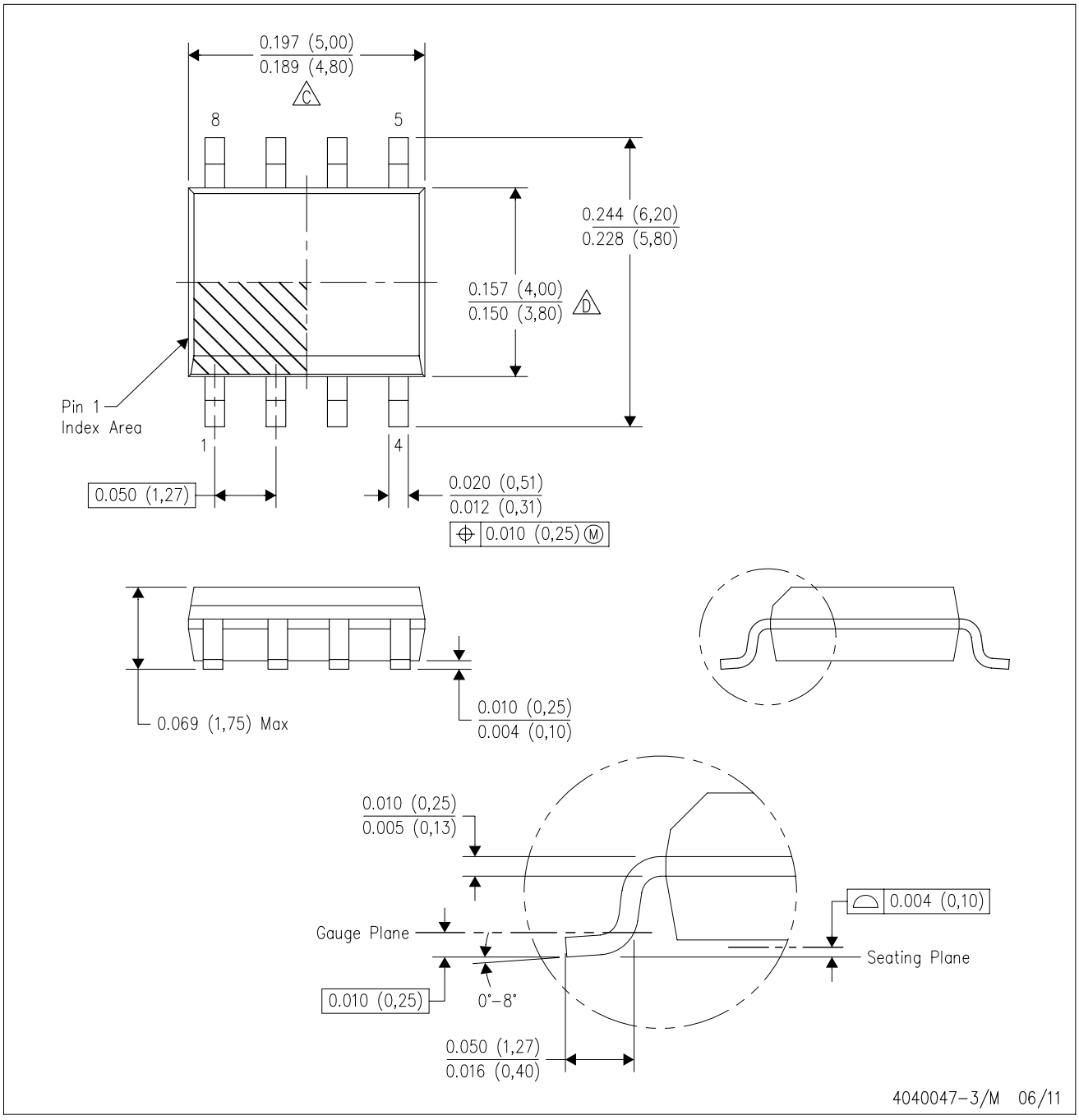
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

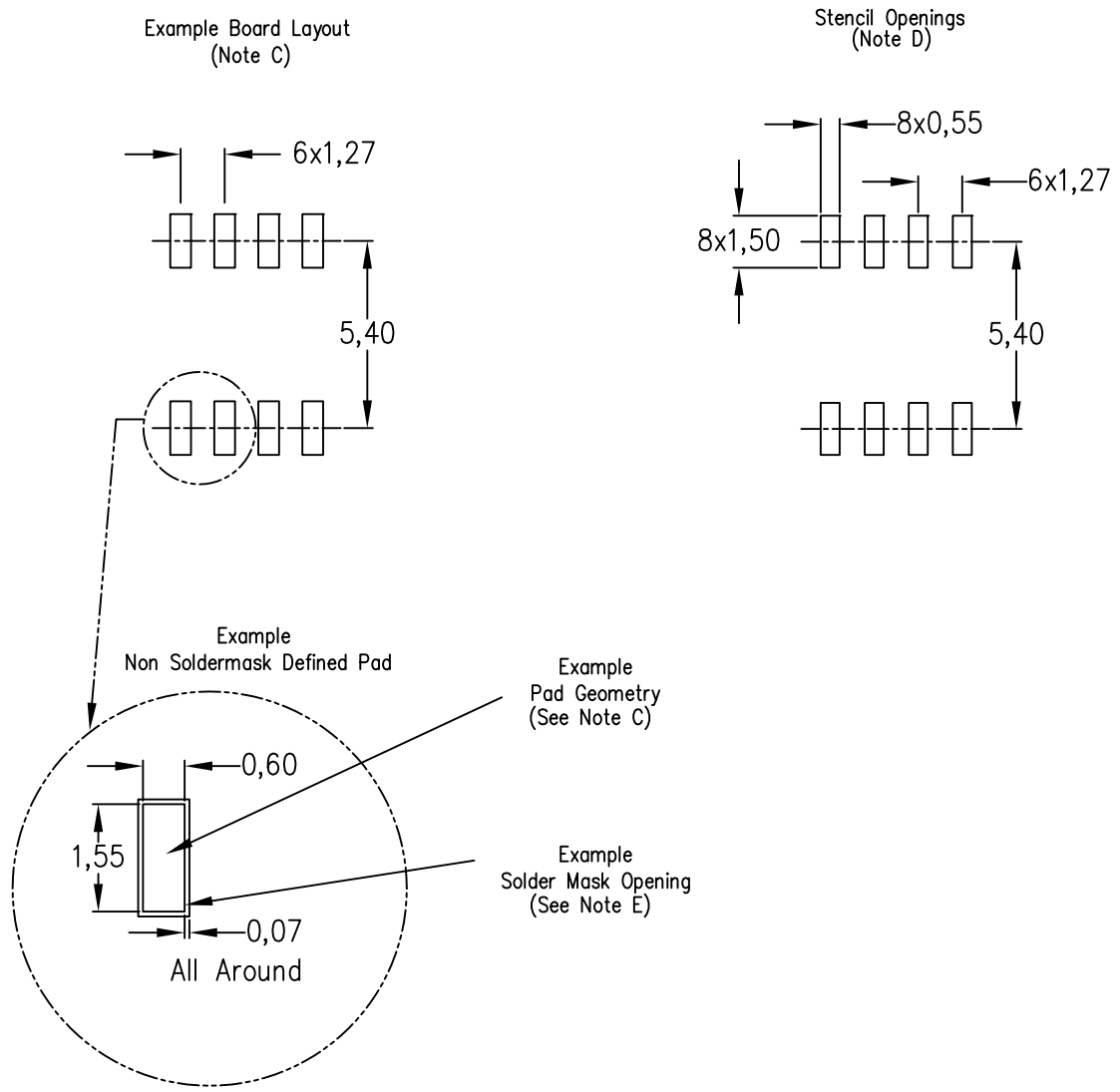
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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