National Semiconductor

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LM3671
2MHz , 600mA Step-Down DC-DC Converter in SOT23-5

General Description

The LM3671 step-down DC-DC converter is optimized for powering ultra-low voltage circuits from a single Li-Ion cell or 3 cell NiMH/NiCd batteries. It provides up to 600mA load current, over an input voltage range from 2.8V to 5.5V. There are several different fixed voltage output options available as well as an adjustable output voltage version.

The device offers superior features and performance for mobile phones and similar portable applications with complex power management systems. Automatic intelligent switching between PWM low-noise and PFM low-current mode offers improved system control. During full-power operation, a fixed-frequency 2 MHz (typ). PWM mode drives loads from ~70 mA to 600 mA max. Hysteretic PFM mode extends the battery life through reduction of the quiescent current to 16 µA (typ) at light loads and system standby. Internal synchronous rectification provides high efficiency. In shutdown mode (Enable pin pulled low) the device turns off and reduces battery consumption to 0.01 µA (typ).

The LM3671 is available in a SOT23-5 package with Pb and No Pb (Lead free) versions. A high switching frequency - 2 MHz (typ) - allows use of tiny surface-mount components. Only three external surface-mount components, an inductor and two ceramic capacitors, are required.

Features

- 16 µA typical quiescent current
- 600 mA maximum load capability
- 2 MHz PWM fixed switching frequency (typ)
- Automatic PFM/PWM mode switching
- Available in fixed output voltages and adjustable version
- SOT23-5 package
- Internal synchronous rectification for high efficiency
- Internal soft start
- 0.01 µA typical shutdown current
- Operates from a single Li-Ion cell or 3 cell NiMH/NiCd batteries
- Only three tiny surface-mount external components required (one inductor, two ceramic capacitors)
- Current overload and Thermal shutdown protection

Applications

- Mobile phones
- PDAs
- MP3 players
- W-LAN
- Portable instruments
- Digital still cameras
- Portable Hard disk drives

Typical Application Circuits

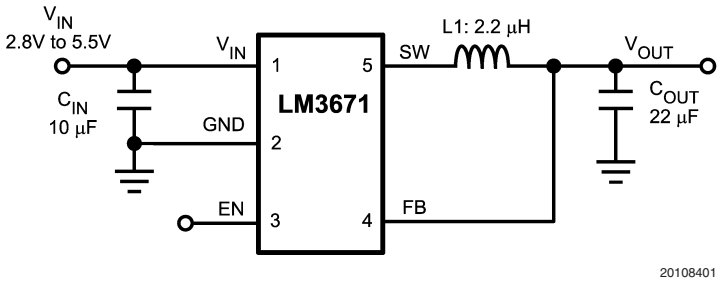


FIGURE 1. Typical Application Circuit

Typical Application Circuits (Continued)

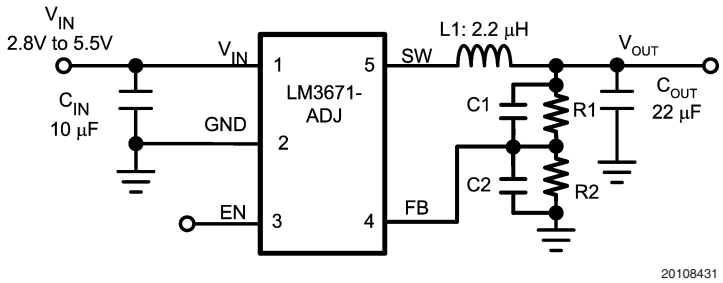
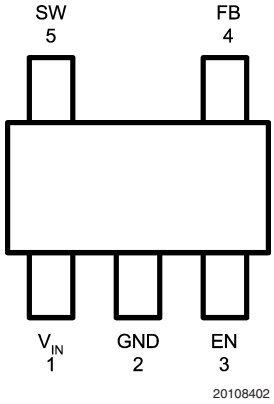


FIGURE 2. Typical Application Circuit for ADJ version

Connection Diagram and Package Mark Information

SOT23-5 Package
NS Package Number MF05A



Note: The actual physical placement of the package marking will vary from part to part.

FIGURE 3. Top View

Pin Descriptions

Pin #	Name	Description
1	V_{IN}	Power supply input. Connect to the input filter capacitor (*Figure 1*).
2	GND	Ground pin.
3	EN	Enable pin. The device is in shutdown mode when voltage to this pin is <0.4V and enabled when >1.0V. Do not leave this pin floating.
4	FB	Feedback analog input. Connect directly to the output filter capacitor for fixed voltage versions. For adjustable version external resistor dividers are required. The internal resistor dividers are disabled for the adjustable version.
5	SW	Switching node connection to the internal PFET switch and NFET synchronous rectifier.

Ordering Information

Voltage Option	Order Number	Spec	Package Marking	Supplied As
ADJ	LM3671MF-ADJ	NOPB	SBTB	1000 units, Tape-and-Reel
	LM3671MFX-ADJ	NOPB		3000 units, Tape-and-Reel
	LM3671MF-ADJ			1000 units, Tape-and-Reel
	LM3671MFX-ADJ			3000 units, Tape-and-Reel
1.2	LM3671MF-1.2	NOPB	SBPB	1000 units, Tape-and-Reel
	LM3671MFX-1.2	NOPB		3000 units, Tape-and-Reel
	LM3671MF-1.2			1000 units, Tape-and-Reel
	LM3671MFX-1.2			3000 units, Tape-and-Reel
1.25	LM3671MF-1.25	NOPB	SDRB	1000 units, Tape-and-Reel
	LM3671MFX-1.25	NOPB		3000 units, Tape-and-Reel
	LM3671MF-1.25			1000 units, Tape-and-Reel
	LM3671MFX-1.25			3000 units, Tape-and-Reel
1.375	LM3671MF-1.375	NOPB	SEDB	1000 units, Tape-and-Reel
	LM3671MFX-1.375	NOPB		3000 units, Tape-and-Reel
	LM3671MF-1.375			1000 units, Tape-and-Reel
	LM3671MFX-1.375			3000 units, Tape-and-Reel
1.5	LM3671MF-1.5	NOPB	SBRB	1000 units, Tape-and-Reel
	LM3671MFX-1.5	NOPB		3000 units, Tape-and-Reel
	LM3671MF-1.5			1000 units, Tape-and-Reel
	LM3671MFX-1.5			3000 units, Tape-and-Reel
1.6	LM3671MF-1.6	NOPB	SDUB	1000 units, Tape-and-Reel
	LM3671MFX-1.6	NOPB		3000 units, Tape-and-Reel
	LM3671MF-1.6			1000 units, Tape-and-Reel
	LM3671MFX-1.6			3000 units, Tape-and-Reel
1.8	LM3671MF-1.8	NOPB	SBSB	1000 units, Tape-and-Reel
	LM3671MFX-1.8	NOPB		3000 units, Tape-and-Reel
	LM3671MF-1.8			1000 units, Tape-and-Reel
	LM3671MFX-1.8			3000 units, Tape-and-Reel
1.875	LM3671MF-1.875	NOPB	SDVB	1000 units, Tape-and-Reel
	LM3671MFX-1.875	NOPB		3000 units, Tape-and-Reel
	LM3671MF-1.875			1000 units, Tape-and-Reel
	LM3671MFX-1.875			3000 units, Tape-and-Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN} Pin: Voltage to GND	−0.2V to 6.0V
FB, SW, EN Pin:	(GND−0.2V) to (V_{IN} + 0.2V)
Continuous Power Dissipation (Note 3)	Internally Limited
Junction Temperature (T_{J-MAX})	+125˚C
Storage Temperature Range	−65˚C to +150˚C
Maximum Lead Temperature (Soldering, 10 sec.)	260˚C
ESD Rating (Note 4)	
Human Body Model:	
V_{IN},GND,SW,FB	2.0 kV
Human Body Model: EN	500V
Machine Model: All Pins	200V

Operating Ratings (Notes 1, 2)

Input Voltage Range	2.8V to 5.5V
Recommended Load Current	0mA to 600 mA
Junction Temperature (T_J) Range	−25˚C to +125˚C
Ambient Temperature (T_A) Range (Note 5)	−25˚C to +85˚C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}) (SOT23-5) for 2 layer board (Note 6)	250˚C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (SOT23-5) for 4 layer board (Note 6)	130˚C/W

Electrical Characteristics (Notes 2, 9, 10)

Limits in standard typeface are for T_J = 25˚C. Limits in **boldface** type apply over the full operating junction temperature range (−25˚C ≤ T_J ≤ +125˚C). Unless otherwise noted, specifications apply to the LM3671 Typical Application Circuit (Figure. 1) with V_{IN} = EN = 3.6V, V_{OUT} = 1.5V

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input Voltage Range	(Note 11)	2.8		5.5	V
V_{OUT}	Output Voltage (Fixed)	I_O = 0 mA	**−2**		**+4**	%
		I_O = 100 mA	**−4**		**+4**	%
	Output Voltage (ADJ)	I_O = 0 mA	**−2**		**+4**	%
		I_O = 100 mA	**−3**		**+4**	%
	Line Regulation	2.8V ≤ V_{IN} ≤ 5.5V I_O = 10 mA		0.045		%/V
	Load Regulation	100 mA ≤ I_O ≤ 300 mA V_{IN}= 3.6V		0.0031		%/mA
V_{REF}	Internal Reference Voltage	(Note 7)		0.5		V
I_{SHDN}	Shutdown Supply Current	EN = 0V		0.01	**1**	µA
I_{Q_PFM}	DC Bias Current into V_{IN}	No load, device is not switching (FB forced higher than programmed output voltage)		16	**35**	µA
$R_{DSON\ (P)}$	Pin-Pin Resistance for PFET	V_{IN}= V_{GS}= 3.6V		380	500	mΩ
$R_{DSON\ (N)}$	Pin-Pin Resistance for NFET	V_{IN}= V_{GS}= 3.6V		250	400	mΩ
I_{LIM}	Switch Peak Current Limit	Open Loop (Note 8)	**830**	1020	**1150**	mA
V_{IH}	Logic High Input		**1.0**			V
V_{IL}	Logic Low Input				**0.4**	V
I_{EN}	Enable (EN) Input Current			0.01	**1**	µA
F_{OSC}	Internal Oscillator Frequency	PWM Mode	**1.6**	2	**2.6**	MHz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J= 150˚C (typ.) and disengages at T_J= 130˚C (typ.).

Note 4: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Note 5: In Applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX}), the maximum power dissipation of the device in the application (P_{D-MAX}) and the junction to ambient thermal resistance of the package (θ_{JA}) in the application, as given by the following equation:T_{A-MAX}= T_{J-MAX}−(θ_{JA}x P_{D-MAX}). Refer to Dissipation rating table for P_{D-MAX} values at different ambient temperatures.

Electrical Characteristics (Notes 2, 9, 10) Limits in standard typeface are for T_J = 25˚C. Limits in **boldface** type apply over the full operating junction temperature range (–25˚C ≤ T_J ≤ +125˚C). Unless otherwise noted, specifications apply to the LM3671 Typical Application Circuit (Figure. 1) with V_{IN} = EN = 3.6V, V_{OUT} = 1.5V (Continued)

Note 6: Junction to ambient thermal resistance is highly application and board layout dependent. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design. Value specified here 250 ˚C/W is based on measurement results using a 2 layer, 4" x 3", 2 oz Cu board as per JEDEC standards. The (θ_{JA}) can be as low as 130 ˚C/W if a 4 layer, 4" x 3", 2/1/1/2 oz. Cu board as per JEDEC standards is used.

Note 7: For the ADJ version the resistor dividers should be selected such that at the desired output voltage,the voltage at the FB pin is 0.5V.

Note 8: Refer to datasheet curves for closed loop data and its variation with regards to supply voltage and temperature. Electrical Characteristic table reflects open loop data (FB=0V and current drawn from SW pin ramped up until cycle by cycle current limit is activated). Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

Note 9: Min and Max limits are guaranteed by design, test or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 10: The parameters in the electrical characteristic table are tested at V_{IN}= 3.6V unless otherwise specified. For performance over the input voltage range refer to datasheet curves.

Note 11: Input voltage range for all voltage options is 2.8V to 5.5V. The voltage range recommended for ideal applications performance for the specified output voltages with 500mA or higher output current is given below:

V_{IN} = 2.8V to 4.5V for 1.0V ≤ V_{OUT} ≤ 1.7V

V_{IN} = 3.0V to 4.5V for V_{OUT} = 1.8V and 1.875V

Dissipation Rating Table

θ_{JA}	$T_A \leq$ 25˚C Power Rating	T_A= 60˚C Power Rating	T_A= 85˚C Power Rating
250˚C/W (2 layer board)	400mW	260mW	160mW
130˚C/W (4 layer board)	770mW	500mW	310mW

Block Diagram

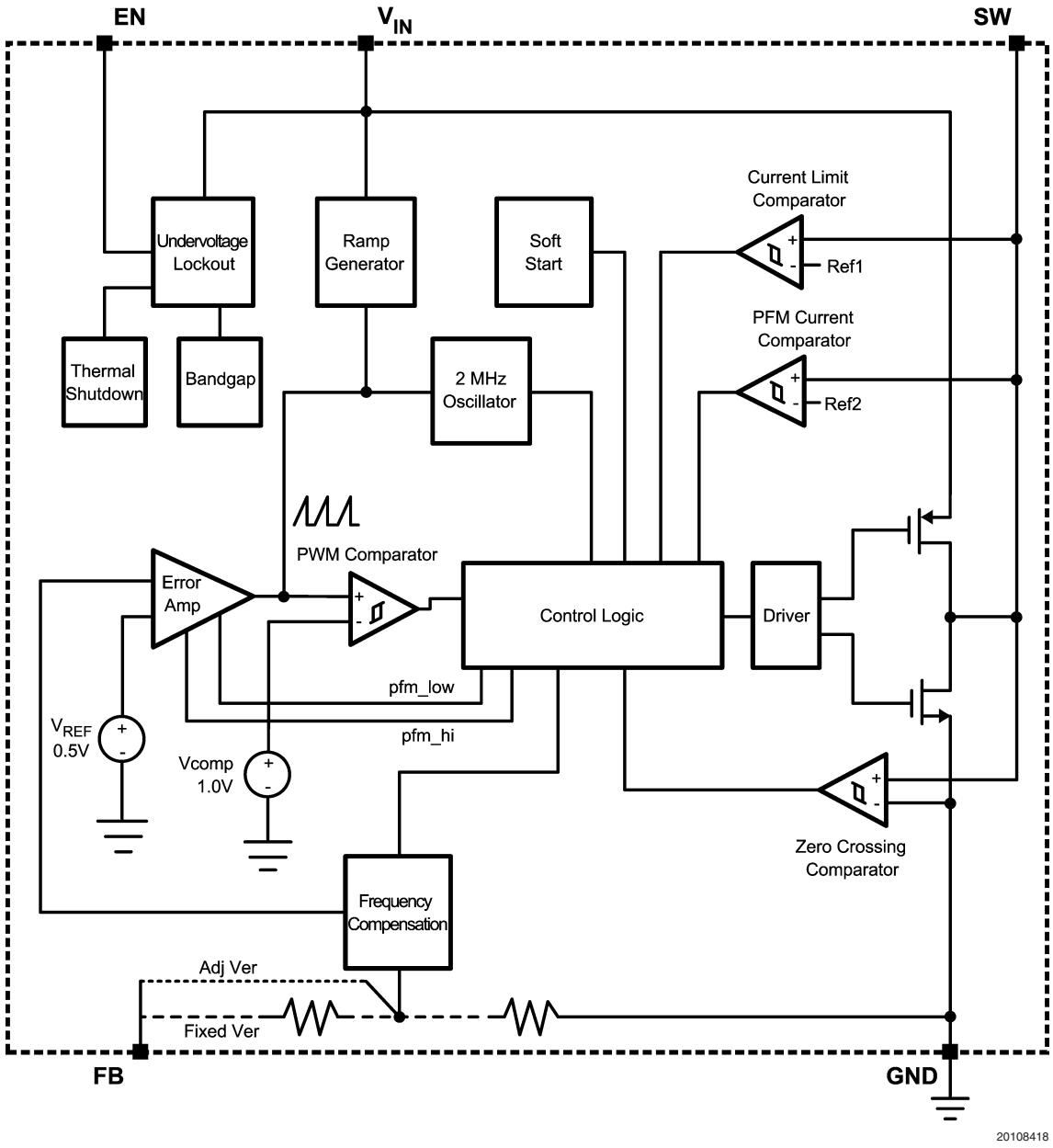
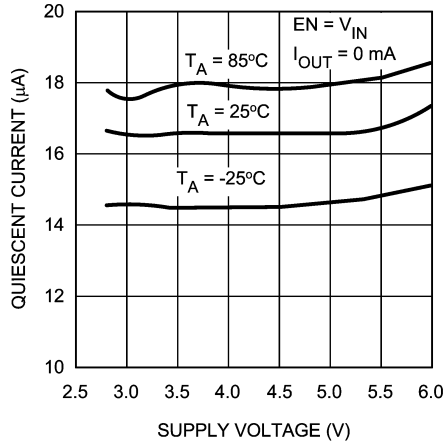


FIGURE 4. Simplified Functional Diagram

Typical Performance Characteristics

LM3671MF, Circuit of *Figure 1*, V_{IN}= 3.6V, T_A= 25˚C, unless otherwise noted.

Quiescent Supply Current vs. Supply Voltage



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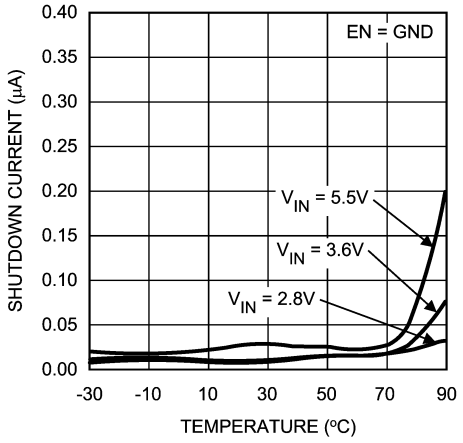
Shutdown Current vs. Temp



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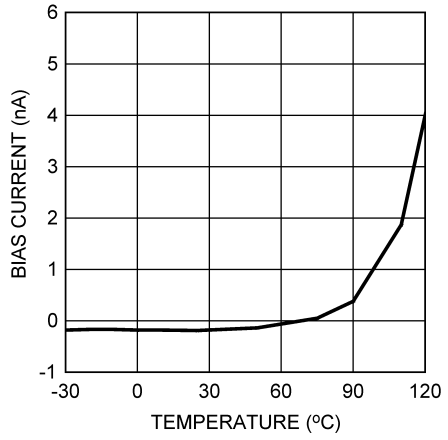
Feedback Bias Current vs. Temp



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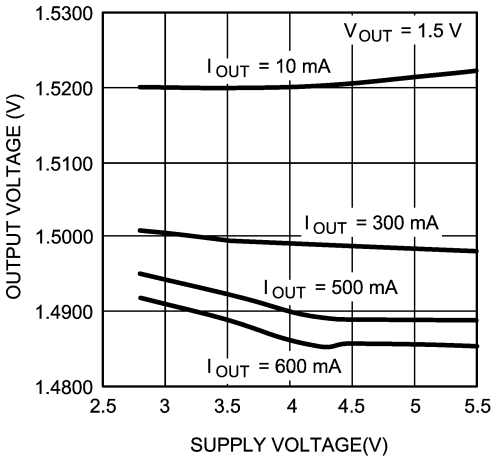
Output Voltage vs. Supply Voltage (V_{OUT} = 1.5V)



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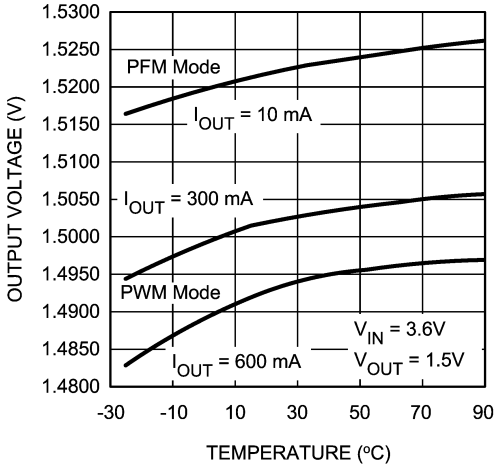
Output Voltage vs. Temperature (V_{OUT} = 1.5V)



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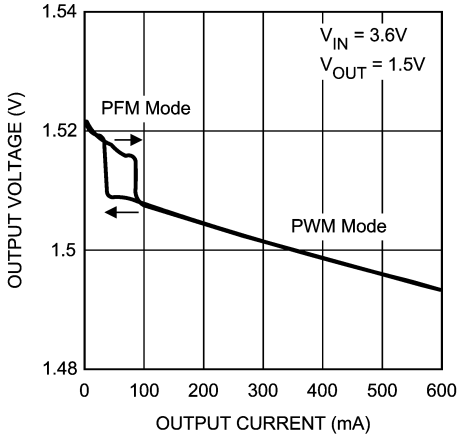
Output Voltage vs. Output Current (V_{OUT} = 1.5V)



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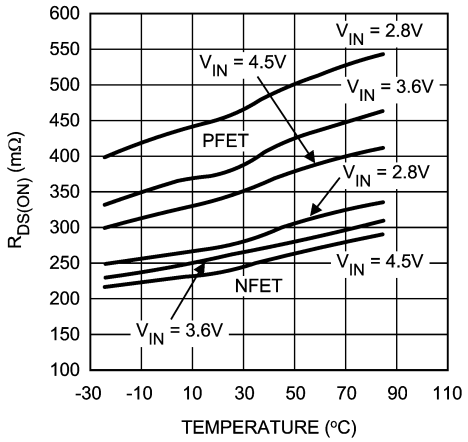
Typical Performance Characteristics (Continued)

$R_{DS(ON)}$ vs. Temperature



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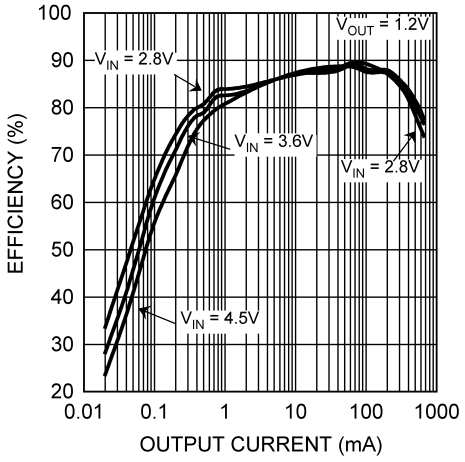
Efficiency vs. Output Current (V_{OUT} = 1.2V, L= 2.2 µH)



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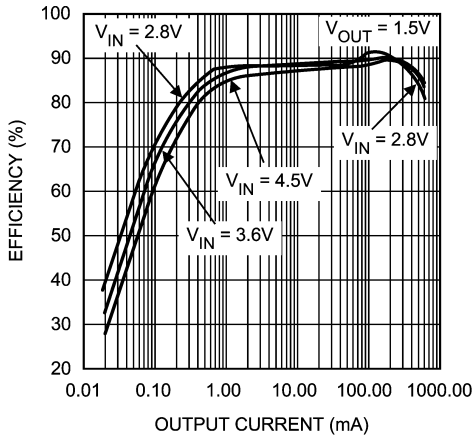
Efficiency vs. Output Current (V_{OUT} = 1.5V, L= 2.2 µH)



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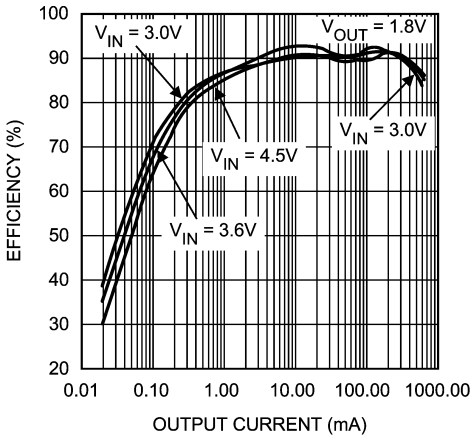
Efficiency vs. Output Current (V_{OUT} = 1.8V, L= 2.2 µH)



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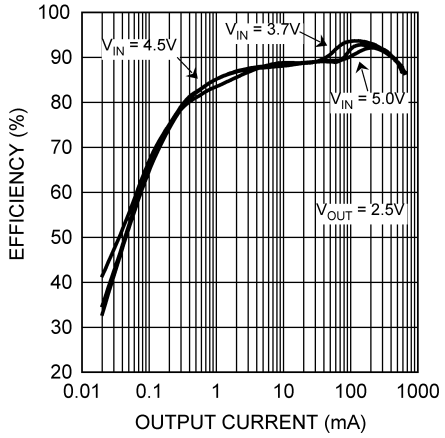
Efficiency vs. Output Current (V_{OUT} = 2.5V, L= 2.2 µH)



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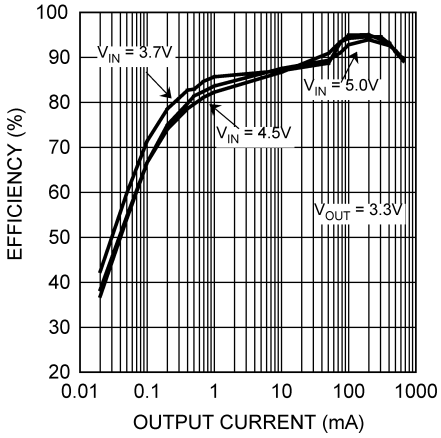
Efficiency vs. Output Current (V_{OUT} = 3.3V, L= 2.2 µH)



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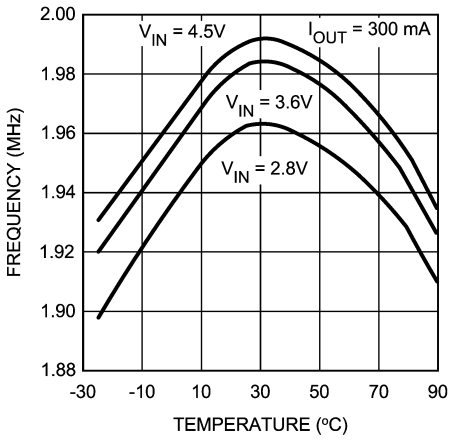
Typical Performance Characteristics (Continued)

Switching Frequency vs. Temperature



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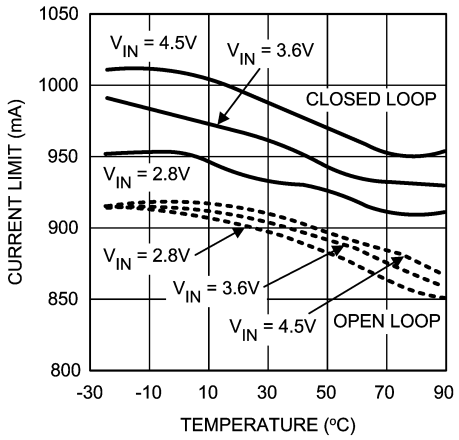
Open/Closed Loop Current Limit vs. Temperature



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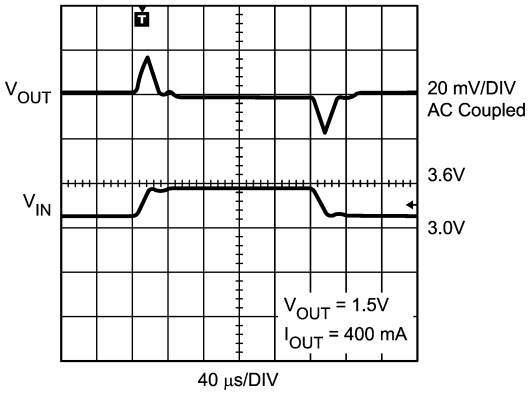
Line Transient Response (PWM Mode)



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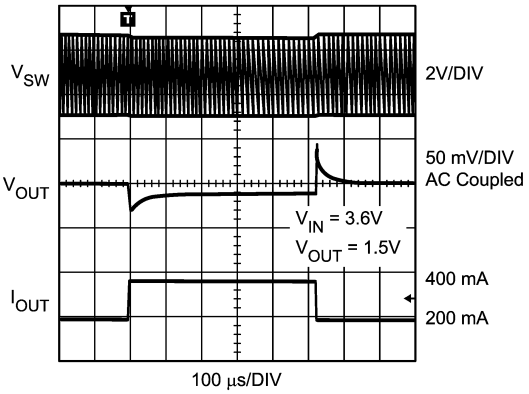
Load Transient Response (PWM Mode)



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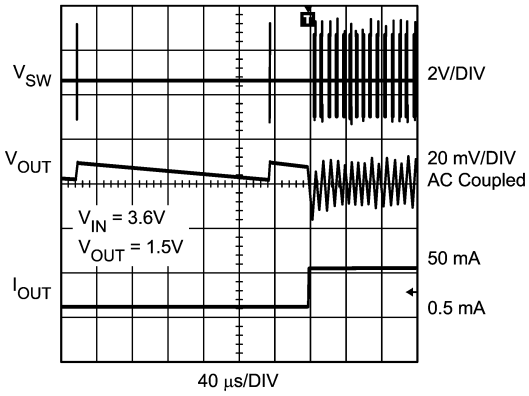
Load Transient Response (PFM Mode 0.5mA to 50mA)



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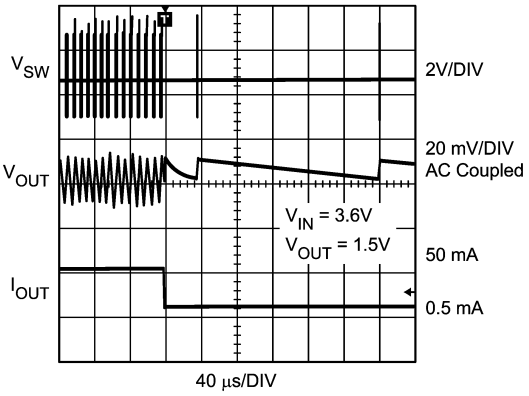
Load Transient Response (PFM Mode 50mA to 0.5mA)



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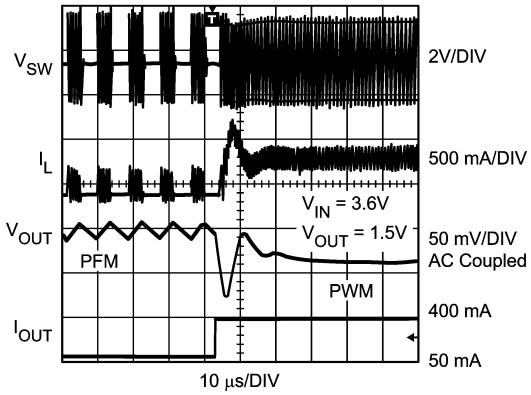
Typical Performance Characteristics (Continued)

Mode Change by Load Transients (PFM to PWM)



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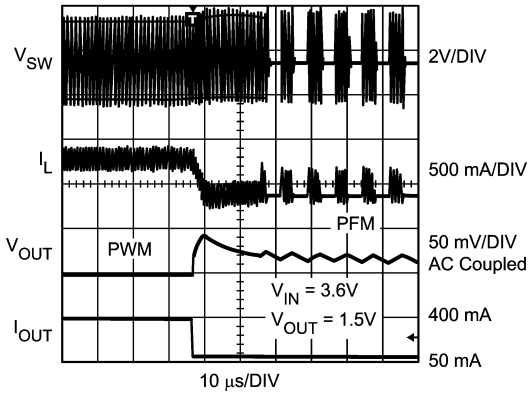
Mode Change by Load Transients (PWM to PFM)



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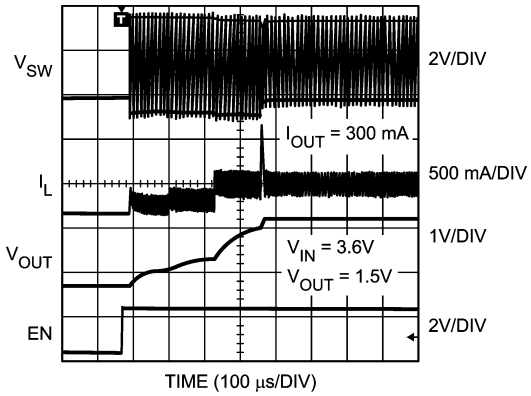
Start Up into PWM Mode (Output Current= 300mA)



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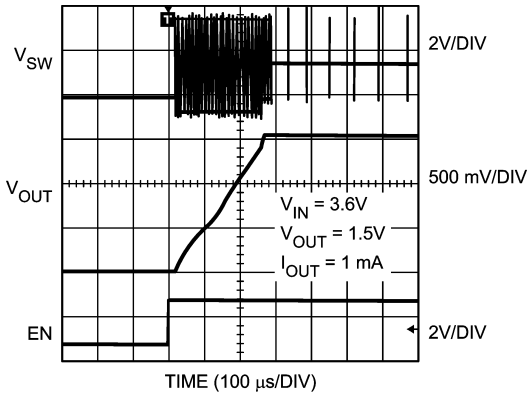
Start Up into PFM Mode (Output Current= 1mA)



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Operation Description

DEVICE INFORMATION

The LM3671, a high efficiency step down DC-DC switching buck converter, delivers a constant voltage from either a single Li-Ion or three cell NiMH/NiCd battery to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, the LM3671 has the ability to deliver up to 600 mA depending on the input voltage,output voltage, ambient temperature and the inductor chosen.

There are three modes of operation depending on the current required - PWM, PFM, and shutdown. The device operates in PWM mode at load currents of approximately 80 mA or higher, having voltage tolerance of ±4% with 90% efficiency or better. Lighter load currents cause the device to automatically switch into PFM for reduced current consumption (I_Q = 16 µA typ) and a longer battery life. Shutdown mode turns off the device, offering the lowest current consumption ($I_{Q,\ SHUTDOWN}$ = 0.01 µA typ).

Additional features include soft-start, under voltage protection, current overload protection, and thermal shutdown protection. As shown in *Figure 1*, only three external power components are required for implementation.

The part uses an internal reference voltage of 0.5V. It is recommended to keep the part in shutdown until the input voltage is 2.8V or higher.

CIRCUIT OPERATION

The LM3671 operates as follows. During the first portion of each switching cycle, the control block in the LM3671 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of (V_{IN}–V_{OUT})/L, by storing energy in a magnetic field.

During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of - V_{OUT}/L.

The output filter stores charge when the inductor current is high, and releases it when inductor current is low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM OPERATION

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

While in PWM (Pulse Width Modulation) mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch.

The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

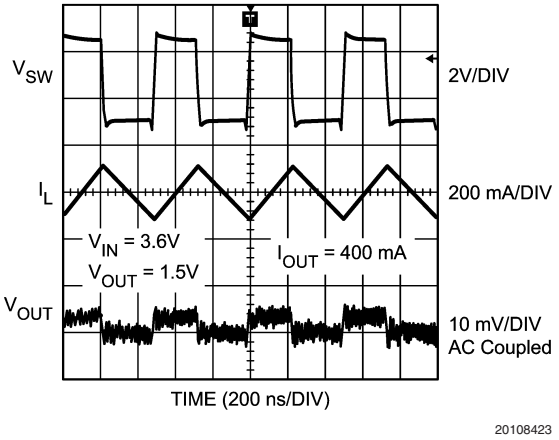

FIGURE 5. Typical PWM Operation

Internal Synchronous Rectification

While in PWM mode, the LM3671 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Current Limiting

A current limit feature allows the LM3671 to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 1020 mA (typ). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

PFM OPERATION

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

A. The inductor current becomes discontinuous.

B. The peak PMOS switch current drops below the I_{MODE} level, (Typically I_{MODE} < 30mA + V_{IN}/42 Ω).

Operation Description (Continued)

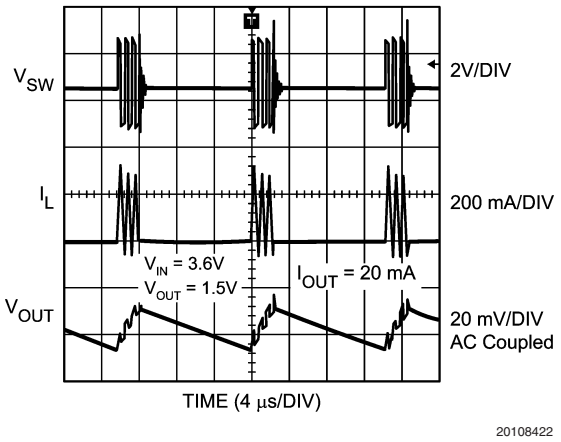

FIGURE 6. Typical PFM Operation

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between ~0.6% and ~1.7% above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is: I_{PFM} = 112mA + $V_{IN}/27\Omega$.

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see *Figure 7*), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is 16µA (typ), which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage (average voltage in pfm mode) to ~1.15% above the nominal PWM output voltage.

If the load current should increase during PFM mode (see *Figure 7*) causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode. When V_{IN} =2.8V the part transitions from PWM to PFM mode at ~35mA output current and from PFM to PWM mode at ~85mA , when V_{IN}=3.6V, PWM to PFM transition happens at ~50mA and PFM to PWM transition happens at ~100mA, when V_{IN} =4.5V, PWM to PFM transition happens at ~65mA and PFM to PWM transition happens at ~115mA.

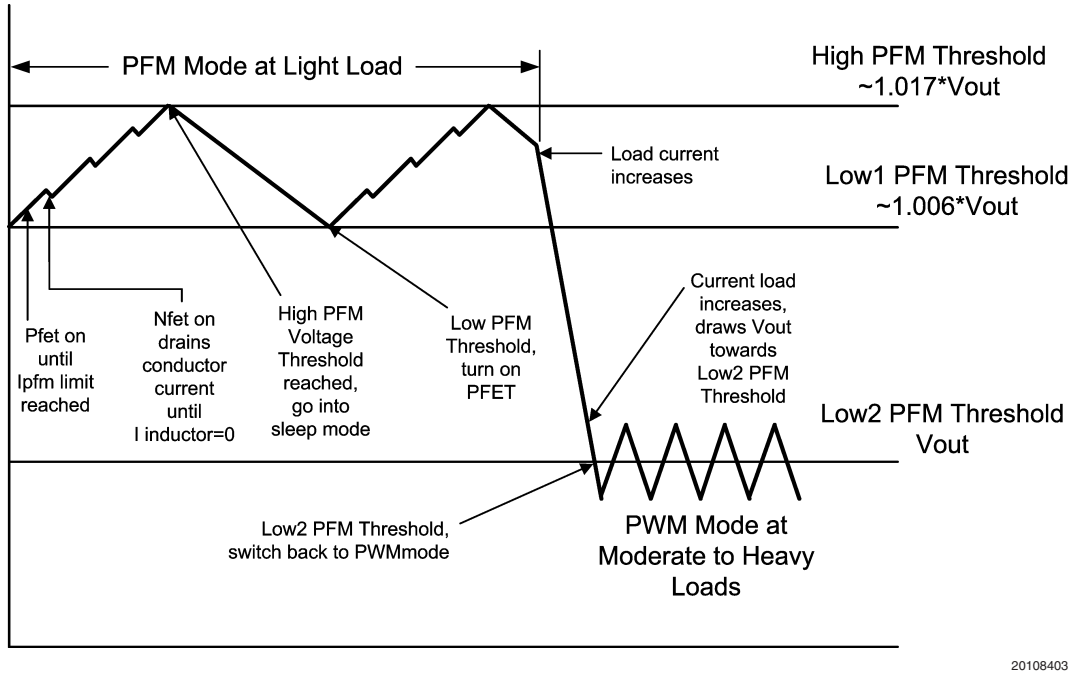

FIGURE 7. Operation in PFM Mode and Transfer to PWM Mode

SHUTDOWN MODE

Setting the EN input pin low (<0.4V) places the LM3671 in shutdown mode. During shutdown the PFET switch, NFET switch, reference, control and bias circuitry of the LM3671 are turned off. Setting EN high (>1.0V) enables normal operation. While turning on the device with EN, soft start is activated. It is recommended to set EN pin low to turn off the LM3671 during system power up and undervoltage conditions when the supply is less than 2.8V. Do not leave the EN pin floating.

Operation Description (Continued)

SOFT START

The LM3671 has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after Vin reaches 2.8V. Soft start is implemented by increasing switch current limit in steps of 70mA, 140mA, 280mA and 1020mA (typ. switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up. Typical start-up times with 22µF output capacitor and 300mA load current is 400 µs and with 1mA load current its 275µs.

LDO - LOW DROP OUT OPERATION

The LM3671-ADJ can operate at 100% duty cycle (no switching, PMOS switch completely on) for low drop out support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage. When device operates near 100% duty cycle, output voltage ripple is slightly higher, approximately 25 mV.

The minimum input voltage needed to support the output voltage is

$V_{IN,\ MIN} = I_{LOAD} * (R_{DSON,\ PFET} + R_{INDUCTOR}) + V_{OUT}$

- I_{LOAD} Load current
- $R_{DSON,\ PFET}$ Drain to source resistance of PFET switch in the triode region
- $R_{INDUCTOR}$ Inductor resistance

Application Information

OUTPUT VOLTAGE SELECTION FOR LM3671-ADJ

The output voltage of the adjustable parts can be programmed through the resistor network connected from V_{OUT} to FB then to GND. V_{OUT} will be adjusted to make the voltage at FB equal to 0.5V. The resistor from FB to GND (R2) should be 200 kΩ to keep the current drawn through this network well below the 16 µA quiescent current level (PFM mode) but large enough that it is not susceptible to noise. If R2 is 200 kΩ, and given the V_{FB} is 0.5V, the current through the resistor feedback network will be 2.5 µA.

The formula for output voltage selection is:

$$V_{OUT} = V_{FB} * \left(1 + \frac{R1}{R2}\right)$$

- V_{OUT}: output voltage (volts)
- V_{FB} : feedback voltage = 0.5V
- R1: feedback resistor from V_{OUT} to FB
- R2: feedback resistor from FB to GND

For any output voltage greater than or equal to 1.0V a zero must be added around 45 kHz for stability. The formula for calculation of C1 is:

$$C1 = \frac{1}{(2 * \pi * R1 * 45\ kHz)}$$

For output voltages higher than 2.5V a pole must be placed at 45 kHz as well. If the pole and zero are at the same frequency the formula for calculation of C2 is:

$$C2 = \frac{1}{(2 * \pi * R2 * 45\ kHz)}$$

The formula for location of zero and pole frequency created by adding C1,C2 are given below. It can be seen that by adding C1, a zero as well as a higher frequency pole is introduced.

$$Fz = \frac{1}{(2 * \pi * R1 * C1)}$$

$$Fp = \frac{1}{2 * \pi * (R1 \| R2) * (C1+C2)}$$

See the "LM3671-ADJ configurations for various V_{OUT}" table.These values are subject to change when the LM3671-ADJ part is released.

Application Information (Continued)

LM3671-ADJ configurations for various V_{OUT}

V_{OUT}(V)	R1(kΩ)	R2 (kΩ)	C1 (pF)	C2 (pF)	L (µH)	C_{IN} (µF)	C_{OUT}(µF)
1.0	200	200	18	none	2.2	10	22
1.1	191	158	18	none	2.2	10	22
1.2	280	200	12	none	2.2	10	22
1.5	360	180	10	none	2.2	10	22
1.6	442	200	8.2	none	2.2	10	22
1.7	432	180	8.2	none	2.2	10	22
2.5	402	100	8.2	none	2.2	10	22
2.8	464	100	8.2	33	2.2	10	22
3.3	562	100	6.8	33	2.2	10	22

INDUCTOR SELECTION

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple. Different saturation current rating specs are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25˚C so ratings at max ambient temperature of application should be requested from manufacturer.

There are two methods to choose the inductor saturation current rating.

Method 1:

The saturation current is greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{where } I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 * L}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right)$$

- I_{RIPPLE}: average to peak inductor current
- I_{OUTMAX}: maximum load current (600mA)
- V_{IN}: maximum input voltage in application
- L : min inductor value including worst case tolerances (30% drop can be considered for method 1)
- f : minimum switching frequency (1.6Mhz)
- V_{OUT}: output voltage

Method 2:

A more conservative and recommended approach is to choose an inductor that has saturation current rating greater than the max current limit of 1150mA.

A 2.2 µH inductor with a saturation current rating of at least 1150 mA is recommended for most applications.The inductor's resistance should be less than 0.3Ω for good efficiency. *Table 1* lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost bobbin models is unacceptable.

INPUT CAPACITOR SELECTION

A ceramic input capacitor of 10 µF, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the V_{IN} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The input filter capacitor supplies current to the PFET switch of the LM3671 in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{L * f * I_{OUTMAX} * V_{IN}}$$

The worst case is when $V_{IN} = 2 * V_{OUT}$

Application Information (Continued)

TABLE 1. Suggested Inductors and Their Suppliers

Model	Vendor	Dimensions LxWxH(mm)	D.C.R (max)
DO3314-222MX	Coilcraft	3.3 x 3.3 x 1.4	200 mΩ
LPO3310-222MX	Coilcraft	3.3 x 3.3 x 1.0	150 mΩ
ELL5GM2R2N	Panasonic	5.2 x 5.2 x 1.5	53 mΩ
CDRH2D14-2R2	Sumida	3.2 x 3.2 x 1.55	94 mΩ

OUTPUT CAPACITOR SELECTION

Use a 22 µF, 6.3V ceramic capacitor. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process. The LM3671 has been evaluated with 22 µF, 6.3V, 0805 with worst case tolerances including dc bias effects. The use of two 10 µF, 6.3V, 0805 caps will give an overall higher capacitance value when dc bias is considered.

The output filter capacitor smoothes out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its R_{ESR} and can be calculated as:

Voltage peak-to-peak ripple due to capacitance can be expressed as follows

$$V_{PP-C} = \frac{I_{RIPPLE}}{4*f*C}$$

Voltage peak-to-peak ripple due to ESR can be expressed as follows

$V_{PP-ESR} = (2 * I_{RIPPLE}) * R_{ESR}$

Because these two components are out of phase the rms value can be used to get an approximate value of peak-to-peak ripple.

Voltage peak-to-peak ripple, root mean squared can be expressed as follows

$$V_{PP-RMS} = \sqrt{V_{PP-C}^2 + V_{PP-ESR}^2}$$

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

TABLE 2. Suggested Capacitors and Their Suppliers

Model	Type	Vendor	Voltage Rating	Case Size Inch (mm)
22 µF for C_{OUT}				
GRM21BR60J226K	Ceramic, X5R	Murata	6.3V	0805 (2012)
C2012X5R0J226K	Ceramic, X5R	TDK	6.3V	0805 (2012)
JMK212BJ226K	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)
10 µF for C_{IN}				
GRM21BR60J106K	Ceramic, X5R	Murata	6.3V	0805 (2012)
JMK212BJ106K	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)
C2012X5R0J106K	Ceramic, X5R	TDK	6.3V	0805 (2012)

BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability.

Application Information (Continued)

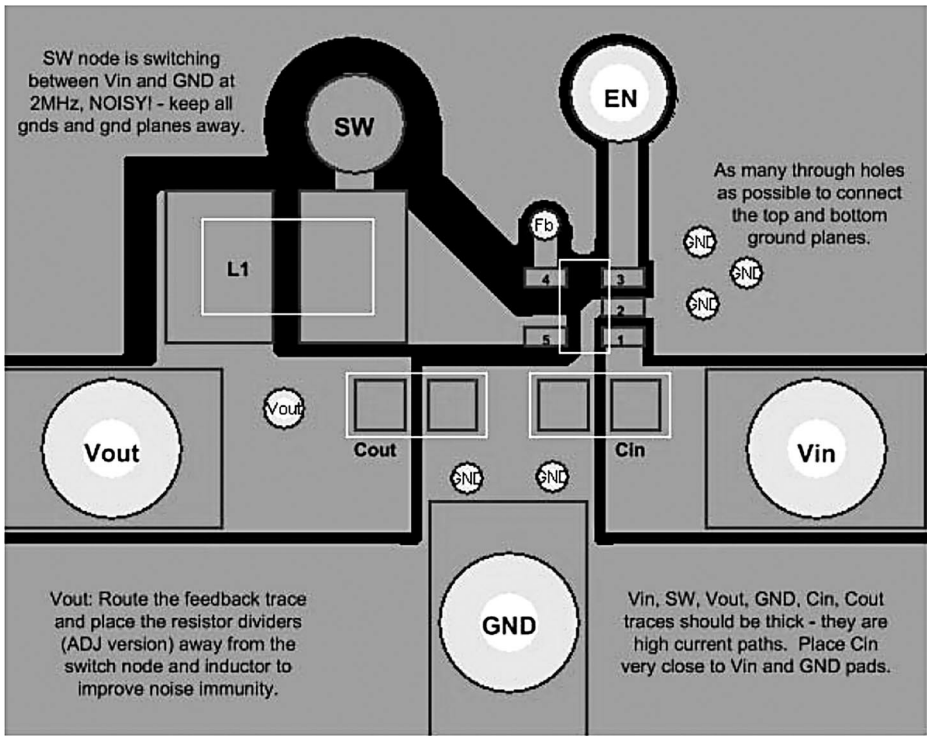

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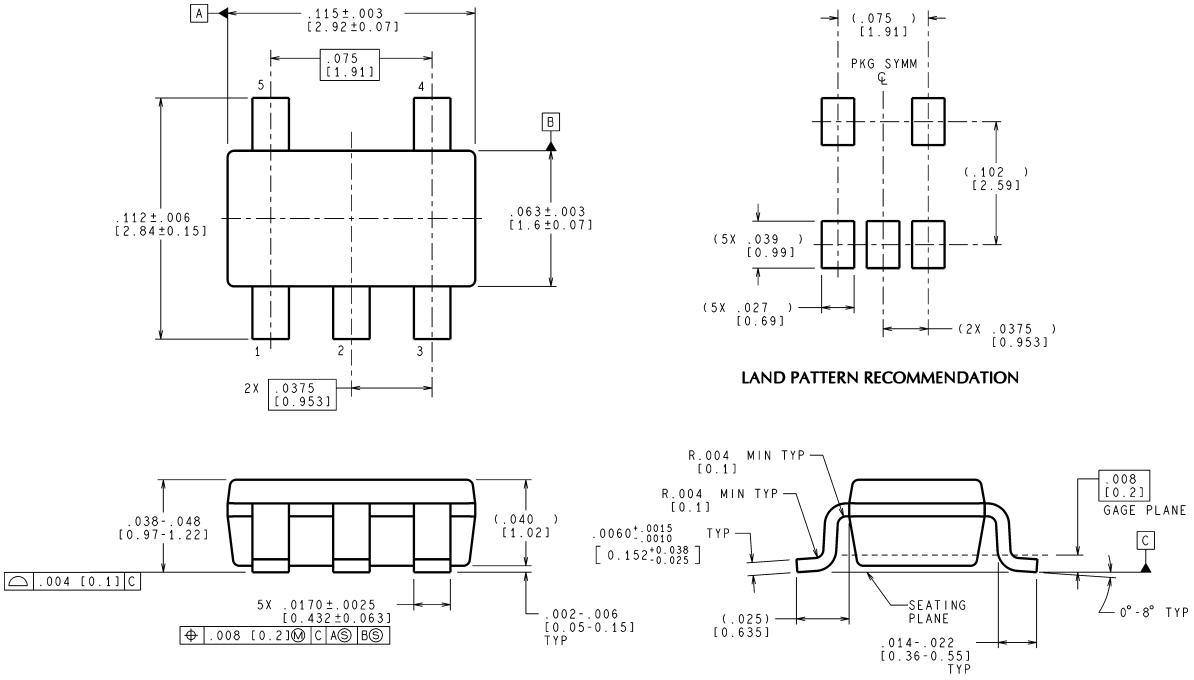
FIGURE 8. Board Layout Design Rules for the LM3671

Good layout for the LM3671 can be implemented by following a few simple design rules, as illustrated in *Figure 8*.

1. *Place the LM3671, inductor and filter capacitors close together and make the traces short.* The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{IN} and GND pin.
2. *Arrange the components so that the switching current loops curl in the same direction.* During the first half of each cycle, current flows from the input filter capacitor through the LM3671 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the LM3671 by the inductor to the output filter capacitor and then back through ground forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. *Connect the ground pins of the LM3671 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias.* This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3671 by giving it a low-impedance ground connection.
4. *Use wide traces between the power components and for power connections to the DC-DC converter circuit.* This reduces voltage errors caused by resistive losses across the traces.
5. *Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.* The voltage feedback trace must remain close to the LM3671 circuit and should be direct but should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed. In the same manner for the adjustable part it is desired to have the feedback dividers on the bottom layer.
6. *Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry.* Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

Physical Dimensions inches (millimeters) unless otherwise noted



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