SH79F3283

Enhanced 8051 Microcontroller with 12bit ADC

1. Features

- 8bits micro-controller with Pipe-line structured 8051 compatible instruction set
- Flash ROM: 32K Bytes
- RAM: internal 256 Bytes, external 1280 Bytes, LCD RAM: 28 Bytes
- EEPROM-like: 1024 Bytes
- Operation Voltage:
  f_{OSC} = 32.768kHz - 16MHz, V_{DD} = 2.0V - 5.5V
- Oscillator (code option)
  - Crystal oscillator: 32.768kHz
  - Crystal oscillator: 2MHz - 16MHz
  - Ceramic oscillator: 2MHz - 16MHz
  - Internal RC: 12MHz (±2%)/128K
- 46/42/30 CMOS bi-directional I/O pins
- Built-in pull-up resistor for input pin
- Four 16-bit timer/counters: T2, T3, T4 and T5
- One 12-bit PWM
- One 8-bit PWM
- Powerful interrupt sources:
  - Timer2, 3, 4, 5
  - INT0, 1, 2, 3
  - INT40 - INT47
  - ADC, EUART, SCM, LPD
  - PWM, SPI
- EUART0, EUART1 (No EUART1 in 32 PIN package)
- SPI Interface (Master/Slave Mode)
- Buzzer
- 9 channels 12-bits Analog Digital Converter (ADC), with comparator function built-in
- LED driver:
  - 3-8 X 8 dots (1/3 - 1/8 duty)
- LCD driver:
  - 8 X 24 dots (1/8 duty, 1/4 bias)
  - 6 X 26 dots (1/6 duty, 1/4 or 1/3 bias)
  - 5 X 27 dots (1/5 duty, 1/3 bias)
  - 4 X 28 dots (1/4 duty, 1/3 bias)
- Low Voltage Reset (LVR) function (enabled by code option)
  - LVR voltage level 1: 4.1V
  - LVR voltage level 2: 3.7V
  - LVR voltage level 3: 2.8V
  - LVR voltage level 4: 2.1V
- CRC verify module built-in, check size is optional
- Support SWE simulation, write and read
- CPU Machine cycle: 1 oscillator clock
- Watch Dog Timer (WDT)
- Warm-up Timer
- Support Low power operation modes:
  - Idle Mode
  - Power-Down Mode
- Flash Type
- Package: TQFP48/LQFP44/LQFP32

2. General Description

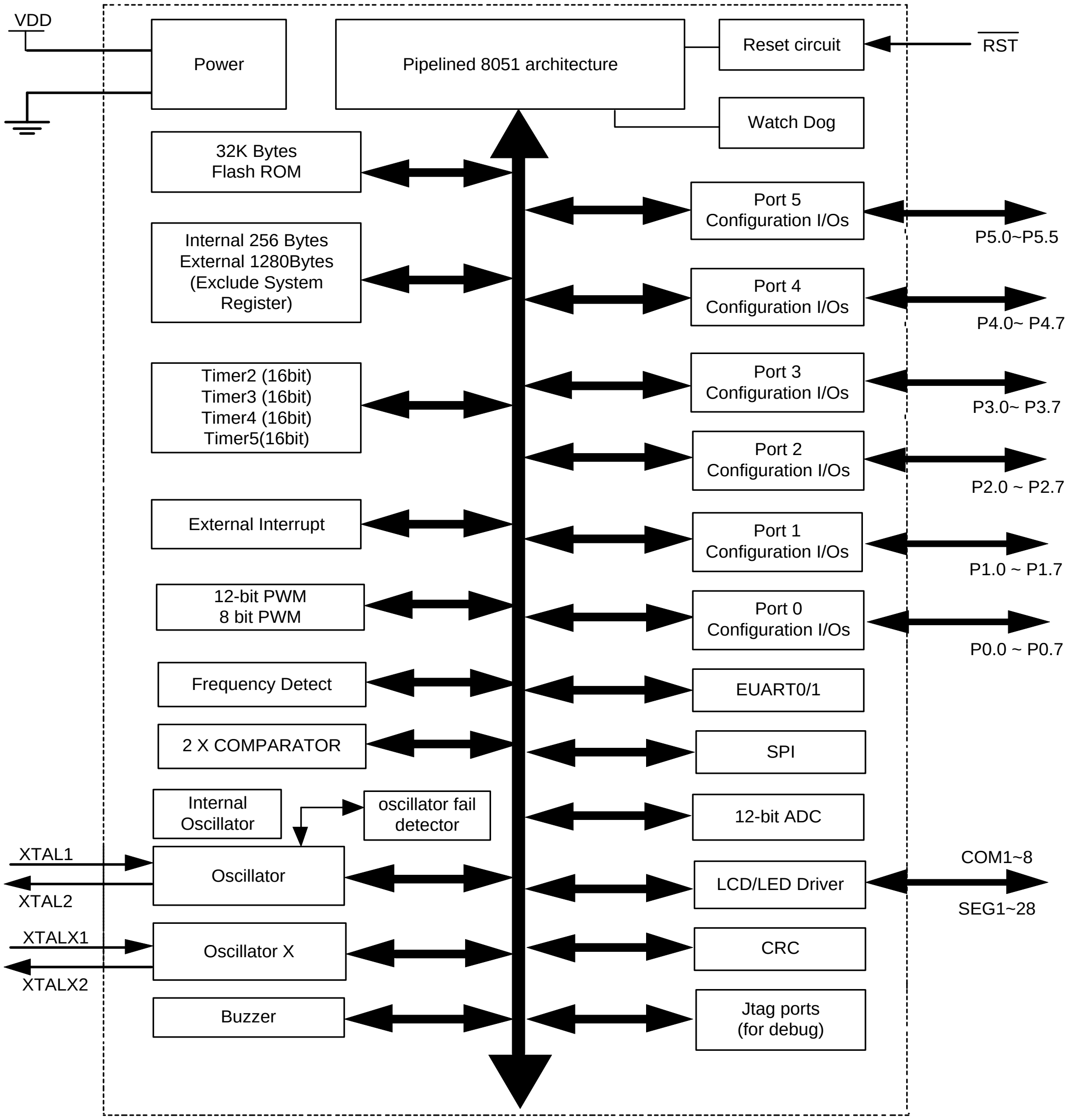
The SH79F3283 is a high performance 8051 compatible micro-controller, regard to its build-in Pipe-line instruction fetch structure, that helps the SH79F3283 can perform more fast operation speed and higher calculation performance, if compare SH79F3283 with standard 8051 at same clock speed.

The SH79F3283 retains most features of the standard 8051. These features include internal 256 bytes RAM, UART and INT0, INT1, INT2 and INT3. In addition, the SH79F3283 provides external 1280 bytes RAM, Four 16-bit timer/counters T2-T5. It also contains 32K bytes Flash memory block both for program and data.

Also the ADC, EUART, SPI, LCD Driver, PWM timer and CRC module functions are incorporated in SH79F3283.

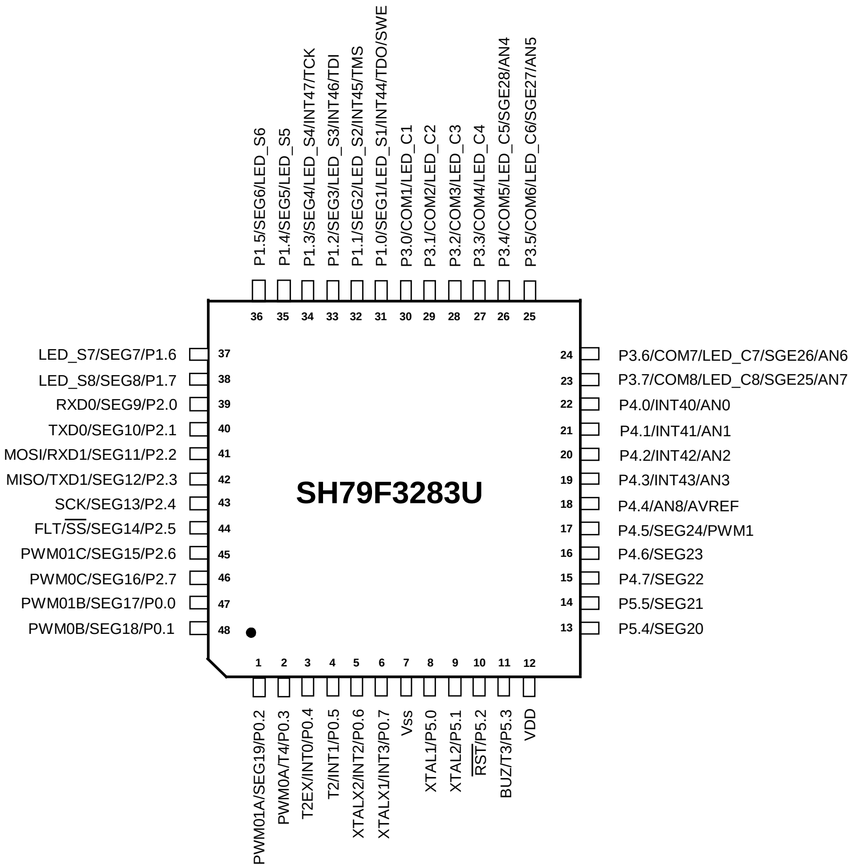
For high reliability and low power consumption, the SH79F3283 builds in Watchdog Timer, Low Voltage Reset function and SCM function. And SH79F3283 also supports two power saving modes to reduce power consumption.

3. Block Diagram



4. Pin Configuration

4.1 TQFP48

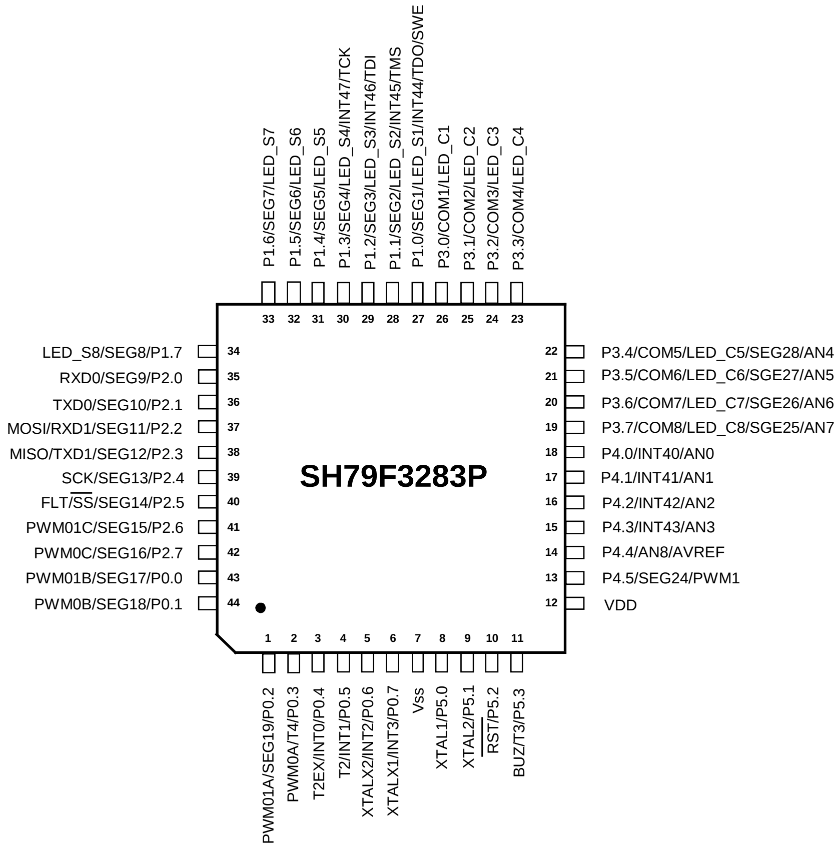


Pin Configuration Diagram TQFP48

Note:

The out most pin function has the highest priority, and the inner most pin function has the lowest priority (Refer to Pin Configuration Diagram. This means when one pin is occupied by a higher priority function (if enabled) cannot be used as the lower priority functional pin, even when the lower priority function is also enabled. Until the higher priority function is closed by software, can the corresponding pin be released for the lower priority function to use.

4.2 LQFP44

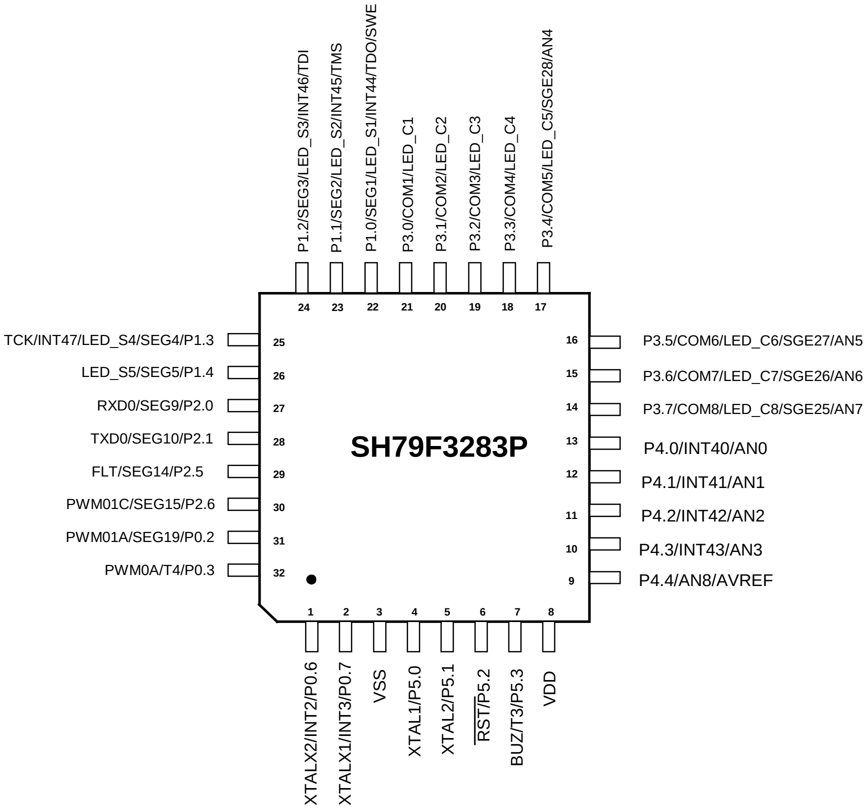


Pin Configuration Diagram LQFP44

Note:

The out most pin function has the highest priority, and the inner most pin function has the lowest priority (Refer to Pin Configuration Diagram. This means when one pin is occupied by a higher priority function (if enabled) cannot be used as the lower priority functional pin, even when the lower priority function is also enabled. Until the higher priority function is closed by software, can the corresponding pin be released for the lower priority function to use.

4.3 LQFP32



Pin Configuration Diagram LQFP32

Note:

The out most pin function has the highest priority, and the inner most pin function has the lowest priority (Refer to Pin Configuration Diagram. This means when one pin is occupied by a higher priority function (if enabled) cannot be used as the lower priority functional pin, even when the lower priority function is also enabled. Until the higher priority function is closed by software, can the corresponding pin be released for the lower priority function to use.

Table 4.1 Pin Function

Pin No. (TQFP48)	Pin No. (LQFP44)	Pin No. (LQFP32)	Pin Name	Default Function
1	1	31	PWM01A/SEG19/P0.2	P0.2
2	2	32	PWM0A/T4/P0.3	P0.3
*3	*3	-	T2EX/INT0/P0.4	P0.4
*4	*4	-	T2/INT1/P0.5	P0.5
5	5	1	XTALX2/INT2/P0.6	P0.6
6	6	2	XTALX1/INT3/P0.7	P0.7
7	7	3	V_{SS}	----
8	8	4	XTAL1/P5.0	----
9	9	5	XTAL2/P5.1	----
10	10	6	$\overline{\text{RST}}$/P5.2	$\overline{\text{RST}}$
11	11	7	BUZ/T3/P5.3	P5.3
12	12	8	V_{DD}	----
13	-	-	SEG20/P5.4	P5.4
14	-	-	SEG21/P5.5	P5.5
15	-	-	SEG22/P4.7	P4.7
16	-	-	SEG23/P4.6	P4.6
17	13	-	PWM1/SEG24/P4.5	P4.5
18	14	9	AVREF/AN8/P4.4	P4.4
19	15	10	AN3/INT43/P4.3	P4.3
20	16	11	AN2/INT42/P4.2	P4.2
21	17	12	AN1/INT41/P4.1	P4.1
22	18	13	AN0/INT40/P4.0	P4.0
23	19	14	AN7/SEG25/LED_C8/COM8/P3.7	P3.7
24	20	15	AN6/SEG26/LED_C7/COM7/P3.6	P3.6
25	21	16	AN5/SEG27/LED_C6/COM6/P3.5	P3.5
26	22	17	AN4/SEG28/LED_C5/COM5/P3.4	P3.4
27	23	18	LED_C4/COM4/P3.3	P3.3
28	24	19	LED_C3/COM3/P3.2	P3.2
29	25	20	LED_C2/COM2/P3.1	P3.1
30	26	21	LED_C1/COM1/P3.0	P3.0
31	27	22	INT44/LED_S1/SEG1/P1.0	P1.0
32	28	23	INT45/LED_S2/SEG2/P1.1	P1.1
33	29	24	INT46/LED_S3/SEG3/P1.2	P1.2
34	30	25	INT47/LED_S4/SEG4/P1.3	P1.3
35	31	26	LED_S5/SEG5/P1.4	P1.4
36	32	-	LED_S6/SEG6/P1.5	P1.5

(to be continued)

(continue)

Pin No. (TQFP48)	Pin No. (LQFP44)	Pin No. (LQFP32)	Pin Name	Default Function
37	33	-	LED_S7/SEG7/P1.6	P1.6
38	34	-	LED_S8/SEG8/P1.7	P1.7
39	35	27	RXD0/SEG9/P2.0	P2.0
40	36	28	TXD0/SEG10/P2.1	P2.1
41	37	-	MOSI/RXD1/SEG11/P2.2	P2.2
42	38	-	MISO/TXD1/SEG12/P2.3	P2.3
43	39	-	SCK/SEG13/P2.4	P2.4
44	40	29	FLT/SS/SEG14/P2.5	P2.5
45	41	30	PWM01C/SEG15/P2.6	P2.6
46	42	-	PWM0C/SEG16/ P2.7	P2.7
47	43	-	PWM01B/SEG17/P0.0	P0.0
48	44	-	PWM0B/SEG18/P0.1	P0.1

***Note:** P0.4, P0.5 are configured as N-channel open drain IO.*

5. Pin Description

Pin No.	Type	Description
I/O PORT		
P0.0 - P0.7	I/O	8 bit General purpose CMOS I/O
P1.0 - P1.7	I/O	8 bit General purpose CMOS I/O
P2.0 - P2.7	I/O	8 bit General purpose CMOS I/O
P3.0 - P3.7	I/O	8 bit General purpose CMOS I/O
P4.0 - P4.7	I/O	8 bit General purpose CMOS I/O
P5.0 - P5.5	I/O	6 bit General purpose CMOS I/O
Timer		
T2	I/O	Timer2 external input/baud rate clock output
T3	I	Timer3 external input
T4	I/O	Timer4 external input/output
T2EX	I	Timer2 Reload/Capture/Direction Control
PWM		
PWM0A/0B/0C	O	Output pin for 12-bit PWM0 timer
PWM01A/01B/01C	O	Output pin for 12-bit PWM0 timer with fixed phase relationship of PWM0
FLT	I	PWM0 Fault Detect input
PWM1	O	Output pin for 8-bit PWM1 timer
EUART		
RXD0/1	I	EUART0/1 data input
TXD0/1	O	EUART0/1 data output
SPI		
MOSI	I/O	SPI Master output Slave input
MISO	I/O	SPI Master input Slave output
SCK	I/O	SPI serial clock
$\overline{\text{SS}}$	I	SPI Slave Select
ADC		
AN0 - AN7	I	ADC input channel
AVREF	I	External ADC reference voltage input
LCD		
COM1 - COM8	O	Common signal output for LCD display
SEG1 - SEG28	O	Segment signal output for LCD display
LED		
LED_C1 - LED_C8	O	Common signal output for LCD display
LED_S1 - LED_S8	O	Segment signal output for LCD display

(to be continued)

(continue)

Interrupt & Reset & Clock & Power		
INT0 - INT3	I	External interrupt 0-3 input source
INT40 - INT47	I	External interrupt 40-47 input source
$\overline{\text{RST}}$	I	The device will be reset by a low voltage on this pin longer than 10us, an internal resistor about 30kΩ to V_{DD}, So using only an external capacitor to GND can cause a power-on reset.
XTAL1	I	Oscillator input
XTAL2	O	Oscillator output
XTALX1	I	Oscillator X input
XTALX2	O	Oscillator X output
V_{SS}	P	Ground
V_{DD}	P	Power supply (2.0 - 5.5V)
Buzzer		
BUZ	O	Buzzer output pin
Programmer		
TDO (P1.0)	O	Debug interface: Test data out
TMS (P1.1)	I	Debug interface: Test mode select
TDI (P1.2)	I	Debug interface: Test data in
TCK (P1.3)	I	Debug interface: Test clock in
SWE (P1.0)	I/O	Single simulation interface. If the power on or down slope of V_{DD} is greater than 500ms/V, it is recommended to connect 47k-1m resistor to GND or V_{DD} to increase the stability of the chip
Note: *When P1.0-1.3 used as debug interface, functions of P1.0-1.3 are blocked.*		

6. SFR Mapping

The SH79F3283 provides 256 bytes of internal RAM to contain general-purpose data memory and Special Function Register (SFR). The SFR of the SH79F3283 fall into the following categories:

CPU Core Registers:	ACC, B, PSW, SP, DPL, DPH
Enhanced CPU Core Registers:	AUXC, DPL1, DPH1, INSCON, XPAGE
Power and Clock Control Registers:	PCON, SUSLO
Flash Registers:	IB_OFFSET, IB_DATA, IB_CON1, IB_CON2, IB_CON3, IB_CON4, IB_CON5
Data Memory Register:	XPAGE
Hardware Watchdog Timer Registers:	RSTSTAT
System Clock Control Register:	CLKCON, SCMCON
Interrupt System Registers:	IEN0, IEN1, IENC, IPH0, IPL0, IPH1, IPL1, EXF0, EXF1, EXCON
I/O Port Registers:	P0, P1, P2, P3, P4, P5, P0CR, P1CR, P2CR, P3CR, P4CR, P5CR, P0PCR, P1PCR, P2PCR, P3PCR, P4PCR, P5PCR, P0OS
Timer Registers:	TCON, T2CON, T2MOD, TH2, TL2, RCAP2L, RCAP2H, T3CON, TH3, TL3, T4CON, TH4, TL4, SWTHL, T5CON, TH5, TL5
EUART Registers:	SCON, SBUF, SADEN, SADDR, PCON, SCON1, SBUF1, SADEN1, SADDR1, SBRTL, SBRTH, BFINE
SPI Registers:	SPCON, SPSTA, SPDAT
ADC Registers:	ADCON, ADT, ADCH, ADDL, ADDH, ADCON1
LCD Registers:	DISPCON, DISPCON1, DISPCLK0, P0SS, P1SS, P2SS, P3SS
LED Registers:	DISPCON, DISPCLK0, P1SS, P3SS
BUZZER Registers:	BUZCON
PWM Registers:	PWMEN, PWMEN1, PWM0C, PWM0PL, PWM0PH, PWM0DL, PWM0DH, PWM1C, PWM1P, PWM1D
LPD Registers:	LPDCON
CRC Registers:	CRCCON, CRCDL, CRCDH

Table 6.1 CPU Core SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ACC	E0H	Accumulator	00000000	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
B	F0H	B Register	00000000	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
AUXC	F1H	C Register	00000000	C.7	C.6	C.5	C.4	C.3	C.2	C.1	C.0
PSW	D0H	Program Status Word	00000000	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81H	Stack Pointer	00000111	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
DPL	82H	Data Pointer Low byte	00000000	DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0
DPH	83H	Data Pointer High byte	00000000	DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0
DPL1	84H	Data Pointer 1 Low byte	00000000	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0
DPH1	85H	Data Pointer 1 High byte	00000000	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0
INSCON	86H	Data pointer select	-0--00-0	-	BKS0	-	-	DIV	MUL	-	DPS

Table 6.2 Power and Clock control SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	87H	Power Control	000-0000	SMOD	SSTAT	SSTAT1	-	GF1	GF0	PD	IDL
SUSLO	8EH	Suspend Mode Control	00000000	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0

Table 6.3 Flash control SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFFSET	FBH Bank0	Low byte offset of flash memory for programming	00000000	IB_OFFSET.7	IB_OFFSET.6	IB_OFFSET.5	IB_OFFSET.4	IB_OFFSET.3	IB_OFFSET.2	IB_OFFSET.1	IB_OFFSET.0
IB_DATA	FCH Bank0	Data Register for programming flash memory	00000000	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
IB_CON1	F2H Bank0	Flash Memory Control Register 1	00000000	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
IB_CON2	F3H Bank0	Flash Memory Control Register 2	----0000	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
IB_CON3	F4H Bank0	Flash Memory Control Register 3	----0000	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
IB_CON4	F5H Bank0	Flash Memory Control Register 4	----0000	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
IB_CON5	F6H Bank0	Flash Memory Control Register 5	----0000	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0
XPAGE	F7H Bank0	Memory Page	-0000000	-	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
FLASHCON	A7H Bank0	Flash access control	-------0	-	-	-	-	-	-	-	FAC

Table 6.4 WDT SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	B1H Bank0	Watchdog Timer Control	0-000000*	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0

***Note:** RSTSTAT initial value is determined by different RESET.*

Table 6.5 CLKCON SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	B2H Bank0	System Clock Control Register	111000--	32k_ SPDUP	CLKS1	CLKS0	SCMIF	HFON	FS	-	-
SCMCON	A1H Bank0	SCM Clock Control Register	-----011	-	-	-	-	-	SCK2	SCK1	SCK0

Table 6.6 Interrupt SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	A8H Bank0	Interrupt Enable Control 0	00000000	EA	EADC	ET2	ES	ECMP	EX1	ET5	EX0
IEN1	A9H Bank0	Interrupt Enable Control 1	00000000	ESCM_LPD _CRC	ET4	EPWM	ET3_ES1	EX4	EX3	EX2	ESPI
IENC	BAH Bank0	Interrupt 4channel enable control	00000000	EXS47	EXS46	EXS45	EXS44	EXS43	EXS42	EXS41	EXS40
IENC1	BBH Bank0	Interrupt channel enable control 1	-0000000	-	ECRC	ES1	ET3	ECMP1	ECMP2	ESCM	ELPD
IPH0	B4H Bank0	Interrupt Priority Control High 0	-0000000	-	PADCH	PT2H	PSH	PCMPH	PX1H	PT5H	PX0H
IPL0	B8H Bank0	Interrupt Priority Control Low 0	-0000000	-	PADCL	PT2L	PSL	PCMPL	PX1L	PT5L	PX0L
IPH1	B5H Bank0	Interrupt Priority Control High 1	00000000	PSCMH	PT4H	PPWMH	PT3S1H	PX4H	PX3H	PX2H	PSPIH
IPL1	B9H Bank0	Interrupt Priority Control Low 1	00000000	PSCML	PT4L	PPWML	PT3S1L	PX4L	PX3L	PX2L	PSPIL
EXF0	E8H Bank0	External interrupt Control 0	00000000	IT4.1	IT4.0	IT3.1	IT3.0	IT2.1	IT2.0	IE3	IE2
EXF1	D8H Bank0	External interrupt Control 1	00000000	IF47	IF46	IF45	IF44	IF43	IF42	IF41	IF40
EXCON	8BH Bank0	External interrupt Sample Control	00000000	I1PS1	I1PS0	I1SN1	I1SN0	I0PS1	I0PS0	I0SN1	I0SN0

Table 6.7 Port SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0	80H Bank0	8-bit Port 0	00000000	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
P1	90H Bank0	8-bit Port 1	00000000	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P2	A0H Bank0	8-bit Port 2	00000000	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
P3	B0H Bank0	8-bit Port 3	00000000	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
P4	C0H Bank0	8-bit Port 4	00000000	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
P5	80H Bank1	6-bit Port 5	--000000	-	-	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0
P0CR	E1H Bank0	Port0 input/output direction control	00000000	P0CR.7	P0CR.6	P0CR.5	P0CR.4	P0CR.3	P0CR.2	P0CR.1	P0CR.0
P1CR	E2H Bank0	Port1 input/output direction control	00000000	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P2CR	E3H Bank0	Port2 input/output direction control	00000000	P2CR.7	P2CR.6	P2CR.5	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
P3CR	E4H Bank0	Port3 input/output direction control	00000000	P3CR.7	P3CR.6	P3CR.5	P3CR.4	P3CR.3	P3CR.2	P3CR.1	P3CR.0
P4CR	E5H Bank0	Port4 input/output direction control	00000000	P4CR.7	P4CR.6	P4CR.5	P4CR.4	P4CR.3	P4CR.2	P4CR.1	P4CR.0
P5CR	E1H Bank1	Port5 input/output direction control	--000000	-	-	P5CR.5	P5CR.4	P5CR.3	P5CR.2	P5CR.1	P5CR.0
P0PCR	E9H Bank0	Internal pull-high enable for Port0	00000000	P0PCR.7	P0PCR.6	P0PCR.5	P0PCR.4	P0PCR.3	P0PCR.2	P0PCR.1	P0PCR.0
P1PCR	EAH Bank0	Internal pull-high enable for Port1	00000000	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P2PCR	EBH Bank0	Internal pull-high enable for Port2	00000000	P2PCR.7	P2PCR.6	P2PCR.5	P2PCR.4	P2PCR.3	P2PCR.2	P2PCR.1	P2PCR.0
P3PCR	ECH Bank0	Internal pull-high enable for Port3	00000000	P3PCR.7	P3PCR.6	P3PCR.5	P3PCR.4	P3PCR.3	P3PCR.2	P3PCR.1	P3PCR.0
P4PCR	EDH Bank0	Internal pull-high enable for Port4	00000000	P4PCR.7	P4PCR.6	P4PCR.5	P4PCR.4	P4PCR.3	P4PCR.2	P4PCR.1	P4PCR.0
P5PCR	E9H Bank1	Internal pull-high enable for Port5	--000000	-	-	P5PCR.5	P5PCR.4	P5PCR.3	P5PCR.2	P5PCR.1	P5PCR.0
P0OS	EFH Bank0	Output mode control	--00----	-	-	P0OS.5	P0OS.4	-	-	-	-

Table 6.8 Timer SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	88H Bank0	Timer/Counter Control	----0000	-	-	-	-	IE1	IT1	IE0	IT0
T2CON	C8H Bank0	Timer/Counter 2 Control	00000000	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
T2MOD	C9H Bank0	Timer/Counter 2 Mode	0-----00	TCLKP2	-	-	-	-	-	T2OE	DCEN
RCAP2L	CAH Bank0	Timer/Counter 2 Reload /Capture Low Byte	00000000	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
RCAP2H	CBH Bank0	Timer/Counter 2 Reload /Capture High Byte	00000000	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
TL2	CCH Bank0	Timer/Counter 2 Low Byte	00000000	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
TH2	CDH Bank0	Timer/Counter 2 High Byte	00000000	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
T3CON	88H Bank1	Timer/Counter 3 Control	0-00-000	TF3	-	T3PS.1	T3PS.0	-	TR3	T3CLKS.1	T3CLKS.0
SWTHL	89H Bank1	Timer/Counter data switch	------00	-	-	-	-	-	-	T5HLCON	T3HLCON
TL3	8CH Bank1	Timer/Counter 3 Low Byte	00000000	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0
TH3	8DH Bank1	Timer/Counter 3 High Byte	00000000	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0
T4CON	C8H Bank1	Timer/Counter 4 Control	00000000	TF4	TC4	T4PS1	T4PS0	T4M1	T4M0	TR4	T4CLKS
TL4	CCH Bank1	Timer/Counter 4 Low Byte	00000000	TL4.7	TL4.6	TL4.5	TL4.4	TL4.3	TL4.2	TL4.1	TL4.0
TH4	CDH Bank1	Timer/Counter 4 High Byte	00000000	TH4.7	TH4.6	TH4.5	TH4.4	TH4.3	TH4.2	TH4.1	TH4.0
T5CON	C0H Bank1	Timer/Counter 5 Control	0-00--0-	TF5	-	T5PS1	T5PS0	-	-	TR5	-
TL5	CEH Bank1	Timer/Counter 5 Low Byte	00000000	TL5.7	TL5.6	TL5.5	TL5.4	TL5.3	TL5.2	TL5.1	TL5.0
TH5	CFH Bank1	Timer/Counter 5 High Byte	00000000	TH5.7	TH5.6	TH5.5	TH5.4	TH5.3	TH5.2	TH5.1	TH5.0

Table 6.9 EUART SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON	98H Bank0	EUART0 Serial Control	00000000	SM0/FE	SM1/RXOV	SM2/TXCOL	REN	TB8	RB8	TI	RI
SBUF	99H Bank0	EUART0 Serial Data Buffer	00000000	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
SADEN	9BH Bank0	EUART0 Slave Address Mask	00000000	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
SADDR	9AH Bank0	EUART0 Slave Addres	00000000	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
PCON	87H Bank0	Power & serial Control	00--0000	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
SCON1	98H Bank1	EUART1 Serial Control	00000000	SM10/FE1	SM11/ RXOV1	SM12/ TXCOL1	REN1	TB18	RB18	TI1	RI1
SBUF1	99H Bank1	EUART1 Serial Data Buffer	00000000	SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0
SADEN1	9AH Bank1	EUART1 Slave Address Mask	00000000	SADEN1.7	SADEN1.6	SADEN1.5	SADEN1.4	SADEN1.3	SADEN1.2	SADEN1.1	SADEN1.0
SADDR1	9BH Bank1	EUART1 Slave Addres	00000000	SADDR1.7	SADDR1.6	SADDR1.5	SADDR1.4	SADDR1.3	SADDR1.2	SADDR1.1	SADDR1.0
SBRTH	9DH Bank1	EUART1 Baudrate Generator	00000000	SBRTEN	SBRT.14	SBRT.13	SBRT.12	SBRT.11	SBRT.10	SBRT.9	SBRT.8
SBRTL	9CH Bank1	EUART1 Baudrate Generator	00000000	SBRT.7	SBRT.6	SBRT.5	SBRT.4	SBRT.3	SBRT.2	SBRT.1	SBRT.0
BFINE	9EH Bank1	EUART1 Baudrate Generator	0000----	BFINE.7	BFINE.6	BFINE.5	BFINE.4	-	-	-	-

Table 6.10 SPI SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPCON	A2H Bank0	SPI Control	00000000	DIR	MSTR	CPHA	CPOL	SSDIS	SPR2	SPR1	SPR0
SPSTA	F8H Bank0	SPI Status	00000---	SPEN	SPIF	MODF	WCOL	RXOV	-	-	-
SPDAT	A3H Bank0	SPI Data	00000000	SPDAT7	SPDAT6	SPDAT5	SPDAT4	SPDAT3	SPDAT2	SPDAT1	SPDAT0

Table 6.11 ADC SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	93H Bank0	ADC Control	00000000	ADON	ADCIF	EC	REFC	SCH2	SCH1	SCH0	GO/$\overline{\text{DONE}}$
ADT	94H Bank0	ADC Time Configuration	00000000	TADC2	TADC1	TADC0	CDIR	TS3	TS2	TS1	TS0
ADCH	95H Bank0	ADC Channel Configuration	00000000	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
ADDL	96H Bank0	ADC Data Low Byte	----0000	-	-	-	-	A3	A2	A1	A0
ADDH	97H Bank0	ADC Data High Byte	00000000	A11	A10	A9	A8	A7	A6	A5	A4
ADCON1	92H Bank0	ADC Control 1	-----000	-	-	-	-	-	RESO	CH8	SCH3

Table 6.12 Buzzer SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BUZCON	BDH Bank0	Buzzer output control	----0000	-	-	-	-	BCA2	BCA1	BCA0	BZEN

Table 6.13 LCD SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DISPCON	ABH Bank0	LCD Control	00000000	DISPSEL	LCDON	ELCC	DUTY0	VOL3	VOL2	VOL1	VOL0
DISPCON1	ADH Bank0	LCD Control 1	00000000	MODSW	DUTY2	DUTY1	RLCD	FCCTL1	FCCTL0	MOD1	MOD0
DISPCLK0	ACH Bank0	LCD clock 0	------00	-	-	-	-	-	-	DCK1	DCK0
P0SS	B6H Bank0	P0 mode select	00000000	P4S7	P4S6	P4S5	P5S5	P5S4	P0S2	P0S1	P0S0
P1SS	9CH Bank0	P1 mode select	00000000	P1S7	P1S6	P1S5	P1S4	P1S3	P1S2	P1S1	P1S0
P2SS	9DH Bank0	P2 mode select	00000000	P2S7	P2S6	P2S5	P2S4	P2S3	P2S2	P2S1	P2S0
P3SS	9EH Bank0	P3 mode select	00000000	P3S7	P3S6	P3S5	P3S4	P3S3	P3S2	P3S1	P3S0

Table 6.14 LED SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DISPCON	ABH Bank0	LED Control	00-0----	DISPSEL	LEDON	-	DUTY0	-	-	-	-
DISPCON1	ADH Bank0	LED Control 1	000-----	MODSW	DUTY2	DUTY1	-	-	-	-	-
DISPCLK0	ACH Bank0	LED clock 0	------00	-	-	-	-	-	-	DCK1	DCK0
P1SS	9CH Bank0	P1 mode select	00000000	P1S7	P1S6	P1S5	P1S4	P1S3	P1S2	P1S1	P1S0
P3SS	9EH Bank0	P3 mode select	00000000	P3S7	P3S6	P3S5	P3S4	P3S3	P3S2	P3S1	P3S0

Table 6.15 PWM SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMEN	CFH Bank0	PWM0 timer enable	00000000	EPWM0	EFLT	PWM01COE	PWM01BOE	PWM01AOE	PWM0COE	PWM0BOE	PWM0AOE
PWMLO	E7H Bank0	PWM0 register Lock	00000000	PWMLO.7	PWMLO.6	PWMLO.5	PWMLO.4	PWMLO.3	PWMLO.2	PWMLO.1	PWMLO.0
PWM0C	D2H Bank0	12-bit PWM0 Control	00000000	PWM0IE	PWM0IF	TnCK02	FLTS	FLTC	PWM0S	TnCK01	TnCK00
PWM0PL	D3H Bank0	12-bit PWM0 Period Control low byte	00000000	PP0.7	PP0.6	PP0.5	PP.4	PP0.3	PP0.2	PP0.1	PP0.0
PWM0PH	D4H Bank0	12-bit PWM0 Period Control high byte	----0000	-	-	-	-	PP0.11	PP0.10	PP0.9	PP0.8
PWM0DL	D5H Bank0	12-bit PWM0 Duty Control low byte	00000000	PD0.7	PD0.6	PD0.5	PD0.4	PD0.3	PD0.2	PD0.1	PD0.0
PWM0DH	D6H Bank0	12-bit PWM0 Duty Control high byte	----0000	-	-	-	-	PD0.11	PD0.10	PD0.9	PD0.8
PWM0DT	D1H Bank0	12-bit PWM0 Dead time control	00000000	DT0.7	DT0.6	DT0.5	DT0.4	DT0.3	DT0.2	DT0.1	DT0.0
PWM1C	D9H Bank0	8-bit PWM1 Control	0000-000	PWM1EN	PWM1S	TnCK11	TnCK10	-	PWM1IE	PWM1IF	PWM1OE
PWM1P	DAH Bank0	8-bit PWM1 Period Control	00000000	PP1.7	PP1.6	PP1.5	PP1.4	PP1.3	PP1.2	PP1.1	PP1.0
PWM1D	DBH Bank0	8-bit PWM1 Duty Control	00000000	PD1.7	PD1.6	PD1.5	PD1.4	PD1.3	PD1.2	PD1.1	PD1.0

Table 6.16 LPD SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPDCON	B3H Bank0	LPD Control	00000000	LPDEN	LPDF	LPDMD	LPDIF	LPDS3	LPDS2	LPDS1	LPDS0

Table 6.17 CRC SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CRCCON	FDH Bank0	CRC verify control	00--0000	CRC_GO	CRCIF	-	-	CRCADR3	CRCADR2	CRCADR1	CRCADR0
CRCDL	F9H Bank0	CRC verify result low byte	00000000	CRCD7	CRCD6	CRCD5	CRCD4	CRCD3	CRCD2	CRCD1	CRCD0
CRCDH	FAH Bank0	CRC verify result high byte	00000000	CRCD15	CRCD14	CRCD13	CRCD12	CRCD11	CRCD10	CRCD9	CRCD8

Note: *- :Unimplemented*

SFR Map

Bank0

	Bit addressable	**Non Bit addressable**							
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	
F8H	SPSTA	CRCDL	CRCDH	IB_OFFSET	IB_DATA	CRCCON			FFH
F0H	B	AUXC	IB_CON1	IB_CON2	IB_CON3	IB_CON4	IB_CON5	XPAGE	F7H
E8H	EXF0	P0PCR	P1PCR	P2PCR	P3PCR	P4PCR		P0OS	EFH
E0H	ACC	P0CR	P1CR	P2CR	P3CR	P4CR		PWMLO	E7H
D8H	EXF1	PWM1C	PWM1P	PWM1D					DFH
D0H	PSW	PWM0DT	PWM0C	PWM0PL	PWM0PH	PWM0DL	PWM0DH		D7H
C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2		PWMEN	CFH
C0H	P4	CMP1CON	CMP2CON	CMPCON0	CMPCON1	INVCON	INVCTL	INVCTH	C7H
B8H	IPL0	IPL1	IENC	IENC1		BUZCON			BFH
B0H	P3	RSTSTAT	CLKCON	LPDCON	IPH0	IPH1	P0SS		B7H
A8H	IEN0	IEN1	DISPCLK1	DISPCON	DISPCLK0	DISPCON1			AFH
A0H	P2	SCMCON	SPCON	SPDAT		ISPLO	ISPCON	FLASHCON	A7H
98H	SCON	SBUF	SADDR	SADEN	P1SS	P2SS	P3SS		9FH
90H	P1		ADCON1	ADCON	ADT	ADCH	ADDL	ADDH	97H
88H	TCON			EXCON			SUSLO		8FH
80H	P0	SP	DPL	DPH	DPL1	DPH1	INSCON	PCON	87H
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	

Bank1

	Bit addressable	**Non Bit addressable**							
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	
F8H									FFH
F0H	B	AUXC						XPAGE	F7H
E8H		P5PCR							EFH
E0H	ACC	P5CR							E7H
D8H									DFH
D0H	PSW								D7H
C8H	T4CON				TL4	TH4	TL5	TH5	CFH
C0H	T5CON								C7H
B8H	IPL0	IPL1							BFH
B0H					IPH0	IPH1			B7H
A8H	IEN0	IEN1							AFH
A0H									A7H
98H	SCON1	SBUF1	SADDR1	SADEN1	SBRTL	SBRTH	BFINE		9FH
90H									97H
88H	T3CON	SWTHL			TL3	TH3	SUSLO		8FH
80H	P5	SP	DPL	DPH	DPL1	DPH1	INSCON	PCON	87H
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	

Note: *The unused addresses of SFR are not available.*

7. Normal Function

7.1 CPU

7.1.1 CPU Core SFR

Feature

- CPU core registers: ACC, B, PSW, SP, DPL, DPH

Accumulator

ACC is the Accumulator register. Instruction system adopts A as mnemonic symbol of accumulator.

B Register

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Stack Pointer (SP)

The Stack Pointer Register is 8 bits special register, It is incremented before data is stored during PUSH, CALL executions and it is decremented after data is out of stack during POP, RET, RETI executions. The stack may reside anywhere in on-chip internal RAM (00H-FFH). On reset, the Stack Pointer is initialized to 07H causing the stack to begin at location 08H.

Program Status Word Register (PSW)

The PSW register contains program status information.

Data Pointer Register (DPTR)

DPTR consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

Table 7.1 PSW Register

D0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset Value (POR/WDT/LVR/PIN))	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	CY	**Carry flag bit** 0: no carry or borrow in an arithmetic or logic operation 1: a carry or borrow in an arithmetic or logic operation
6	AC	**Auxiliary Carry flag bit** 0: no auxiliary carry or borrow in an arithmetic or logic operation 1: an auxiliary carry or borrow in an arithmetic or logic operation
5	F0	**F0 flag bit** Available to the user for general purposes
4-3	RS[1:0]	**R0-R7 Register bank select bits** 00: Bank0 (Address to 00H-07H) 01: Bank1 (Address to 08H-0FH) 10: Bank2 (Address to 10H-17H) 11: Bank3 (Address to 18H-1FH)
2	OV	**Overflow flag bit** 0: no overflow happen 1: an overflow happen
1	F1	**F1 flag bit** Available to the user for general purposes
0	P	**Parity flag bit** 0: In the Accumulator, the bits whose value is 1 is even number 1: In the Accumulator, the bits whose value is 1 is odd number

7.1.2 Enhanced CPU core SFRs

- Extended 'MUL' and 'DIV' instructions: 16bit X 8bit, 16bit/8bit
- Dual Data Pointer
- Enhanced CPU core registers: AUXC, DPL1, DPH1, INSCON

The SH79F3283 has modified 'MUL' and 'DIV' instructions. These instructions support 16 bit operand. A new register - the register AUXC is applied to hold the upper part of the operand/result.

The AUXC register is used during 16 bit operand multiply and divide operations. For other instructions it can be treated as another scratch pad register.

After reset, the CPU is in standard mode, which means that the 'MUL' and 'DIV' instructions are operating like the standard 8051 instructions. To enable the 16 bit mode operation, the corresponding enable bit in the INSCON register must be set.

	Operation		Result		
			A	B	AUXC
MUL	INSCON.2 = 0; 8 bit mode	(A)*(B)	Low Byte	High Byte	---
	INSCON.2 = 1; 16 bit mode	(AUXC A)*(B)	Low Byte	Middle Byte	High Byte
DIV	INSCON.3 = 0; 8 bit mode	(A)/(B)	Quotient Low Byte	Remainder	---
	INSCON.3 = 1; 16 bit mode	(AUXC A)/(B)	Quotient Low Byte	Remainder	Quotient High Byte

Dual Data Pointer

Using two data pointers can accelerate data memory moves. The standard data pointer is called DPTR and the new data pointer is called DPTR1.

DPTR1 is similar to DPTR, which consists of a high byte (DPH1) and a low byte (DPL1). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

The DPS bit in INSTCON register is used to choose the active pointer by setting 1 or 0. And all DPTR-related instructions will use the currently selected data pointer.

7.1.3 Register

Table 7.2 Data Pointer Select Register

86H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INSCON	-	BKS0	-	-	DIV	MUL	-	DPS
R/W	-	R/W	-	-	R/W	R/W	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	-	-	0	0	-	0

Bit Number	Bit Mnemonic	Description
6	**BKS0**	**SFR Bank Selection Bit** 0: SFR Bank0 selected 1: SFR Bank1 selected
3	**DIV**	**16 bit/8 bit Divide Selection Bit** 0: 8 bit Divide 1: 16 bit Divide
2	**MUL**	**16 bit/8 bit Multiply Selection Bit** 0: 8 bit Multiply 1: 16 bit Multiply
0	**DPS**	**Data Pointer Selection Bit** 0: Data pointer 1: Data pointer1

7.2 RAM

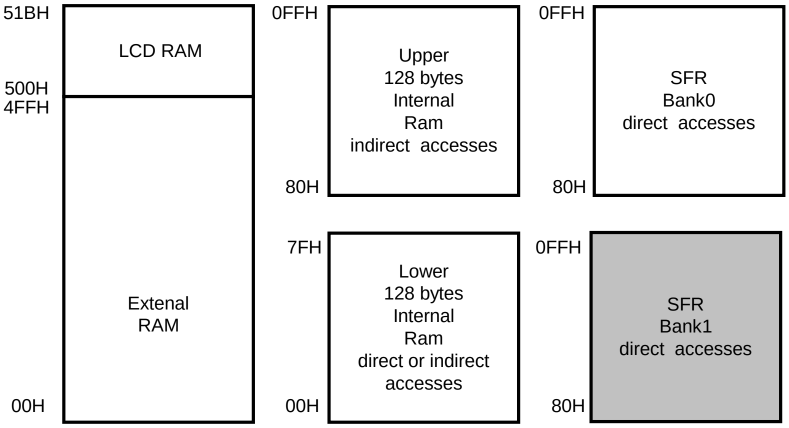
7.2.1 Features

SH79F3283 provides both internal RAM and external RAM for random data storage. The internal data memory is mapped into four separated segments:

- The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- The Special Function Registers (SFR, addresses 80H to FFH) are directly addressable only.
- The 1280 bytes of external RAM (addresses 00H to FFH) are indirectly accessed by MOVX instructions.

The Upper 128 bytes occupy the same address space as SFR, but they are physically separate from SFR space. When an instruction accesses an internal location above address 7FH, the CPU can distinguish whether to access the upper 128 bytes data RAM or to access SFR by different addressing mode of the instruction.

SH79F3283 provides an extra 1280 bytes of RAM to support high-level language in external data space. Also, SH79F3283 provides 28 bytes LCD RAM (500H - 51BH).



The Internal and External RAM Configuration

The SH79F3283 provides traditional method for accessing of external RAM. Use *MOVXA, @Ri* or *MOVX @Ri, A;* to access external low 256 bytes RAM; *MOVX A, @DPTR* or *MOVX @DPTR, A* also to access external 1308 bytes RAM.

In SH79F3283 the user can also use XPAGE register to access external RAM only with *MOVX A, @Ri* or *MOVX @Ri, A* instructions. The user can use XPAGE to represent the high byte address of RAM above 256 Bytes.

In Flash SSP mode, the XPAGE can also be used as sector selector (Refer to SSP Function).

7.2.2 Register

Table 7.3 Data Memory Page Register

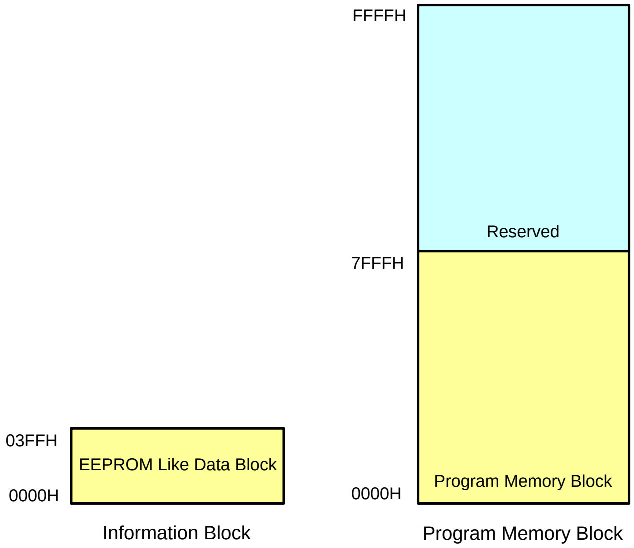
F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	-	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
6-0	**XPAGE[6:0]**	RAM Page Selector

7.3 Flash Program Memory

7.3.1 Features

- The program memory consists 32 X 1KB sectors, total 32KB
- Programming and erase can be done over the full operation voltage range
- Write, read and erase operation are all supported by In-Circuit Programming (ICP)
- Support overall/sector erase and programming
- Minimum program/erase cycles: Program area: 10000
  EEPROM-like area: 100,000
- Minimum years data retention: 10
- Low power consumption



The SH79F3283 embeds 32K flash program memory for program code. The flash program memory provides electrical erasure and programming and supports In-Circuit Programming (ICP) mode and Self-Sector Programming (SSP) mode. Every sector is 1024 bytes.

The SH79F3283 also embeds 1024 bytes EEPROM-like memory block for storing user data. Every sector is 256 bytes. It has 4 sectors.

Flash operation defined:

In-Circuit Programming (ICP): Through the Flash programmer to wipe the Flash memory, read and write operations.

Self-Sector Programming (SSP) mode: User Program code run in Program Memory to wipe the flash memory, read and write operations.

Flash Memory Supports the Following Operations:

(1) Code Protection Control Mode

SH79F3283 code protection function provides a high-performance security measures for the user. Each partition has four modes are available.
Code protection mode 0: allow/forbid any programmer write/read operations (not including overall erasure).
Code protection mode 1: allow/forbid through MOVC instructions to read operation in other sectors, or through SSP mode to erased/write operation.
Code-protect control mode 2: Used to enable/disable the erase/write EEPROM operation through **SSP** Function.
Code-protect control mode 3: Customer password, write by customer, consists of 6 bytes. To enable the wanted protect mode, the user must use the Flash Programmer to set the corresponding protect bit.
The user must use the following two ways to complete code protection control mode Settings:
1. Flash programmer in ICP mode is set to corresponding protection bit to enter the protected mode.
2. The SSP mode does not support code protection control mode programming.

(2) Mass Erase

Regardless of the state of the code protection control mode, the overall erasure operation will erase all programs, code options, the code protection bit, but they will not erase EEPROM-like memory block.
The user must use the following way to complete the overall erasure:
The Flash programmer in ICP mode sends overall erasure instruction to run overall erasure.
The SSP mode does not support overall erasure mode.

(3) Sector Erase

Sector erasure operations will erase the content of selected sector. The user program (SSP) and Flash programmer can perform this operation.
For user programs to perform the operation, code protection mode 1 in the selected sector must be forbidden.
For Flash programmer to perform the operation, code protection mode 0 in the selected sector must be forbidden.
The user must use one of the following two ways to complete sector erasure:

1. Flash programmer in ICP mode send sector erasure instruction to run sector erasure.
2. Through the SSP function sends sector erasure instruction to run sector erasure (see chapter SSP).

(4) EEPROM-like Memory Block Erasure

EEPROM-like memory block erasure operations will erase the content in EEPROM-like memory block. The user program (SSP) and Flash programmer can perform this operation.
The user must use one of the following two ways to complete EEPROM-like memory block erasure:

1. Flash programmer in ICP mode send EEPROM-like memory block erasure instruction to run EEPROM-like memory block erasure.
2. Through the SSP function send EEPROM-like memory block erasure instruction to run EEPROM-like memory block erasure (see chapter SSP).

(5) Write/Read Code

Write/read code operation can read or write code from flash memory block. The user program (SSP) and Flash programmer can perform this operation.
For user programs to perform the operation, code protection mode 1 in the selected sector must be forbidden. Regardless of the security bit Settings or not, the user program can read/write the sector which contains program itself.
For Flash programmer to perform the operation, code protection mode 0 in the selected sector must be forbidden.
The user must use one of the following two ways to complete write/read code:

1. Flash programmer in ICP mode send write/read code instruction to run write/read code.
2. Through the SSP function send write/read code instruction to run write/read code.

(6) Write/Read EEPROM-like Memory Block

EEPROM-like memory block operation can read or write data from EEPROM-like memory block. The user program (SSP) and Flash programmer can perform this operation.
The user must use one of the following two ways to complete write/read EEPROM-like memory block:

1. Flash programmer in ICP mode send write/read EEPROM-like memory block instruction to run write/read EEPROM-like memory block.
2. Through the SSP function send write/read EEPROM-like memory block instruction to run write/read EEPROM-like memory block.

Flash Memory Block Operation Summary

Operation	ICP	SSP
Code protection	support	non support
Sector erasure	support (no security bit)	support (no security bit)
Overall erasure	support	non support
EEPROM-like memory block erasure	support	support
Write/read code	Support (no security bit)	support (no security bit)
Read/write EEPROM-like memory block	support	support

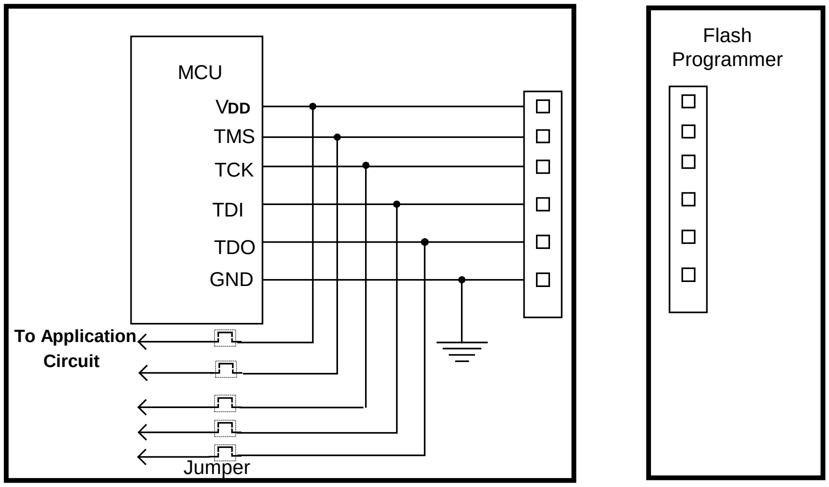
7.3.2 Flash Operation in ICP Mode

ICP has two modes: four JTAG pins and single SWE pin. ICP mode is performed without removing the micro-controller from the system. In ICP mode, the user system must be power-off, and the programmer can refresh the program memory through ICP programming interface. The ICP programming interface consists of 6 pins (V_{DD}, GND, TCK, TDI, TMS, TDO/SWE).

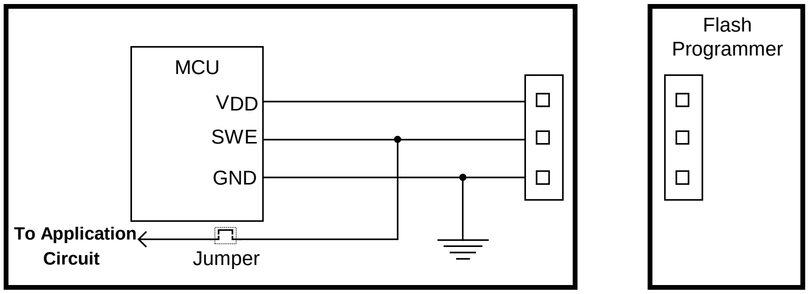
SH79F3283 provides two types JTAG pins, the four JTAG pins (TDO, TDI, TCK, TMS) and the single SWE pin (SWE) are used to enter the programming mode. Only after the four pins are inputted the specified waveform, the CPU will enter the programming mode. For more detail description please refers to the FLASH Programmer's user guide.

In ICP mode, all the flash operations are completed by the programmer through 6-wire interface. Since the program signal is very sensitive, 6 jumpers are needed (V_{DD}, GND, TDO/SWE, TDI, TCK, TMS) to separate the program pins from the application circuit, as show in the following diagram.

Four JTAG Pins Mode:



Single SWE Pin Mode:



The recommended steps are as following:

(1) The jumpers must be open to separate the programming pins from the application circuit before programming.

(2) Connect the programming interface with programmer and begin programming.

(3) Disconnect programmer interface and connect jumpers to recover application circuit after programming is complete.

7.4 SSP Function

The SH79F3283 provides SSP (Self Sector Programming) function, each sector can be sector erased or programmed by the user’s code if the selected sector is not be protected. But once sector has been programmed, it cannot be reprogrammed before sector erase.

The SH79F3283 builds in a complex control flow to prevent the code from carelessly modification. If the dedicated conditions are not met (IB_CON2-5), the SSP will be terminated.

7.4.1 Register

Table 7.4 Memory Page Register for Programming (For Flash memory, one sector is 1024 bytes)

F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	-	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
6-2	**XPAGE[6:2]**	Sector of the flash memory to be programmed, 0000 means sector 0, and so on
1-0	**XPAGE[1:0]**	High 2 Address of the flash memory sector to be programmed

Table 7.5 Memory Page Register for Programming (For EEPROM-like memory, one sector is 256 bytes)

F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	-	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
6-2	**XPAGE[6:2]**	Reserved
1-0	**XPAGE[1:0]**	Sector of the flash memory to be programmed, 00 means sector 0, and so on

Table 7.6 Offset of Flash Memory for Programming

FBH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFFSET	IB_OFFSET.7	IB_OFFSET.6	IB_OFFSET.5	IB_OFFSET.4	IB_OFFSET.3	IB_OFFSET.2	IB_OFFSET.1	IB_OFFSET.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_OFFSET[7:0]**	Low 8 Address of Offset of the flash memory sector to be programmed

Table 7.7 Data Register for Programming

FCH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_DATA	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_DATA[7:0]**	Data to be programmed

Table 7.8 SSP Type select Register

F2H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON1	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	IB_CON1[7:0]	**SSP Type select** 0xE6: Sector Erase 0x6E: Sector Programming

Table 7.9 SSP Flow Control Register1

F3H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON2	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	IB_CON2[3:0]	Must be 05H, otherwise Flash Programming will terminate

Table 7.10 SSP Flow Control Register2

F4H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON3	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	IB_CON3[3:0]	Must be 0AH,otherwise Flash Programming will terminate

Table 7.11 SSP Flow Control Register3

F5H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON4	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

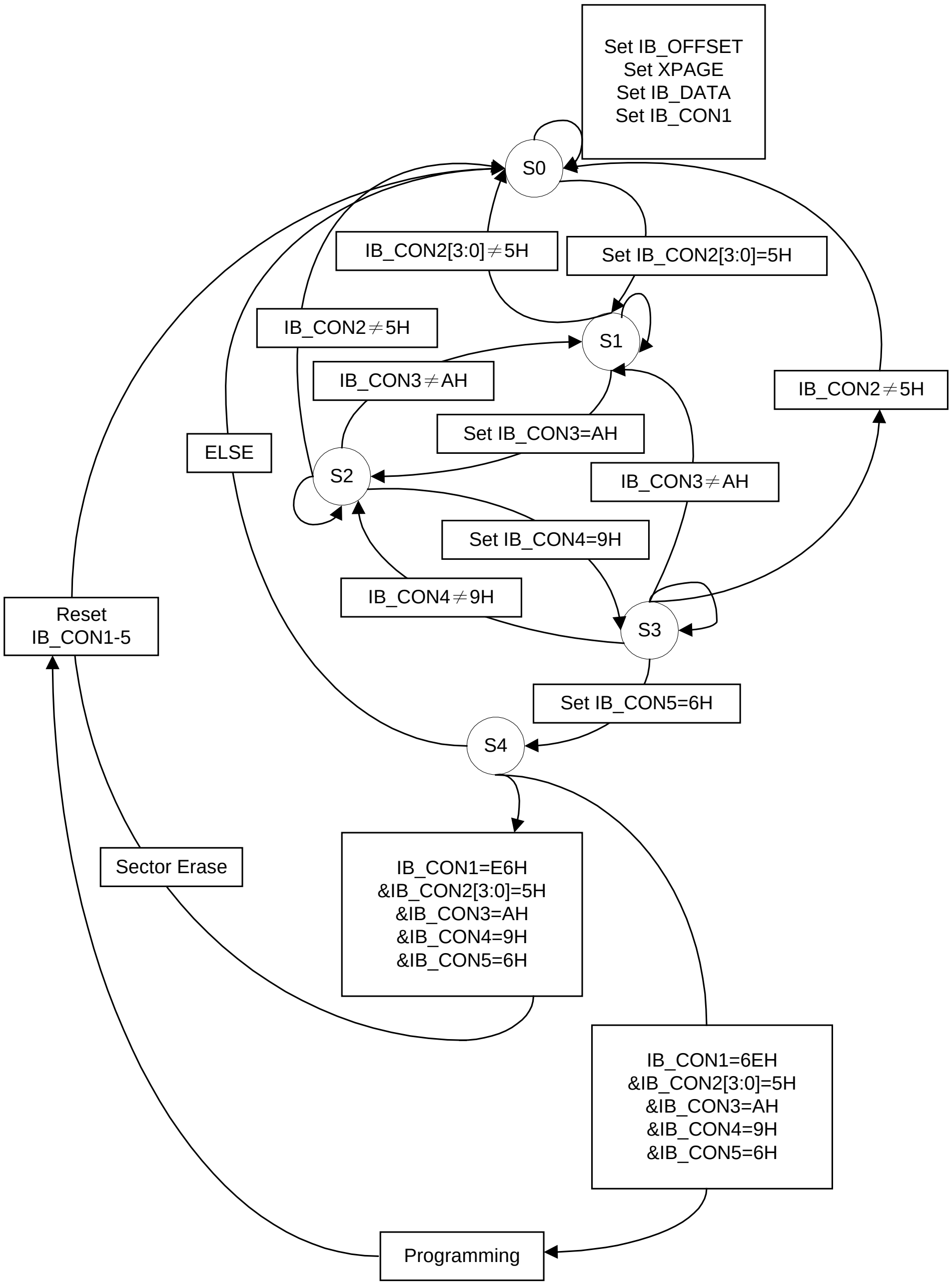
Bit Number	Bit Mnemonic	Description
3-0	IB_CON4[3:0]	Must be 09H, otherwise Flash Programming will terminate

Table 7.12 SSP Flow Control Register4

F6H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON5	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	IB_CON5[3:0]	Must be 06H, otherwise Flash Programming will terminate

7.4.2 Flash Control Flow



7.4.3 SSP Programming Notice

To successfully complete SSP programming, the user’s software must be set as the following the steps:

(1) For Code/Data Programming:

1. Disable interrupt;
2. Fill in the XPAGE, IB_OFFSET for the corresponding address;
3. Fill in IB_DATA if programming is wanted;
4. Fill in IB_CON1-5 sequentially;
5. Add 4 nops for more stable operation;
6. Code/Data programming, CPU will be in IDLE mode;
7. Go to Step 2 if more data are to be programmed;
8. Clear XPAGE; enable interrupt if necessary.

(2) For Sector Erase:

1. Disable interrupt;
2. Fill in the XPAGE for the corresponding sector;
3. Fill in IB_CON1-5 sequentially;
4. Add 4 NOPs for more stable operation;
5. Sector Erase, CPU will be in IDLE mode;
6. Go to step 2 if more sectors are to be erased;
7. Clear XPAGE; enable interrupt if necessary.

(3) For Code Reading:

Just Use “MOVC A, @A+DPTR” or “MOVC A, @A+PC”.

(4) For EEPROM-Like:

Step is same as code programming, the differences are:
1. Set FAC bit in FLASHCON register before programming or erase EEPROM-Like;
2. One sector of EEPROM-Like is 256 bytes, not 1024 bytes.

Note:

(1) The system clock is not less than 200 KHZ to ensure normal FLASH programming

(2) FAC must be cleared when you don't need to do EEPROM-like operation.

FLASHCON Register Description is as follows:

Table 7.13 Flash Access Control Register

A7H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FLASHCON	-	-	-	-	-	-	-	FAC
R/W	-	-	-	-	-	-	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	-	0

Bit Number	Bit Mnemonic	Description
7-1	**-**	**Reserved**
0	**FAC**	**FAC: Flash access control** 0: MOVC or SSP access main memory 1: MOVC or SSP access EEPROM-like

7.5 System Clock and Oscillator

7.5.1 Features

- Six oscillator types: 32.768kHz crystal oscillator, crystal oscillator, ceramic oscillator and 16MHz/12MHz/8MHz /128kHz internal RC
- 4 Oscillator pin (XTAL1, XTAL2, XTALX1, XTALX2)
- Built-in 16MHz/12MHz/8MHz/128KHz Internal RC
- Built-in 32.768kHz speed up circuit
- Built-in system clock prescaler

7.5.2 Clock Definition

The SH79F3283 have several internal clocks defined as below:

OSCCLK: the oscillator clock is selected from the four oscillator types (32.768kHz crystal oscillator, crystal oscillator, ceramic oscillator and internal 16M/12M/8M RC/128K oscillator from XTAL input). f_{OSC} is defined as the OSCCLK frequency. t_{OSC} is defined as the OSCCLK period.

OSCXCLK: the oscillator clock is select from the four oscillator types (32.768kHz crystal oscillator, crystal oscillator, ceramic oscillator and internal 16M/12M/8M RC/128K oscillator from XTALX input). f_{OSC} is defined as the OSCXCLK frequency. t_{OSC} is defined as the OSCXCLK period.

***Note:** OSCXCLK does not exist when code option OP_OSC is not 0011, 0110, 1010, 1101 (32.768kHz/128kHz RC is not selected, Refer to **code option** section for details)*

WDTCLK: the internal WDT RC clock. f_{WDT} is defined as the WDTCLK frequency. t_{WDT} is defined as the WDTCLK period.

OSCSCLK: the input clock of system clock frequency prescaler. It can be OSCCLK or OSCXCLK. f_{OSCS} is defined as the OSCSCLK frequency. t_{OSCS} is defined as the OSCSCLK period.

SYSCLK: system clock, the output clock of system clock prescaler. It is the CPU instruction clock. f_{SYS} is defined as the SYSCLK frequency. t_{SYS} is defined as the SYSCLK period.

7.5.3 Description

SH79F3283 has six oscillator types: 32.768kHz crystal oscillator, crystal oscillator/ceramic oscillator (2MHz-16MHz) and internal RC (16MHz, 12MHz, 8MHz, 128KHz), which is selected by code option OP_OSC (Refer to code option section for details). SH79F3283 has 4 oscillator pins (XTAL1, XTAL2, XTALX1, XTALX2), which can generate 1 or 2 clocks from 3 oscillator types. They also are selected by code option OP_OSC (Refer to code option section for details). The oscillator generates the basic clock pulse that provides the system clock to supply CPU and on-chip peripherals.

7.5.4 Register

Table 7.14 System Clock Control Register

B2H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	32K_SPDUP	CLKS1	CLKS0	SCMIF	HFON	FS	-	-
R/W	R/W	R/W	R/W	R	R/W	R/W	-	-
Reset Value (POR/WDT/LVR/PIN)	1	1	1	0	0	0	-	-

Bit Number	Bit Mnemonic	Description
7	**32K_SPDUP**	**32.768kHz oscillator speed up mode control bit** 0: 32.768kHz oscillator normal mode, cleared by software. 1: 32.768kHz oscillator speed up mode, set by hardware or software. This control bit is set by hardware automatically in all kinds of RESET such as Power on reset, watch dog reset etc. to speed up the 32.768kHz Oscillator oscillating, shorten the 32.768kHz oscillator start-oscillating time. And this bit also can be set or cleared by software if necessary. Such as set before entering Power-down mode and cleared when Power-down mode wakes up. It should be noticed that turning off 32.768kHz oscillator speed up (clear this bit) could reduce the system power consumption. Only when code option OP_OSC is 1010 or 1101, this bit is valid. (32.768kHz oscillator is selected, Refer to **code option** section for details)

(to be continued)

(continue)

6-5	**CLKS [1: 0]**	**SYSCLK Prescaler Register** 00: $f_{SYS} = f_{OSCS}$ 01: $f_{SYS} = f_{OSCS}/2$ 10: $f_{SYS} = f_{OSCS}/4$ 11: $f_{SYS} = f_{OSCS}/12$ If 32.768kHz oscillator is selected as OSCSCLK, these control bits is invalid.
3	**HFON**	**OSCXCLK On-Off control Register** 0: turn off OSCXCLK 1: turn on OSCXCLK Only when code option OP_OSC is 0011, 0110, 1010, 1101 this bit is valid. (32.768kHz oscillator/128kHz internal RC is selected, refer to **code option** section for details)
2	**FS**	**Frequency Select Register** 0: 32.768kHz/128kHz is selected as OSCSCLK. 1: OSCXCLK is selected as OSCSCLK. Only when code option OP_OSC is 0011, 0110, 1010. 1101 this bit is valid. (32.768kHz oscillator/128kHz internal RC is selected, refer to **code option** section)

Note:

(1) If code option OP_OSC is 0011, 1010, OSCXCLK is Internal 12M RC, if code option OP_OSC is 0110, 1101, OSCXCLK is oscillator from XTALX1 input.

(2) HFON and FS is valid only when code option OP_OSC is 0011, 0110, 1010, 1101

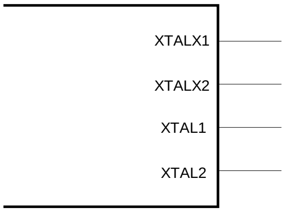
(3) When OSCXCLK is used as OSCSCLK (that is HFON = 1 and FS = 1), HFON is can't be cleared by software.

(4) When OSCSCLK changed from 32.768kHz/128kHz to OSCXCLK, if OSCXCLK is off, the setting must be done as the following steps:
a. Set HFON = 1 to turn on the OSCXCLK
b. Wait at least Oscillator Warm-up timer (Refer to Warm-up Timer section for details)
c. Set FS = 1 to select OSCXCLK as OSCSCLK.

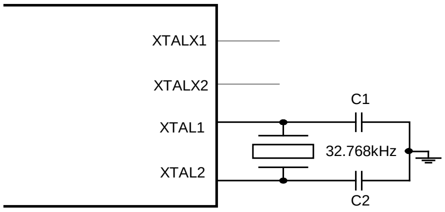
(5). When OSCSCLK changed from OSCXCLK to 32.768kHz/128kHz, the setting must be done as the following steps:
a. Clear FS to select 32.768kHZ/128k as OSCSCLK.
b. Add one NOP
c. Clear HFON (reduce power consumption)
d. Add four NOPs.

7.5.5 Oscillator Type

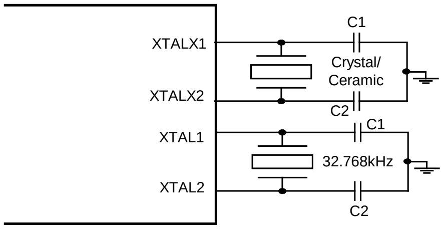
(1) OP_OSC = 0000, 0001, 0011, 0100: internal RC 16M/12M/8M/128K, XTAL, XTALX shared with IO.



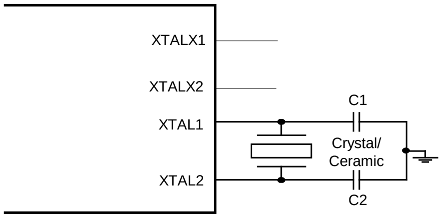
(2) OP_OSC = 1010, 1011: 32.768kHz Crystal Oscillator at XTAL, Internal RC can be enabled, XTALX shared with IO.



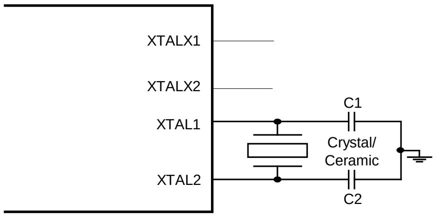
(3) OP_OSC = 1101: 32.768kHz Crystal Oscillator at XTAL, 2M - 12M Crystal/Ceramic oscillator from XTALX input



(4) OP_OSC = 1110: 2M - 12M Crystal/Ceramic oscillator from XTAL input, XTALX shared with IO.



(5) OP_OSC = 0110: 128kHz internal RC, 2M - 12M Crystal/Ceramic oscillator from XTAL input, XTALX shared with IO.



7.5.6 Capacitor Selection for Oscillator

Ceramic Oscillator		
Frequency	**C1**	**C2**
3.58MHz	-	-
4MHz	-	-

Crystal Oscillator		
Frequency	**C1**	**C2**
32.768kHz	10 - 12pF	10 - 12pF
4MHz	8 - 22pF	8 - 22pF
12MHz	8 - 22pF	8 - 22pF

Note:

(1) Capacitor values are used for design guidance only!

(2) These capacitors were tested with the crystals listed above for basic start-up and operation. They are ***not optimized.***

(3) Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

(4) Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures.

7.6 System Clock Monitor (SCM)

In order to enhance the system reliability, SH79F3283 contains a system clock monitor (SCM) module. If the system clock breaks down (for example the external oscillator stops oscillating), the built-in SCM will switch the OSCCLK to the internal RC clock, and set system clock monitor bit (SCMIF) to 1. And the SCM interrupt will be generated when EA and ESCM is enabled. If the external oscillator comes back, SCM will switch the OSCCLK back to the external oscillator and clears the SCMIF automatically.

Select SCM clock by set up SCMCON, if the built-in SCM detect the system clock breaks down, that will switch the OSCCLK to the internal SCM clock.

The SCM function is valid when using external clock only.

Notes:

The SCMIF is read only register; it can be clear to 0 or set to 1 by hardware only.

If SCMIF is cleared, the SCM switches the system clock to the state before system clock breaks down automatically.

If Internal RC is selected as OSCSCLK by code option (Refer to ***code option*** *section for detail), the SCM can not work.*

Table 7.15 System Clock Control Register

B2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	-	-	-	SCMIF	-	-	-	-
R/W	-	-	-	R	-	-	-	-
Reset Value (POR/WDT/LVR/PIN	-	-	-	0	-	-	-	-

Bit Number	Bit Mnemonic	Description
4	**SCMIF**	**System Clock Monitor flag bit** 0: Clear by hardware to indicate system clock is normal 1: Set by hardware to indicate system clock fails

Table 7.16 SCM Clock Control Register

A1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCMCON	-	-	-	-	-	SCK2	SCK1	SCK0
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN	-	-	-	-	-	0	1	1

Bit Number	Bit Mnemonic	Description
2-0	**SCK[2:0]**	**SCM Clock select bits** 000: 2MHz 001: 4MHz 010: 6MHz 011: 8MHz (Default) 100: 12MHz 101-111: 16MHz

7.7 I/O Port

7.7.1 Features

- 46/42/30 bi-directional I/O ports
- Share with alternative functions

The SH79F3283 has 46 bi-directional I/O ports. The PORT data is put in Px register. The PORT control register (PxCRy) controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PxPCRy when the PORT is used as input (x = 0-5, y = 0-7).

For SH79F3283, some I/O pins can share with alternative functions. There exists a priority rule in CPU to avoid these functions conflicts when all the functions are enabled. (Refer to **Port Share** Section for details).

7.7.2 Register

Table 7.17 Port Control Register

E1H - E5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0CR (E1H, Bank0)	P0CR.7	P0CR.6	P0CR.5	P0CR.4	P0CR.3	P0CR.2	P0CR.1	P0CR.0
P1CR (E2H, Bank0)	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P2CR (E3H, Bank0)	P2CR.7	P2CR.6	P2CR.5	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
P3CR (E4H, Bank0)	P3CR.7	P3CR.6	P3CR.5	P3CR.4	P3CR.3	P3CR.2	P3CR.1	P3CR.0
P4CR (E5H, Bank0)	P4CR.7	P4CR.6	P4CR.5	P4CR.4	P4CR.3	P4CR.2	P4CR.1	P4CR.0
P5CR (E1H, Bank1)	-	-	P5CR.5	P5CR.4	P5CR.3	P5CR.2	P5CR.1	P5CR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PxCRy** **x = 0-5, y = 0-7**	**Port input/output control Register** 0: input mode 1: output mode

Table 7.18 Port Pull up Resistor Control Register

E9H - ECH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0PCR (E9H, Bank0)	P0PCR.7	P0PCR.6	P0PCR.5	P0PCR.4	P0PCR.3	P0PCR.2	P0PCR.1	P0PCR.0
P1PCR (EAH, Bank0)	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P2PCR (EBH, Bank0)	P2PCR.7	P2PCR.6	P2PCR.5	P2PCR.4	P2PCR.3	P2PCR.2	P2PCR.1	P2PCR.0
P3PCR (ECH, Bank0)	P3PCR.7	P3PCR.6	P3PCR.5	P3PCR.4	P3PCR.3	P3PCR.2	P3PCR.1	P3PCR.0
P4PCR (EDH, Bank0)	P4PCR.7	P4PCR.6	P4PCR.5	P4PCR.4	P4PCR.3	P4PCR.2	P4PCR.1	P4PCR.0
P5PCR (E9H, Bank1)	-	-	P5PCR.5	P5PCR.4	P5PCR.3	P5PCR.2	P5PCR.1	P5PCR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PxPCRy** **x = 0-5, y = 0-7**	**Input Port internal pull-high resistor enable/disable control** 0: internal pull-high resistor disabled 1: internal pull-high resistor enabled

Table 7.19 Port Data Register

80H - C0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0 (80H, Bank0)	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
P1 (90H, Bank0)	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P2 (A0H, Bank0)	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
P3 (B0H, Bank0)	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
P4 (C0H, Bank0)	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
P5 (80H, Bank1)	-	-	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**Px.y** **x = 0-5, y = 0-7**	Port Data Register

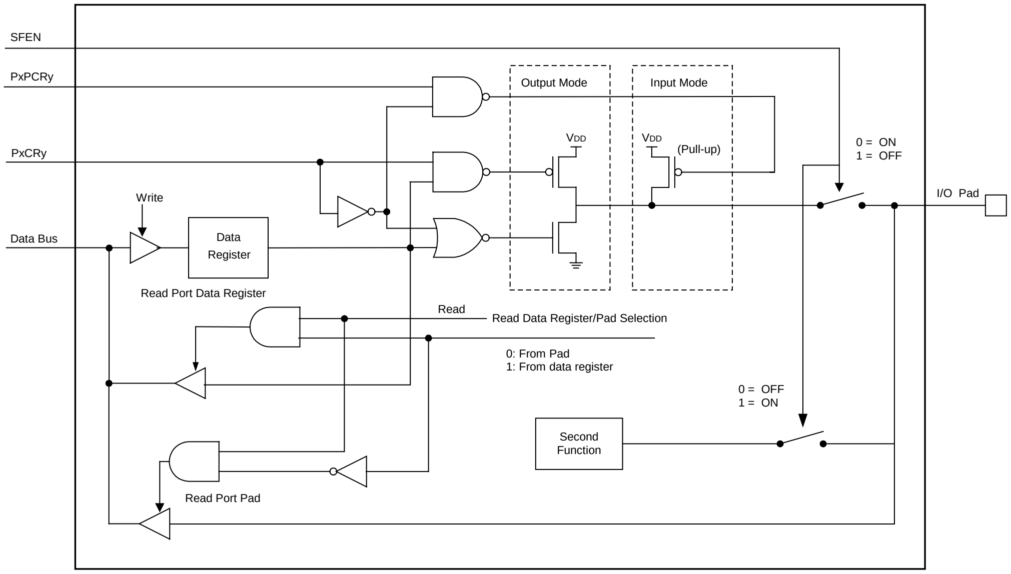
Table 7.20 Port mode select Register

EFH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0OS	-	-	P0OS.5	P0OS.4	-	-	-	-
R/W	-	-	R/W	R/W	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	-	-	0	0	-	-	-	-

Bit Number	Bit Mnemonic	Description
5-4	**P0OS.x** **x = 5-4**	**Port0 output mode select** 0: Port output mode is CMOS 1: Port output mode is N-channel open drain

Note: *P0.4, P0.5 art configured as N-channel open drain I/O, but voltage provided for this pin can't exceed V_{DD}+0.3V.*

7.7.3 Port Diagram



Note:

(1) The input source of reading input port operation is from the input pin directly.

(2) The input source of reading output port operation has two paths, one is from the port data Register, and the other is from the output pin directly.

(3) The read Instruction distinguishes which path is selected: The read-modify-write instruction is for the reading of the data register in output mode, and the other instructions are for reading of the output pin directly.

(4) The destination of writing port operation is the data register regardless of the port shared as the second function or not.

7.7.4 Port Share

The 46/42/30 bi-directional I/O ports can also share second or third special function. But the share priority should obey the **Outer Most Inner Lest** rule:

The out most pin function in **Pin Configuration** has the highest priority, and the inner most pin function has the lowest priority. This means when one pin is occupied by a higher priority function (if enabled), it cannot be used as the lower priority functional pin, even the lower priority function is also enabled. Only until the higher priority function is closed by hardware or software, can the corresponding pin be released for the lower priority function use. Also the function that need pull up resister is also controlled by the same rule.

When port share function is enabled, the user can modify PxCR, PxPCR (x = 0-5), but these operations will have no effect on the port status until the second function was disabled.

When port share function is enabled, any read or write operation to port will only affect the data register. The value of the port pin keeps unchanged until the second function was disabled.

PORT0:

- LCD Segment 17-19 (P0.0-P0.2)
- PWM01B: PWM01B output (P0.0)
- PWM0B: PWM0B output (P0.1)
- PWM01A: PWM01A output (P0.2)
- PWM0A: PWM0A output (P0.3)
- INT0: external inturrupt0 (P0.4)
- INT1: external inturrupt1 (P0.5)
- INT2: external inturrupt2 (P0.6)
- INT3: external inturrupt3 (P0.7)
- T2: Timer2 external input/baud rate clock output (P0.5)
- T2EX: Timer2 reload/capture control (P0.4)
- T4: Timer4 external input/Baud-rate clock output (P0.3)

Table 7.21 PORT0 Share Table

Pin No.			Priority	Function	Enable bit
TQFP48	LQFP44	LQFP32			
47	43	-	1	PWM01B	Set **EPWM1** bit and **PWM01BOE** bit in **PWMEN** Register
			2	SEG17	Clear **DISPSEL** bit in **DISPCON** Register and set **P0S0** in **P0SS** Register
			3	P0.0	Above condition is not met
48	44	-	1	PWM0B	Set **EPWM0** bit and **PWM01BOE** bit in **PWMEN** Register
			2	SEG18	Clear **DISPSEL** bit in **DISPCON** Register and set **P0S1** in **P0SS** Register
			3	P0.1	Above condition is not met
1	1	31	1	PWM01A	Set **EPWM0**bit and **PWM01AOE** bit in **PWMEN** Register
			2	SEG19	Clear **DISPSEL** bit in **DISPCON** Register and set **P0S2** in **P0SS** Register
			3	P0.2	Above condition is not met
2	2	32	1	PWM0A	Set **EPWM0** bit and **PWM01AOE** bit in **PWMEN** Register
			2	T4	Set **TR4** bit and **T4CLKS** bit in **T4CON** register (Auto Pull up) or clear **T4CLKS** bit and set **TC4** bit or set **TR4** bit in Mode2
			3	P0.3	Above condition is not met
3	3	-	1	T2EX	In mode 0, 2, 3, set **EXEN2** bit in **T2CON** register, or in mode 1 set **DCEN** bit in **T2MOD** register or in mode 1, clear **DCEN** bit and set **EXEN2** bit (Auto Pull up)
			2	INT0	Set **EX0** bit in **IEN0** Register and Port0.4 is in input mode
			3	P0.4	Above condition is not met
4	4	-	1	T2	Set **TR2** bit and **C/$\overline{\mathbf{T2}}$** bit in **T2CON** register (Auto Pull up) or clear **C/$\overline{\mathbf{T2}}$** bit and set **T2OE** bit in **T2MOD** register.
			2	INT1	Set **EX1** bit in **IEN0** Register and Port0.5 is in input mode
			3	P0.5	Above condition is not met
5	5	1	1	XTALX2	Selected by Code Option
			2	INT2	Set **EX2** bit in **IEN1** Register and Port0.6 is in input mode
			3	P0.6	Above condition is not met
6	6	2	1	XTALX1	Selected by Code Option
			2	INT3	Set **EX3** bit in **IEN1** Register and Port0.7 is in input mode
			3	P0.7	Above condition is not met

Note: *Pin3, Pin4 art open drain port when P0OS is 30H.*

PORT1:

- LED Segment 1-8 (P1.0-P1.7)
- LCD Segment 1-8 (P1.0-P1.7)
- INT44-INT47 (P1.0-P1.3): External interrupt input

Table 7.22 PORT1 Share Table

Pin No.			Priority	Function	Enable bit
TQFP48	LQFP44	LQFP32			
31-34	27-30	22-25	1	INT44-47	Set **EX4** bit in **IEN1** register and **EXS44-47** bit in **IENC** register, P1.0-P1.3 in input mode
			2	LED S1-4	Set **DISPSEL** bit in **DISPCON** Register and set **P1S0-P1S3** in **P0SS** Register
			3	LCD SEG1-4	Clear **DISPSEL** bit in **DISPCON** Register and set **P1S0-P1S3** in **P0SS** Register
			4	P1.0-P1.3	Above condition is not met
35-38	31-34	26	1	LED S5-8	Set **DISPSEL** bit in **DISPCON** Register and set **P1S4-P1S7** in **P0SS** Register 1
			2	LCD SEG5-8	Clear **DISPSEL** bit in **DISPCON** Register and set **P1S4-P1S7** in **P0SS** Register
			3	P1.4-P1.7	Above condition is not met

PORT2:

- RXD0: EUART0 data input (P2.0)
- TXD0: EUART0 data output (P2.1)
- MOSI: SPI Master output Slave input (P2.2)
- MISO: SPI Master input Slave output (P2.3)
- SCK: SPI Serial Clock (P2.4)
- FLT: Fault input pin (P2.5)
- LCD Segment 9-16 (P2.0-P2.7)
- $\overline{SS}$: SPI Slave selection (P2.5)
- PWM0C: PWM0C output (P2.7)
- PWM01C: PWM01C output (P2.6)

Table 7.23 PORT2 Share Table

Pin No.			Priority	Function	Enable bit
TQFP48	LQFP44	LQFP32			
39	35	27	1	RXD0	Set **REN** bit in **SCON** Register (Auto Pull up)
			2	SEG9	Clear **DISPSEL** bit in **DISPCON** Register and set **P2S0** in **P2SS** Register
			3	P2.0	Above condition is not met
40	36	28	1	TXD0	Do write operation to **SBUF** register
			2	SEG10	Clear **DISPSEL** bit in **DISPCON** Register and set **P2S1** in **P2SS** Register
			3	P2.1	Above condition is not met
41	37	-	1	MOSI	Set **SPEN** bit in **SPSTAT** register in Slave mode (when **SPEN**, **CPHA**, **SSDIS** bits all set in Slave mode, Auto Pull up)
			2	RXD1	Set **REN1** bit in **SCON1** Register (Auto Pull up)
			3	SEG11	Clear **DISPSEL** bit in **DISPCON** Register and set **P2S2** in **P2SS** Register
			4	P2.2	Above condition is not met

(to be continued)

(continued)

42	38	-	1	MISO	Set **SPEN** bit in **SPSTAT** register (when **SPEN** bit in **SPSTAT** register in Master mode, Auto Pull up)
			2	TXD1	Do write operation to **SBUF1** register
			3	SEG12	Clear **DISPSEL** bit in **DISPCON** Register and set **P2S3** in **P2SS** Register
			4	P2.3	Above condition is not met
43	39	-	1	SCK	Set **SPEN** bit in **SPSTAT** register (when **SPEN**, **CPHA**, **SSDIS** bits all set in Slave mode, Auto Pull up)
			2	SEG13	Clear **DISPSEL** bit in **DISPCON** Register and set **P2S4** in **P2SS** Register
			3	P2.4	Above condition is not met
44	40	29	1	FLT	Set **EFLT** bit in **PWMEN** register
			2	$\overline{SS}$	When **SPEN** = 1, Clear **SSDIS** bit in **SPCON** register in SPI Master mode or clear **SSDIS** bit when **CPHA** = 1 in **SPCON** register in SPI slave mode or clear **CPHA** bit in **SPCON** register in SPI slave mode (When **SPEN** = 1 & Master = 1 & **SSDIS** = 1, auto pull-high or **SPEN** = 1 & Master = 0, auto pull-high)
			3	SEG14	Clear **DISPSEL** bit in **DISPCON** Register and set **P2S5** in **P2SS** Register
			4	P2.5	Above condition is not met
45	41	30	1	PWM01C	Set **EPWM1** bit and **PWM01COE** bit in **PWMEN** Register
			2	SEG15	Clear **DISPSEL** bit in **DISPCON** Register and set **P2S6** in **P2SS** Register
			3	P2.6	Above condition is not met
46	42	-	1	PWM0C	Set **EPWM1** bit and **PWM01COE** bit in **PWMEN** Register
			2	SEG16	Clear **DISPSEL** bit in **DISPCON** Register and set **P2S7** in **P2SS** Register
			3	P2.7	Above condition is not met

PORT3:
- LED COM1-COM8 (P3.0-P3.7)
- LCD COM1-COM8 (P3.0-P3.7)
- AN4-AN7: ADC input channel (P3.4-P3.7)

Table 7.24 PORT3 Share Table

Pin No.			Priority	Function	Enable bit
TQFP48	**LQFP44**	**LQFP32**			
23-26	19-22	14-17	1	AN7-AN4	Set **CH7-4** bit in **ADCH** Register and set **ADON** bit in **ADCON** Register, and set **SCH [2:0]**
			2	LED_C8 -LED_C5	Set **P3S7-P3S4** bits in **P3SS** register and set **DISPSEL** bit and set **DUTY** bit in **DISPCON** register
			3	COM8-COM5	Set **P3S7-P3S4** bits in **P3SS** register, clear **DISPSEL** bit and set **DUTY** bit in **DISPCON** register
			4	P3.7-P3.4	Above condition is not met
27-30	23-26	18-21	1	LED_C4 -LED_C1	Set **P3S3-P3S0** bits in **P3SS** register and set **DISPSEL** bit and set **DUTY** bit in **DISPCON** register
			2	COM4-COM1	Set **P3S3-P3S0** bits in **P3SS** register, clear **DISPSEL** bit and set **DUTY** bit in **DISPCON** register
			3	P3.3-P3.0	Above condition is not met

PORT4:

- INT40-INT43 (P4.0-P4.3): External interrupt input
- AN0-AN3, AN8 (P4.0-P4.4): ADC input channel
- LCD SEGMENT22-24 (P4.5-P4.7)
- AVREF (P4.4): AD reference voltage
- PWM1: PWM1 output (P4.5)

Table 7.25 PORT4 Share Table

Pin No.			Priority	Function	Enable bit
TQFP48	**LQFP44**	**LQFP32**			
15-16	-	-	1	SEG22-23	Set **P4S7-P4S6** bits in **P0SS** register, clear **DISPSEL** bit in **DISPCON** register
			2	P4.6-P4.7	Above condition is not met
17	13	-	1	PWM1	Set **PWM1EN** bit and set **PWM1OE** bit in **PWM1C** register
			2	SEG24	Set **P4S5** bits in **P0SS** register, clear **DISPSEL** bit in **DISPCON** register
			3	P4.5	Above condition is not met
18	14	9	1	AVREF	Set **REFC** bit in **ADCON** register
			2	AN8	Set **CH8** bit in **ADCH** Register and set **SCH [2:0]**
			3	P4.4	Above condition is not met
19	15	10	1	AN3	Set **CH3** bit in **ADCH** Register and set **SCH [2:0]**
			2	INT43	Set **EX4** bit in **IEN1** register and set **EXS43** bit in **IENC** register, P4.3 in input mode
			3	P4.3	Above condition is not met
20	16	11	1	AN2	Set **CH2** bit in **ADCH** Register and set **SCH [2:0]**
			2	INT42	Set **EX4** bit in **IEN1** register and set **EXS42** bit in **IENC** register, P4.2 in input mode
			3	P4.2	Above condition is not met
21	17	12	1	AN1	Set **CH1** bit in **ADCH** Register and set **SCH [2:0]**
			2	INT41	Set **EX4** bit in **IEN1** register and set **EXS41** bit in **IENC** register, P4.1 in input mode
			3	P4.1	Above condition is not met
22	18	13	1	AN0	Set **CH0** bit in **ADCH** Register and set **SCH [2:0]**
			2	INT40	Set **EX4** bit in **IEN1** register and set **EXS40** bit in **IENC** register, P4.0 in input mode
			3	P4.0	Above condition is not met

PORT5:

- XTAL1 (P5.0): oscillator input
- XTAL2 (P5.1): oscillator output
- $\overline{\text{RST}}$ (P5.2): system reset pin
- PWM1 (P5.3): PWM1 output
- BUZ (P5.3): Buzzer output
- T3 (P5.3): Timer3 external input
- LCD SEGMENT20-21 (P5.4-P5.5)

Table 7.26 PORT5 Share Table

Pin No.			Priority	Function	Enable bit
TQFP48	LQFP44	LQFP32			
8	8	4	1	XTAL1	Selected by Code Option
			2	P5.0	Above condition is not met
9	9	5	1	XTAL2	Selected by Code Option
			2	P5.1	Above condition is not met
10	10	6	1	$\overline{\text{RST}}$	Selected by Code Option
			2	P5.2	Selected by Code Option
11	11	7	1	BUZ	Set **BZEN** bit in **BUZCON** register
			2	T3	Set **TR3** bit in **T3CON** register and **T3CLKS[1:0]** = 01 (Auto Pull up)
			3	P5.3	Above condition is not met
13	-	-	1	SEG20	Set **P5S4** bits in **P0SS** register, set **DISPSEL** bit and **DUTY** bit in **DISPCON** register
			2	P5.4	Above condition is not met
14	-	-	1	SEG21	Set **P5S5** bits in **P0SS** register, set **DISPSEL** bit and **DUTY** bit in **DISPCON** register
			2	P5.5	Above condition is not met

7.8 Timer

7.8.1 Features

- The SH79F3283 has four timers (Timer2, 3, 4, 5)
- Timer2 is compatible with the standard 8052 and has up or down counting and programmable clock output function
- Timer3 is a 16-bit auto-reload timer and can operate even in Power-Down mode
- Timer4 is a 16-bit auto-reload timer and can be selected as a baud-rate generator
- Timer5 is a 16-bit auto-reload timer

7.8.2 Timer2

The Timer 2 is implemented as a 16-bit register accessed as two cascaded data registers: TH2 and TL2. It is controlled by the register T2CON and T2MOD. The Timer2 interrupt can be enabled by setting the ET2 bit in the IEN0 register. (Refer to Interrupt Section for details)

C/$\overline{T2}$ selects system clock (timer operation) or external in T2 (count operation) as the timer clock input. Setting TR2 allows Timer2/Count2 Data Register to increment by the selected input.

Timer2 Modes

Timer2 has 4 operating modes: Capture/Reload, Auto-reload mode with up counter and Baud Rate Generator and Programmable clock-output. These modes are selected by the combination of RCLK, TCLK and CP/RL2.

Table 7.27 Timer2 Mode select

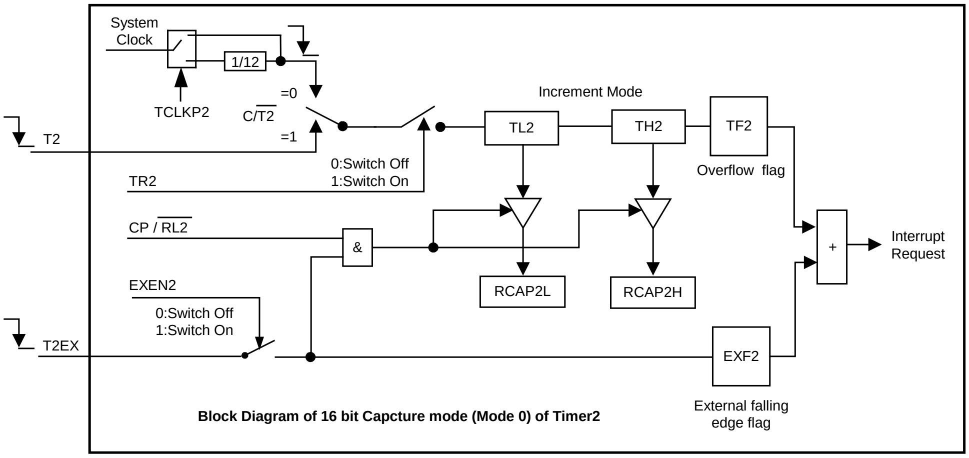
C/$\overline{T2}$	T2OE	DCEN	TR2	CP/RL2	RCLK	TCLK	MODE	
X	0	X	1	1	0	0	0	16 bit capture
X	0	0	1	0	0	0	1	16 bit auto-reload timer
X	0	1	1	0	0	0		
X	0	X	1	X	1	X	2	Baud-Rate generator
					X	1		
0	1	X	1	X	0	0	3	Programmable clock-output only
					1	X	3	Programmable clock-output with Baud-Rate generator
					X	1		
1	1	X	1	X	X	X		Not recommending
X	X	X	0	X	X	X	X	Timer2 stops, the T2EX channel still enable

Mode0: 16 bit Capture

In the capture mode, two options are selected by bit EXEN2 in T2CON.

If EXEN2 = 0, Timer2 is 16-bit timer or counter which will set TF2 on overflow to generate an interrupt if ET2 is enable.

If EXEN2 = 1, Timer2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured to RCAP2H and RCAP2L respectively, In addition, a 1-to-0 transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can also generate an interrupt if ET2 is enabled.



Block Diagram of 16 bit Capcture mode (Mode 0) of Timer2

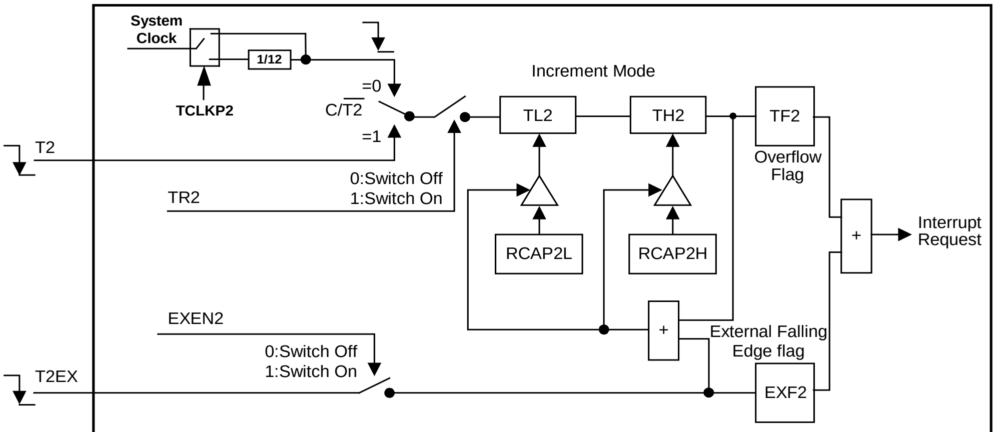
Mode1: 16 bit auto-reload Timer

Timer2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit in T2MOD. After reset, the DCEN bit is set to 0 so that Timer2 will default to count up. When DCEN is set, Timer2 can count up or down, depending on the value of the T2EX pin.

When DCEN = 0, two options are selected by bit EXEN2 in T2CON.

If EXEN2 = 0, Timer2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L, which are pressed by software.

If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if ET2 is enabled.



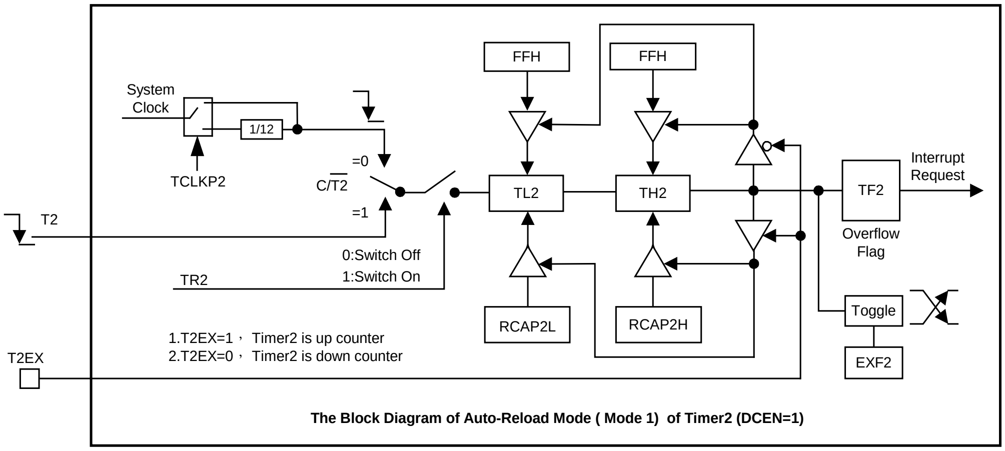
The Block Diagram of Auto Relode Mode (Mode 1)of Timer2 (DCEN=0)

Setting the DCEN bit enables Timer2 to count up or down. When DCEN = 1, the T2EX pin controls the direction of the count, and EXEN2's control is invalid.

A logical "1" at T2EX makes Timer2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logical "0" at T2EX makes Timer2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.



The Block Diagram of Auto-Reload Mode (Mode 1) of Timer2 (DCEN=1)

Mode2: Baud-Rate Generator

Timer2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON. The baud rates for transmit and receive can be different if Timer2 is used for the receiver or transmitter and Timer4 is used for the other.

Setting RCLK and/or TCLK will put Timer2 into its baud rate generator mode, which is similar to the auto-reload mode.

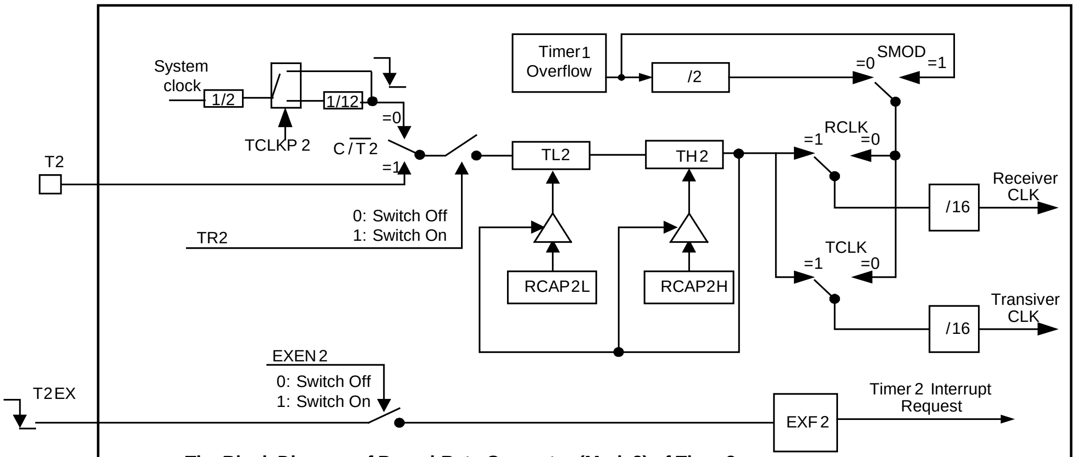
Over flow of Timer2 will causes the Timer2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L that preset by software. But this will not generate an interrupt.

If EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload. Thus when Timer2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

The baud rate in EUART mode 1 & 3 is determined by the timer 2 overflow ratio according to the following equation.

$$\text{BaudRate} = \frac{1}{2 \times 16} \times \frac{f_{SYS}}{65536 - [\text{RCAP2H}, \text{RCAP2L}]} \text{; } C/\overline{T2} = 0$$

$$\text{BaudRate} = \frac{1}{16} \times \frac{f_{T2}}{65536 - [\text{RCAP2H}, \text{RCAP2L}]} \text{; } C/\overline{T2} = 1$$



The Block Diagram of Baund-Rate Generator (Mode2) of Timer2

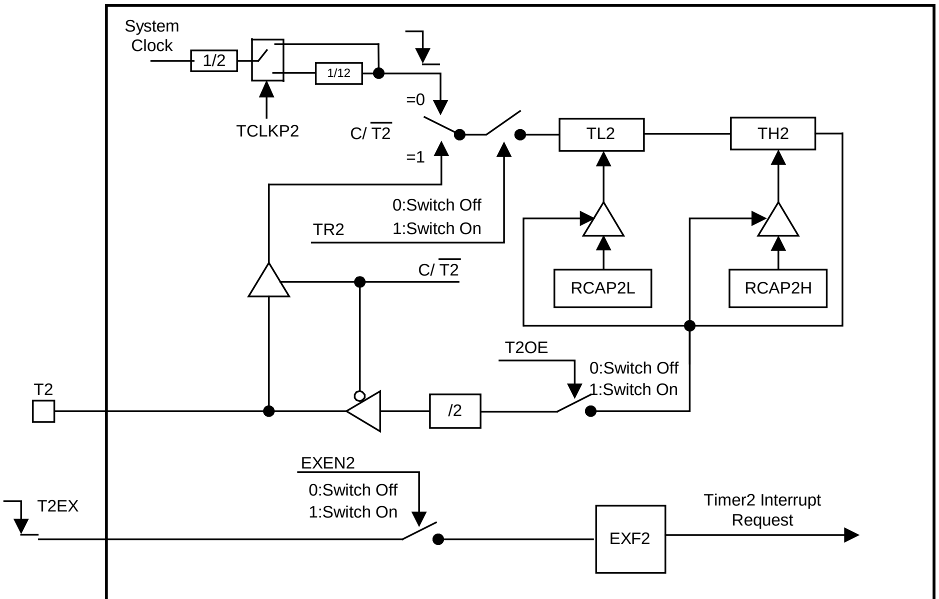
Mode3: Programmable Clock Output

A 50% duty cycle clock can be programmed to come out on P0.5. To configure the Timer2 as a clock generator, bit C/$\overline{\text{T2}}$ must be cleared and bit T2OE must be set. Bit TR2 starts and stops the timer.

In this mode T2 will output a 50% duty cycle clock:

$$\text{Clock Out Frequency} = \frac{1}{2 \times 2} \times \frac{f_{SYS}}{65536 - [\text{RCAP2H,RCAP2L}]}$$

Timer2 overflow will not generate an interrupt, so it is possible to use Timer2 as a baud-rate generator and a clock output simultaneously with the same frequency.



The Block Diagram of Programmable Clock output (Mode 3) of Timer2

Note:

(1) Both TF2 and EXF2 can cause timer2 interrupt request, and they have the same vector address.

(2) TF2 and EXF2 are set as 1 by hardware while event occurs. But they can also be set by software at any time. Only the software and the hardware reset will be able to clear TF2 & EXF2 to 0.

(3) When EA = 1 & ET2 = 1, setting TF2 or EXF2 as 1 will cause a timer2 interrupt.

(4) While Timer2 is used as baud rate generator , writing TH2/TL2, writing RCAPH2/RCAPL2 will affect the accutacy of baud rate, thus might make cause communication error.

Registers

Table 7.28 Timer2 Control Register

C8H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**TF2**	**Timer2 overflow flag bit** 0: No overflow(must be cleared by software) 1: Overflow (Set by hardware if RCLK = 0 & TCLK = 0)
6	**EXF2**	**External event input (falling edge) from T2EX pin detected flag bit** 0: No external event input (Must be cleared by software) 1: Detected external event input (Set by hardware if EXEN2 = 1)
5	**RCLK**	**EUART0 Receive Clock control bit** 0: Timer4 generates receiving baud-rate 1: Timer2 generates receiving baud-rate
4	**TCLK**	**EUART0 Transmit Clock control bit** 0: Timer4 generates transmitting baud-rate 1: Timer2 generates transmitting baud-rate
3	**EXEN2**	**External event input (falling edge) from T2EX pin used as Reload/Capture trigger enable/disable control bit** 0: Ignore events on T2EX pin 1: Cause a capture or reload when a negative edge on T2EX pin is detected, when Timer 2 is not used to clock the EUART (T2EX always has a pull up resistor)
2	**TR2**	**Timer2 start/stop control bit** 0: Stop Timer2 1: Start Timer2
1	**C/$\overline{T2}$**	**Timer2 Timer/Counter mode selected bit** 0: Timer Mode, T2 pin is used as I/O port 1: Counter Mode, the internal pull-up resister is turned on
0	**CP/$\overline{RL2}$**	**Capture/Reload mode selected bit** 0: 16-bits timer/counter with reload function 1: 16-bits timer/counter with capture function

Table 7.29 Timer2 Mode Control Register

C9H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2MOD	TCLKP2	-	-	-	-	-	T2OE	DCEN
R/W	R/W	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
7	**TCLKP2**	**Prescaler control bit** 0: Timer2 source is system clock 1:Timer2 source is 1/12 prescaler of system clock
1	**T2OE**	**Timer2 Output Enable bit** 0: Set P0.5/T2 as clock input or I/O port 1: Set P0.5/T2 as clock output (Baud-Rate generator mode)
0	**DCEN**	**Down Counter Enable bit** 0: Disable Timer2 as up/down counter, Timer2 is an up counter 1: Enable Timer2 as up/down counter

Table 7.30 Timer2 Reload/Capture Data Registers

CAH-CDH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCAP2L	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
RCAP2H	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
TL2	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
TH2	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**RCAP2L.x**	**Timer2 Reload/Capture Data Low & High byte, x = 0 - 7**
	RCAP2H.x	
7-0	**TL2.x**	**Timer2 Low/High byte counter, x = 0 - 7**
	TH2.x	

7.8.3 Timer3

Timer3 is a 16-bit auto-reload timer. It is accessed as two cascaded data registers: TH3 and TL3. It is controlled by the T3CON register. The Timer3 interrupt can be enabled by setting ET3 bit in IEN1 register (Refer to **Interrupt** Section for details).

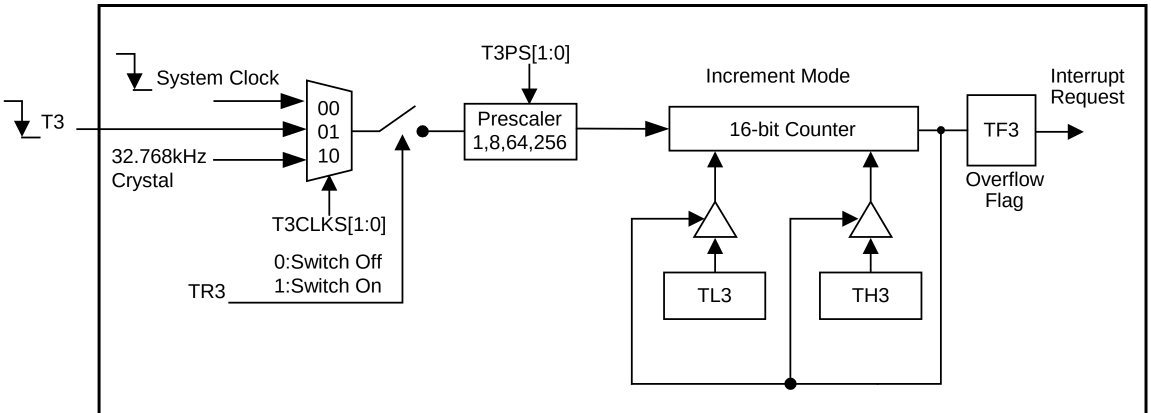
Timer3 has only one operating mode: 16-bit Counter/Timer with auto-reload. Timer3 also supports the following features: selectable prescaler setting and Operation during CPU Power-Down mode.

Timer3 consists of a 16-bit Counter/Timer register (TH3, TL3). When writing to TH3 and TL3, they are used as Timer reload register. When reading from TH3 and TL3, they are used as Counter register. Setting the TR3 bit enables Timer 3 to count up. The Timer will overflow from 0xFFFF to 0x0000 and set the TF3 bit. This overflow also causes the 16-bit value written in timer load register to be reloaded into the timer counter register. Writing to TH3 also can cause the 16-bit value written in timer load register to be reloaded into the timer counter register.

Read or write operation to TH3 and TL3 should follow these steps:

Write operation: Low bits first, High bits followed.

Read operation: High bits first, Low bits followed.



The Block Diagram of Timer3

Timer3 can operate in Power-Down mode.

When OP_OSC[3:0] (Refer to Code Option Section for details) is 1010, 1101, 0011 or 0110, T3CLKS [1:0] can select 00, or 10. When OP_OSC[3:0] is not 1010, 1101, 0011 or 0110, T3CLKS[1:0] can only be selected as 00 or 01, and 10 will be an invalid value.

If T3CLKS[1:0] is 00, Timer 3 can't work in Power Down mode. If T3CLKS[1:0] is 01 and external clock input from T3 Pin, Timer3 can work in CPU normal mode or Power Down mode If T3CLKS[1:0] is 10 and OP_OSC[3:0] is 1010, 1101, 0011 or 0110, Timer3 can work in CPU normal mode or Power Down mode If T3CLKS[1:0] is 10 and OP_OSC[3:0] is not 1010, 1101, 0011 or 0110, Timer3 can't work. It can be described in the following table.

OP_OSC[3:0]	T3CLKS[1:0]	Can work in Normal Mode	Can work in Power Down Mode
1010, 1101, 0011 or 0110	00	YES	NO
	01	YES	YES
	10	YES	YES
Not 1010, 1101, 0011 or 0110	00	YES	NO
	01	YES	YES
	10	NO	NO

Note:

(1) When TH3 and TL3 read or written, must make sure TR3 = 0.

(2) TF3 cleared by hardware, and the interrupt vector address is as the same as Uart1. Please pay attention to the interrupt flag, when use both Timer3 and Uart1.

Registers

Table 7.31 Timer3 Control Register

88H, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T3CON	TF3	-	T3PS.1	T3PS.0	-	TR3	T3CLKS.1	T3CLKS.0
R/W	R/W	-	R/W	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN	0	-	0	0	-	0	0	0

Bit Number	Bit Mnemonic	Description
7	**TF3**	**Timer3 overflow flag bit** 0: No overflow (cleared by hardware) 1: Overflow (Set by hardware)
5-4	**T3PS[1:0]**	**Timer3 input clock Prescaler Select bits** 00: 1/1 01: 1/8 10: 1/64 11: 1/256
2	**TR3**	**Timer3 start/stop control bit** 0: Stop Timer3 1: Start Timer3
1-0	**T3CLKS[1:0]**	**Timer3 Counter/Timer mode select bits** 00: System clock 01: External clock from pin T3, auto pull-up 10: External 32.768kHz crystal or internal 128kHZ RC 11: reserved

Table 7.32 Timer3 Reload/Counter Data Registers

8CH-8DH, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL3	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0
TH3	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**TL3.x**	**Timer3 Low & High byte counter, x = 0 - 7**
	TH3.x	

Table 7.33 Timer3 Reload/Count Data Register

89H, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SWTHL	-	-	-	-	-	-	T5HLCON	T3HLCON
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN	-	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
0	T3HLCON	0: when read TH3, TL3, return T3 count data 1: when read TH3, TL3, return T3 reload register data

7.8.4 Timer4

Timer4 is a 16-bit auto-reload timer. It is accessed as two cascaded data registers: TH4 and TL4. It is controlled by the T4CON register. The Timer 4 interrupt can be enabled by setting ET4 bit in IEN1 register (Refer to **interrupt** Section for details).

When writing to TH4 and TL4, they are used as timer load register. When reading from TH4 and TL4, they are used as timer counter register. Setting the TR4 bit enables Timer 4 to count up. The timer will overflow from 0xFFFF to 0x0000 and set the TF4 bit. This overflow also causes the 16-bit value written in timer load register to be reloaded into the timer counter register. Writing to TH4 also can cause the 16-bit value written in timer load register to be reloaded into the timer counter register.

Read or write operation to TH4 and TL4 should follow these steps:

Write operation: Low bits first, High bits followed.

Read operation: High bits first, Low bits followed.

Timer4 Modes

Timer4 has three operating modes: 16-bit auto-reload timer, serial port Baud Rate Generator and 16 bit auto-reload timer with T4 edge trig. These modes are selected by T4M[1:0] bits in T4CON Register.

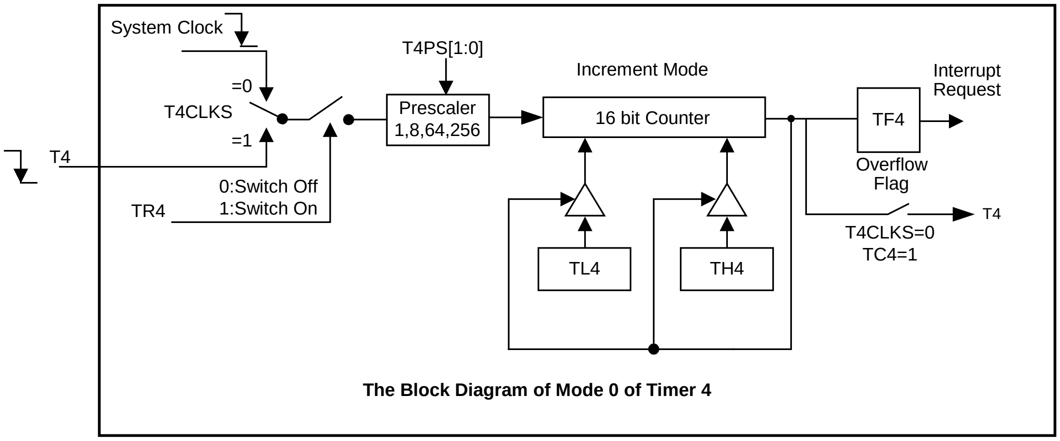
Mode0: 16 bit Auto-Reload Timer

Timer4 operates as 16-bit auto-reload timer in Mode 0. The TH4 register holds the high eight bits of the 16-bit counter/timer, TL4 holds the low eight bits. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the timer overflow flag TF4 (T4CON.7) is set and the 16-bit value in timer load register are reloaded into timer counter register, and an interrupt will occur if Timer 4 interrupts is enabled.

The T4CLKS bit (T4CON.0) selects the counter/timer's clock source. If T4CLKS = 1, external clock from the Pin T4 is selected as Timer4 clock, after prescaled, it will increase the Counter/Timer4 Data register. Else if T4CLKS = 0, the system clock is selected as Timer4 clock.

Setting the TR4 bit (T4CON.1) enables the timer. Setting TR4 does not clear the counter data of Timer4. The timer load register should be loaded with the desired initial value before the timer is enabled.

In Compare mode, the T4 pin is automatically set as output mode by hardware. the internal counter is constantly countered from TH4 and TL4 register value to 0xFFFF. When an overflow occurs, the T4 pin will be inverted. At the same time, interrupt flag bit of Time4 is set. Timer4 must be running in Timer mode (T4CLKS = 0) when compare function enabled.



The Block Diagram of Mode 0 of Timer 4

Mode1: Baud-Rate Generator

Timer4 is selected as the baud rate generator by setting T4MOD bit in T4M[1:0] register. If Timer2 is used for the receiver or transmitter and Timer4 is used for the other, the baud rates for transmit and receive can be different.

The mode is similar to the auto-reload mode. Overflow of Timer4 will causes the Timer4 counter register to be reloaded with the 16-bit value in timer load register. But this will not generate an interrupt.

The baud rates in EUART mode1 and mode3 are determined by Timer4's overflow rate according to the following equation.

$$\text{BaudRate} = \frac{2^{\text{SMOD}}}{2 \times 16} \times \frac{f_{\text{T4}}/\text{PRESCALER}}{65536 - [\text{TH4}, \text{TL4}]}$$

Here, TH4 and TL4 stand for Timer4 reload register.

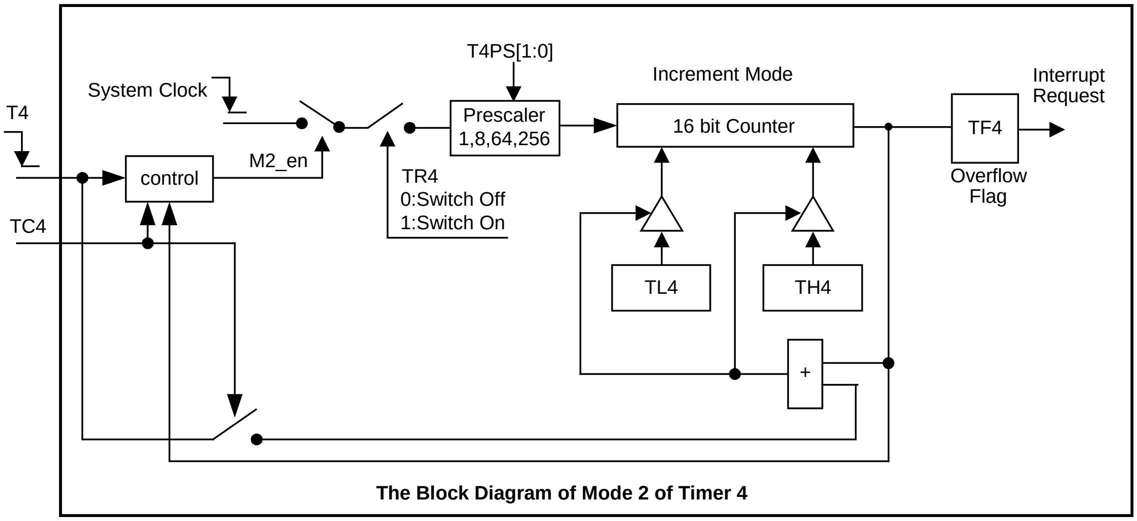
Mode2: Mode2: 16 bit Auto-Reload Timer with T4 Edge Trig

Timer4 operates as 16-bit timer in Mode 2. T4CLKS bit in T4CON.0 will be always 0. Timer4 can select system clock as clock source. Other settings accord with mode 0.

In Mode 2, After setting the TR4 bit (T4CON.1), Timer4 does not start counting but waits the trig signal (rising or falling edge controlled by T4M[1:0]) from T4. An active trig signal will start the Timer4. When Timer 4 overflows from 0XFFFF to 0x0000, TF4 will be set, TH4 and TL4 will be reloaded from timer load register, and Timer4 holds and waits the next trig edge.

When Timer4 is working, an active trig signal maybe come, if TC4 = 0, the trig signal will be ignored; if TC4 = 1, Timer4 will be re-trigged.

Setting TR4 does not clear the counter data of Timer4. The timer register should be loaded with the desired initial value before the timer is enabled.



The Block Diagram of Mode 2 of Timer 4

control : M2_en set to 1 when T4 edge trig, M2_en set to 0 when counter overflow

Note: *When Timer4 is used as a counter, the frequency of input signal of T4 pin must be less than half of system clock.*

Registers

Table 7.34 Timer4 Control Register

C8H, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T4CON	TF4	TC4	T4PS1	T4PS0	T4M1	T4M0	TR4	T4CLKS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**TF4**	**Timer4 overflow flag bit** 0: No overflow (cleared by hardware) 1: Overflow (Set by hardware)
6	**TC4**	**Compare function Enable bit** When T4M[1:0] = 00 0: Disable compare function of Timer4 1: Enable compare function of Timer4 When T4M[1:0] = 10 or 11 0: Timer4 can't be re-trigged 1: Timer4 can be re-trigged
5-4	**T4PS[1:0]**	**Timer4 input clock Prescale Select bits** 00: 1/1 01: 1/8 10: 1/64 11: 1/256
3-2	**T4M[1:0]**	**Timer4 Mode Select bit** 00: Mode0, 16-bit auto-reload timer 01: Mode1, baud-rate generator for EUART 10: Mode2 with rising edge trig from pin T4 (system clock only, T4CLKS is invalid) 11: Mode2 with falling edge trig from pin T4 (system clock only, T4CLKS is invalid)
1	**TR4**	**Timer4 start/stop control bit** 0: Stop Timer4 1: Start Timer4
0	**T4CLKS**	**Timer4 Clock Source select bit** 0: System clock, T4 pin is used as I/O port 1: External clock from pin T4 (On the falling edge), the internal pull-up resister is turned on

Table 7.35 Timer4 Reload/Counter Data Registers

CCH-CDH, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL4	TL4.7	TL4.6	TL4.5	TL4.4	TL4.3	TL4.2	TL4.1	TL4.0
TH4	TH4.7	TH4.6	TH4.5	TH4.4	TH4.3	TH4.2	TH4.1	TH4.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**TL4.x**	**Timer4 Low & High byte counter, x = 0 - 7**
	TH4.x	

7.8.5 Timer5

Timer5 is a 16-bit auto-reload timer. It is accessed as two cascaded data registers: TH5 and TL5. It is controlled by the T5CON register. The interrupt can be enabled by setting ET5 bit in IEN0 register (Refer to **interrupt** Section for details).

When writing to TH5 and TL5, they are used as timer load register. When reading from TH5 and TL5, they are used as timer counter register. Setting the TR5 bit enables Timer5 to count up. The timer will overflow from 0xFFFF to 0x0000 and set the TF5 bit. This overflow also causes the 16-bit value written in timer load register to be reloaded into the timer counter register. Writing to TH4 also can cause the 16-bit value written in timer load register to be reloaded into the timer counter register.

Read or write operation to TH5 and TL5 should follow these steps:

Write operation: Low bits first, High bits followed.

Read operation: High bits first, Low bits followed.

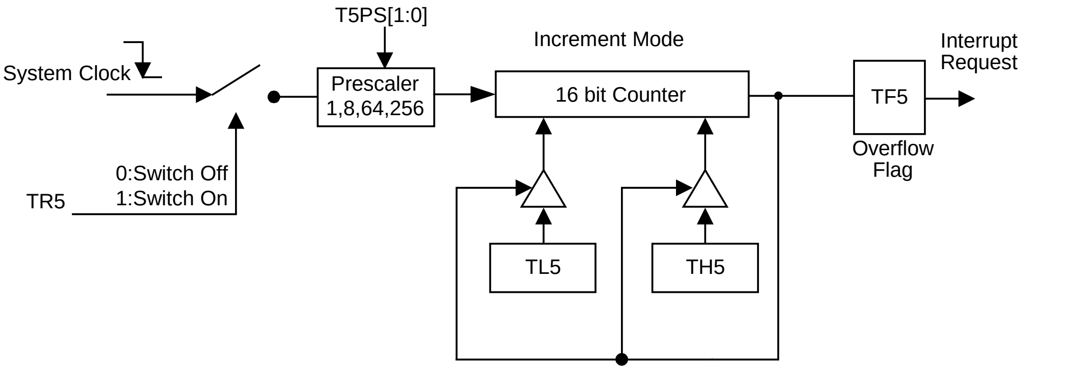
Timer5 Modes

Timer5 has one operating modes: 16-bit auto-reload timer.

Mode0: 16 bit Auto-Reload Counter/Timer

Timer5 operates as 16-bit counter/timer in Mode 0. The TH5 register holds the high eight bits of the 16-bit counter/timer, TL5 holds the low eight bits. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the timer overflow flag TF5 (T5CON.7) is set and the 16-bit value in timer load register are reloaded into timer counter register, and an interrupt will occur if Timer 5 interrupts is enabled.

Setting the TR5 bit (T5CON.1) enables the timer. Setting TR5 does not clear the counter data of Timer4. The timer load register should be loaded with the desired initial value before the timer is enabled.



The Block Diagram of Mode 0 of Timer 5

Registers

Table 7.36 Timer5 Control Register

C0H, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T5CON	TF5	-	T5PS1	T5PS0	-	-	TR5	-
R/W	R/W	-	R/W	R/W	-	-	R/W	-
Reset Value (POR/WDT/LVR/PIN)	0	-	0	0	-	-	0	-

Bit Number	Bit Mnemonic	Description
7	**TF5**	**Timer5 overflow flag bit** 0: No overflow (cleared by hardware) 1: Overflow (Set by hardware)
5-4	**T5PS[1:0]**	**Timer5 input clock Prescale Select bits** 00: 1/1 01: 1/8 10: 1/64 11: 1/256
1	**TR5**	**Timer5 start/stop control bit** 0: Stop Timer5 1: Start Timer5

Table 7.37 Timer5 Reload/Counter Data Registers

CEH-CFH, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL5	TL5.7	TL5.6	TL5.5	TL5.4	TL5.3	TL5.2	TL5.1	TL5.0
TH5	TH5.7	TH5.6	TH5.5	TH5.4	TH5.3	TH5.2	TH5.1	TH5.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**TL5.x**	**Timer5 Low & High byte counter, x = 0 - 7**
	TH5.x	

Table 7.38 Timer5 Reload/Count Data Register

89H, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SWTHL	-	-	-	-	-	-	T5HLCON	T3HLCON
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
1	T5HLCON	0: when read TH5, TL5, return T5 count data 1: when read TH5, TL5, return T5 reload register data

7.9 Interrupt

7.9.1 Feature

- 15 interrupt sources
- 4 interrupt priority levels

The SH79F3283 provides total 15 interrupt sources: 5 external interrupts (INT0, INT1, INT2, INT3, INT4), INT4 has 8 interrupt sources (INT40-47, which share the same vector address), 4 timer interrupts (Timer2, 3, 4, 5), two EUART interrupt, SPI interrupt, ADC Interrupt, PWM interrupts, SCM interrupt and LPD interrupt.

7.9.2 Interrupt Enable Control

Each interrupt source can be individually enabled or disabled by setting or clearing the corresponding bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains global interrupt enable bit, EA, which can enable/disable all the interrupts at once. Generally, after reset, all interrupt enable bits are set to 0, which means that all the interrupts are disabled.

7.9.3 Register

Table 7.39 Primary Interrupt Enable Register

A8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	EA	EADC	ET2	ES0	-	EX1	ET5	EX0
R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	-	0	0	0

Bit Number	Bit Mnemonic	Description
7	EA	**All interrupt enable bit** 0: Disable all interrupt 1: Enable all interrupt
6	EADC	**ADC interrupt enable bit** 0: Disable ADC interrupt 1: Enable ADC interrupt
5	ET2	**Timer2 overflow interrupt enable bit** 0: Disable Timer2 overflow interrupt 1: Enable Timer2 overflow interrupt
4	ES0	**EUART0 interrupt enable bit** 0: Disable EUART0 interrupt 1: Enable EUART0 interrupt
2	EX1	**External interrupt1 enable bit** 0: Disable external interrupt1 1: Enable external interrupt1
1	ET5	**Timer5 overflow interrupt enable bit** 0: Disable Timer5 overflow interrupt 1: Enable Timer5 overflow interrupt
0	EX0	**External interrupt0 enable bit** 0: Disable external interrupt0 1: Enable external interrupt0

Table 7.40 Secondary Interrupt Enable Register

A9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN1	ESCM_LPD _CRC	ET4	EPWM	ET3_ES1	EX4	EX3	EX2	ESPI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**ESCM_LPD_CRC**	**SCM/LPD/CRC interrupt enable bit** 0: Disable SCM/LPD/CRC interrupt 1: Enable SCM/LPD/CRC interrupt
6	**ET4**	**Timer4 overflow interrupt enable bit** 0: Disable Timer4 overflow interrupt 1: Enable Timer4 overflow interrupt
5	**EPWM**	**PWM interrupt enable bit** 0: Disable PWM interrupt 1: Enable PWM interrupt
4	**ET3_ES1**	**Timer3/EUART0 overflow interrupt enable bit** 0: Disable timer3/EUART0 overflow interrupt 1: Enable timer3/EUART0 overflow interrupt
3	**EX4**	**External interrupt4 enable bit** 0: Disable external interrupt4 1: Enable external interrupt4
2	**EX3**	**External interrupt3 enable bit** 0: Disable external interrupt3 1: Enable external interrupt3
1	**EX2**	**External interrupt2 enable bit** 0: Disable external interrupt2 1: Enable external interrupt2
0	**ESPI**	**SPI interrupt enable bit** 0: Disable SPI interrupt 1: Enable SPI interrupt

Note:

(1) To enable External interrupt0/12/3/4, the corresponding port must be set to input mode before using it.

(2) EPWM is the both PWM0 and PWM1 interrupt enable bit. To enable PWM timer interrupt, the EPWM bit here should be set. Also, the PWMIE in PWM interrupt control register should be set.

Table 7.41 Interrupt channel Enable Register

BAH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IENC	EXS47	EXS46	EXS45	EXS44	EXS43	EXS42	EXS41	EXS40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**EXS4x (x = 7-0)**	**External interrupt4 channel select bit (x = 7-0)** 0: Disable external interrupt 4x 1: Enable external interrupt 4x

Table 7.42 Interrupt channel Enable Register1

BBH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IENC1	-	ECRC	ES1	ET3	-	-	ESCM	ELPD
R/W	-	R/W	R/W	R/W	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	-	-	0	0

Bit Number	Bit Mnemonic	Description
6	**ECRC**	**CRC interrupt enable bit** 0: Disable CRC interrupt 1: Enable CRC interrupt
5	**ES1**	**EUART1 interrupt enable bit** 0: Disable EUART1 interrupt 1: Enable EUART1 interrupt
4	**ET3**	**Timer3 interrupt enable bit** 0: Disable Timer3 interrupt 1: Enable Timer3 interrupt
1	**ESCM**	**SCM interrupt enable bit** 0: Disable SCM interrupt 1: Enable SCM interrupt
0	**ELPD**	**LPD interrupt enable bit** 0: Disable LPD interrupt 1: Enable LPD interrupt

7.9.4 Interrupt Flag

Each Interrupt source has its own interrupt flag, when interrupt occurs, corresponding flag will be set by hardware, the interrupt flag bits are listed in interrupt abstract table.

When an external interrupt **INT0/1/2/3** is generated, if the interrupt was edge trigged, the flag IEx (x = 0-3) that generated this interrupt is cleared by hardware when the service routine is vectored. If the interrupt was level trigged, then the requesting external source directly controls the request flag, rather than the on-chip hardware.

When **INT4** generates an interrupt, the flag (IF4x (x = 0-7) in EXF1 register) that generated this interrupt should be cleared by user's program because the same vector entrance was used in INT4. But if INT4 is set up as level trigged, the flag can't be cleared by user's program, it only be controlled by peripheral signal level that connect to INT source pin.

The **Timer2** interrupt is generated by the logical OR of flag TF2 in T2CON register, which is set by hardware. None of these flags can be cleared by hardware after CPU responses to the interrupt, the flag must be cleared by software

When the **Timer3** counter overflow, set interrupt flag bit TF3 in T3CON to 1 to generate Timer3 interrupt. The flag will be cleared automatically by hardware after CPU responses to the interrupt.

When the **Timer4** counter overflow, set interrupt flag bit TF4 in T4CON to 1 to generate Timer4 interrupt. The flag will be cleared automatically by hardware after CPU responses to the interrupt.

When the **Timer5** counter overflow, set interrupt flag bit TF5 in T5CON to 1 to generate Timer5 interrupt. The flag will be cleared automatically by hardware after CPU responses to the interrupt.

The **EUARTx(x = 0, 1) interrupt**s is generated by the logical OR of flag RI and TI in SCON/SCON1 register, which is set by hardware. Neither of these flags can be cleared by hardware when the service routine is vectored. In fact, the service routine will normally have to determine whether it was the receive interrupt flag or the transmission interrupt flag that generated the interrupt, so the flag must be cleared by software.

The **ADC interrupt** is generated by ADCIF bit in ADCON. If an interrupt is generated, the converted result in ADCDH/ADCDL will be valid. If continuous compare function in ADC module is Enable, ADCIF will not be clear at each conversion when conversion results is less than the compare value. But if converted result is larger than compare value, ADCIF bit will be 1. The flag must be cleared by software.

The **SPI interrupt** are generated by SPIF in SPSTA or set MODF. The flags can be cleared by software.

The **SCM interrupt** is generated by SCMIF in CLKCON register, which is set by hardware. And the flag can only be cleared by hardware.

The **LPD interrupt** is generated by LPDF in LPDCON register. And the flag can only be cleared by hardware. By setting the LPDMD, can choose when the V_{DD} voltage is above or below the LPD set generated when the detecting voltage interruption of LPD.

The **PWM interrupts** are generated by PWMxIF in PWMxC (x = 0, 1). The flags can be cleared by software.

The **CRC interrupt** is generated by CRCIF in CRCCON. The flags can be cleared by software.

Table 7.43 External Interrupt 0/1 Control Register

88H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	-	-	-	-	IE1	IT1	IE0	IT0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
1, 3	**IEx (x = 0, 1)**	**External interrupt x request flag bit** 0: No interrupt pending 1: Interrupt is pending
0, 2	**ITx (x = 0, 1)**	**External interrupt x trigger mode selection bit** 0: Low level trigger 1: Falling edge trigger

Table 7.44 External Interrupt Flag Register

E8H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXF0	IT4.1	IT4.0	IT3.1	IT3.0	IT2.1	IT2.0	IE3	IE2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-6	**IT4[1:0]**	**External interrupt4 trigger mode selection bit** 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge IT4 [1:0] is effect on external interrupt 4x at the same mode
5-4	**IT3[1:0]**	**External interrupt3 trigger mode selection bit** 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge
3-2	**IT2[1:0]**	**External interrupt2 trigger mode selection bit** 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge
1	**IE3**	**External interrupt3 request flag bit** 0: No interrupt pending 1: Interrupt is pending
0	**IE2**	**External interrupt2 request flag bit** 0: No interrupt pending 1: Interrupt is pending

Table 7.45 External Interrupt 4 Flag Register

D8H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXF1	IF47	IF46	IF45	IF44	IF43	IF42	IF41	IF40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IF4x (x = 7-0)**	**External interrupt4 request flag bit** 0: No interrupt pending 1: Interrupt is pending IF4x is cleared by software

7.9.5 Interrupt Vector

When an interrupt occurs, the program counter is pushed onto the stack and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are listed in **Interrupt Summary table**.

7.9.6 Interrupt Priority

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing corresponding bits in the interrupt priority control registers IPL0, IPH0, IPL1, and IPH1. The interrupt priority service is described below.

An interrupt service routine in progress can be interrupted by a higher priority interrupt, but can not by another interrupt with the same or lower priority.

The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If the same priority interrupt source apply for the interrupt at the beginning of the instruction cycle at the same time, an internal polling sequence determines which request is serviced.

Interrupt Priority		
Priority bits		Interrupt Lever Priority
IPHx	IPLx	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 7.46 Interrupt Priority Control Registers

B8H, B4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IPL0	-	PADCL	PT2L	PS0L	-	PX1L	PT5L	PX0L
IPH0	-	PADCH	PT2H	PS0H	-	PX1H	PT5H	PX0H
R/W	-	R/W	R/W	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	-	0	0	0
B9H, B5H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
IPL1	PSCML	PT4L	PPWML	PT3S1L	PX4L	PX3L	PX2L	PSPIL
IPH1	PSCMH	PT4H	PPWMH	PT3S1H	PX4H	PX3H	PX2H	PSPIH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PxxxL/H**	Corresponding interrupt source xxx's priority level selection bits

7.9.7 Interrupt Handling

The interrupt flags are sampled and captured at each machine cycle. All interrupts are sampled at the rising edge of the clock. If one of the flags was set, the CPU will find it and the interrupt system will generate a LCALL to the appropriate service routine, LCALL generated by hardware is not blocked by any of the following conditions:

An interrupt of equal or higher priority is already in progress.

The current cycle is not in the final cycle of the instruction in progress. In other words, any interrupt request cannot get response before executing instructions to complete.

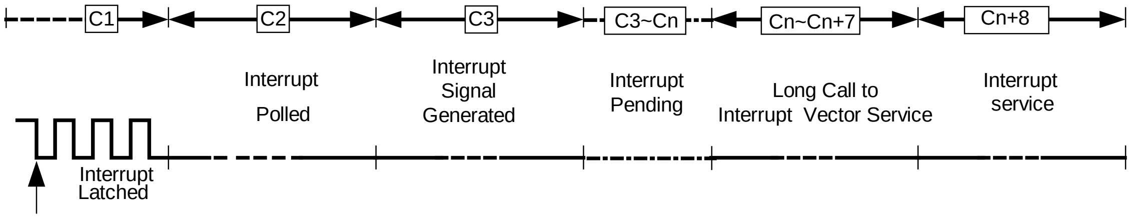
The instruction in progress is RETI or visit the special register IEN0/1 or IPLH instruction. This ensures that if the instruction in progress is RETI or read and write IEN0/1 or IPLH then at least one more instruction except RETI will be executed before any interrupt is vectored to; this delay guarantees that the CPU can observe the changes of the interrupt status.

Note:

Since priority change normally needs 2 instructions, it is recommended to disable corresponding Interrupt Enable flag to avoid interrupt between these 2 instructions during the change of priority.

If the flag is no longer active when the blocking condition is removed, the denied interrupt will not be serviced. Every polling cycle interrogates only the valid interrupt requests.

The polling cycle/LCALL sequence is illustrated below:



Interrupt Response Time

The hardware-generated LCALL pushes the contents of the program counter onto the stack (but it does not save the PSW). Then vector address of the corresponding interrupt source (referring to the interrupt vector table) will be stored in the program counter.

Interrupt service execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that the interrupt routine is no longer in progress, and then pops the top two bytes from the stack and reloads the program counter. Execution of the interrupted program continues from the point where it was stopped. The RET instruction can also return to the original address to continue, but the interrupt priority control system still think the interrupt in a same priority is responsed, in this case, the same priority or lower priority interrupt will not be responsed.

7.9.8 Interrupt Response Time

If an interrupt is detected, its request flag will be set in every machine cycle after detection. The value will be kept by the internal circuitry until the next machine cycle; the CPU will generate an interrupt at the third machine cycle. If the request is active and conditions are right for it to be acknowledged, hardware instruction LCALL will call service routine which requeste interrupt at the next instruction to be executed. Otherwise the interrupt will pending. The call itself takes 7 machine cycles. Therefore, from the external interrupt request to start the implementation of interrupt program requires at least 3+7 completed machine cycle.

A longer response time would be obtained if the request was blocked by one of the above three previously listed conditions. If an interrupt of equal or higher priority is already in progress, the additional wait time obviously depends on the length of the other interrupt's service routine.

If the instruction in progress is not in its final cycle and the instruction in progress is RETI, the additional wait time is 8 machine cycles. For a single interrupt system, if the next instruction is 20 machine cycles long (the longest instructions DIV & MUL are 20 machine cycles long for 16 bit operation), adding the LCALL instruction 7 machine cycles the total response time is 2+8+20+7 machine cycles.

Thus interrupt response time is always more than 10 machine cycles and less than 37 machine cycles.

7.9.9 External Interrupt Inputs

The SH79F3283 has 5 external interrupt inputs. External interrupt0-3 each has one vector address. External interrupt 4 has 8 inputs; all of them share one vector address. These external interrupts can be programmed to be level-triggered or edge-triggered by clearing or setting bit IT1 or IT0 in register TCON and register EXF1. If ITn = 0 (n = 0 - 1), external interrupt 0/1 is triggered by a low level detected at the INT0/1 pin. If ITn = 1 (n = 0 - 1), external interrupt 0/1 is edge triggered. In this mode if consecutive samples of the INT0/1 pin show a high level in one cycle and a low level in the next cycle, interrupt request flag in register r EXF1 is set, causing an interrupt request. Since the external interrupt pins are sampled once each machine cycle, an input high or low level should be held for at least one machine cycle to ensure proper sampling.

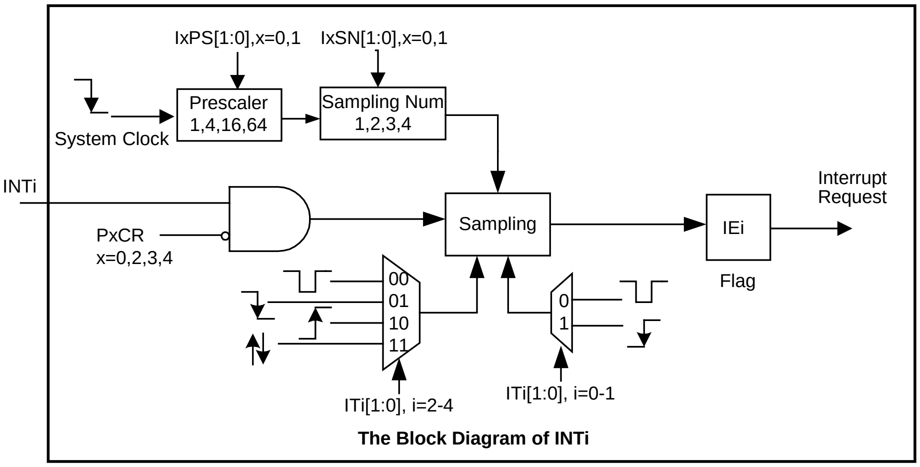
If the external interrupt is edge-triggered, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is detected and that interrupt request flag is set. Notice that IE0-1 is automatically cleared by CPU when the service routine is called while IF4x should be cleared by software. External interrupt4 operates in the similar ways except have different registers and have more selection of trigger.

If the external interrupt is level-triggered, the external source must hold the request active until the requested interrupt is generated, which will take 2 machine cycles. If the external interrupt is still asserted when the interrupt service routine is completed, another interrupt will be generated. It is not necessary to clear the interrupt flag IEx (x = 0, 1, 2, 3) when the interrupt is level sensitive, it simply tracks the input pin level.

In order to satisfy the different request interrupt response, there can set sample clock Prescaler Select bits and sample times Select bits in EXCON register

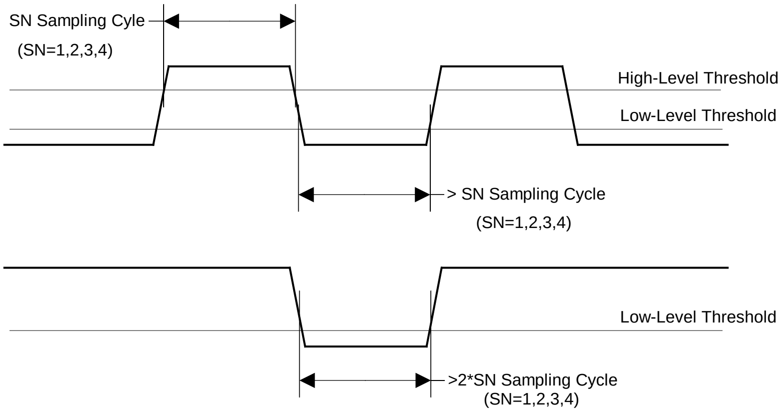
Sample clock Prescaler Select bits and sample times Select bits in EXCON register are invalid in the IDLE and Power-Down mode.

If an external interrupt is enabled when the SH79F3283 is put into Power down or Idle mode, the interrupt occurrence will cause the processor to wake up and resume operation.



The Block Diagram of INTi

Note: *The INT0/1/2/3 interrupt flag will be cleared by hardware, but IF40-IF47 must be cleared by software*



External Interrupt Detecting

Table7.47 External interrupt sample times control register

8BH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXCON	I1PS1	I1PS0	I1SN1	I1SN0	I0PS1	I0PS0	I0SN1	I0SN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-6	**I1PS[1:0]**	**INT4 sample clock Prescaler Select bits** 00: 1/1 01: 1/4 10: 1/16 11: 1/64
5-4	**I1SN[1:0]**	**INT4 sample times Select bits** 00: 1 01: 2 10: 3 11: 4
3-2	**I0PS[1:0]**	**INT0/1/2/3 sample clock Prescaler Select bits** 00: 1/1 01: 1/4 10: 1/16 11: 1/64
1-0	**I0SN[1:0]**	**INT0/1/2/3 sample times Select bits** 00: 1 01: 2 10: 3 11: 4

Note: *If I0SN[1:0] = 11, the INT0/1/2/3 (falling edge trigger) need sample 4 times low-level to generate the interrupt flag*

7.9.10 Interrupt Summary

Source	Vector Address	Enable bits	Flag bits	Polling Priority	Interrupt number (C51)
Reset	0000H	-	-	0 (highest)	-
INT0	0003H	EX0	IE0	1	0
Timer5	000BH	ET5	TF5	2	1
INT1	0013H	EX1	IE1	3	2
EUART0	0023H	ES0	RI+TI	5	4
Timer2	002BH	ET2	TF2+EXF2	6	5
ADC	0033H	EADC	ADCIF	7	6
SPI	003BH	ESPI	SPIF	8	7
INT2	0043H	EX2	IE2	9	8
INT3	004BH	EX3	IE3	10	9
INT4	0053H	EX4+IENC	IF43-40	11	10
Timer3	005BH	ET3+ET3_ES1	TF3	12	11
PWM	0063H	EPWM	PWM0/1IF	13	12
Timer4	006BH	ET4	TF4	14	13
SCM/LPD/CRC	0073H	ESCM/ELPD/ECRC+ESCM_LPD_CRC	SCMIF/LPDF/CRCIF	15 (lowest)	14

8. Enhanced Function

8.1 LCD Driver

Normal Resistor LCD Driver with Fast charge

The LCD driver contains a controller, a duty cycle generator with 4/8 Common signal pins and 28/27/26/24 Segment driver pins. Segment 1-28 and COM1-COM4 can also be used as I/O port, it is controlled by the P0SS, P1SS, P2SS, P3SS, register. LCD COM1-COM8 can be shared with LED Driver. The 28 bytes display data RAM is addressed to 500H-51BH, which could be used as data memory if needed.

The MCU consists normal display topologies with contrast adjustment which supports both 1/4duty-1/3bias and 1/5duty-1/3 bias, 1/6duty-1/3 bias, 1/6duty-1/4 bias and 1/8duty-1/4 bias driving mode. DISPSEL (DISPCON.7) must be cleared before LCD working. When ELCC in DISPCON is set, the LCD power supply V_{LCD} is selected by VOL[0:3]. When ELCC is cleared, V_{LCD} equals $V_{DD.}$

When MCU enters the Power-down mode, the LCD will be turned off. If 32.768kHz crystal/128kHz works in Power-down mode, the LCD is still working. During the Power in Reset, Pin Reset, LVR Reset and Watchdog Reset, the LCD will be turned off, and Common and Segment will output low.

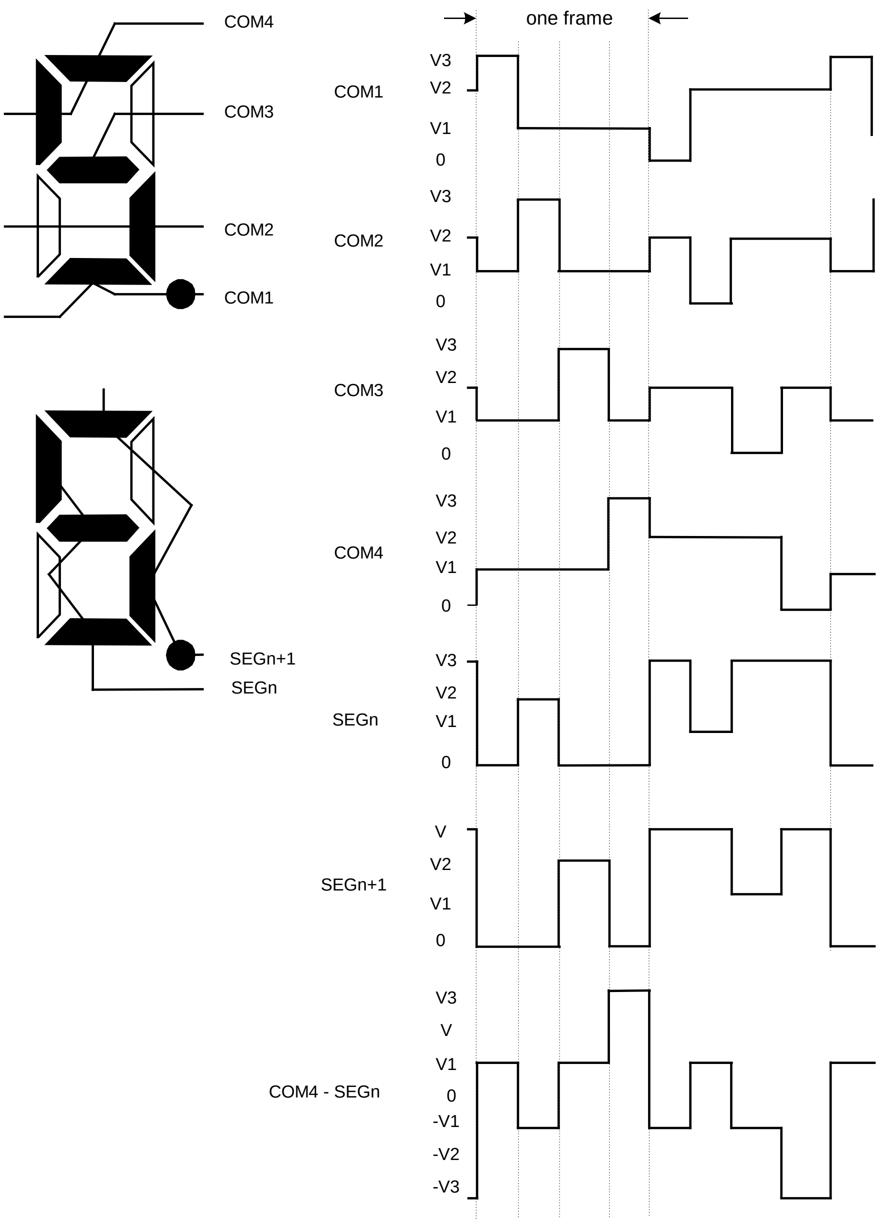
The features of the LCD Normal Display Mode include the following:

- LCD clock is decided by code option OP_OSC
- When OP_OSC[3:0] is 1010, 1011 or 1101, LCD clock source is 32.768kHz, DISPCLK0 register is invalid, LCD frame is 64Hz.
- When OP_OSC[3:0] is others, LCD clock source is 128kHz, set DCK[1:0] bits in DISPCLK0 register, select 1/4, 1/3, 1/2, 1/1, prescaler, so that the LCD frame is 256/4Hz, 256/3Hz, 256/2Hz, 256/1Hz.
- When OP_OSC[3:0] is 0000, 0001, 1110, in stop mode, the LCD clock will be turned off. When OP_OSC[3:0] is 0011, 0100, 0110, 1010, 1011, 1101, and MCU worked in high frequency mode ,in stop mode, the LCD clock is still working. When OP_OSC[3:0] is 0011, 0100, 0110, 1010, 1011, 1101, and MCU worked in low frequency mode ,in stop mode, the LCD clock will be turned off, and the LCD clock is still working in IDLE mode.
- LCD worked 1/4duty-1/3bias and 1/5duty-1/3 bias, 1/6duty-1/3 bias, 1/6duty-1/4 bias and 1/8duty-1/4 bias driving mode by set DUTY[2:0] bits in DISPCON register.
- 16 levels contrast adjustment by configuring the VOL[3:0] bits in DISPCON register.
- LCD bias resistor (R_{LCD}) can be selected as 20K/75K/300KΩ when select 1/3 bias. LCD bias resistor (R_{LCD}) can be selected as 15K/56K/225KΩ when select 1/4 bias. The sum LCD bias resistor (R_{LCD}) is 60K/225K/900K.

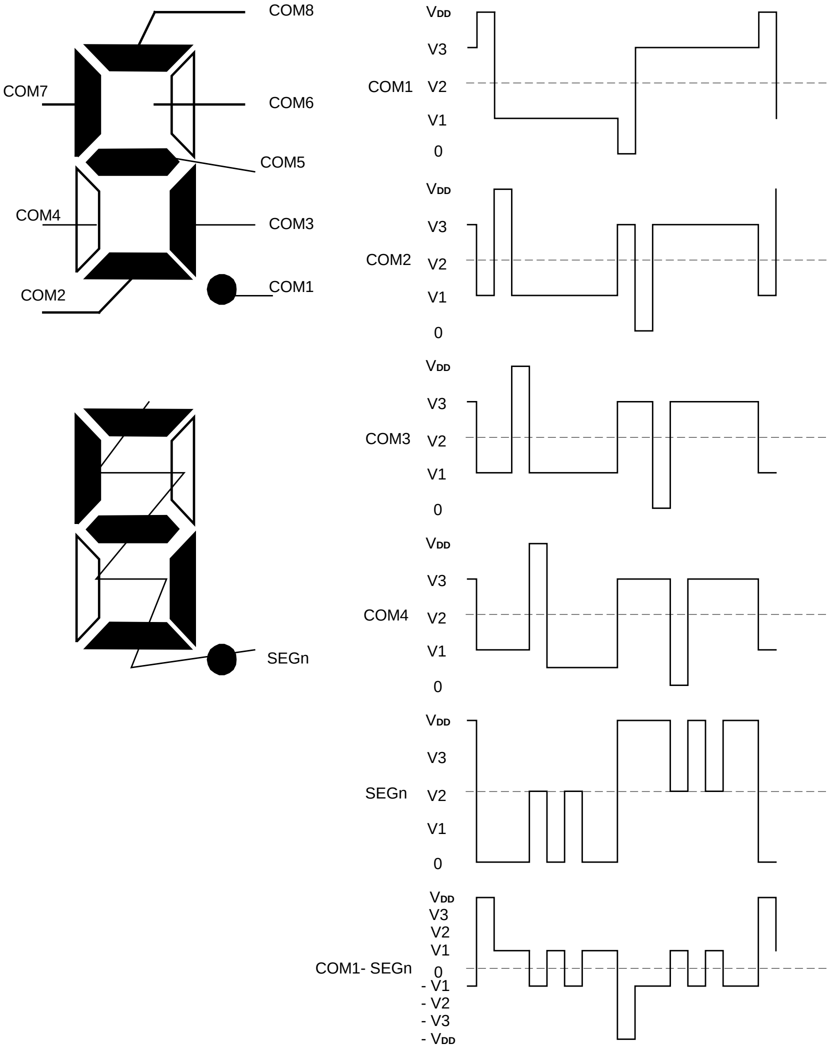
Fast Charge mode or Normal resistor mode is selected by set MOD[1:0] bits in DISPCON1 register. Fast Charge mode can effectively reduce the power consumption.

When refresh the display data 20k bias resistors are selected to provide larger current to get better LCD display effect, but it not suitable for some low current consume application. When keep the display data 75K/300k bias resistors are selected to save drive current, but the LCD display effect will down.

Therefore SH79F3283 provides both the low power consumption and display effect of the display mode. Set MOD[1:0] = 10 to select this mode. When refresh the display data 20k bias resistors are selected to provide larger current. When keep the display data 75K/300k bias resistors are selected to save drive current. Charging time is selected as 1/8, 1/16, 1/32 or 1/64 of LCD com period by FCCTL[1:0] in DISPCON1register.



LCD Waveform (1/4duty, 1/3bias)



LCD Waveform (1/8duty, 1/4bias)

8.1.1 Register

Table 8.1 LCD Control Register

ABH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DISPCON	DISPSEL	LCDON	ELCC	DUTY0	VOL3	VOL2	VOL1	VOL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**DISPSEL**	**LCD/LED control bit** 0: select LCD driver 1: select LED driver
6	**LCDON**	**LCD control bit** 0: turn off LCD driver 1: turn on LCD driver
5	**ELCC**	**LCD contrast on/off control bit** 0: disable contrast 1: enable contrast
4	**DUTY0**	**LCD duty selection bit (Combination control with DUTY[2:1])** **Refer to DUTY[2:1]**
3-0	**VOL[3:0]**	**LCD contrast control bits** 0000: V_{LCD} = 0.531V_{DD} 0001: V_{LCD} = 0.563V_{DD} 0010: V_{LCD} = 0.594V_{DD} 0011: V_{LCD} = 0.625V_{DD} 0100: V_{LCD} = 0.656V_{DD} 0101: V_{LCD} = 0.688V_{DD} 0110: V_{LCD} = 0.719V_{DD} 0111: V_{LCD} = 0.750V_{DD} 1000: V_{LCD} = 0.781V_{DD} 1001: V_{LCD} = 0.813V_{DD} 1010: V_{LCD} = 0.844V_{DD} 1011: V_{LCD} = 0.875V_{DD} 1100: V_{LCD} = 0.906V_{DD} 1101: V_{LCD} = 0.938V_{DD} 1110: V_{LCD} = 0.969V_{DD} 1111: V_{LCD} = 1.000V_{DD}

Note: *SH79F3283 has LCD and LED driver, but cannot work at the same time. When DISPSEL = 1, LCD is disabled, when DISPSEL = 0, LED is disable.*

Table 8.2 LCD Control Register 1

ADH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DISPCON1	MODSW	DUTY2	DUTY1	RLCD	FCCTL1	FCCTL2	MOD1	MOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**MODSW**	**LCD/LED shared control bit** 0: P0SS is valid 1: all the LCD/LED Pins worked as IO
6-5	**DUTY[2:1]**	**LCD duty selection bit (Combination control with DUTY0)** 000: **1/4** duty, **1/3** bias (4 COM X 28 SEG) COM: COM1-4 SEG: SEG1-28 001: **1/8** duty, **1/4** bias (8 COM X 24 SEG) COM: COM1-8 SEG: SEG1-24 010: **1/4** duty, **1/3** bias (4 COM X 28 SEG) COM: COM5-8 shared as COM1-4 SEG: SEG1-24, COM1-4 shared as SEG25-28 011: **1/5** duty, **1/3** bias (5 COM X 27 SEG) COM: COM1-5 SEG: SEG1-24, COM6-8 shared as SEG25-27 100: **1/6** duty, **1/3** bias (6 COM X 26 SEG) COM: COM1-6 SEG: SEG1-24, COM7-8 shared as SEG25-SEG26 101: **1/6** duty, **1/4** bias (6 COM X 26 SEG) COM: COM1-6 SEG: SEG1-24, COM7-8 shared as SEG25-SEG26 others: **1/4** duty, **1/3** bias (4 COM X 28 SEG) COM: COM1-4 SEG: SEG1-28
4	**RLCD**	**LCD bias resistor control bit** 0: LCD bias resistor sum is 225k 1: LCD bias resistor sum is 900k
3-2	**FCCTL[1:0]**	**Fast charge time control bits** 00: 1/8LCD com period 01: 1/16 LCD com period 10: 1/32 LCD com period 11: 1/64 LCD com period
1-0	**MOD[1:0]**	**LCD driver mode control bits** 00: traditional mode, bias resistor sum is 225k/900k 01: traditional mode, bias resistor sum is 60k 10: fast charge mode, bias resistor sum between 60k and 225k/900k

Note: *When MODSW = 1, set OP_MODSW to keep LCD counter data or not. When OP_MODSW = 0, the LCD counter data scan continue, when OP_MODSW = 1, the LCD counter data scan stop, keep the data, continue scan when MODSW = 0.*

Table 8.3 LCD Clock Control Register

ACH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DISPCLK0	-	-	-	-	-	-	DCK1	DCK0
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN	-	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
1-0	**DCK[1:0]**	**LCD clock prescaler select bit** 00: 1/4 prescaler 01: 1/3 prescaler 10: 1/2 prescaler 11: 1/1 prescaler ***Note:*** *this register is valid when LCD clock is 128K RC only.*

Note:

(1) When OP_OSC[3:0] is 1010, 1011 or 1101, LCD clock source is 32.768kHz, DISPCLK0 register is invalid, LCD frame is 64Hz.

(2) When OP_OSC[3:0] is others, LCD clock source is 128kHz, set DCK[1:0] bits in DISPCLK0 register, select 1/4, 1/3, 1/2, 1/1, prescaler, so that the LCD frame is 256/4Hz, 256/3Hz, 256/2Hz, 256/1Hz.

Table 8.4 Px Mode Select Register

B6H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0SS	P4S7	P4S6	P4S5	P5S5	P5S4	P0S2	P0S1	P0S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-5	**P4S[7:5]**	**P4 mode select bit** 0: P4.5-P4.7 is I/O 1: P4.5-P4.7 shared as Segment (SEG22-24)
4-3	**P5S[5:4]**	**P5 mode select bit** 0: P5.4-P5.5 is I/O 1: P5.4-P5.5 shared as Segment (SEG20 - SEG21)
2-0	**P0S[2:0]**	**P0 mode select bit** 0: P0.0-P0.2 is I/O 1: P0.0-P0.2 shared as Segment (SEG17 - SEG19)

Table 8.5 P1 mode select register

9CH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1SS	P1S7	P1S6	P1S5	P1S4	P1S3	P1S2	P1S1	P1S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**P1S[7:0]**	**P1 mode select bit** 0: P1.0-P1.7 is I/O 1: P1.0-P1.7 shared as Segment (SEG1 - SEG8)

Table 8.6 P2 mode select register

9DH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2SS	P2S7	P2S6	P2S5	P2S4	P2S3	P2S2	P2S1	P2S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**P2S[7:0]**	**P2 mode select bit** 0: P2.0-P2.7 is I/O 1: P2.0-P2.7 shared as Segment (SEG9 - SEG16)

Table 8.7 P3 mode select register

9EH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P3SS	P3S7	P3S6	P3S5	P3S4	P3S3	P3S2	P3S1	P3S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**P3S[7:0]**	**P3 mode select bit** 0: P3.0-P3.7 is I/O 1: P8.0-P8.7 share as Segment (SEG25-SEG28) or Common (COM1-COM8)

8.1.2 Configuration of LCD RAM

LCD 1/4 duty, 1/3 bias (COM1 - 4, SEG1 - 28)

Address	7	6	5	4	3	2	1	0
	-	-	-	-	COM4	COM3	COM2	COM1
500H	-	-	-	-	SEG1	SEG1	SEG1	SEG1
501H	-	-	-	-	SEG2	SEG2	SEG2	SEG2
502H	-	-	-	-	SEG3	SEG3	SEG3	SEG3
503H	-	-	-	-	SEG4	SEG4	SEG4	SEG4
504H	-	-	-	-	SEG5	SEG5	SEG5	SEG5
505H	-	-	-	-	SEG6	SEG6	SEG6	SEG6
506H	-	-	-	-	SEG7	SEG7	SEG7	SEG7
507H	-	-	-	-	SEG8	SEG8	SEG8	SEG8
508H	-	-	-	-	SEG9	SEG9	SEG9	SEG9
509H	-	-	-	-	SEG10	SEG10	SEG10	SEG10
50AH	-	-	-	-	SEG11	SEG11	SEG11	SEG11
50BH	-	-	-	-	SEG12	SEG12	SEG12	SEG12
50CH	-	-	-	-	SEG13	SEG13	SEG13	SEG13
50DH	-	-	-	-	SEG14	SEG14	SEG14	SEG14
50EH	-	-	-	-	SEG15	SEG15	SEG15	SEG15
50FH	-	-	-	-	SEG16	SEG16	SEG16	SEG16
510H	-	-	-	-	SEG17	SEG17	SEG17	SEG17
511H	-	-	-	-	SEG18	SEG18	SEG18	SEG18
512H	-	-	-	-	SEG19	SEG19	SEG19	SEG19
513H	-	-	-	-	SEG20	SEG20	SEG20	SEG20
514H	-	-	-	-	SEG21	SEG21	SEG21	SEG21
515H	-	-	-	-	SEG22	SEG22	SEG22	SEG22
516H	-	-	-	-	SEG23	SEG23	SEG23	SEG23
517H	-	-	-	-	SEG24	SEG24	SEG24	SEG24
518H	-	-	-	-	SEG25	SEG25	SEG25	SEG25
519H	-	-	-	-	SEG26	SEG26	SEG26	SEG26
51AH	-	-	-	-	SEG27	SEG27	SEG27	SEG27
51BH	-	-	-	-	SEG28	SEG28	SEG28	SEG28

LCD 1/8 duty, 1/4 bias (COM1 - 8, SEG1 - 24)

Address	7	6	5	4	3	2	1	0
	COM8	COM7	COM6	COM5	COM4	COM3	COM2	COM1
500H	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1
501H	SEG2	SEG2	SEG2	SEG2	SEG2	SEG2	SEG2	SEG2
502H	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3
503H	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4
504H	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5
505H	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6
506H	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7
507H	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8
508H	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9
509H	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10
50AH	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11
50BH	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12
50CH	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13
50DH	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14
50EH	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15
50FH	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16
510H	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17
511H	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18
512H	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19
513H	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20
514H	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21
515H	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22
516H	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23
517H	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24

LCD 1/5 duty, 1/3 bias (COM1 - 5, SEG1 - 27)

Address	7	6	5	4	3	2	1	0
	-	-	-	COM5	COM4	COM3	COM2	COM1
500H	-	-	-	SEG1	SEG1	SEG1	SEG1	SEG1
501H	-	-	-	SEG2	SEG2	SEG2	SEG2	SEG2
502H	-	-	-	SEG3	SEG3	SEG3	SEG3	SEG3
503H	-	-	-	SEG4	SEG4	SEG4	SEG4	SEG4
504H	-	-	-	SEG5	SEG5	SEG5	SEG5	SEG5
505H	-	-	-	SEG6	SEG6	SEG6	SEG6	SEG6
506H	-	-	-	SEG7	SEG7	SEG7	SEG7	SEG7
507H	-	-	-	SEG8	SEG8	SEG8	SEG8	SEG8
508H	-	-	-	SEG9	SEG9	SEG9	SEG9	SEG9
509H	-	-	-	SEG10	SEG10	SEG10	SEG10	SEG10
50AH	-	-	-	SEG11	SEG11	SEG11	SEG11	SEG11
50BH	-	-	-	SEG12	SEG12	SEG12	SEG12	SEG12
50CH	-	-	-	SEG13	SEG13	SEG13	SEG13	SEG13
50DH	-	-	-	SEG14	SEG14	SEG14	SEG14	SEG14
50EH	-	-	-	SEG15	SEG15	SEG15	SEG15	SEG15
50FH	-	-	-	SEG16	SEG16	SEG16	SEG16	SEG16
510H	-	-	-	SEG17	SEG17	SEG17	SEG17	SEG17
511H	-	-	-	SEG18	SEG18	SEG18	SEG18	SEG18
512H	-	-	-	SEG19	SEG19	SEG19	SEG19	SEG19
513H	-	-	-	SEG20	SEG20	SEG20	SEG20	SEG20
514H	-	-	-	SEG21	SEG21	SEG21	SEG21	SEG21
515H	-	-	-	SEG22	SEG22	SEG22	SEG22	SEG22
516H	-	-	-	SEG23	SEG23	SEG23	SEG23	SEG23
517H	-	-	-	SEG24	SEG24	SEG24	SEG24	SEG24
518H	-	-	-	SEG25	SEG25	SEG25	SEG25	SEG25
519H	-	-	-	SEG26	SEG26	SEG26	SEG26	SEG26
51AH	-	-	-	SEG27	SEG27	SEG27	SEG27	SEG27

LCD 1/6 duty, 1/3 or 1/4 bias (COM1 - 6, SEG1 - 26)

Address	7	6	5	4	3	2	1	0
	-	**-**	**COM6**	**COM5**	**COM4**	**COM3**	**COM2**	**COM1**
500H	-	-	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1
501H	-	-	SEG2	SEG2	SEG2	SEG2	SEG2	SEG2
502H	-	-	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3
503H	-	-	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4
504H	-	-	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5
505H	-	-	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6
506H	-	-	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7
507H	-	-	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8
508H	-	-	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9
509H	-	-	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10
50AH	-	-	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11
50BH	-	-	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12
50CH	-	-	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13
50DH	-	-	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14
50EH	-	-	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15
50FH	-	-	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16
510H	-	-	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17
511H	-	-	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18
512H	-	-	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19
513H	-	-	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20
514H	-	-	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21
515H	-	-	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22
516H	-	-	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23
517H	-	-	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24
518H	-	-	SEG25	SEG25	SEG25	SEG25	SEG25	SEG25
519H	-	-	SEG26	SEG26	SEG26	SEG26	SEG26	SEG26

8.2 LED Driver

The LED driver contains a controller, a duty generator with 3-8 Common signal pins and 8 Segment driver pins. Support 1/3-1/8 duty voltage driver mode, the 1/3-1/8 duty is adjustable. Set DISPSEL bit can select the LED driver mode.

LED SEG1-SEG8 can be shared as I/O. When DISPSEL = 1, LCD is disable and LED is enable. The P0SS and P2SS registers are invalid, select the mode of LED_SEG 1-8 and LED_C1-LED_C8 is controlled by P1SS, P3SS registers.

The DISPSEL bit must be set to 1 before enable LED driver.

The Common Ports integrated large current sink ability, when OP_P37-P34 = 0 and OP_P33-P.0 = 1, the Port3 large current sink ability is enable. (Refer to Code Option)

During the Power in Reset, Pin Reset, LVR Reset and Watchdog Reset, the LED driver will be turned off.

8.2.1 Register

Table 8.8 LED Control Register

ABH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DISPCON	DISPSEL	LEDON	-	DUTY0	-	-	-	-
R/W	R/W	R/W	-	R/W	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	0	0	-	0	-	-	-	-

Bit Number	Bit Mnemonic	Description
7	**DISPSEL**	**LCD/LED control bit** 0: select LCD driver 1: select LED driver
6	**LEDON**	**LED control bit** 0: turn off LED driver 1: turn on LED driver
4	**DUTY0** **DUTY[2:1]**	**LED duty selection bit (Combination control with DUTY[2:1])** **Refer to DUTY[2:1]**

Note: *SH79F3283 has LCD and LED driver, but cannot work at the same time. When DISPSEL = 1, LCD is disabled, when DISPSEL = 0, LED is disable.*

Table 8.9 LED Control Register 1

ADH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DISPCON1	MODSW	DUTY2	DUTY1	-	-	-	-	-
R/W	R/W	R/W	R/W	-	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	0	0	0	-	-	-	-	-

Bit Number	Bit Mnemonic	Description
6-5	**DUTY0** **DUTY[2:1]**	**LED duty selection bit (Combination control with DUTY0)** 000: 1/4 duty 001: 1/8 duty 010: 1/3 duty 011: 1/5 duty 100: 1/6 duty 101: 1/7 duty others: 1/4 duty
7	**MODSW**	**LCD/LED shared control bit** 0: P0SS is valid 1: all the LCD/LED Pins worked as IO ***Note***: *When MODSW = 1, set OP_MODSW to keep LCD counter data or not. When OP_MODSW = 0, the LCD counter data scan continue, when OP_MODSW = 1, the LCD counter data scan stop, keep the data, continue scan when MODSW = 0.*

Table 8.10 LED Clock Control Register

ACH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DISPCLK0	-	-	-	-	-	-	DCK0.1	DCK0.0
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
1-0	**DCK[1:0]**	**LED clock prescaler select bit** 00: 1/4 prescaler 01: 1/3 prescaler 10: 1/2 prescaler 11: 1/1 prescaler ***Note:*** *this register is valid when LCD clock is 128K RC only.*

Note:

(1) When OP_OSC[3:0] is 1010, 1011 or 1101, LCD clock source is 32.768kHz, DISPCLK0 register is invalid, LCD frame is 64Hz.

(2) When OP_OSC[3:0] is others, LCD clock source is 128kHz, set DCK[1:0] bits in DISPCLK0 register, select 1/4, 1/3, 1/2, 1/1, prescaler, so that the LCD frame is 256/4Hz, 256/3Hz, 256/2Hz, 256/1Hz.

Table 8.11 P1 mode select register

9CH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1SS	P1S7	P1S6	P1S5	P1S4	P1S3	P1S2	P1S1	P1S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**P1S[7:0]**	**P1 mode select bit** 0: P1.0-P1.7 is I/O 1: P1.0-P1.7 shared as Segment (LED_S1 - LED_S8)

Table 8.12 P3 mode select register

9EH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P3SS	P3S7	P3S6	P3S5	P3S4	P3S3	P3S2	P3S1	P3S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**P3S[7:0]**	**P3 mode select bit** 0: P3.0-P3.7 is I/O 1: P3.0-P3.7 shared as Common (LED_C1 - LED_C8)

8.2.2 Configuration of LED RAM

LED 1/3 duty (LED_C1 - 3, LED_S1 - 8)

Address		7	6	5	4	3	2	1	0
500H	COM1	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
501H	COM2	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
502H	COM3	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1

LED 1/4 duty (LED_C1 - 4, LED_S1 - 8)

Address		7	6	5	4	3	2	1	0
500H	COM1	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
501H	COM2	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
502H	COM3	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
503H	COM4	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1

LED 1/5 duty (LED_C1 - 5, LED_S1 - 8)

Address		7	6	5	4	3	2	1	0
500H	COM1	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
501H	COM2	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
502H	COM3	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
503H	COM4	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
504H	COM5	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1

LED 1/6 duty (LED_C1 - 6, LED_S1 - 8)

Address		7	6	5	4	3	2	1	0
500H	COM1	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
501H	COM2	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
502H	COM3	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
503H	COM4	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
504H	COM5	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
505H	COM6	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1

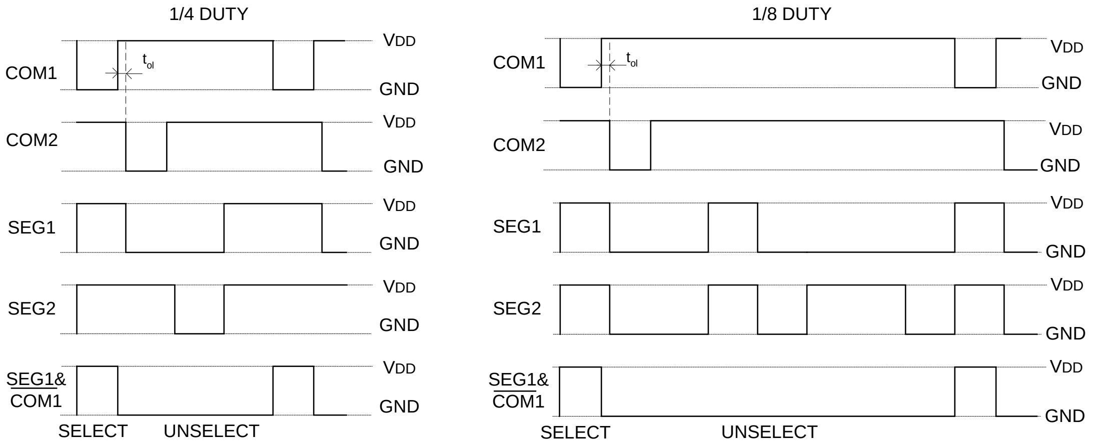
LED 1/7 duty (LED_C1 -7, LED_S1 - 8)

Address		7	6	5	4	3	2	1	0
500H	COM1	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
501H	COM2	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
502H	COM3	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
503H	COM4	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
504H	COM5	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
505H	COM6	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
506H	COM7	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1

LED 1/8 duty (LED_C1 - 8, LED_S1 - 8)

Address		7	6	5	4	3	2	1	0
500H	COM1	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
501H	COM2	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
502H	COM3	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
503H	COM4	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
504H	COM5	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
505H	COM6	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
506H	COM7	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
507H	COM8	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1

LED Waveform



Note: *t_{OL} is overlap time of LED Common, t_{OL} = 20µs - 40µs*

8.3 12-bit PWM0 (Pulse Width Modulation)

8.3.1 Feature

- Three complementary output with dead time control
- Provided overflow and duty interrupt function on every PWM period
- Selectable output polarity
- Fault detect function provided to disable PWM output immediately
- Lock register provided to avoid PWM control register to be unexpected change

The SH79F3283 has one 12-bit PWM module, which can provide the pulse width modulation waveform with the period and the duty being controlled individually by corresponding register.

PWM timer can be turned to inactive state by the input of FLT pin automatically if EFLT is set

PWM timer also provides 1 interrupts for PWM0. This makes it possible to change period or duty of next cycle in every PWM period.

8.3.2 PWM Module Enable

Table 8.13 PWM Module Enable Register

CFH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMEN	EPWM0	EFLT	PWM01COE	PWM01BOE	PWM01AOE	PWM0COE	PWM0BOE	PWM0AOE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**EPWM0**	**12 bit PWM0 output enable bit** 0: disable PWM0, shared as I/O 1: enable PWM0
6	**EFLT**	**FLT pin configuration** 0: general purpose I/O or $\overline{SS}$ pin 1: PWM Fault Detect input pin
5-3	**PWM01COE** **PWM01BOE** **PWM01AOE**	**12 bit PWM output PWM01x enable** 0: PWM01x (x = A, B, C) output disable, shared as I/O 1: PWM01x output enable
2-0	**PWM0COE** **PWM0BOE** **PWM0AOE**	**12 bit PWM output PWM0x enable** 0: PWM0x (x = A, B, C) output disable, shared as I/O 1: PWM0x output enable

PWM output will be disabled at the same time when the PWM Enable register is clear to 0.

The main purpose of the FLT pin is to inactivate the PWM output signals and driver them into an inactive state. The action of the FLT is performed directly in hardware so that when a fault occurs, it can be managed quickly and the PWM output are put into an inactive state to save the power devices connected to the PWM. The FLT pin has no internal pull-high resistor.

If EFLT is set to 0, it means the level on FLT pin has no effect on PWM timer.

8.3.3 PWM Timer Lock Register

This register is used to control the change of PWM timer enable register, PWM control register and PWM period register and PWM duty register. Only when the data in this register is #55h, it is possible to change these register. Otherwise they cannot be changed.

This register is to enhance the anti-noise ability of SH79F3283.

Table 8.14 PWM Timer Lock Register

E7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMLO	PWMLO.7	PWMLO.6	PWMLO.5	PWMLO.4	PWMLO.3	PWMLO.2	PWMLO.1	PWMLO.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PWMLO[7:0]**	**PWM lock register** 55h: enable to change PWM related registers else: disable to change PWM related registers

8.3.4 12-bit PWM Timer

The SH79F3283 has one 12-bit PWM module. The PWM module can provide the pulse width modulation waveform with the period and the duty being controlled, individually. The PWMC is used to control the PWM module operation with proper clocks. The PWMPH/L is used to control the period cycle of the PWM module output. PWMDH/L is used to control the duty in the waveform of the PWM module output.

It is acceptable to change these 3 registers during PWM output Enable. All the change will take affect at the next PWM period.

Table 8.15 12-bit PWM Control Register

D2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM0C	PWM0IE	PWM0IF	TnCK02	FLTS	FLTC	PWM0S	TnCK01	TnCK00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**PWM0IE**	**PWM0 interrupt enable bit (When EPWM bit in IEN1 is set)** 0: Disable PWM0 interrupt 1: Enable PWM0 interrupt
6	**PWM0IF**	**PWM0 interrupt flag bit** 0: Clear by software 1: Set by hardware to indicate that the PWM0 period counter overflow
5	**TnCK02**	**12 bit PWM clock source select bit (Combination control with TnCK0[1:0])** **Refer to TnCK0[1:0]**
4	**FLTS**	**FLT states bit** 0: PWM is normal states, cleared by software 1: PWM is in inactive states, set automatically by hardware
3	**FLTC**	**FLT pin configuration** 0: inactivate the PWM output when FLT is low level 1: inactivate the PWM output when FLT is high level
2	**PWM0S**	**PWM0 output normal mode of duty cycle** 0: high active, PWM0 output high during duty time, output low during remain period time 1: low active, PWM0 output low during duty time, output high during remain period time
1-0	**TnCK0[1:0]**	**12 bit PWM clock source select bit (Combination control with TnCK02])** 000: oscillator clock/2 001: oscillator clock/4 010: oscillator clock/8 011: oscillator clock/16 100: oscillator clock/1 101: oscillator clock/32 110: oscillator clock/64 111: oscillator clock/256 ***Note:*** *when OP_OSC is 0000, 0011 or 1010, PWM clock is internal RC; when OP_OSC is 1110, PWM clock is crystal/ceramic from XTAL pin; when OP_OSC is 0110 or 1101, PWM clock is crystal/ceramic from XTALX pin.*

Note:

(1) Inactivate PWM here means PWM0 outputs keep Low (if PWM0S = 0) or High (if PWM0S = 1).

(2) The PWM output will remain in the inactive states as soon as the high/low level of FLT pin is detected

(3) Clearing FLTS bit when a FAULT input is coming will not success.

Table 8.16 PWM Period Control Register (PWM0PL)

D3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM0PL	PP0.7	PP0.6	PP0.5	PP0.4	PP0.3	PP0.2	PP0.1	PP0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PP0[7:0]**	12-bit PWM period low 8 bits registers

Table 8.17 PWM Period Control Register (PWM0PH)

D4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM0PH	-	-	-	-	PP0.11	PP0.10	PP0.9	PP0.8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**PP0[11:8]**	12-bit PWM period high 4 bits registers

PWM output period cycle = [PP0.11, PP0.0] X PWM clock.
When [PP0.11, PP0.0] = 000H, If PWM0S = 0, regardless of the PWM duty cycle, PWM0x(x = A, B, C) output low.
When [PP0.11, PP0.0] = 000H, If PWM0S = 1, regardless of the PWM duty cycle, PWM0x(x = A, B, C) output high.

Table 8.18 PWM Duty Control Register (PWM0DL)

D5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM0DL	PD0.7	PD0.6	PD0.5	PD0.4	PD0.3	PD0.2	PD0.1	PD0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PD0[7:0]**	12-bit PWM duty low 8 bits registers

Table 8.19 PWM Duty Control Register (PWM0DH)

D6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM0DH	-	-	-	-	PD0.11	PD0.10	PD0.9	PD0.8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**PD0[11:8]**	12-bit PWM duty high 4 bits registers

PWM output duty cycle = [PD0.11, PD0.0] X PWM clock.

If [PP0.11, PP0.0] ≤ [PD0.11, PD0.0], PWM0x(x = A, B, C) outputs high level when the PWM0S bit is set to “0”.

If [PP0.11, PP0.0] ≤ [PD0.11, PD0.0], PWM0x(x = A, B, C) outputs GND level when the PWM0S bit is set to “1”.

Programming Note:

(1) Set PWMLO register to 55H and select the PWM module system clock.

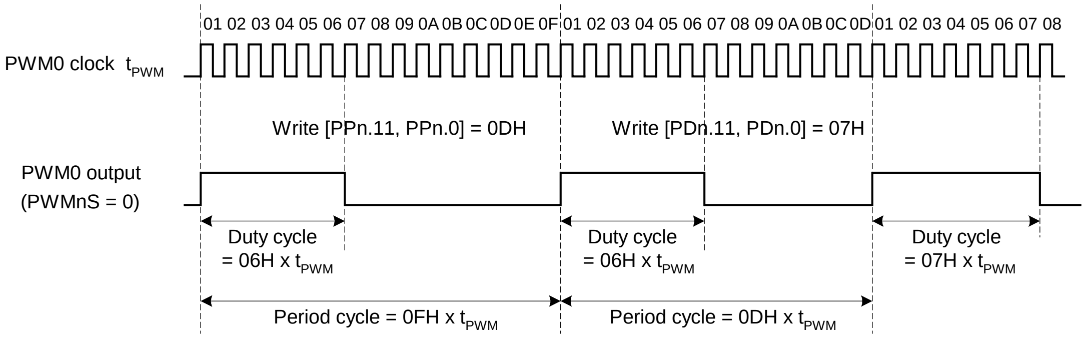
(2) Set the PWM period/duty cycle by writing proper value to the PWM period control register (PWMP) or PWM duty control register (PWMD). First set the low Byte, then the high Byte. Note that even if the high constant value keeps unchanged, it also needs to rewrite once, otherwise, the low modify is invalid.

(3) Select the PWM output mode (high level valid or low level valid) by writing the PWM0S bit in the PWM control register (PWMC).

(4) In order to output the desired PWM waveform, enable the PWM module by writing "1" to the EPWM0x (x = A, B, C) or EPWM01x (x = A, B, C) bit in the PWM control register (PWMC).

(5) If the PWM period cycle or duty cycle is to be changed, the writing flow should be followed as described in step 2 or step 3. The modified reloading counter value will take effect in the next period.

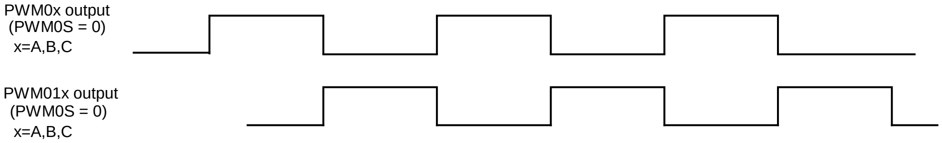
(6) Change the data in PWMLO register not equal to 55h in order to enhance the anti-noise ability.


01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 01 02 03 04 05 06 07 08
PWM0 clock t_{PWM}
Write [PPn.11, PPn.0] = 0DH
Write [PDn.11, PDn.0] = 07H
PWM0 output
(PWMnS = 0)
Duty cycle
= 06H x t_{PWM}
Duty cycle
= 06H x t_{PWM}
Duty cycle
= 07H x t_{PWM}
Period cycle = 0FH x t_{PWM}
Period cycle = 0DH x t_{PWM}

PWM0 Output Period or Duty Cycle Changing Example

8.3.5 PWM01x (x = A, B, C)

Generally PWM0x(x = A, B, C) have a 180 degree phase delay with PWM01x (x = A, B, C) as shown below when there is no dead time inserted. It is automatically generated by hardware when EPWM01x (x = A, B, C) in PWM timer enable register is set.



PWM0 and PWM01 Output Waveform

Note:

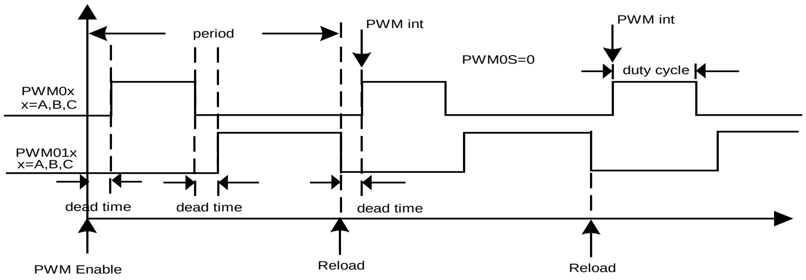
(1) That even if PWM0x(x = A, B, C) are disable, PWM01x(x = A, B, C) can also work if enable.

(2) If EFLT is set, when a valid event occurs on FLT pin, PWM0x(x = A, B, C) and PWM01x(x = A, B, C) are both LOW (PWMS = 0) or both HIGH (PWMS = 1).

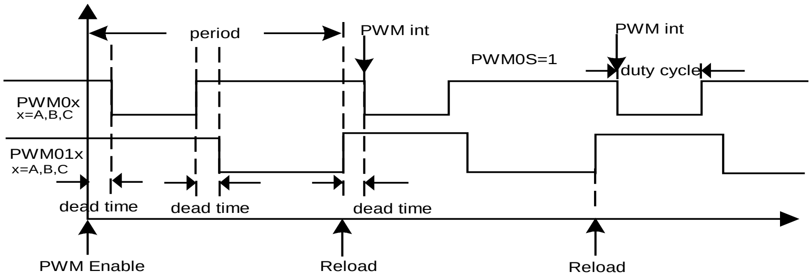
8.3.6 Dead time

SH79F3283 provides dead time function on-chip.

When PWM0S = 0, the dead time is generated as below.



When PWM0S = 1, the dead time is generated as below.



By writing PWM0 dead time control register, a dead time can be generated between PWM0x (x = A, B, C) and PWM01x (x = A, B, C).

PWM01x (x = A, B, C) has the same period as PWM0x (x = A, B, C)

Note:

(1) The dead time must be set before PWM output enable. Otherwise, dead time will not change. So in order to change dead time, please disable PWM output first (While PWMLO is #55H), then change the dead time, enable PWM output. Finally, change the data in PWMLO not equal to #55H in order to make sure the PWM registers would not be changed by noise.

(2) In order to generate dead time, please make sure that (PWM0x Period-PWM0x Duty) > 2 X PWM01x dead time control. Otherwise the output of PWM01x is high level when PWMS = 1 or GND when PWMS = 0.

(3) PWMDT is to used to control Dead Time, the step value is fixed oscillator clock time, but period and duty value is refer to TnCK2-0. 2 oscillator clocks at least.

(4) If dead time is needed, any time when PWM is disabled, before enable PWM again, dead time register must be clear to 0 at first, and then set the proper value.

Table 8.20 PWM0 Dead Time Control Register

D1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM0DT	DT0.7	DT0.6	DT0.5	DT0.4	DT0.3	DT0.2	DT0.1	DT0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**DT0[7:0]**	**12 bit PWM0 dead time control** The dead time period = (DT0.7 - DT0.0) X t_{OSC}

8.4 12-bit PWM1 (Pulse Width Modulation)

8.4.1 Feature

- 8 bit resolution ratio, provide prescaler function
- Provided overflow and duty interrupt function on every PWM period
- Selectable output polarity, can be use as normal timer when the enable bit is set to 0

The SH79F3283 has one 8-bit PWM module, which can provide the pulse width modulation waveform with the period and the duty being controlled individually by corresponding register. The PWM module clock source or pin output selection is controlled by PWM1C register. The PWM module Period selection is controlled by PWM1P register. The PWM module Duty selection is controlled by PWM1D register.

8.4.2 Register

Table 8.21 PWM1 Control Register

D9H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1C	PWM1EN	PWM1S	TnCK11	TnCK10	-	PWM1IE	PWM1IF	PWM1OE
R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	-	0	0	0

Bit Number	Bit Mnemonic	Description
7	**PWM1EN**	**PWM1 module enable control bit** 0: disable PWM1 module 1: enable PWM1 module
6	**PWM1S**	**PWM1 output normal mode of duty cycle** 0: high active, PWM1 output high during duty time, output low during remain period time 1: low active, PWM1 output low during duty time, output high during remain period time
5-4	**TnCK1[1:0]**	**PWM1 clock select bit** 00: system clock/1 01: system clock/8 10: system clock/64 11: system clock/256
2	**PWM1IE**	**PWM1 interrupt enable bit (When EPWM bit in IEN1 is set)** 0: Disable PWM1interrupt 1: Enable PWM1 interrupt
1	**PWM1IF**	**PWM1 interrupt flag bit** 0: Clear by software 1: Set by hardware to indicate that the PWM1 period counter overflow
0	**PWM1OE**	**PWM1 output control bit** 0: PWM1 is disable, shared as I/O ***Note:*** *This bit is set to 0, but PWM1EN = 1, so that PWM1 module is still working, just no waveform output. PWM1* can be use as normal timer 1: PWM1 is enable ***Note:*** *If this bit is set to 1 and PWM1EN = 0, so that PWM1 output inactive level (Select high level output low level, select low level output high level)*

Table 8.22 PWM1 Period Control Register (PWM1PL)

DAH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1P	PWM1P.7	PWM1P.6	PWM1P.5	PWM1P.4	PWM1P.3	PWM1P.2	PWM1P.1	PWM1P.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PWM1P[7:0]**	**PWM1output Period = PWM1P * PWM clock** When PWM1P = 00H, if PWM1S = 0, PWM1 output low When PWM1P = 00H, if PWM1S = 1, PWM1 output high

Table 8.23 PWM1 Duty Control Register (PWM1DL)

DBH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1D	PWM1D.7	PWM1D.6	PWM1D.5	PWM1D.4	PWM1D.3	PWM1D.2	PWM1D.1	PWM1D.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PWM1D[7:0]**	**PWM1 Duty control bit** **Special Case:** 1 When PWM1P ≤ PWM1D: If PWM1S = 0, PWM1 output high level If PWM1S = 1, PWM1 output low level 2 WhenPWM1D = 00H: If PWM1S = 0, PWM1 output low level If PWM1S = 1, PWM1 output high level

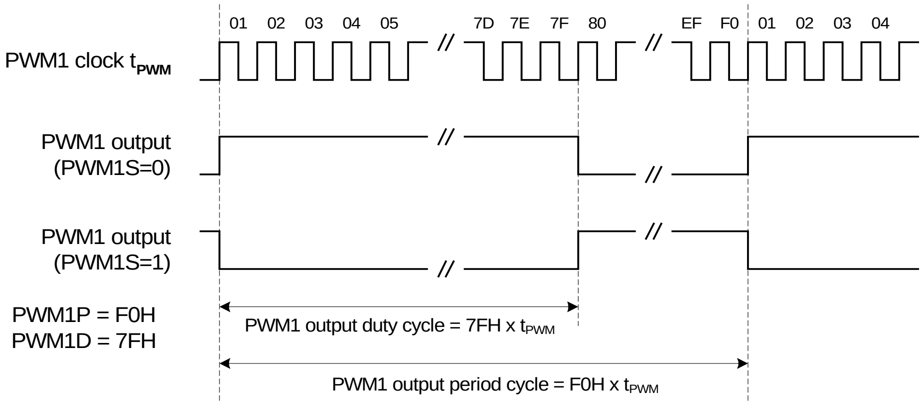
Note:

(1) PWM1EN bit control PWM1 disable or enable

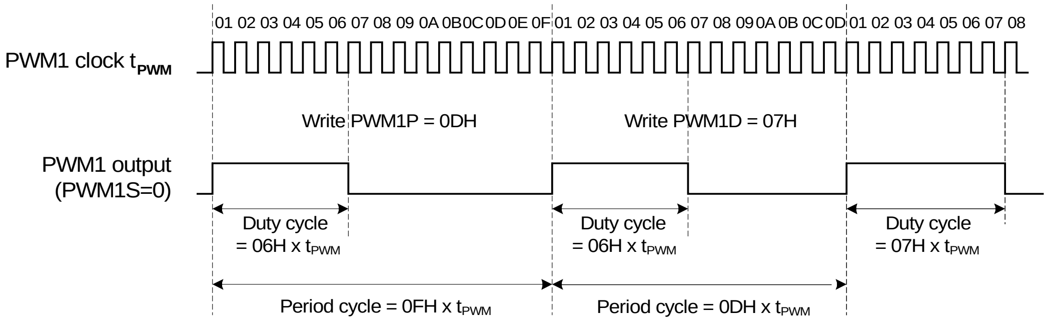
(2) PWM1OE bit control P4.5 is IO or PWM1 output port

(3) EPWM bit in IEN1 register control PWM1 interrupt disable or enable

(4) If PWM1EN = 1, PWM1 module enable, but PWM1OE = 0, PWM1 output disable, PWM1 can be used as a 8-bit timer.



PWM1 Output Example


01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 01 02 03 04 05 06 07 08
PWM1 clock t_{PWM}
Write PWM1P = 0DH
Write PWM1D = 07H
PWM1 output (PWM1S=0)
Duty cycle = 06H x t_{PWM}
Duty cycle = 06H x t_{PWM}
Duty cycle = 07H x t_{PWM}
Period cycle = 0FH x t_{PWM}
Period cycle = 0DH x t_{PWM}

PWM1 Output Period or Duty Cycle Changing Example

8.5 EUART

8.5.1 Feature

- The SH79F3283 has two enhanced EUART (EUART0/1) which are compatible with the conventional 8051
- The EUART0 baud rate can be selected from the divided clock of the system clock, or Timer4/2 overflow rate, The Euart1 baud rate generator is an 15-bit up-counting timer
- Enhancements over the standard 8051 the EUART include Framing Error detection and automatic address recognition
- The EUART can be operated in four modes

8.5.2 EUART0

The EUART0 can be operated in 4 modes. Users must initialize the SCON before any communication can take place. This involves selection of the Mode and the baud rate. The Timer4/2 should also be initialized if the mode 1 or the mode 3 is used.

In all of the 4 modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TXD0 pin and shift in 8 bits on the RxD0 pin. Reception is initiated in the other modes by the input start bit if REN = 1. The external transmitter will start the communication by transmitting the start bit.

EUART Mode Summary

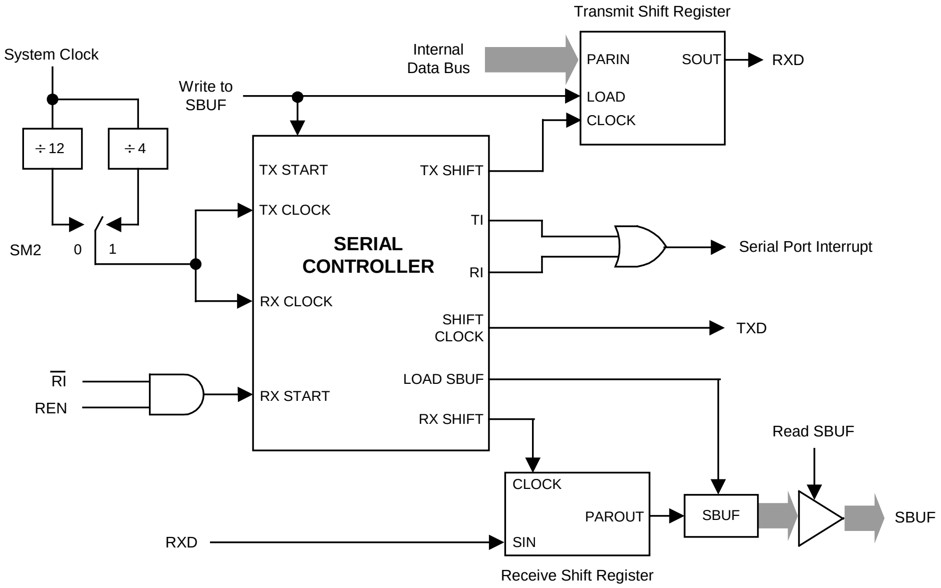
SM0	SM1	Mode	Type	Baud Rate	Frame Size	Start Bit	Stop Bit	9th bit
0	0	0	Synch	f_{SYS}/(4 or 12)	8 bits	NO	NO	None
0	1	1	Asynch	Timer 4 or 2 overflow rate/(16 or 32)	10 bits	1	1	None
1	0	2	Asynch	f_{SYS}/(32 or 64)	11 bits	1	1	0, 1
1	1	3	Asynch	Timer 4 or 2 overflow rate/(16 or 32)	11 bits	1	1	0, 1

Mode0: Synchronous Mode, Half duplex

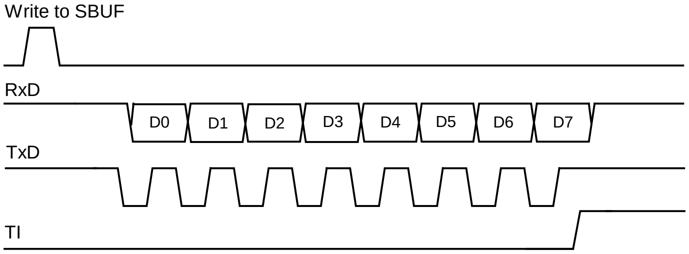
This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD pin. TXD is used to output the shift clock. The TXD clock is provided by the 3283 whether the device is transmitting or receiving. Therefore, this mode is a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted / received first.

The baud rate is programmable to either 1/12 or 1/4 of the system clock. This baud rate is determined in the SM2 bit (SCON.5). When this bit is set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock. The only difference from standard 8051 is that SH79F3283 in the mode 0 has variable baud rate.

The functional block diagram is shown below. Data enters and exits the serial port on the RXD pin. The TXD pin is used to output the SHIFT CLOCK. The SHIFT CLOCK is used to shift data into and out of the SH79F3283.

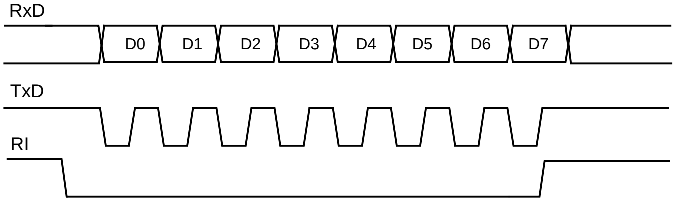


Any instruction that uses SBUF as a destination register ("write to SBUF" signal) will start the transmission. The next system clock tells the Tx control block to commence a transmission. The data shift occurs at the falling edge of the SHIFT CLOCK, and the contents of the transmit shift register is shifted one position from left to the right. As data bits shift to the right, zeros come in from the left. After transmission of all 8 bits in the transmit shift register, the Tx control block will deactivates SEND and sets TI (SCON.1) at the rising edge of the next system clock.



Send Timing of Mode 0

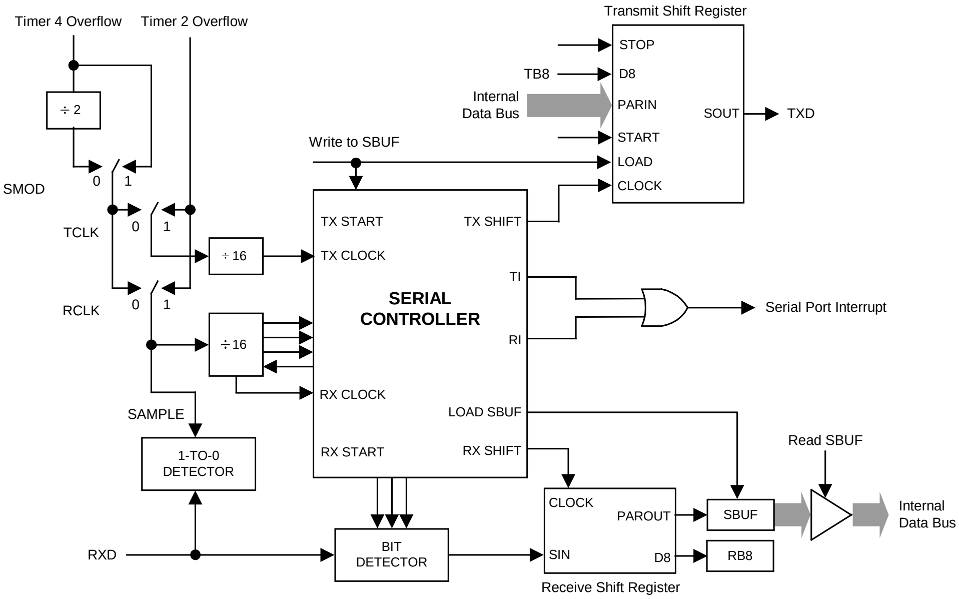
Reception is initiated by the condition REN (SCON.4) = 1 and RI (SCON.0) = 0. The next system clock activates RECEIVE. The data latch occurs at the rising edge of the SHIFT CLOCK, and the contents of the receive shift register are shifted one position to the left. After the receiving of all 8 bits into the receive shift register, the RX control block will deactivates RECEIVE and sets RI at the rising edge of the next system clock, and the reception will not be enabled till the RI is cleared by software.



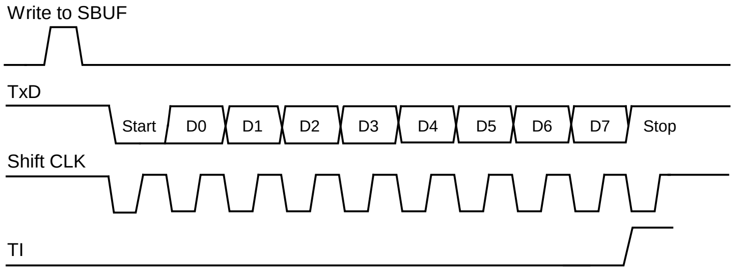
Receive Timing of Mode 0

Mode1: 8-Bit EUART, Variable Baud Rate, Asynchronous Full-Duplex

This mode provides the 10 bits full duplex asynchronous communication. The 10 bits consist of a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When receiving, the eight data bits are stored in SBUF and the stop bit goes into RB8 (SCON.2). The serial receive and transmit baud rate is 1/16 of the Timer4/2 overflow (Refer to **Baud Rate** Section for details). The functional block diagram is shown below.



Transmission begins with a “write to SBUF” signal, and it actually commences at the next system clock following the next rollover in the divide-by-16 counter (divide baud-rate by 16), thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SUBF” signal. The start bit is firstly put out on TXD pin, then the 8 bits of data is the next. After all 8 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TXD pin, and the TI flag is set at the same time that the stop is send.



Send Timing of Mode 1

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data with the detection of a falling edge on the RXD pin. For this purpose RXD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps the divide-by-16 counter to synchronize with the serial data of RXD pin.

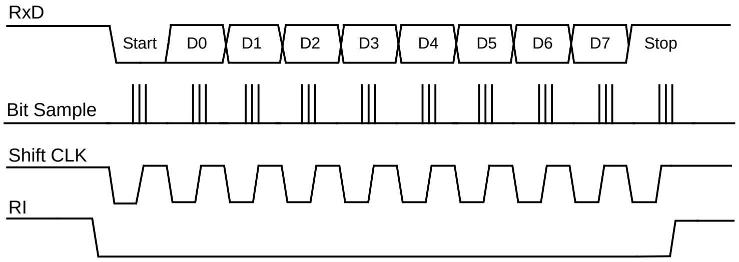
The divide-by-16 counter divides each bit time into 16 states. The bit detector samples the value of RXD at the 7th, 8th and 9th counter states of each bit time. At least 2 the sampling values have no difference in the state of the three samples, data can be received This is done for noise rejection. If the first bit after the falling edge of RXD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again waiting for a falling edge in the RXD pin. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register. After shifting in 8 data bits and the stop bit, the SBUF and RB8 are loaded and RI is set, if the following conditions are met:

1. RI must be 0

2. Either SM2 = 0, or the received stop bit = 1

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.

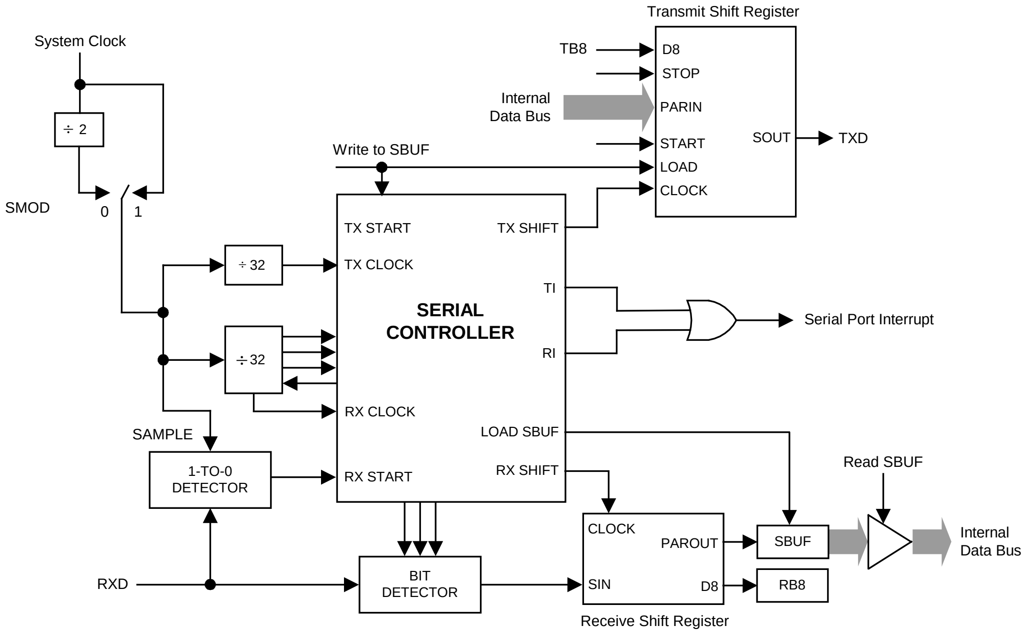
At the time, the receiver goes back to looking for another falling edge on the RXD pin. And the user should clear RI by software for further reception.



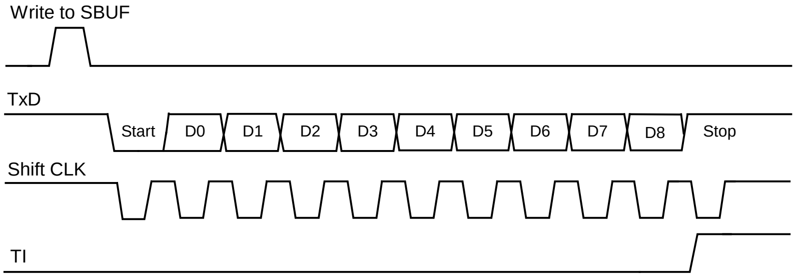
Receive Timing of Mode 1

Mode2: 9-Bit EUART, Fixed Baud Rate, Asynchronous Full-Duplex

This mode provides the 11 bits full duplex asynchronous communication. The 11 bit consists of one start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). Mode 2 supports multiprocessor communications and hardware address recognition (Refer to Multiprocessor Communication Section for details). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1, for example, the parity bit P in the PSW or used as data/address flag in multiprocessor communications. When data is received, the 9th data bit goes into RB8 and the stop bit is not saved. The baud rate is programmable to either 1/32 or 1/64 of the system working frequency, as determined by the SMOD bit in PCON. The functional block diagram is shown below:



Transmission begins with a “write to SBUF” signal, the “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register. Transmission actually commences at the next system clock following the next rollover in the divide-by-16 counter (thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SUBF” signal). The start bit is firstly put out on TXD pin, then the 9 bits of data is the next. After all 9 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TXD pin, and the TI flag is set at the same time.



Send Timing of Mode 2

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RXD pin. For this purpose RXD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps the divide-by-16 counter to synchronize with the serial data of RXD pin.

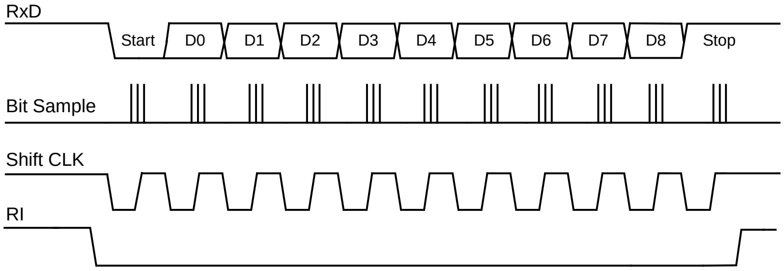
The divide-by-16 counter divides each bit time into 16 states. The bit detector samples the value of RXD at the 7th, 8th and 9th counter state of each bit time. At least 2 the sampling values have no difference in the state of the three samples, data can be received. This is done for noise rejection. If the first bit detected after the falling edge of RXD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again waiting for a falling edge in the RXD pin. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register. After shifting in 9 data bits and the stop bit, the SBUF and RB8 are loaded and RI is set, if the following conditions are met:

1. RI must be 0

2. Either SM2 = 0, or the received 9th bit = 1 and the received byte accords with Given Address

If these conditions are met, then the 9th bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.

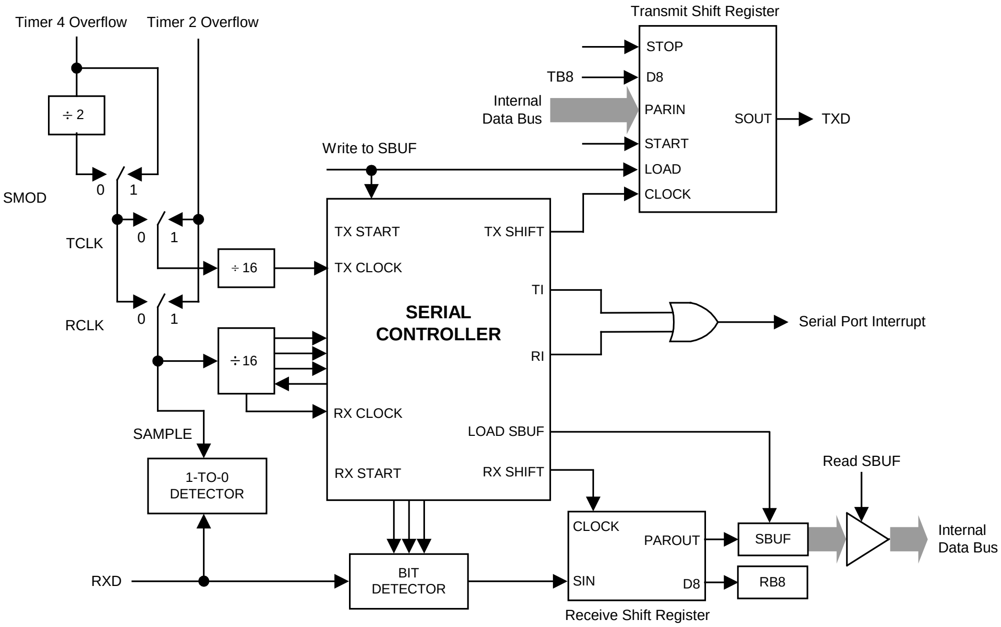
At the time, the receiver goes back to looking for another falling edge on the RXD pin. And the user should clear RI by software for further reception.



Receive Timing of Mode 2

Mode3: 9-Bit EUART, Variable Baud Rate, Asynchronous Full-Duplex

Mode3 uses transmission protocol of the Mode2 and baud rate generation of the Mode1.



Baud Rate Generate

In Mode0, the baud rate is programmable to either 1/12 or 1/4 of the system clock. This baud rate is determined by SM2 bit. When set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock.

In Mode1 & Mode3, the baud rate can be selected from Timer4/2 overflow rate.

Individually set TCLK (T2CON.4) and RCLK (T2CON.5) to 1 to select Timer2 as baud clock source of TX & RX (Refer to "Timer" section for details). Whether TCLK or RCLK is set to logic 1, Timer2 is baud rate generator mode. If TCLK and RCLK are logic 0, Timer4 will be used as the baud clock source of TX & RX.

The Mode1 & 3 baud rate equations are shown below. [RCAP2H, RCAP2L] is the 16-bit auto-reload register for Timer2, and [TH4, TL4] is the 16-bit reload register for Timer4.

$\mathrm{BaudRate} = \frac{1}{2 \times 16} \times \frac{f_{SYS}}{65536 - [\mathrm{RCAP2H}, \mathrm{RCAP2L}]}$, Baud Rate using Timer2, the clock source of Timer2 is system clock.

$\mathrm{BaudRate} = \frac{1}{16} \times \frac{f_{T2}}{65536 - [\mathrm{RCAP2H}, \mathrm{RCAP2L}]}$, Baud Rate using Timer2, the clock source of T2 input pin.

$\mathrm{BaudRate} = \frac{2^{SMOD}}{2 \times 16} \times \frac{f_{T4}/\mathrm{PRESCALER}}{65536 - [\mathrm{TH4}, \mathrm{TL4}]}$, Baud Rate using Timer4, Timer4 works in Mode1.

In Mode2, the baud rate is programmable to either 1/32 or 1/64 of the system clock. This baud rate is determined by the SMOD bit (PCON.7). When this bit is set to 0, EUART runs at 1/64 of the system clock. When set to 1, EUART runs at 1/32 of the system clock.

$$\mathrm{BaudRate} = 2^{\mathrm{SMOD}} \times (\frac{f_{\mathrm{SYS}}}{64})$$

Multi-Processor Communication

Software Address Recognition

Modes2 and 3 of the EUART have a special function for multi-processor communication. In these modes, 9 data bits are received. The 9th bit goes into RB8. Then a stop bit follows. The EUART can be programmed such that when the stop bit is received, the serial port interrupt will be activated (i.e. the request flag RI is set) only if RB8 = 1. This feature is enabled by setting the bit SM2 in SCON.

A way to use this feature in multiprocessor communications is as follows. If the master processor wants to transmit a block of data to one of the several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte by using the 9th bit. The 9th bit is 1 in an address byte, the 9th bit is 0 in a data byte.

If SM2 is 1, slave will not respond to data byte interrupt. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. After having received a complete message, the slave sets SM2 again. The slaves that were not addressed keep their SM2 setting and go on with their business, ignoring the incoming data bytes.

Note: *In Mode0, SM2 is used to select baud rate doubling. In Mode1, SM2 can be used to check the validity of the stop bit. If SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.*

Automatic (Hardware) Address Recognition

In Mode2 & 3, setting the SM2 bit will configure EUART act as following: when a stop bit is received, EUART will generate an interrupt only if the 9th bit that goes into RB8 is logic 1 (address byte) and the received data byte matches the EUART slave address. Following the received address interrupt, the slave should clear its SM2 bit to enable interrupts to receive the following data byte(s).

The 9-bit mode requires that the 9th information bit is 1 to indicate that the received information is address rather than data. When the master processor wants to transmit a block of data to one of the slaves, it must first send out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte, which ensures that they will be interrupted only by the reception of an address byte. The Automatic address recognition feature further ensures that only the address matching slave will be interrupted. The address comparison is done by hardware not software.

After being interrupted, the address matching slave clears the SM2 bit to receive data bytes. The un-addressed slaves will be unaffected, they will be still waiting for their address. Once the entire message is received, the addressed slave should set its SM2 bit to ignore all not address byte in transmission until it receives the next address byte.

The Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given Address. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address (SADDR) and the address shield (SADEN). The slave address is an 8-bit byte stored in the SADDR register. The SADEN register is actually used to define whether the byte value in SADDR is valid or not. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is i. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR. Use of the Given Address allows multiple slaves to be recognized while excluding others.

	Slave 1	Slave 2
SADDR	10100100	10100111
SADEN (bit = 0 will be ignored)	11111010	11111001
Given Address	10100x0x	10100xx1
Broadcast Address (SADDR or SADEN)	1111111x	11111111

The given address for slave 1 and 2 differs in the LSB. For slave 1, it is ignore LSB, while for slave 2 LSB is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (10100000). Similarly the bit 1 is 0 for slave 1 and ignores the bit 1 for slave 2. Hence to communicate only with slave 2, the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 2 position is ignored for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN. The zeros in the result are defined as neglect. In most cases, the Broadcast Address is FFh, this address will be responded by all slaves.

On reset, the SADDR and SADEN are initialized to 00h. The two results set Given Address and Broadcast Address to XXXXXXXX (all bits are ignored). This effectively removes the multiprocessor communications feature, since any selectivity is disabled. This ensures that the EUART will reply to any address, which it is compatible with the 80C51 microcontrollers that do not support automatic address recognition. So the user may implement multiprocessor communication by software recognition address according to the above mentioned method.

Frame Error Detection

Frame error detection is available when the SSTAT bit in register PCON is set to logic 1.All the 3 error falg bits should be cleared by software after they are set, even when the following frames received without any error will not be cleared automatically.

Note: *The SSTAT bit must be logic 1 to access any of the status bits (FE, RXOV, and TXCOL). The SSTAT bit must be logic 0 to access the Mode Select bits (SM0, SM1, and SM2).*

Transmit Collision

The Transmit Collision bit (TXCOL bit in register SCON) set ‘1’ when a transmission is still in progress and user software writes data to the SBUF register. If collision occurs, the new data will be ignored and the transmit buffer will not be written.

Receive Overflow

The Receive Overflow bit (RXOV in register SCON) set ‘1’ if a new data byte is latched into the receive buffer before software has read the previous byte. The previous data is lost when this happen.

Frame Error

The Frame Error bit (FE in register SCON) set ‘1’ if an invalid (low) STOP bit is detected.

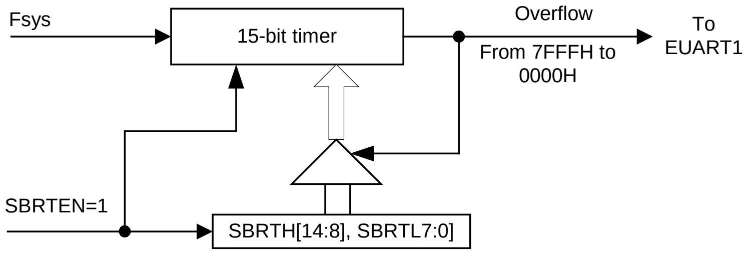
Break Detection

A break is detected when any 11 consecutive bits are detected as low. Since a break condition also satisfies the requirements for a framing error, a break condition will also result in reporting a framing error. Once a break condition has been detected, the UART will go into an idle state and remain in this idle state until a valid stop bit (rising edge on RxD pin) has been received.

8.5.3 EUART1

The control and operate mode of EUART1 is similar to EUART0, the different is EUART1 has a baud rate generator is an 15-bit up-counting timer.

Otherwise, the baud rate generator of EURART1 has baud rate fine adjustment function by set BFINE register.



Baudrate Generator for EUART

$$\text{SBRToverflowrate} = \frac{\text{Fsys}}{32768 - \text{SBRT}}, \quad SBRT = [SBRTH, SBRTL]$$

So that, the baud rate computational formula of EUART1 in different modes as shown below.

Mode0:

In Mode0, the baud rate is programmable to either 1/12 or 1/4 of the system frequency. This baud rate is determined by SM2 bit. When set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock.

Mode1 and Mode3:

In Mode1 & Mode3, the baud rate can be fine adjusted.

The Mode1 & 3 baud rate equations are shown below,

$$BaudRate = \frac{Fsys}{16 \times (32768 - SBRT) + BFINE}$$

For example: Fsys = 8MHz, to get 115200Hz baud rate, computing method of SBRT and SFINE as shown below:

8000000/16/115200 = 4.34

SBRT = 32768 - 4 = 32764

115200 = 8000000/(16 X 4 + BFINE)

BFINE = 5.4 ≈ 5

This fine tuning method to calculate the actual baud rate is 115942Hz and the error is 0.64%, but the error is 8.5% In the past computing method.

Mode2:

In Mode2, the baud rate is programmable to either 1/32 or 1/64 of the system clock. This baud rate is determined by the SMOD bit (PCON.7). When this bit is set to 0, the serial port runs at 1/64 of the clock. When set to 1, the serial port runs at 1/32 of the clock.

$$BaudRate = 2^{SMOD} \times (\frac{F_{SYS}}{64})$$

***Note:** TF3 cleared by hardware, and the interrupt vector address is as the same as Uart1. Please pay attention to the interrupt flag, when use both Timer3 and Uart1.*

8.5.4 Register

Table 8.24 EUART0 Control & Status Register

98H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON	SM0 /FE	SM1 /RXOV	SM2 /TXCOL	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-6	**SM[0:1]**	**EUART0 Serial mode control bit, when SSTAT = 0** 00: mode 0, Synchronous Mode, fixed baud rate 01: mode 1, 8 bit Asynchronous Mode, variable baud rate 10: mode 2, 9 bit Asynchronous Mode, fixed baud rate 11: mode 3, 9 bit Asynchronous Mode, variable baud rate
7	**FE**	**EUART0 Frame Error flag, when FE bit is read, SSTAT bit must be set 1** 0: No Frame Error, clear by software 1: Frame error occurs, set by hardware
6	**RXOV**	**EUART0 Receive Over flag, when RXOV bit is read, SSTAT bit must be set 1** 0: No Receive Over, clear by software 1: Receive over occurs, set by hardware
5	**SM2**	**EUART0 Multi-processor communication enable bit (9th bit '1' checker), when SSTAT = 0** 0: In Mode0, baud-rate is 1/12 of system clock In Mode1, disable stop bit validation check, any stop bit will set RI to generate interrupt In Mode2 & 3, any byte will set RI to generate interrupt 1: In Mode0, baud-rate is 1/4 of system clock In Mode1, Enable stop bit validation check, only valid stop bit (1) will set RI to generate interrupt In Mode2 & 3, only address byte (9th bit = 1) will set RI to generate interrupt
5	**TXCOL**	**EUART0 Transmit Collision flag, when TXCOL bit is read, SSTAT bit must be set 1** 0: No Transmit Collision, clear by software 1: Transmit Collision occurs, set by hardware
4	**REN**	**EUART0 Receiver enable bit** 0: Receive Disable 1: Receive Enable
3	**TB8**	**The 9th bit to be transmitted in Mode2 & 3 of EUART0, set or clear by software**
2	**RB8**	**The 9th bit to be received in Mode1, 2 & 3 of EUART0** In Mode0, RB8 is not used In Mode1, if receive interrupt occurs, RB8 is the stop bit that was received In Modes2 & 3 it is the 9th bit that was received
1	**TI**	**Transmit interrupt flag of EUART0** 0: cleared by software 1: Set by hardware at the end of the 8th bit time in Mode0, or at the beginning of the stop bit in other modes
0	**RI**	**Receive interrupt flag of EUART0** 0: cleared by software0 1: Set by hardware at the end of the 8th bit time in Mode0, or during the stop bit time in other modes

Table 8.25 EUART0 Data Buffer Register

99H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBUF	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**SBUF[7:0]**	This SFR accesses two registers; a transmit shift register and a receive latch register A write of SBUF will send the byte to the transmit shift register and then initiate a transmission A read of SBUF returns the contents of the receive latch

Table 8.26 Power Control Register

87H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD	SSTAT	SSTAT1	-	GF1	GF0	PD	IDL
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**SMOD**	**Baud rate doubler** Set SMOD in Mode1 & 3, the baud-rate of EUART0is doubled if using time4 as baud-rate generator**(Fit EUART0)** set SMOD in Mode2, the baud-rate of EUART is doubled **(Both fit EUART0 and EUART0)**
6	**SSTAT**	**SCON[7:5] function select bit** 0: SCON[7:5] operates as SM0, SM1, SM2 1: SCON[7:5] operates as FE, RXOV, TXCOL
5	**SSTAT1**	**SCON1[7:5] function select bit** 0: SCON1[7:5] operates as SM10, SM11, SM12 1: SCON1[7:5] operates as FE1, RXOV1, TXCOL1
3-0	**-**	**Other: See "Power Management" chapter**

Table 8.27 EUART0 Slave Address & Address Mask Register

9AH-9BH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SADDR	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
SADEN	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**SADDR[7:0]**	**SFR SADDR defines the EUART0's slave address**
7-0	**SADEN[7:0]**	**SFR SADEN is a bit mask to determine which bits of SADDR are checked against a received address** 0: Corresponding bit in SADDR is a "don't care" 1: Corresponding bit in SADDR is checked against a received address

Table 8.28 EUART1 Control & Status Register

98H, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON1	SM10 /FE1	SM11 /RXOV1	SM12 /TXCOL1	REN1	TB18	RB18	TI1	RI1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-6	**SM1[0:1]**	**EUART1 Serial mode control bit, when SSTAT1 = 0** 00: mode 0, Synchronous Mode, fixed baud rate 01: mode 1, 8 bit Asynchronous Mode, variable baud rate 10: mode 2, 9 bit Asynchronous Mode, fixed baud rate 11: mode 3, 9 bit Asynchronous Mode, variable baud rate
7	**FE1**	**EUART1 Frame Error flag, when FE bit is read, SSTAT1 bit must be set 1** 0: No Frame Error, clear by software 1: Frame error occurs, set by hardware
6	**RXOV1**	**EUART1 Receive Over flag, when RXOV bit is read, SSTAT1 bit must be set 1** 0: No Receive Over, clear by software 1: Receive over occurs, set by hardware
5	**SM12**	**EUART0 Multi-processor communication enable bit (9th bit '1' checker), when SSTAT = 1** 0: In Mode0, baud-rate is 1/12 of system clock In Mode1, disable stop bit validation check, any stop bit will set RI to generate interrupt In Mode2 & 3, any byte will set RI to generate interrupt 1: In Mode0, baud-rate is 1/4 of system clock In Mode1, Enable stop bit validation check, only valid stop bit (1) will set RI to generate interrupt In Mode2 & 3, only address byte (9th bit = 1) will set RI to generate interrupt
5	**TXCOL1**	**EUART1 Transmit Collision flag, when TXCOL1 bit is read, SSTAT1 bit must be set 1** 0: No Transmit Collision, clear by software 1: Transmit Collision occurs, set by hardware
4	**REN1**	**EUART1 Receiver enable bit** 0: Receive Disable 1: Receive Enable
3	**TB18**	**The 9th bit to be transmitted in Mode2 & 3 of EUART1, set or clear by software**
2	**RB18**	**The 9th bit to be received in Mode1, 2 & 3 of EUART1** In Mode0, RB8 is not used In Mode1, if receive interrupt occurs, RB8 is the stop bit that was received In Modes2 & 3 it is the 9th bit that was received
1	**TI1**	**Transmit interrupt flag of EUART1** 0: cleared by software 1: Set by hardware at the end of the 8th bit time in Mode0, or at the beginning of the stop bit in other modes
0	**RI1**	**Receive interrupt flag of EUART1** 0: cleared by software0 1: Set by hardware at the end of the 8th bit time in Mode0, or during the stop bit time in other modes

Table 8.29 EUART1 Data Buffer Register

99H, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBUF1	SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**SBUF1[7:0]**	This SFR accesses two registers; a transmit shift register and a receive latch register A write of SBU1F will send the byte to the transmit shift register and then initiate a transmission A read of SBUF1 returns the contents of the receive latch

Table 8.30 EUART1 Slave Address & Address Mask Register

9AH-9BH, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SADDR1	SADDR1.7	SADDR1.6	SADDR1.5	SADDR1.4	SADDR1.3	SADDR1.2	SADDR1.1	SADDR1.0
SADEN1	SADEN1.7	SADEN1.6	SADEN1.5	SADEN1.4	SADEN1.3	SADEN1.2	SADEN1.1	SADEN1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**SADDR1[7:0]**	**SFR SADDR defines the EUART1's slave address**
7-0	**SADEN1[7:0]**	**SFR SADEN1 is a bit mask to determine which bits of SADDR1 are checked against a received address** 0: Corresponding bit in SADDR1 is a "don't care" 1: Corresponding bit in SADDR1 is checked against a received address

Table 8.31 EUART1 Baud rate generator register

9DH-9CH, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBRTH	SBRTEN	SBRT.14	SBRT.13	SBRT.12	SBRT.11	SBRT.10	SBRT.9	SBRT.8
SBRTL	SBRT.7	SBRT.6	SBRT.5	SBRT.4	SBRT.3	SBRT.2	SBRT.1	SBRT.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**SBRTEN**	**EUART1 Baud rate enable control bit** 0: disable (default) 1: enable
6-0, 7-0	**SBRT[14:0]**	**EUART1 Baud rate bits**

Table 8.32 EUART1 Baud rate generator fine-tune register

9EH, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BFINE	BFINE.7	BFINE.6	BFINE.5	BFINE.4	-	-	-	-
R/W	R/W	R/W	R/W	R/W	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	-	-	-	-

Bit Number	Bit Mnemonic	Description
7-4	**BFINE[7:4]**	**EUART0 Baud rate generator fine-tune register**

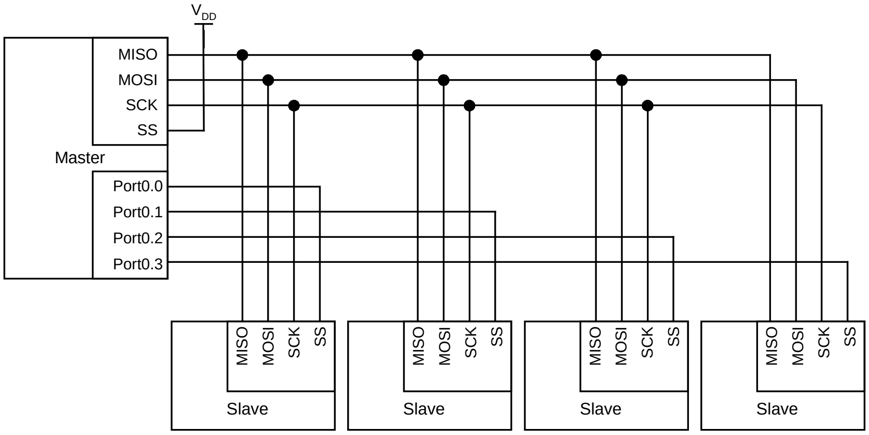
8.6 Serial Peripheral Interface (SPI)

8.6.1 Features

- Full-duplex, three-wire synchronous transfers
- Master or slave operation
- Six programmable master clock rates
- Serial clock with programmable polarity and phase
- Master mode fault error flag with MCU interrupt capability
- Write collision flag protection
- Selectable LSB or MSB transfer

The Serial Peripheral Interface (SPI) Module allows full-duplex, synchronous, serial communication between the MCU and peripheral devices, including other MCUs.

The following diagram shows a typical SPI bus configuration using one master controller and many slave peripherals. The bus is made of three wires connecting all the devices. The master device selects the individual slave devices by using four pins of a parallel port to control the four SS pins of the Slave devices.



8.6.2 Signal Description

(1) Master Output Slave Input (MOSI)

This 1-bit signal is directly connected between the master device and slave devices. The MOSI line is used to transfer data in series from the master to the slave. Therefore, it is an output signal from the master, and an input signal to a slave.

(2) Master Input Slave Output (MISO)

This 1-bit signal is directly connected between the slave devices and master device. The MISO line is used to transfer data in series from the slave to the master. Therefore, it is an output signal from the slave, and an input signal to the master. The MISO pin is placed in a high-impedance state when the SPI operates as a slave that is not selected ($\overline{SS}$ high).

A static high level on the $\overline{SS}$ pin puts the MISO line of a slave in a high-impedance state.

(3) SPI Serial Clock (SCK)

This signal is used to synchronize the data movement both in and out of the devices through their MOSI and MISO lines. It is driven by the master for eight clock cycles, which allows exchanging one byte on the serial lines. The SCK signal is ignored by a SPI slave when the slave is not selected ($\overline{SS}$ high).

(4) Slave Select ($\overline{SS}$)

Each slave peripheral is selected by one slave select pin ($\overline{SS}$). This signal must stay low for any active slave. It is obvious that only one master ($\overline{SS}$ high) can drive the network. The master may select each slave device by software through port pins. To prevent bus conflicts on the MISO line, only one slave should be selected at a time by the master for a transmission.

In a master configuration, the $\overline{SS}$ line can be used in conjunction with the MODF flag in the SPI status register to prevent multiple masters from driving MOSI and SCK.

The $\overline{SS}$ pin could be used as a general IO if the following conditions are met:

(a) The device is configured as a master and the SSDIS control bit in SPCON is set. This kind of configuration can happen when only one master is driving the network. Therefore, the MODF flag in the SPSTA will never be set.

(b) The device is configured as a slave with CPHA and SSDIS control bits set. This kind of configuration can happen when the network comprises only one master and one slave only. Therefore, the device should always be selected and the master will never use the slave's $\overline{SS}$ pin to select the target communication slave.

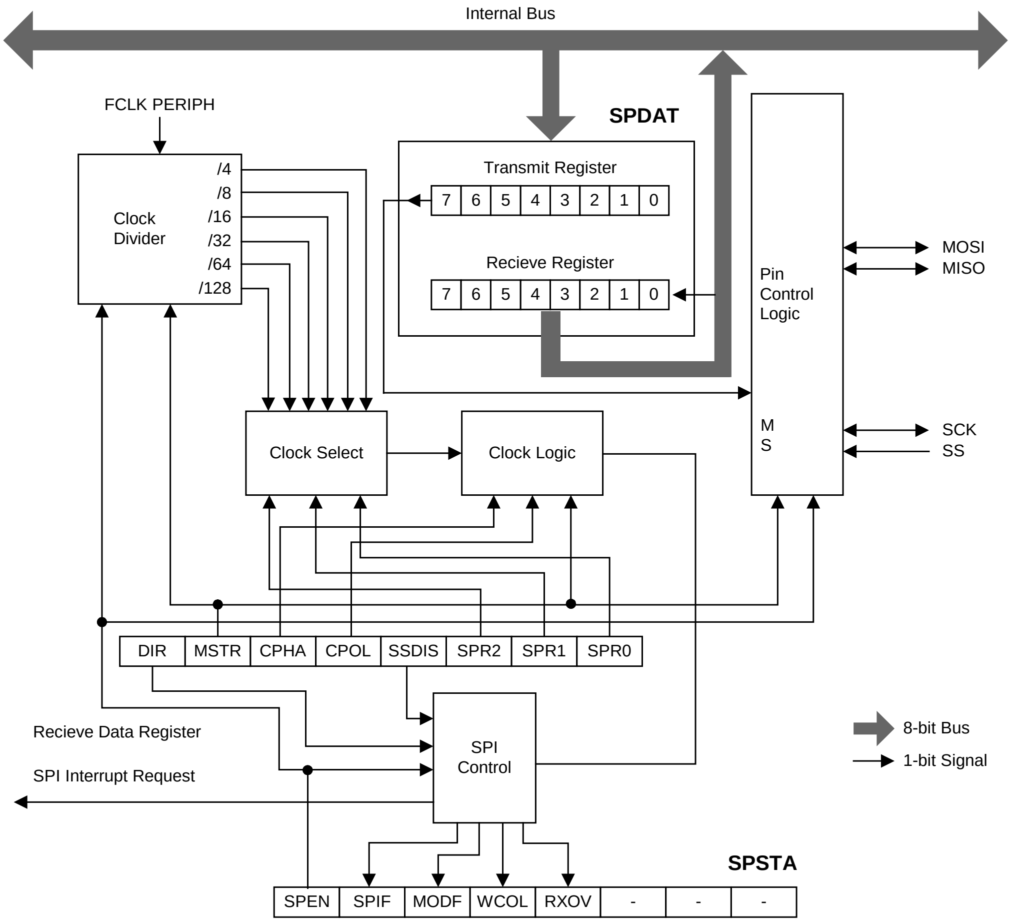
***Note:** When CPHA = '0', a falling edge of $\overline{SS}$ pin is used to start the transmission.*

8.6.3 Baud Rate

In master mode, the baud rate is chosen from one of the six clock rates by the division of the internal clock by 4, 8, 16, 32, 64 or 128 set by the three bits SPR[2:0] in the SPCON register.

8.6.4 Functional Description

The following diagram shows a detailed structure of the SPI module.



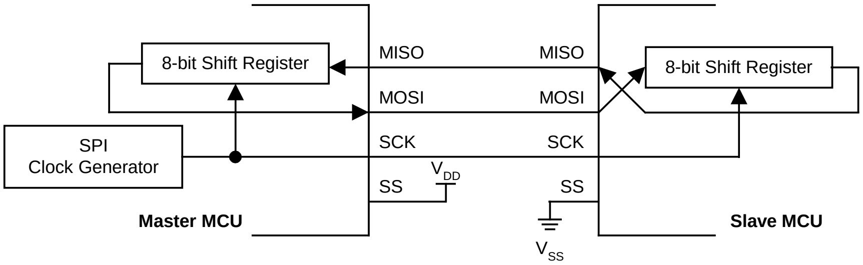
SPI Module Block Diagram

8.6.5 Operating Modes

The Serial Peripheral Interface can be configured as one of the two modes, master mode or slave mode. The configuration and initialization of the SPI module is made through SPCON (the serial peripheral control register) and SPSTA (the serial peripheral status register). Once the SPI is configured, the data exchange is made using SPCON, SPSTA and SPDAT (the serial peripheral data register).

During an SPI transmission, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (SCK) synchronizes shifting and sampling on the two serial data lines (MOSI and MISO). A slave select line ($\overline{SS}$) allows individual selection of a SPI slave; SPI slaves that are not selected do not interfere with SPI bus activities.

When the SPI master transmits data to the SPI slave via the MOSI line, the SPI slave responds by sending data to the SPI master via the MISO line. This implies full-duplex transmission with both data out and data in synchronized with the same clock. Both transmit shift register and receive shift register uses the same SFR Address, a write operation to SPDAT will write to the transmit shift register, and a read operation from SPDAT will retrieve the data in receive shift register.



Full-Duplex Master-Slave Interconnection Diagram

Master Mode

(1) Enable

A SPI master device initiates all data transfers on a SPI bus. The SPI operates in master mode when the MSTR is set in SPCON register. Only one master can initiate transmission.

(2) Transmit

When in SPI master mode, writing a byte of data to the SPI data register (SPDAT) will write to the transmit shift buffer. If the transmit shift register already contains data, the SPI master will generate a WCOL signal to indicate writing too fast. But the data in transmit shift register will not be affected, and the transmission continues uninterrupted. Else if the transmit shift register is empty, the SPI master will immediately shifts out the data serially on the MOSI line while providing the serial clock on SCK. The SPIF flag in SPSTA register is set to logic ‘1’ at the end of the transfer. If interrupts are enabled, an interrupt request is generated when the SPIF flag is set.

(3) Receive

While the master transfers data to a slave on the MOSI line, the addressed slave simultaneously transfers the contents of its transmit shift register to the master’s receive shift register on the MISO line in a full-duplex operation. Therefore, the SPIF flag serves as both a transmit-complete and receive-data-ready flag. The data byte received from the slave is transferred MSB-first or LSB-first into the master's shift register. When a byte is fully shifted into the register, it is moved to the receive buffer where it can be read by the processor by reading SPDAT. If an overrun occurs, RXOV signal will be set to indicate data over-run occurs, and the receive shift register keep the byte that SPIF was lastly set, also the SPI master will not receive any further data until SPIF was cleared.

Slave Mode

(1) Enable

The SPI operates in slave mode when the MSTR is cleared in the SPCON register. Before a data transmission occurs, the slave select ($\overline{SS}$) pin of the Slave device must be set to ’0’. The $\overline{SS}$ pin must remain low until the 1-byte transmission is complete.

(2) Transmit & Receive

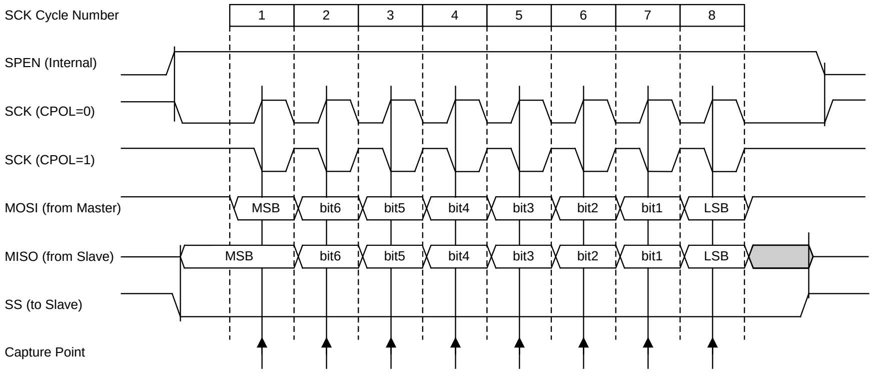
When in SPI slave mode, bytes are shifted in through the MOSI pin and out through the MISO pin by a master device controlling the SCK signal. A bit counter counts SCK edges. When 8 bits have been shifted in the receive shift register and another 8 bits have been shifted out the transmit shift register, the SPIF flag is set to logic ‘1’. Data is read from the receive shift register by reading SPDAT. If interrupts are enabled, an interrupt request is generated when the SPIF flag is set.

To prevent an overflow condition, the SPI slave software must clear the SPIF bit in SPSTA register before another byte enters the receive shift register. Else a RXOV signal will be set to indicate data over-run occurs, and the receive shift register keep the byte that SPIF was lastly set, also the SPI slave will not receive any further data until SPIF was cleared.

A SPI slave cannot initiate transfers. Data to be transferred to the master device is pre-loaded into the shift register by writing to SPDAT. Writes to SPDAT are placed in the transmit buffer first. So a SPI slave must complete the write to the SPDAT (transmit shift register) in one SPI clock before the master starts a new transmission. If the write to SPDAT is late in the first transmission, the SPI slave will transmit a ‘0x00’ byte in the following transmission. if the write operation occurs during this time, a WCOL signal will be set. If the transmit shift register already contains data, the SPI slave will generate a WCOL signal to indicate writing too fast. But the data in transmit shift register will not be affected, and the transmission continues uninterrupted.

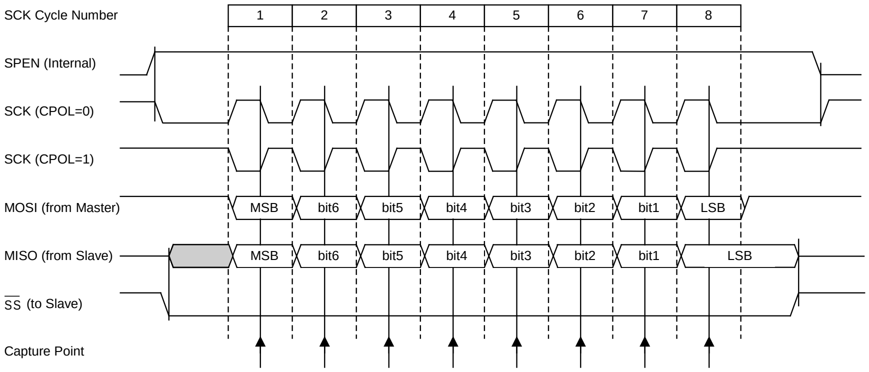
8.6.6 Transmission Formats

Software can select any of four combinations of serial clock (SCK) phase and polarity using two bits in the SPCON, the clock polarity CPOL and the clock phase CPHA. CPOL defines the default SCK line level in idle state. It has no significant effect on the transmission format. CPHA defines the edges on which the input data are sampled and the edges on which the output data are shifted. The clock phase and polarity should be identical for the master and the communicating slave.



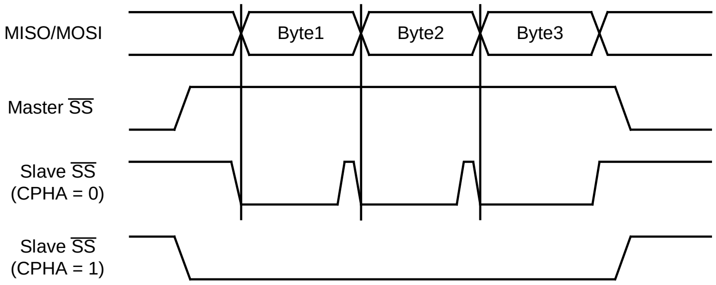
Data Transmission Format (CPHA = 0)

If CPHA = 0, the first SCK edge is the capture strobe. Therefore the slave must begin driving its data before the first SCK edge, and a falling edge on the $\overline{\text{SS}}$ pin is used to start the transmission. The $\overline{\text{SS}}$ pin must be toggled high and then low between each byte transmitted. So SSDIS bit is invalid when CPHA = 0.



Data Transmission Format (CPHA = 1)

If CPHA = 1, the master begins driving its MOSI pin on the first SCK edge. Therefore the slave uses the first SCK edge as a start transmission signal. So the user must put the SPDAT before the second edge of the first SCK. The $\overline{\text{SS}}$ pin can remain low between transmissions. This format may be preferred in systems with only one master and only one slave.



CPHA/$\overline{\text{SS}}$ Timing

***Note:** Before SPI is configured as Slave mode and CPOL bit in SPCON is cleared, the P2.4SCK pin must be set to input mode and enable pull-high resistor before SPEN bit in SPSTA is set to logic ‘1’.*

8.6.7 Error Conditions

The following flags in the SPSTA signal SPI error conditions:

(1) Mode Fault (MODF)

Mode fault error in master mode SPI indicates that the level on the $\overline{SS}$ pin is inconsistent with the actual mode of the device. MODF is set to warn that there may be a multi-master conflict for system control. In this case, the SPI system is affected in the following ways:

- An SPI receiver/error CPU interrupt request is generated;
- The SPEN bit in SPSTA is cleared. This disables the SPI;
- The MSTR bit in SPCON is cleared.

When $\overline{SS}$ Disable (SSDIS bit in the SPCON register) is cleared, the MODF flag is set when the $\overline{SS}$ signal becomes '0'. However, as stated before, for a system with one Master, if the $\overline{SS}$ pin of the master device is pulled low, there is no way that another master attempts to drive the network. In this case, to prevent the MODF flag from being set, software can set the SSDIS bit in the SPCON register and therefore making the $\overline{SS}$ pin as a general-purpose I/O pin.

The user must clear the MODF bit by software, and enable SPEN in SPCON register again for further communication, and enable MSTR bit to continue master mode.

(2) Write Collision (WCOL)

A write collision (WCOL) flag in the SPSTA is set when a write to the SPDAT register is done during a transmit sequence. WCOL does not cause an interruption, and the transfer continues uninterrupted. The WCOL bit is cleared by software.

(3) Overrun Condition (RXOV)

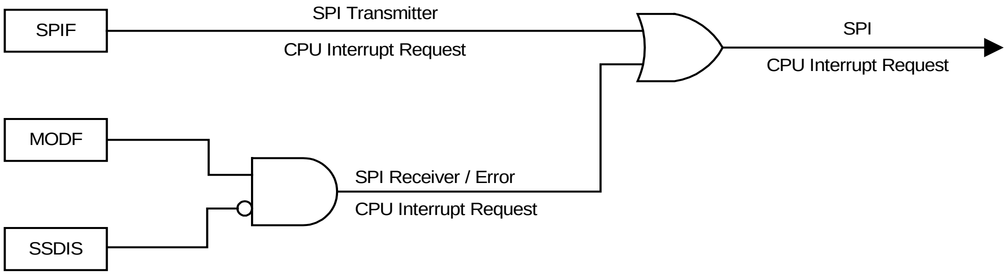
An overrun condition occurs when the master or slave tries to send several data bytes and the slave or master has not cleared the SPIF bit issuing from the previous data byte transmitted. In this case, the receive shift register keep the byte that SPIF was lastly set, also the SPI device will not receive any further data until SPIF was cleared. The SPIF still keep on invoke interrupt before it is cleared, though the transmission can still be driven by SCK. RXOV does not generate an interruption, the RXOV bit is cleared by software.

8.6.8 Interrupts

Two SPI status flags can generate a CPU interrupt requests SPIF & MODF.

Serial Peripheral data transfer flag: SPIF. This bit is set by hardware when a transfer has been completed.

Mode Fault flag: MODF. This bit becomes set to indicate that the level on the $\overline{SS}$ pin is inconsistent with the mode of the SPI. MODF with SSDIS reset will generate receiver/error CPU interrupt requests. When SSDIS is set, no MODF interrupt request is generated.



SPI Interrupt Requests Generation

8.6.9 Registers

Table 8.33 Serial Peripheral Control Register

A2H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPCON	DIR	MSTR	CPHA	CPOL	SSDIS	SPR2	SPR1	SPR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**DIR**	**Transfer Direction Selection** 0: MSB first 1: LSB first
6	**MSTR**	**Serial Peripheral Master** 0: Configure the SPI as a Slave 1: Configure the SPI as a Master
5	**CPHA**	**Clock Phase** 0: Data sampled on first edge of SCK period 1: Data sampled on second edge of SCK period
4	**CPOL**	**Clock Polarity** 0: SCK line low in idle state 1: SCK line high in idle state
3	**SSDIS**	**$\overline{\text{SS}}$ Disable** 0: Enable $\overline{\text{SS}}$ pin in both Master and Slave modes 1: Disable $\overline{\text{SS}}$ pin in both master and slave modes MODF interrupt request will not generate, if SSDIS is set. In Slave mode, this bit has no effect if CPHA = 0.
2-0	**SPR[2:0]**	**Serial Peripheral Clock Rate** 000: $f_{SYS}/4$ 001: $f_{SYS}/8$ 010: $f_{SYS}/16$ 011: $f_{SYS}/32$ 100: $f_{SYS}/64$ Others: $f_{SYS}/128$

Table 8.34 Serial Peripheral Status Register

F8H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPSTA	SPEN	SPIF	MODF	WCOL	RXOV	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	-	-	-
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	-	-	-

Bit Number	Bit Mnemonic	Description
7	**SPEN**	**SPI Enable** 0: Disable the SPI interface 1: Enable the SPI interface
6	**SPIF**	**Serial Peripheral data transfer flag** 0: Clear by software 1: Set by hardware to indicate that the data transfer has been completed
5	**MODF**	**Mode Fault** 0: Cleared by software 1: Set by hardware to indicate that the $\overline{SS}$ pin is at inappropriate logic level
4	**WCOL**	**Write Collision flag** 0: Cleared by software to indicate write collision has be processed 1: Set by hardware to indicate that a collision has been detected
3	**RXOV**	**Receive Overrun** 0: Cleared by software to indicate receive overrun has be processed 1: Set by hardware to indicate that a receive overrun has been detected

Table 8.35 Serial Peripheral Data Register

A3H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPDAT	SPDAT7	SPDAT6	SPDAT5	SPDAT4	SPDAT3	SPDAT2	SPDAT1	SPDAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**SPDAT[7:0]**	A write to SPDAT places data directly into the transfer shift register. A Read of the SPDAT returns the value located in the receive shift register.

Note: *When SPI is disabled, the data of SPDAT is invalid.*

8.7 Analog Digital Converter (ADC)

8.7.1 Feature

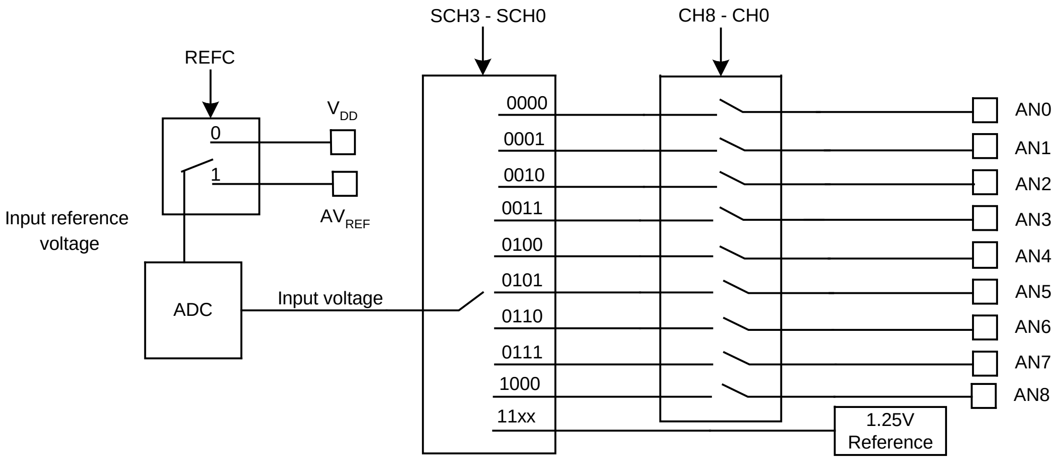
- 12-bit Resolution
- Build in V_{REF}
- Selectable external or built-in V_{REF}
- 9 analog Channels input

The SH79F3283 includes a single ended, 12-bit SAR Analog to Digital Converter (ADC) with build in reference voltage connected to the V_{DD}, users also can select the AVREF port input reference voltage. The 10 ADC channels are shared with 1 ADC module; each channel can be programmed to connect with the analog input individually. Only one channel can be available at one time. GO/$\overline{\text{DONE}}$ signal is available to start convert, and indicate end of convert. When conversion is completed, the data in AD convert data register will be updated and ADCIF bit in ADCON register will be set. If ADC Interrupt is enabled, the ADC interrupt will be generated.

The ADC integrates a digital compare function to compare the value of analog input and the digital value in the AD converter. If this function is enabled (set EC bit in ADCON register) and ADC module is enabled (set ADON bit in ADCON register). When the corresponding digital value of analog input is larger than the compare value in register (ADDH/L), the ADC interrupt will occur, otherwise no interrupt will be generated. The digital comparator can work continuously when GO/$\overline{\text{DONE}}$ bit is set until software clear, which behaviors different with the AD converter operation mode.

The ADC module including digital compare module can wok in Idle mode and the ADC interrupt will wake up the Idle mode, but is disabled in Power-Down mode.

8.7.2 ADC Diagram



ADC Diagram

8.7.3 Register

Table 8.36 ADC Control Register

93H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	ADON	ADCIF	EC	REFC	SCH2	SCH1	SCH0	GO/$\overline{\text{DONE}}$
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**ADON**	**ADC Enable bit** 0: Disable the ADC module 1: Enable the ADC module
6	**ADCIF**	**ADC Interrupt Flag bit** 0: No ADC interrupt, cleared by software. 1: Set by hardware to indicate that the AD Convert has been completed, or analog input is larger than ADDATH/L if compare is enabled
5	**EC**	**Compare Function Enable bit** 0: Compare function disabled 1: Compare function enabled
4	**REFC**	**Reference Voltage Select bit** 0: the reference voltage connected to V_{DD} 1: the reference voltage input from V_{REF} pin
3-1	**SCH[2:0]**	**ADC channel Select bits (Combination control with SCH3)** 0000: ADC channel AN0 0001: ADC channel AN1 0010: ADC channel AN2 0011: ADC channel AN3 0100: ADC channel AN4 0101: ADC channel AN5 0110: ADC channel AN6 0111: ADC channel AN7 1000: ADC channel AN8 11xx: internal 1.25V Reference
0	**GO/$\overline{\text{DONE}}$**	**ADC status flag bit** 0: Automatically cleared by hardware when AD convert is completed. Clearing this bit during converting time will stop current conversion. If Compare function is enabled, this bit will not be cleared by hardware until software clear. 1: Set to start AD convert or digital compare.

Note:

(1) When select the reference voltage input from V_{REF} pin (REFC = 1), the P4.4 is shared as V_{REF} input.

(2) After set ADON to 1, please set a 10us delay, then set GO/DONE to 1 to ensure the ADC normal operate.

Table 8.37 ADC Control Register 1

92H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON1	-	-	-	-	-	RESO	CH8	SCH3
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	0	0	0

Bit Number	Bit Mnemonic	Description
2	**RESO**	**ADC Resolution select bit** 0: Resolution is 12bit, ADDH is the high byte, ADDL[3:0] is the low 4 bit 1: Resolution is 10bit, ADDH is the high byte, ADDL[1:0] is the low 2 bit
1	**CH8**	**Channel Configuration bits** 0: P4.4 is I/O port 1: P4.4 is ADC input port ***Note:*** *If REFC = 1, P4.4 is AVREF input pin, this bit is invalid.*
0	**SCH3**	**ADC channel Select bits (Combination control with SCH[2:0])** 1000: ADC channel AN8 11xx: internal 1.25V Reference ***Note:*** *set up time < 12us*

Table 8.38 ADC Time Configuration Register

94H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADT	TADC2	TADC1	TADC0	CDIR	TS3	TS2	TS1	TS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-5	**TADC[2:0]**	**ADC Clock Period Select bits** 000: ADC Clock Period t_{AD} = 2 t_{SYS} 001: ADC Clock Period t_{AD} = 4 t_{SYS} 010: ADC Clock Period t_{AD} = 6 t_{SYS} 011: ADC Clock Period t_{AD} = 8 t_{SYS} 100: ADC Clock Period t_{AD} = 12 t_{SYS} 101: ADC Clock Period t_{AD} = 16 t_{SYS} 110: ADC Clock Period t_{AD} = 24 t_{SYS} 111: ADC Clock Period t_{AD} = 32 t_{SYS}
4	**CDIR**	**ADC compare polarity select bit(EC = 1)** 0: Analog input > ADDATH/L, set ADCIF to1 1: Analog input < ADDATH/L, set ADCIF to1
3-0	**TS[3:0]**	**Sample time select bits** 2 t_{AD} ≤ Sample time = (TS [3:0]+1) X t_{AD} ≤ 15 t_{AD}

Note:

(1) Make sure that $t_{AD} \geqq 1\mu s$;

(2) The minimum sample time is 2 t_{AD}, even TS[3:0] = 0000;

(3) The maximum sample time is 15 t_{AD}, even TS[3:0] = 1111;

(4) Evaluate the series resistance connected with ADC input pin before set TS[3:0];

(5) Be sure that the series resistance connected with ADC input pin is no more than 10kΩ when 2 t_{AD} sample time is selected;

(6) Total conversion time is: 12 t_{AD} + sample time.

For Example

System Clock (SYSCLK)	TADC[2:0]	t_{AD}	TS[3:0]	Sample Time	Conversion Time
32.768kHz	000	30.5 *2=61μs	0000	2*61=122μs	12*61+122=854μs
	000	30.5 *2=61μs	0111	8*61=488μs	12*61+488=1220μs
	000	30.5 *2=61μs	1111	15*61=915μs	12*61+915=1647μs
	111	30.5 *32=976μs	0000	2*976=1952μs	12*976+1952=13664μs
	111	30.5 *32=976μs	0111	8*976=7808μs	12*976+7808=19520μs
	111	30.5 *32=976μs	1111	15*976=14640μs	12*976+14640=26352μs
4MHz	000	0.25 *2=0.5μs	-	-	(t_{AD} < 1μs, Not recommended)
	001	0.25 *4=1μs	0000	2*1=2μs	12*1+2=14μs
	001	0.25 *4=1μs	0111	8*1=8μs	12*1+8=20μs
	001	0.25 *4=1μs	1111	15*1=15μs	12*1+15=27μs
	111	0.25 *32=8μs	0000	2*8=16μs	12*8+16=112μs
	111	0.25 *32=8μs	0111	8*8=64μs	12*8+64=160μs
	111	0.25 *32=8μs	1111	15*8=120μs	12*8+120=216μs
12MHz	000	0.083*2=0.166μs	-	-	(t_{AD} < 1μs, Not recommended)
	100	0.083*12=1μs	0000	2*1=2μs	12*1+2=14μs
	100	0.083*12=1μs	0111	8*1=8μs	12*1+8=20μs
	100	0.083*12=1μs	1111	15*1=15μs	12*1+15=27μs
	111	0.083*32=2.7μs	0000	2*2.7=5.4μs	12*2.7+5.4=37.8μs
	111	0.083*32=2.7μs	0111	8*2.7=21.6μs	12*2.7+21.6=54μs
	111	0.083*32=2.7μs	1111	15*2.7=40.5μs	12*2.7+40.5=72.9μs

Table 8.39 ADC Channel Configure Register

95H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCH	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**CH[7:0]**	**Channel Configuration bits** 0: P4.0-P4.3, P3.4-P3.7 are I/O port 1: P4.0-P4.3, P3.4-P3.7 are ADC input port

Table 8.40 AD Converter Data Register (Compare Value Register)

96H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADDL	-	-	-	-	A3	A2	A1	A0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0
97H, Bank0	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
ADDH	A11	A10	A9	A8	A7	A6	A5	A4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0 **7-0**	**A11-A0**	**ADC Data register** Digital Value of sampled analog voltage, updated when conversion is completed If ADC Compare function is enabled (EC = 1), this is the value to be compared with the analog input ***Note:*** *RESO = 0, Resolution is 12 bit, [A11:A4] is the high 8 bit, [A3:A0] is the low 4 bit.* *RESO = 1, Resolution is 12 bit, [A11:A4] is the high 8 bit, [A1:A0] is the low 2 biit*

The Approach for AD Conversion:

(1) Select the analog input channels and reference voltage.

(2) Enable the ADC module with the selected analog channel.

(3) Delay 10us

(4) Set GO/$\overline{\text{DONE}}$ = 1 to start the AD conversion.

(5) Wait until GO/$\overline{\text{DONE}}$ = 0 or ADCIF = 1, if the ADC interrupt is enabled, the ADC interrupt will occur, user need clear ADCIF by software.

(6) Acquire the converted data from ADDH/ADDL.

(7) Repeat step 3-5 if another conversion is required.

The Approach for Digital Compare Function:

(1) Select the analog input channels and reference voltage.

(2) Write ADDH/ADDL to set the compare value.

(3) Delay 10us

(4) Set EC = 1 to enable compare function.

(5) Enable the ADC module with the selected analog channel.

(6) Set GO/$\overline{\text{DONE}}$ = 1 to start the compare function.

(7) If the analog input is lager than compare value set in ADDH/ADDL, the ADCIF will be set to 1. if the ADC interrupt is enabled, the ADC interrupt will occur,user need clear ADCIF by software.

(8) The compare function will continue work until the GO/$\overline{\text{DONE}}$ bit is cleared to 0.

8.8 Buzzer

8.8.1 Feature

- Output a signal (square wave) used for tones such as confirmation tone
- Selectable whether to output one of 8 output frequencies or to disable the output

8.8.2 Register

Table 8.41 Buzzer Output Control Register

BDH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BUZCON	-	-	-	-	BCA2	BCA1	BCA0	BZEN
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-1	**BCA[2:0]**	**Buzzer output carrier frequency control bits** 000: system clock/8192 001: system clock/4096 010: system clock/2048 011: system clock/1024 100: system clock/512 101: system clock/32 110: system clock/16 111: system clock/8
0	**BZEN**	**Enable buzzer output control bit** 0: P5.3 is I/O port 1: P5.3 is buzzer output port

8.9 Low Power Detect (LPD)

8.9.1 Feature

- Low power detect and generate interrupt
- LPD detect voltage is selectable
- LPD de-bounce timer T_{LPD} is about 30-60µs

The low power detect (LPD) is used to monitor the supply voltage and generate an internal flag if the voltage decrease below the specified value. It is used to inform CPU whether the power is shut off or the battery is used out, so the software may do some protection action before the voltage drop down to the minimal operation voltage.

The LPD interrupt can wake the power down mode up.

8.9.2 Register

Table 8.42 Low Power Detection Control Register

B3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPDCON	LPDEN	LPDF	LPDMD	LPDIF	LPDS3	LPDS2	LPDS1	LPDS0
R/W	R/W	R*	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**LPDEN**	**LPD Enable bit** 0: Disable lower power detection 1: Enable lower power detection
6	**LPDF**	**LPD status Flag bit** 0: No LPD happened, clear by hardware, 1: LPD happened, set by hardware
5	**LPDMD**	**LPD mode select bit** 0: When V_{DD} below LPD voltage, LPDF is set 1: When V_{DD} above LPD voltage, LPDF is set
4	**LPDIF**	**LPD interrupt flag bit** 0: No LPD happened, clear by software 1: LPD happened, set by hardware
3-0	**LPDS[3:0]**	**LPD Voltage Select bit** 0000: 2.40V 0001: 2.55V 0010: 2.70V 0011: 2.85V 0100: 3.00V 0101: 3.15V 0110: 3.30V 0111: 3.45V 1000: 3.60V 1001: 3.75V 1010: 3.90V 1011: 4.05V 1100: 4.20V 1101: 4.35V 1110: 4.50V 1111: 4.65V

8.10 Low Voltage Reset (LVR)

8.10.1 Feature

- Enabled by the code option and V_{LVR} is 4.1V, 3.7V, 2.8V or 2.1V
- LVR de-bounce timer T_{LVR} is 30-60µs
- When the power supply voltage is lower than the set voltage V_{LVR}, it will cause the internal reset

The LVR function is used to monitor the supply voltage and generate an internal reset in the device when the supply voltage below the specified value V_{LVR}. The LVR de-bounce timer T_{LVR} is about 30µs-60µs.

The LVR circuit has the following feature when the LVR function is enabled: (t means the time of the supply voltage below V_{LVR})

Generates a system reset when $V_{DD} \leq V_{LVR}$ and $t \geq T_{LVR}$;

Cancels the system reset when $V_{DD} > V_{LVR}$ or $V_{DD} < V_{LVR}$, but $t < T_{LVR}$.

The LVR function is enabled by the code option.

It is typically used in AC line or large capacity battery applications, where heavy loads may be switched on and cause the MCU supply-voltage temporarily falls below the minimum specified operating voltage.

Low voltage reset can be applied to this, protecting system generates valid reset in the below set voltages.

8.11 Watchdog Timer (WDT) and Reset State

8.11.1 Feature

- Auto detect Program Counter (PC) over range, and generate OVL Reset
- WDT runs even in the Power-Down mode
- Selectable different WDT overflow frequency

OVL Reset

To enhance the anti-noise ability, SH79F3283 built in Program Counter (PC) over range detect circuit, if program counter value is larger than flash Rom size, or detect operation code equal to A5H which is not exist in 8051 instruction set, a OVL reset will be generate to reset CPU, and set WDOF bit. So, to make use of this feature, you should fill unused flash Rom with A5H.

Watchdog Timer

The watchdog timer is a down counter, and its clock source is an independent built-in RC oscillator, so it always runs even in the Power-Down mode. The watchdog timer will generate a device reset when it overflows. It can be enabled or disabled by the code option.

The watchdog timer control bits (WDT.2-0) are used to select different overflow time. The watchdog timer overflow flag (WDOF) will be automatically set to “1” by hardware when overflow happens. To prevent overflow happen, by reading or writing the WDT register RSTSTAT, the watchdog timer should re-count before the overflow happens.

There are also some reset flags in this register as below:

8.11.2 Register

Table 8.43 Reset Control Register

B1H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR)	0	-	1	0	0	0	0	0
Reset Value (WDT)	1	-	u	u	u	0	0	0
Reset Value (LVR)	u	-	u	1	u	0	0	0
Reset Value (PIN)	u	-	u	u	1	0	0	0

Bit Number	Bit Mnemonic	Description
7	WDOF	**Watch Dog Timer Overflow or OVL Reset Flag** Set by hardware when WDT overflow or OVL reset happened, cleared by software or Power On Reset 0: Watch Dog not overflows or no OVL reset generated 1: Watch Dog overflow or OVL reset occurred
5	PORF	**Power On Reset Flag** Set only by Power On Reset, cleared only by software 0: No Power On Reset. 1: Power On Reset occurred.
4	LVRF	**Low Voltage Reset Flag** Set only by Low Voltage Reset, cleared by software or Power On Reset 0: No Low Voltage Reset occurs 1: Low Voltage Reset occurred
3	CLRF	**Pin Reset Flag** Set only by pin reset, cleared by software or Power On Reset 0: No Pin Reset occurs 1: Pin Reset occurred
2-0	WDT[2:0]	**WDT Overflow period control bit** 000: Overflow period minimal value= 4096 ms 001: Overflow period minimal value= 1024 ms 010: Overflow period minimal value = 256 ms 011: Overflow period minimal value = 128 ms 100: Overflow period minimal value = 64ms 101: Overflow period minimal value = 16ms 110: Overflow period minimal value = 4ms 111: Overflow period minimal value = 1ms ***Notes:*** *If WDT_OPT is enabled in application, you must clear WatchDog periodically, and the interval must be less than the minimum value listed above.*

8.12 CRC verification module

8.12.1 Feature

- Generate CRC check code of the Flash Rom Code, verify the Flash Rom Code whether changed or not
- CRC generator polynomial adopt the CRC-CCITT Standard: $X^{16}+X^{12}+X^{5}+1$, high bit first
- Two mode: High speed CRC mode and Normal CRC speed mode

To improve the system reliability, the SH79F3283 has one CRC verification module built-in, CRC check code can be used to generate real-time code, using the generation polynomial: $X^{16}+X^{12}+X^{5}+1$, which adopt the CRC-CCITT Standard. Users can use this check code compared with the theory value, whether the changes in Flash content monitoring. The last two byte can be stored in the ROM region of the CRC theoretical value (not involved in CRC check), or other location (such as class EEPROM region, sequence number area user identification code area, etc.)

Set CRCADR[3:0] bits can select the CRC check size, set CRC_GO bit to 1 to enable CRC module. After CRC check is done, CRC_GO will be cleared automatically by hardware, and set CRCIF to 1, if interrupt enable bit SCM_LPD_CRC and ECRC are both set to 1, the CRC interrupt will generated in CPU, and the interrupt flag CRCIF will be cleared by software.

Normal CRC mode: the time of CPU operating is not influenced by the CRC check operating, but the time of CRC check is long and uncontrollable.

High speed CRC mode: in order to improve the time of CRC check, there is a way which makes CPU into IDLE mode, the time of CRC check will be reduced, and CRC interrupt can wake up IDLE mode.

***Note:** In Power-Down mode, and CRC is operating, this can make the CRC check code incorrectness. So please make sure system not in the Power-Down mode before CRC is done.*

8.12.2 Register

Table 8.44 CRC Control Register

FDH, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CRCCON	CRC_GO	CRCIF	-	-	CRCADR3	CRCADR2	CRCADR1	CRCADR0
R/W	R/W		-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**CRC_GO**	**CRC GO_DONE Control bit** 0: disable CRC module 1: enable CRC module, cleared when CRC check is done
6	**CRCIF**	**CRC interrupt flag bit** 0: CRC check is not done, clear by software 1: CRC check is done, set by hardware
3-0	**CRCADR[3:0]**	**CRC Check address bits** 0000: Check address is 0000 - 07FDH (2K - 2Byte) 0001: Check address is 0000 - 0FFDH (4K - 2Byte) ………… 1110: Check address is 0000 - 77FDH (30K - 2Byte) 1111: Check address is 0000 - 7FFDH (32K - 2Byte)

Table 8.45 CRC Check Data Register

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CRCDL (F9H, Bank0)	CRCD7	CRCD6	CRCD5	CRCD4	CRCD3	CRCD2	CRCD1	CRCD0
CRCDH (FAH, Bank0)	CRCD15	CRCD14	CRCD13	CRCD12	CRCD11	CRCD10	CRCD9	CRCD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**CRCD[15:0]**	**CRC check data register** CRC Check Code updated when CRC Check is completed

Note:

(1) Need a initial value in CRC check data register before CRC enable.

(2) Cannot set CRCADR[3:0] bits and CRCDL/CRCDH when CRC is operating.

(3) The last two bytes in the CRC check region is dropped out of CRC check, so can store the CRC check theoretical value.

8.13 Power Management

8.13.1 Feature

- Two power saving modes: Idle mode and Power-Down mode
- Two ways to exit Idle and Power-Down mode: interrupt and reset

To reduce power consumption, SH79F3283 supplies two power saving modes: Idle mode and Power-Down mode. These two modes are controlled by PCON & SUSLO register.

8.13.2 Idle Mode

In this mode, the clock of CPU is frozen, the program execution is halted, and the CPU will stop at a defined state. But the peripherals continue to be clocked. When entering idle mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all retained.

By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the IDL bit in PCON register, will make SH79F3283 enter Idle mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or IDL bit in the next machine cycle. And the CPU will not enter Idle mode. The setting of IDL bit will be the last instruction that CPU executed.

There are two ways to exit Idle mode:

(1) An interrupt generated. After warm-up time, the clock of the CPU will be restored, and the hardware will clear SUSLO register and IDL bit in PCON register. Then the program will execute the interrupt service routine first, and then jumps to the instruction immediately following the instruction that activated Idle mode.

(2) Reset signal (logic low on the RESET pin, WDT RESET if enabled, LVR RESET if enabled), this will restore the clock of the CPU, the SUSLO register and the IDL bit in PCON register will be cleared by hardware, finally the SH79F3283 will be reset. And the program will execute from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

8.13.3 Power-Down Mode

The Power-Down mode places the SH79F3283 in a very low power state.

When single clock signal input (OP_OSC[3:0] is 0000 or 1110), Power-Down mode will stop all the clocks including CPU and peripherals. When double clock signal input (OP_OSC[3:0] is 0011, 0110, 1010 or 1101), if system clock is 32.768kHz or 128kHzRC, Power-Down mode will stop all the clocks including CPU and peripherals. If high frequency oscillator is used as system clock, 32.768kHz or 128kHzRC clock used in Timer3 will be opened in Power-Down mode. In Power-Down mode, if WDT is enabled, WDT block will keep on working. When entering Power-Down mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all retained.

By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the PD bit in PCON register, will make SH79F3283 enter Power-Down mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or PD bit in the next machine cycle. And the CPU will not enter Power-Down mode.

The setting of PD bit will be the last instruction that CPU executed.

Note: *If IDL bit and PD bit are set simultaneously, the SH79F3283 enters Power-Down mode. The CPU will not go in Idle mode when exiting from Power-Down mode, and the hardware will clear both IDL & PD bit after exit form Power-Down mode.*

There are three ways to exit the Power-Down mode:

(1) An active external Interrupt (such as INT2, INT3 & INT4) and LPD interrupt will make SH79F3283 exit Power-Down mode. The oscillator will start after interrupt happens, after warm-up time, the clocks of the CPU and peripheral will be restored, the SUSLO register and PD bit in PCON register will be cleared by hardware. Program execution resumes with the interrupt service routine. After completion of the interrupt service routine, the instructions which jumped to enter Power-Down mode will continue to run.

(2) Timer3 interrupt will make SH79F3283 exit Power-Down mode when 32.768kHz or 128kHz RC is the clock source. The oscillator will start after interrupt happens, after warm-up time, the clocks of the CPU and peripheral will be restored, the SUSLO register and PD bit in PCON register will be cleared by hardware. Program execution resumes with the interrupt service routine. After completion of the interrupt service routine, the instructions which jumped to enter Power-Down mode will continue to run.

(3) Reset signal (logic low on the RESET pin, WDT RESET if enabled, LVR RESET if enabled). This will restore the clock of the CPU after warm-up time, the SUSLO register and the PD bit in PCON register will be cleared by hardware, finally the SH79F3283 will be reset. And the program will execute from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

Note: *In order to entering Idle/Power-Down, it is necessary to add 3 NOPs after setting IDL/PD bit in PCON.*

8.13.4 Register

Table 8.46 Power Control Register

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD	SSTAT	SSTAT1	-	GF1	GF0	PD	IDL
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**SMOD**	**Baud rate double bit**
6	**SSTAT**	**SCON[7:5] function selection bit**
5	**SSTAT1**	**SCON1[7:5] function selection bit**
3-2	**GF[1:0]**	**General purpose flags for software use**
1	**PD**	**Power-Down mode control bit** 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Power-Down mode
0	**IDL**	**Idle mode control bit** 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Idle mode

Table 8.47 Suspend Mode Control Register

8EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SUSLO	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**SUSLO[7:0]**	This register is used to control the CPU enter suspend mode (Idle or Power-Down). Only consecutive instructions like below will make CPU enter suspend mode. Otherwise the SUSLO, IDL or PD bit will be cleared by hardware in the next machine cycle.

Example

```
IDLE_MODE:
        MOV     SUSLO, #55H
        ORL     PCON, #01H
        NOP
        NOP
        NOP
```

```
POWERDOWN_MODE:
        MOV     SUSLO, #55H
        ORL     PCON, #02H
        NOP
        NOP
        NOP
```

8.14 Warm-up Timer

8.14.1 Feature

- Built-in power on warm-up counter to eliminate unstable state of power on
- Built-in oscillator warm-up counter to eliminate unstable state when oscillation start up

SH79F3283 has a built-in power warm-up counter; it is designed to eliminate unstable state after power on or to do some internal initial operation such as read internal customer code option etc.

SH79F3283 has also a built-in oscillator warm-up counter, it is designed to eliminate unstable state when oscillator starts oscillating in the following conditions: Power-on reset, Pin reset, LVR reset, Watchdog Reset and Wake up from low power consumption mode.

After power-on, SH79F3283 will start power warm-up procedure first, and then oscillator warm-up procedure. Begin to run the program after the overflow.

Power Warm-up Time

Power On Reset/ Pin Reset/ Low Voltage Reset		WDT Reset (Not in Power-Down Mode)		WDT Reset (Wakeup from Power-Down Mode)		Wakeup from Power-Down Mode (Only for interrupt)	
TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*
11ms	YES	≈1ms	NO	≈1ms	YES	≈500us	YES

OSC Warm-up Time

Option: OP_WMT Oscillator Type	00	01	10	11
Ceramic/Crystal	2^{17} X Tosc	2^{14} X Tosc	2^{11} X Tosc	2^{8} X Tosc
32kHz crystal	2^{13} X Tosc			
Internal RC	2^{7} X Tosc			

8.15 Code Option

OP_WDT:

0: Enable WDT function (default)
1: Disable WDT function

OP_WDTPD:

0: Disable WDT function in Power-Down mode (default)
1: Enable WDT function in Power-Down mode

OP_RST:

0: P5.2 used as RST pin (default)
1: P5.2 used as I/O pin

OP_WMT: (unavailable for 32k oscillator or Internal RC)

00: longest warm up time (default)
01: longer warm up time
10: shorter warm up time
11: shortest warm up time

OP_OSC:

0000: Oscillator1 is internal 12M RC, oscillator2 is disabled
0001: Oscillator1 is internal 8M RC, oscillator2 is disabled
0010: Oscillator1 is internal 16M RC, oscillator2 is disabled
0011: Oscillator1 is internal 128k RC, oscillator2 is internal 12M RC
0100: Oscillator1 is internal 128k RC, oscillator2 is internal 8M RC
0110: Oscillator1 is internal 128k RC, oscillator2 is 2M-12M crystal/ceramic oscillator
1010: Oscillator1 is 32.768k crystal oscillator, oscillator2 is internal 12M RC
1011: Oscillator1 is 32.768k crystal oscillator, oscillator2 is internal 8M RC
1101: Oscillator1 is 32.768k crystal oscillator, oscillator2 is 2M-12M crystal/ceramic oscillator
1110: Oscillator1 is 2M-12M crystal/ceramic oscillator, oscillator2 is disabled
Others: Oscillator1 is internal 12M RC, oscillator2 is disabled

Note: *No external oscillator pin in 20 PIN package, OP_OSC only can be set 0000 and 0011.*

OP_LVREN:

0: Disable LVR function (default)
1: Enable LVR function

OP_LVRLE:

00: 4.1V LVR level 1 (default)
01: 3.7V LVR level 2
10: 2.8V LVR level 3
11: 2.1V LVR level 4

OP_SCM:

0: SCM is invalid in warm up period (default)
1: SCM is valid in warm up period

OP_OSCDRIVE:

011: 8M-16M crystal (default)
001: 4M crystal
111: 12M ceramic
101: 8M ceramic
110: 4M ceramic
100: 2M ceramic

OP_P1DRIVE:

0: Port1 drive ability normal mode (default)
1: Port1 drive ability large mode

OP_PORTDRIVE: (Except Port3)

0: Port drive ability normal mode (default)
1: Port drive ability large mode

OP_P33-P30:

0: port3 [3:0] sink ability normal mode
1: port3 [3:0] sink ability large mode (default)

OP_P37-P34:

0: port3 [7:4] sink ability large mode (default)
1: port3 [7:4] sink ability normal mode

OP_MODSW:

0: when MODSW = 1, LCD/LED count timer continue work
1: when MODSW = 1, LCD/LED count timer stop work, keep the common value, when LCD/LED enable again, continue scan present Common

OP_OSCRFB:

00: set OSC feedback resister is 2M
01: set OSC feedback resister is 1M
10: set OSC feedback resister is 500K (default)
10: set OSC feedback resister is 300K

OP_TF3:

0: TF3 Cleared By Hardware
1: TF3 Cleared By Software

9. Instruction Set

ARITHMETIC OPERATIONS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
ADD A, Rn	Add register to accumulator	0x28-0x2F	1	1
ADD A, direct	Add direct byte to accumulator	0x25	2	2
ADD A, @Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A, #data	Add immediate data to accumulator	0x24	2	2
ADDC A, Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
ADDC A, direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A, @Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A, #data	Add immediate data to A with carry flag	0x34	2	2
SUBB A, Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SUBB A, direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A, @Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A, #data	Subtract immediate data from A with borrow	0x94	2	2
INC A	Increment accumulator	0x04	1	1
INC Rn	Increment register	0x08-0x0F	1	2
INC direct	Increment direct byte	0x05	2	3
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
DEC A	Decrement accumulator	0x14	1	1
DEC Rn	Decrement register	0x18-0x1F	1	2
DEC direct	Decrement direct byte	0x15	2	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	1	3
INC DPTR	Increment data pointer	0xA3	1	4
MUL AB 8 X 8 16 X 8	Multiply A and B	0xA4	1	11 20
DIV AB 8 / 8 16 / 8	Divide A by B	0x84	1	11 20
DA A	Decimal adjust accumulator	0xD4	1	1

LOGIC OPERATIONS

Opcode	Description	Code	Byte	Cycle
ANL A, Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A, direct	AND direct byte to accumulator	0x55	2	2
ANL A, @Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A, #data	AND immediate data to accumulator	0x54	2	2
ANL direct, A	AND accumulator to direct byte	0x52	2	3
ANL direct, #data	AND immediate data to direct byte	0x53	3	3
ORL A, Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A, direct	OR direct byte to accumulator	0x45	2	2
ORL A, @Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A, #data	OR immediate data to accumulator	0x44	2	2
ORL direct, A	OR accumulator to direct byte	0x42	2	3
ORL direct, #data	OR immediate data to direct byte	0x43	3	3
XRL A, Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A, direct	Exclusive OR direct byte to accumulator	0x65	2	2
XRL A, @Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2
XRL A, #data	Exclusive OR immediate data to accumulator	0x64	2	2
XRL direct, A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct, #data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	4

LOGIC OPERATIONS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
ANL A, Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A, direct	AND direct byte to accumulator	0x55	2	2
ANL A, @Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A, #data	AND immediate data to accumulator	0x54	2	2
ANL direct, A	AND accumulator to direct byte	0x52	2	3
ANL direct, #data	AND immediate data to direct byte	0x53	3	3
ORL A, Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A, direct	OR direct byte to accumulator	0x45	2	2
ORL A, @Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A, #data	OR immediate data to accumulator	0x44	2	2
ORL direct, A	OR accumulator to direct byte	0x42	2	3
ORL direct, #data	OR immediate data to direct byte	0x43	3	3
XRL A, Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A, direct	Exclusive OR direct byte to accumulator	0x65	2	2
XRL A, @Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2
XRL A, #data	Exclusive OR immediate data to accumulator	0x64	2	2
XRL direct, A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct, #data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	4

DATA TRANSFERS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
MOV A, Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV A, direct	Move direct byte to accumulator	0xE5	2	2
MOV A, @Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV A, #data	Move immediate data to accumulator	0x74	2	2
MOV Rn, A	Move accumulator to register	0xF8-0xFF	1	2
MOV Rn, direct	Move direct byte to register	0xA8-0xAF	2	3
MOV Rn, #data	Move immediate data to register	0x78-0x7F	2	2
MOV direct, A	Move accumulator to direct byte	0xF5	2	2
MOV direct, Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1, direct2	Move direct byte to direct byte	0x85	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	0x86-0x87	2	3
MOV direct, #data	Move immediate data to direct byte	0x75	3	3
MOV @Ri, A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV DPTR, #data16	Load data pointer with a 16-bit constant	0x90	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to A	0x93	1	7
MOVC A, @A+PC	Move code byte relative to PC to A	0x83	1	8
MOVX A, @Ri	Move external RAM (8-bit address) to A	0xE2-0xE3	1	5
MOVX A, @DPTR	Move external RAM (16-bit address) to A	0xE0	1	6
MOVX @Ri, A	Move A to external RAM (8-bit address)	0xF2-F3	1	4
MOVX @DPTR, A	Move A to external RAM (16-bit address)	0xF0	1	5
PUSH direct	Push direct byte onto stack	0xC0	2	5
POP direct	Pop direct byte from stack	0xD0	2	4
XCH A, Rn	Exchange register with accumulator	0xC8-0xCF	1	3
XCH A, direct	Exchange direct byte with accumulator	0xC5	2	4
XCH A, @Ri	Exchange indirect RAM with accumulator	0xC6-0xC7	1	4
XCHD A, @Ri	Exchange low-order nibble indirect RAM with A	0xD6-0xD7	1	4

PROGRAM BRANCHES				
Instructions	**Description**	**Code**	**Byte**	**Cycle**
ACALL addr11	Absolute subroutine call	0x11-0xF1	2	7
LCALL addr16	Long subroutine call	0x12	3	7
RET	Return from subroutine	0x22	1	8
RETI	Return from interrupt	0x32	1	8
AJMP addr11	Absolute jump	0x01-0xE1	2	4
LJMP addr16	Long jump	0x02	3	5
SJMP rel	Short jump (relative address)	0x80	2	4
JMP @A+DPTR	Jump indirect relative to the DPTR	0x73	1	6
JZ rel (not taken) (taken)	Jump if accumulator is zero	0x60	2	3 5
JNZ rel (not taken) (taken)	Jump if accumulator is not zero	0x70	2	3 5
JC rel (not taken) (taken)	Jump if carry flag is set	0x40	2	2 4
JNC rel (not taken) (taken)	Jump if carry flag is not set	0x50	2	2 4
JB bit, rel (not taken) (taken)	Jump if direct bit is set	0x20	3	4 6
JNB bit, rel (not taken) (taken)	Jump if direct bit is not set	0x30	3	4 6
JBC bit, rel (not taken) (taken)	Jump if direct bit is set and clear bit	0x10	3	4 6
CJNE A, direct, rel (not taken) (taken)	Compare direct byte to A and jump if not equal	0xB5	3	4 6
CJNE A, #data, rel (not taken) (taken)	Compare immediate to A and jump if not equal	0xB4	3	4 6
CJNE Rn, #data, rel (not taken) (taken)	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4 6
CJNE @Ri, #data, rel (not taken) (taken)	Compare immediate to Ri and jump if not equal	0xB6-0xB7	3	4 6
DJNZ Rn, rel (not taken) (taken)	Decrement register and jump if not zero	0xD8-0xDF	2	3 5
DJNZ direct, rel (not taken) (taken)	Decrement direct byte and jump if not zero	0xD5	3	4 6
NOP	No operation	0	1	1

BOOLEAN MANIPULATION				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear direct bit	0xC2	2	3
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement direct bit	0xB2	2	3
ANL C, bit	AND direct bit to carry flag	0x82	2	2
ANL C, /bit	AND complement of direct bit to carry	0xB0	2	2
ORL C, bit	OR direct bit to carry flag	0x72	2	2
ORL C, /bit	OR complement of direct bit to carry	0xA0	2	2
MOV C, bit	Move direct bit to carry flag	0xA2	2	2
MOV bit, C	Move carry flag to direct bit	0x92	2	3

10. Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage. . . . .-0.3V to +6.0V

Input/Output Voltage. . . . . GND-0.3V to V_{DD}+0.3V

Operating Ambient Temperature. . . . . -40℃ to +85℃

Storage Temperature. . . . .-55℃ to +125℃

FLASH write/erase operating. . . . . 0℃ to +85℃

***Comments**

Stresses exceed those listed under “**Absolute Maximum Ratings**” may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 2.0V - 5.5V, GND = 0V, T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.∗	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.0	5.0	5.5	V	32.768kHz or 2MHz ≤ f_{OSC} ≤ 16MHz
Operating Current	I_{OP}	-	5	10	mA	f_{OSC} = 12MHz, V_{DD} = 5.0V All output pins unload (including all digital input pins unfloating) CPU on (execute NOP instruction), WDT on, all other function block off
	I_{OP2}	-	25	35	μA	f_{OSC} = 128kHz, OSCX off, V_{DD} = 5.0V All output pins unload (including all digital input pins unfloating) CPU on (execute NOP instruction), LVR off, WDT off, all other function block off
Stand by Current (IDLE)	I_{SB1}	-	3	5	mA	f_{OSC} = 12MHz, V_{DD} = 5.0V All output pins unload, CPU off (IDLE), all digital input pins unfloating LVR on, WDT off, LCD on, all other function block off
	I_{SB2}	-	15	25	μA	f_{OSC} = 128kHz, OSCX off, V_{DD} = 5.0V All output pins unload (including all digital input pins unfloating) (IDLE MODE) LVR on, WDT off, CRC off, LCD off, all other function block off
Stand by Current (Power-Down)	I_{SB3}	-	2	6	μA	Osc off, V_{DD} = 5.0V All output pins unload (including all digital input pins unfloating) CPU off (Power-Down), LVR on, WDT off, CRC off, LCD off, all other function block off
	I_{SB4}	-	4	15	μA	f_{OSC} = 32.768kHz, OSCX off, V_{DD} = 5.0V All output pins unload (including all digital input pins unfloating) CPU off (Power-Down), LVR on, WDT off, CRC off, LCD off, all other function block off
WDT Current	I_{WDT}	-	1	3	μA	All output pins unload, WDT on, V_{DD} = 5.0V
LCD Current	I_{LCD}	-	6	7	μA	Traditional bias resistance mode, V_{DD} = 5V 300kΩ LCD bias resister, contrast[3:0] = 1111
LPD Current	I_{LPD}	-	-	1	μA	V_{DD} = 2.0 - 5.5V

(to be continued)

(continue)

Input Low Voltage 1	V_{IL1}	GND	-	0.3 X V_{DD}	V	I/O Ports
Input High Voltage 1	V_{IH1}	0.7 X V_{DD}	-	V_{DD}	V	I/O Ports
Input Low Voltage 2	V_{IL2}	GND	-	0.2 X V_{DD}	V	$\overline{RST}$, T2, T3, T4, INT0/1/2/3/4, T2EX, RXD0, RXD1, FLT, V_{DD} = 2.4 - 5.5V
Input High Voltage 2	V_{IH2}	0.8 X V_{DD}	-	V_{DD}	V	$\overline{RST}$, T2, T3, T4, INT0/1/2/3/4, T2EX, RXD0, RXD1, FLT, V_{DD} = 2.4 - 5.5V
Input Leakage Current	I_{IL}	-1	-	1	µA	Input pin, V_{IN} = V_{DD} or GND
output Leakage Current	I_{OL}	-1	-	1	µA	Open-drain output, V_{DD} = 5.0V V_{OUT} = V_{DD} or GND
Reset pin pull-up resistor	R_{RPH}	-	30	-	kΩ	V_{DD} = 5.0V, V_{IN} = GND
Pull-up resistor	R_{PH}	-	30	-	kΩ	V_{DD} = 5.0V, V_{IN} = GND
Output High Voltage 1	V_{OH1}	V_{DD} - 0.7	-	-	V	I/O Ports (P0, P2-P5), I_{OH} = -10mA, V_{DD} = 5.0V Select Port drive ability normal mode (Code Option)
Output High Voltage 2	V_{OH2}	V_{DD} - 0.7	-	-	V	I/O Ports (P0, P2-P5), I_{OH} = -18mA, V_{DD} = 5.0V Select Port drive ability large mode (Code Option)
Output High Voltage 3	V_{OH3}	V_{DD} - 0.7	-	-	V	I/O Ports (P1), I_{OH} = -10mA, V_{DD} = 5.0V Select Port1 drive ability normal mode (Code Option)
Output High Voltage 4	V_{OH4}	V_{DD} - 0.7	-	-	V	I/O Ports (P1), I_{OH} = -18mA, V_{DD} = 5.0V Select Port1 drive ability large mode (Code Option)
Output Low Voltage1	V_{OL1}	-	-	GND + 0.6	V	I/O Ports (P0, P1, P2, P4, P5) I_{OL} = 15mA, V_{DD} = 5.0V
Output Low Voltage2	V_{OL2}	-	-	GND + 0.6	V	I/O Ports (P3), I_{OL} = 15mA, V_{DD} = 5.0V Select Port3 drive ability normal mode (Code Option)
large drive port sink current capability	I_{OL}	120	140	-	mA	I/O Ports (P3), V_{DD} = 5.0V, V_{OL} = GND + 1.5V Select Port3 drive ability large mode (Code Option)
LCD output resister	R_{ON}	-	5	-	kΩ	SEG1 - 28, COM1 - 8, V_{DD} = 3.6V - 5.0V The voltage variation of V1, V2, V3 is less than 0.2V

Note:

(1) "" Indicates that the typical value is measured at 5.0V, 25°C, unless otherwise noted.*

(2) Maximum current value flowing through V_{DD} 5.0V, 25°C must be less than 150mA.

(3) Maximum current value flowing through GND 5.0V, 25°C must be less than 200mA.

A/D Converter Electrical Characteristics (V_{DD} = 5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage	V_{AD}	2.5	3	5.5	V	
Resolution	N_R	-	12	-	bit	GND $\le V_{AIN} \le V_{REF}$
A/D Input Voltage	V_{AIN}	GND	-	V_{REF}	V	
A/D Input Resistor*	R_{AIN}	2	-	-	MΩ	V_{IN} = 5.0V
Recommended impedance of analog voltage source	Z_{AIN}	-	-	10	kΩ	
A/D conversion current	I_{AD}	-	1	3	mA	ADC module operating, V_{DD} = 5.0V
A/D Input current	I_{ADIN}	-	-	10	µA	V_{DD} = 5.0V
Differential linearity error	D_{LE}		-	±1	LSB	f_{OSC} = 12MHz, V_{DD} = 5.0V
Integral linearity error	I_{LE}	-	-	±2	LSB	f_{OSC} = 12MHz, V_{DD} = 5.0V
Full scale error	E_F	-	±1	±8	LSB	f_{OSC} = 12MHz, V_{DD} = 5.0V
Offset error	E_Z	-	±0.5	±8	LSB	f_{OSC} = 12MHz, V_{DD} = 5.0V
Total Absolute error	E_{AD}	-	-		LSB	f_{OSC} = 12MHz, V_{DD} = 5.0V
Total Conversion time**	T_{CON}	16	-	-	t_{AD}	12 bit Resolution, V_{DD} = 5.0V, t_{AD} = 1µs
Internal reference	V_{ADREF}	1.225	1.25	1.275	V	±2%, T_A = +25°C

Note:

(1) "" Here the A/D input Resistor is the DC input-resistance of A/D itself.*

*(2) "**" Recommendations ADC connected signal source resistance of less than10kΩ*

AC Electrical Characteristics (V_{DD} = 2.0V - 5.5V, GND = 0V, T_A = +25°C, f_{OSC} = 12MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator start time	T_{OSC}	-	-	1	s	f_{OSC} = 32.768kHz
	T_{OSC}	-	1	2	ms	f_{OSC} = 12MHz
RESET pulse width	t_{RESET}	10	-	-	µs	
WDT RC Frequency	f_{WDT}	-	2	3	kHz	
Frequency Stability (RC)	$\mid \Delta F \mid / F$	-	-	±1	%	RC oscillator: |F - 12MHz|/12MHz (V_{DD} = 2.0 - 5.0V, T_A = +25°C)
		-	-	±2	%	RC oscillator: |F - 12MHz|/12MHz (V_{DD} = 2.0 - 5.0V, T_A = -40°C - +85°C)
		-	-	±2	%	RC oscillator: |F - 128kHz|/128kHz (V_{DD} = 2.0 - 5.0V,T_A = 25°C)

Low Voltage Reset Electrical Characteristics (V_{DD} = 2.0V - 5.5V, GND = 0V, T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVR Voltage1	V_{LVR1}	4.0	4.1	4.2	V	LVR Enable, V_{DD} = 2.0V - 5.5V
LVR Voltage2	V_{LVR2}	3.6	3.7	3.8	V	LVR Enable, V_{DD} = 2.0V - 5.5V
LVR Voltage3	V_{LVR3}	2.7	2.8	2.9	V	LVR Enable, V_{DD} = 2.0V - 5.5V
LVR Voltage4	V_{LVR4}	2.0	2.1	2.2	V	LVR Enable, V_{DD} = 2.0V - 5.5V
LVR Schmidt trigger	V_{SMTLV}	-	50	-	mV	
Drop-Down Pulse Width for LVR	T_{LVR}	-	60	-	µs	

12MHz Crystal Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency	F_{12M}	-	12	-	MHz	
Capacitor	C_L	-	12.5	-	pF	

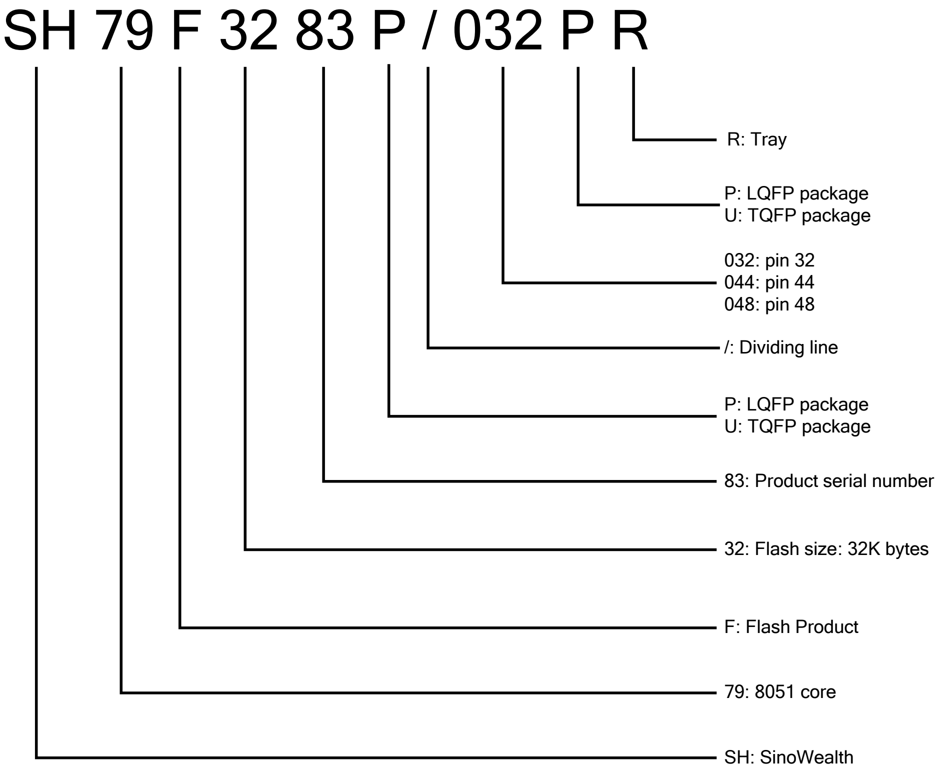
32.768kHz crystal Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency	F_{32k}	-	32768	-	Hz	
Capacitor	C_L	-	12.5	-	pF	

11 Ordering Information

Part No.	Package
SH79F3283P/032PR	LQFP32
SH79F3283P/044PR	LQFP44
SH79F3283U/048UR	TQFP48

12 Product Naming Rules



SH 79 F 32 83 P / 032 P R

R: Tray

P: LQFP package
U: TQFP package

032: pin 32
044: pin 44
048: pin 48

/: Dividing line

P: LQFP package
U: TQFP package

83: Product serial number

32: Flash size: 32K bytes

F: Flash Product

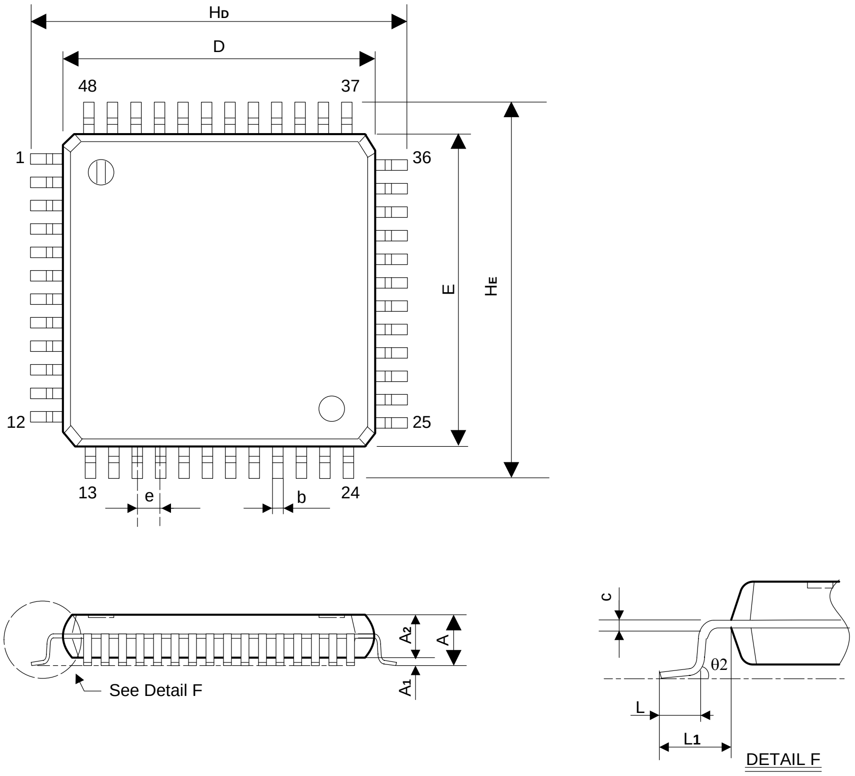
79: 8051 core

SH: SinoWealth

13 Package Information

TQFP48 Outline Dimensions

unit: inch/mm

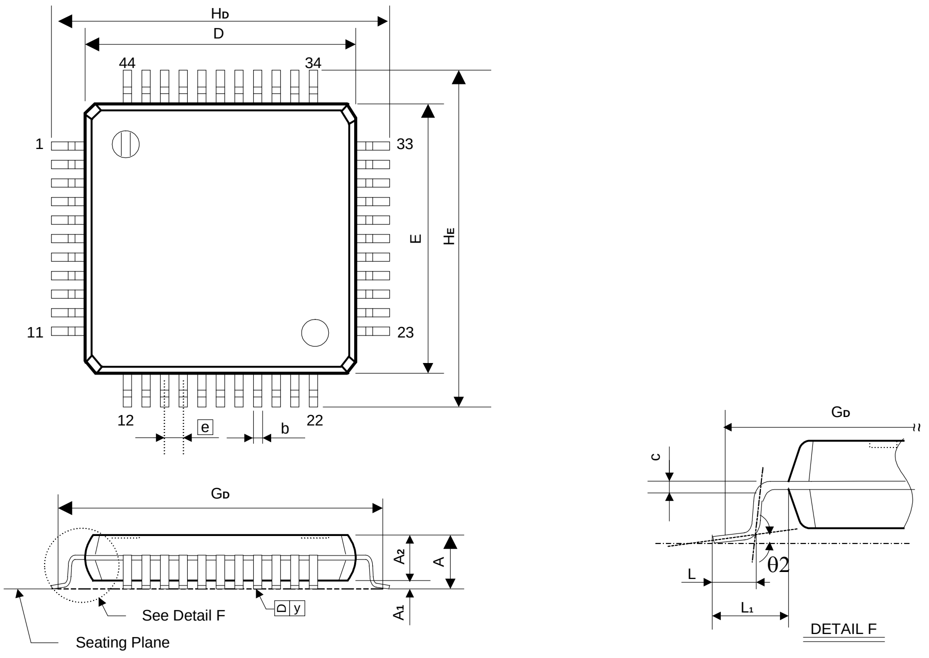


Symbol	Dimensions in inches		Dimensions in mm	
	MIN	MAX	MIN	MAX
A	---	0.047	---	1.2
A1	0.002	0.006	0.05	0.15
A2	0.035	0.041	0.9	1.05
D	0.270	0.281	6.85	7.15
E	0.270	0.281	6.85	7.15
H_D	0.346	0.362	8.8	9.2
H_E	0.346	0.362	8.8	9.2
b	0.005	0.011	0.15	0.27
e	0.020 TYP		0.500 TYP	
c	0.004	0.008	0.090	0.200
L	0.018	0.030	0.45	0.75
L1	0.033	0.045	0.85	1.15
θ2	0°	10°	0°	10°

Notice:

(1) Both package length and width do not include mold flash.
(2) Tolerance is ±0.1mm if not specified.
(3) Coplanarity: 0.1mm max.
(4) Controlling dimension: mm.

LQFP 44 Outline Dimensions (BODY SIZE: 10*10) unit: inch/mm



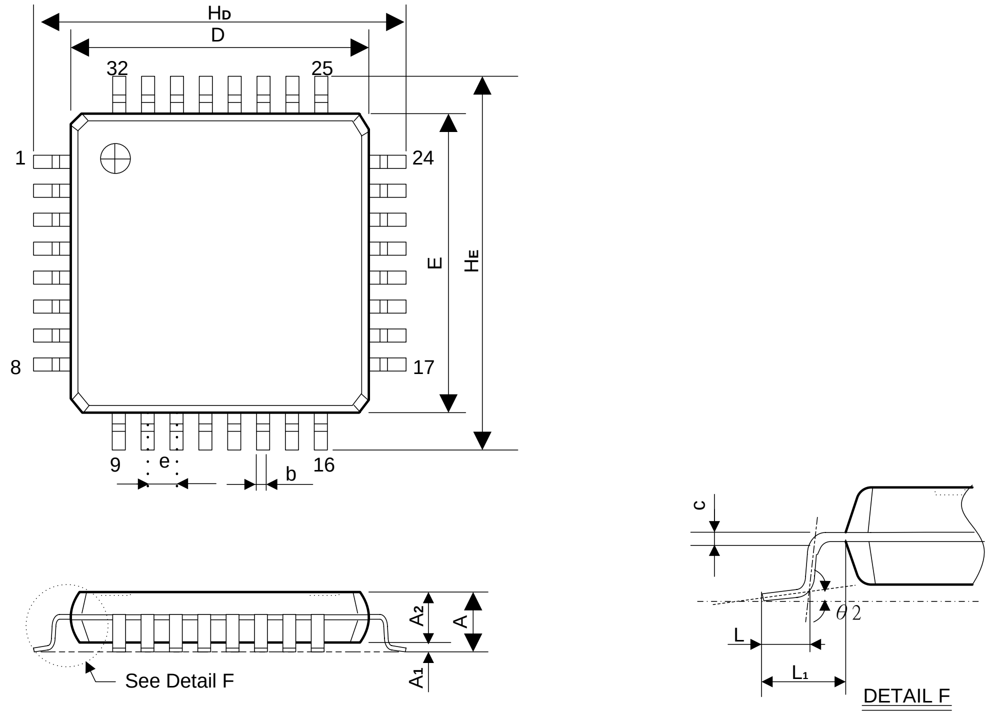
Symbol	Dimensions in inches		Dimensions in mm	
	MIN	MAX	MIN	MAX
A	0.057	0.065	1.45	1.65
A1	0.000	0.001	0.01	0.21
A2	0.051	0.059	1.3	1.5
D	0.388	0.400	9.85	10.15
E	0.388	0.400	9.85	10.15
H_D	0.465	0.480	11.8	12.2
H_E	0.465	0.480	11.8	12.2
b	0.010	0.018	0.25	0.45
e	0.031 TYP		0.8 TYP	
c	0.004	0.008	0.09	0.20
L	0.017	0.031	0.42	0.78
L1	0.037	0.045	0.95	1.15
θ2	0°	10°	0°	10°

Notice:

(1) Both package length and width do not include mold flash.
(2) Tolerance is ±0.1mm if not specified.
(3) Coplanarity: 0.1mm max.
(4) Controlling dimension: mm.

LQFP32 Outline Dimensions

unit: inch/mm



Symbol	Dimensions in inches		Dimensions in mm	
	MIN	MAX	MIN	MAX
A	0.057	0.065	1.45	1.65
A1	0.000	0.008	0.01	0.21
A2	0.051	0.059	1.30	1.50
D	0.268	0.281	6.80	7.15
E	0.268	0.281	6.80	7.15
H_D	0.346	0.362	8.80	9.20
H_E	0.346	0.362	8.80	9.20
b	0.010	0.018	0.25	0.45
e	0.031 TYP		0.8TYP	
c	0.004	0.008	0.09	0.20
L	0.016	0.031	0.40	0.78
L1	0.035	0.043	0.90	1.10
θ2	0°	10°	0°	10°

Notice:

(1) Both package length and width do not include mold flash.
(2) Tolerance is ±0.1mm if not specified.
(3) Coplanarity: 0.1mm max.
(4) Controlling dimension: mm.

14 Product SPEC. Change Notice

Version	Content	Date
2.0	Original	Jun. 2021

IMPORTANT NOTICE

This manual is the property of Sino Wealth Electronic Ltd. and its affiliates ("Company"). This manual, including all of the Company's products ("Products") described herein, is owned by the Company according to relevant laws or treaties. The Company reserves all rights under such laws and treaties, and does not grant you any license to use its patents, copyrights, trademarks and other intellectual property rights.

Any technical information in this manual, including functional descriptions and schematic diagrams, shall not be construed as a license to use or exercise any intellectual property rights. The names and brands (if any) of the relevant third parties are quoted in this manual are the property of their respective owners, for identification purposes only.

The Company does not make any warranty, expressed or implied, about this manual or any Product, including, but not limited to, implied warranties of merchantability and fitness for a particular purpose. The Company shall not be liable for any use of any of Product described in this manual out of its specifications or the Company’s standard. Except for the special Products specified in the applicable agreement, the Products are designed, developed and manufactured for general commercial, industrial, personal and/or domestic applications only. In particular, the Products are prohibited to be used in following fields, such as military, national defense, nuclear energy, medical treatment and others that may cause personal injury, death or environmental damage. Users shall take all actions to ensure that the Products are used and sold in accordance with applicable laws and regulations.

The failure or malfunction of semiconductor products may occur. Users of the Products should therefore give thorough consideration to safety design, including redundancy, fire-prevention measures and etc., to prevent any accidents, fire or community damage that may ensue. Especially, the reference application circuit is not guaranteed to be suitable for the specific application of mass production.

In the event that users breach the above statement, the Company shall not be liable in whole or in part, and users shall hereby release the Company and its -agents and/or distributors from any claim, damage or other liability; At the same time, users shall indemnify the Company and its agents and/or distributors against all claims, costs, damages and other liabilities, including claims for personal injury or death, arising out of any unintended use of the Product.

The information in this manual is related to the Product only. The Company reserves the right to make changes, modifications or improvements to this manual, the Products and services described herein at any time without prior notice. Users are advised to contact our sales department before purchase.

The Company has the final right to interpret this manual.

Content